PPD EED Department Meeting

27 September 2016

EED Department

- Department News
  - Lots of retirements, some new hires
    - Welcome to Vadim Rusu –Duty Head of EED
    - Welcome to Brian Hess – Technician
    - Welcome back to Abder Mekkaoui
  - Department Org Chart can be found online at EED website
    http://ppd.fnal.gov/eed/

Electrical Engineering Department

T. Shaw, Head

V. Rusu, Deputy Head

M. Matulik, Associate Head

Administration Support

C. Johnson

Asic Development

G. Deptuch, Ldr.

Analog	Digital	Test
A. Mekkaoui	J. Hoff	A. Baumbaugh
F. Fahim	D. Braga	
T. Zimmerman	A. Shenai	S. Holm
		L. Dal Monte
		A. Dyer
		L. Scott
		B. Hess

Detector Electronics

P. Rubinov, Ldr.

S. Hansen	C. Gingu
T. Kiper	K. Kuk
S. Los	M. Utes
J. Wu	J. Olsen

Infrastructure & Support

M. Matulik, Ldr.

S. Chappa	D. Huffman
D. Featherston	M. Cherry
W. Jaskierny	T. Cunneen
J. Noyola	
C. Danner	J. Green
P. Lippert	R. Klein
V. Martinez	N. Moibenko

EED Department continued

- Department News
  - Please keep up with required training!
  - Lots of general clean up on the floor as we try to make space for lab areas and new people; need to continually work to reduce clutter
  - FY2016 Performance Reviews will be available for viewing through Fermiworks early October
  - Task Code Guidance can be found at

    http://ppd.fnal.gov/PPD%20Charging%20Practices.pdf
  - CAD tools – an Altium Task Force/Users Group is forming in the department to map out a likely transition to PCB schematic capture and board layout using ONLY Altium in the future (phase out of Mentor)

PPD Charging Practices

Program Support (PS)

- General Training
  - Training common across the lab
  - Examples: Traffic safety, computer security
- Division Activities
  - Management of group, department, division
  - Quality assurance
  - Performance review
  - All-CRO, division, department all-hands meetings
- Charge to department PS code (see table below)

General and Administrative (GA)

- Services on review of Fermilab or non-Fermilab projects/programs/activities
- General outreach/education services
- Fermilab All Hands
- Service on Lab Committees
- Charge to 40PD.40.01.05

Common Site Support (CSS)

- Building Maintenance/Management
- Vehicle Maintenance
- Facility Infrastructure
- Licenses for software not directly associated with projects or operations
- Charge code depends on the task

Conference Travel/attendance/presentations

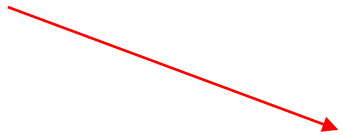
- Charge to activity or project supporting the work

Training Associated with Job Function

- Examples: Working from heights, beryllium handling, crane operation
- Charge to home code

Program Support Task Codes

Department	PS Code
AMD	40PD.08.03
Astro	40PD.70.01.07
CMS	40PD.30.08
DDOD	40PD.80.01.01
EED	40PD.50.01.01



EED Department continued

- Department News

  Carolyn is working to set up a group lunch (courtesy of PPD!) at Chez Leon in October

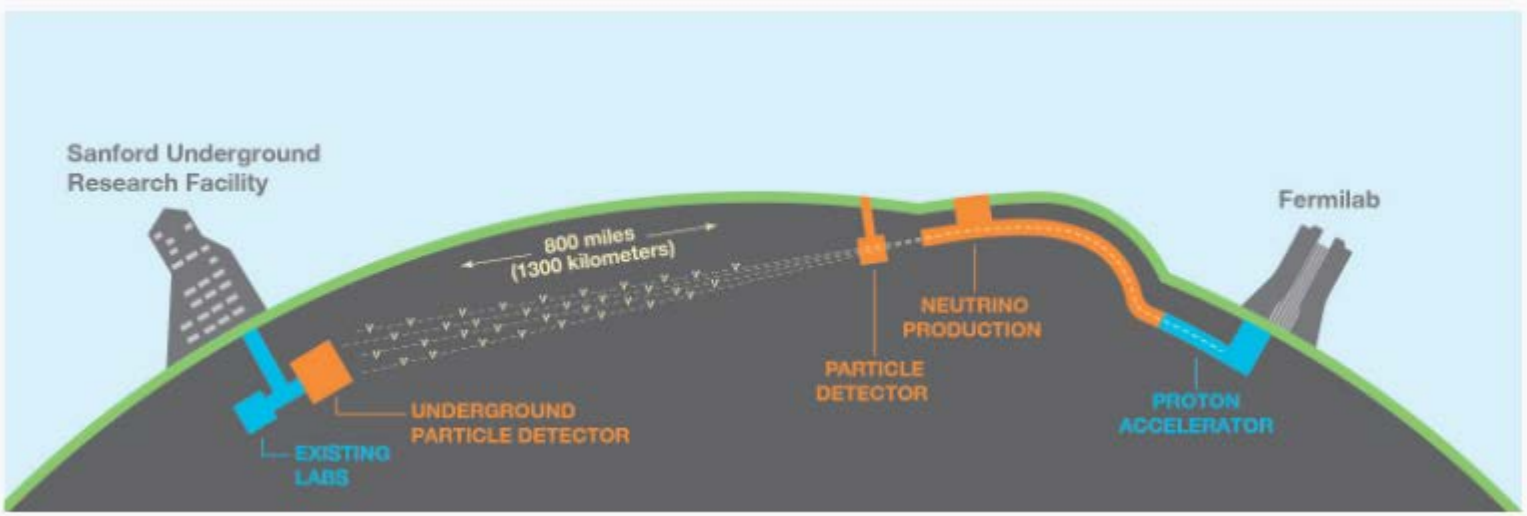
  Details will be announced soon.

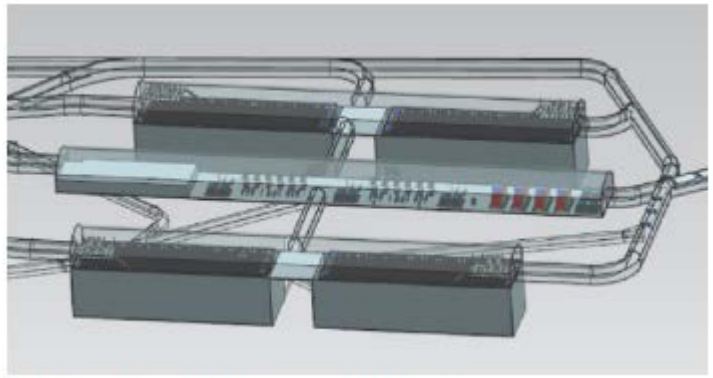
- Questions?

Terri Shaw

Dune Far Detector Project Electrical Engineer

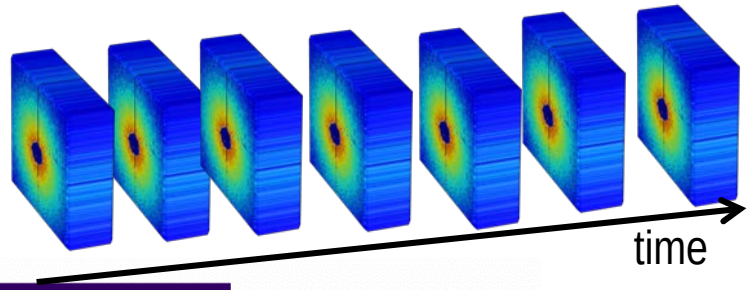
http://www.dunescience.org/



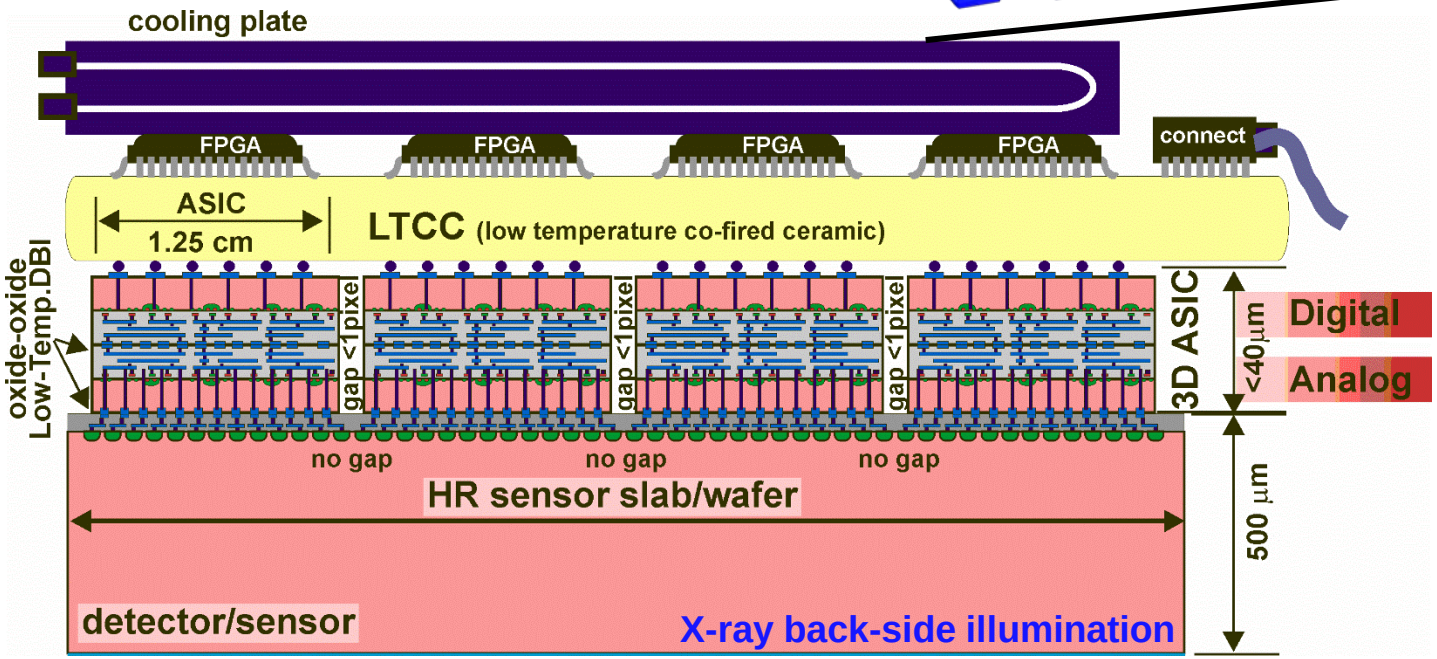


Gregory Deptuch

VIPIC-L camera (Fermilab,BNL,ANL)



Vertically-Integrated Photon Imaging Chip - Large

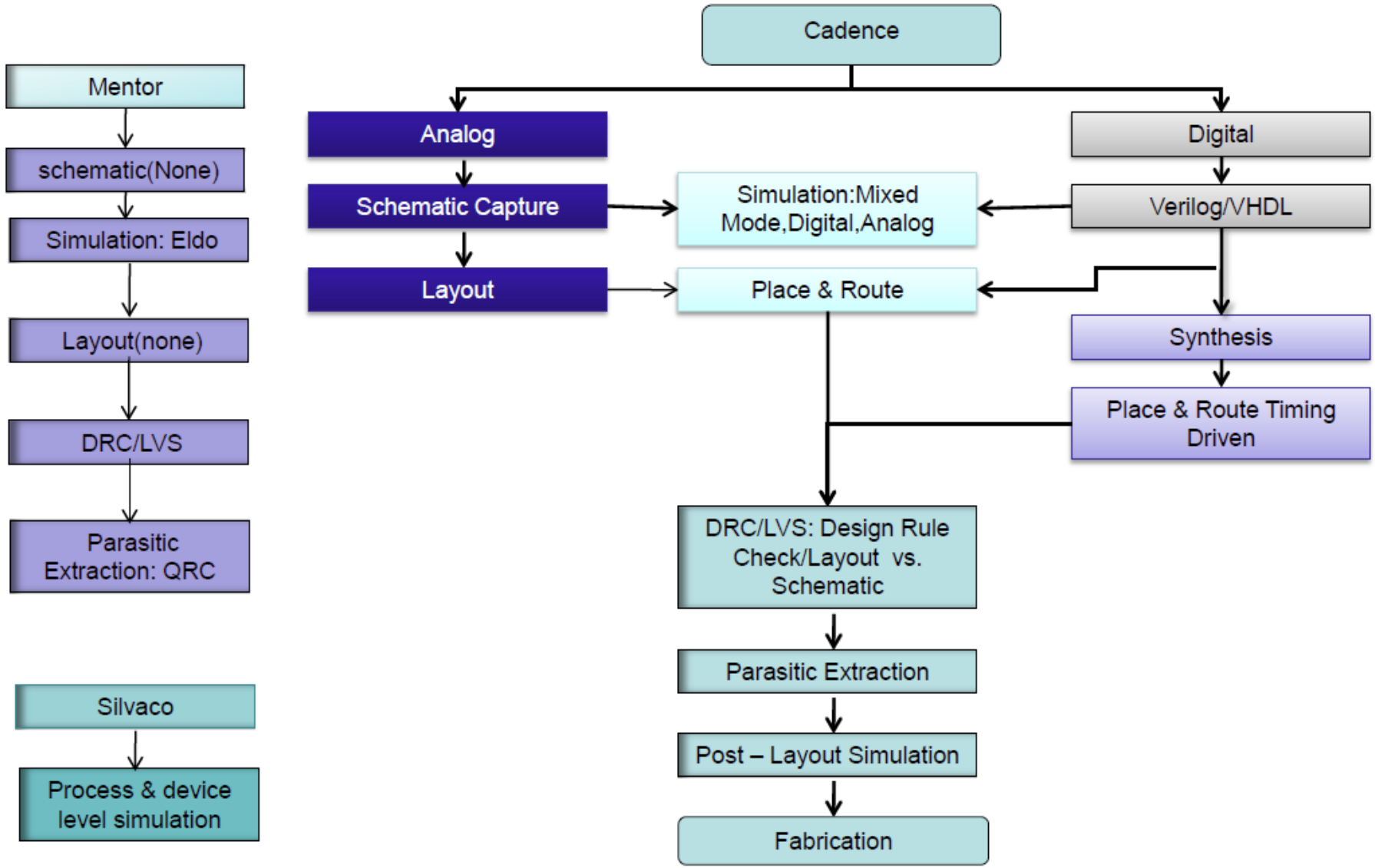


1.2M-pixel, single module camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays,
Funded by DOE Office of Science Office of Basic Energy Sciences (1M$ for Fermilab manpower)
(FWP started in Oct. 2014, completion planned for Sept. 2017)

- VIPIC-L ASIC is a two tier 3D ASIC 1.25 × 1.25 cm^2 with ~120M transistor (largest ASIC built by a US national lab) and 65µm pixel pitch and is configurable in sparsification or imaging mode (up to 78kfps)
- 1 Mpixel = 3 slabs of 2 × 6 VIPIC-L LTD-bonded directly to a Si sensor wafer
- 1FPGA per VIPIC-L (in its footprint) for on the fly data processing (up to 0.72 Tbps of raw data produced)
- Multi-layer (>20 routing layer LTCC) suports b-bonded detector structure

Alpana Shenai

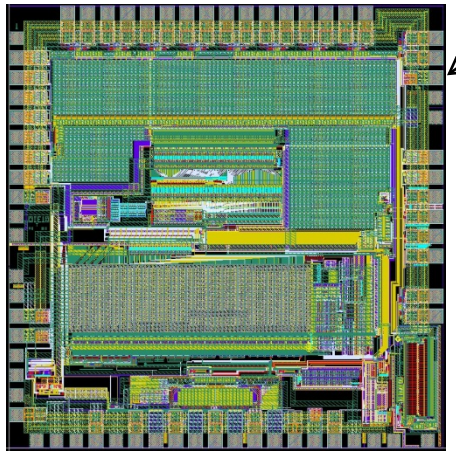
Custom IC Design Tools



Tom Zimmerman

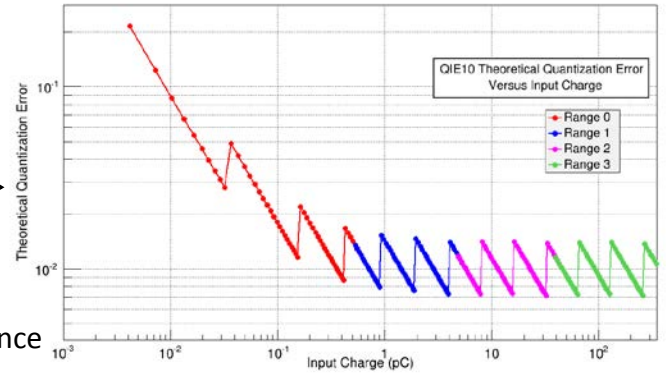
QIE: a multi-decade development effort in high dynamic range floating-point readout chips for HEP

1989: original idea (Bill Foster) **1995:** QIE5 for KTeV **1996:** QIE6 for CDF **1997:** QIE6 for CDF **2002:** QIE7 for MINOS
2003: QIE8 for CMS **2004:** QIE9 for BTeV **2016:** QIE10 and QIE11 for CMS, QIE12 for ATLAS



QIE10: a charge integrating, floating point digitizer for CMS

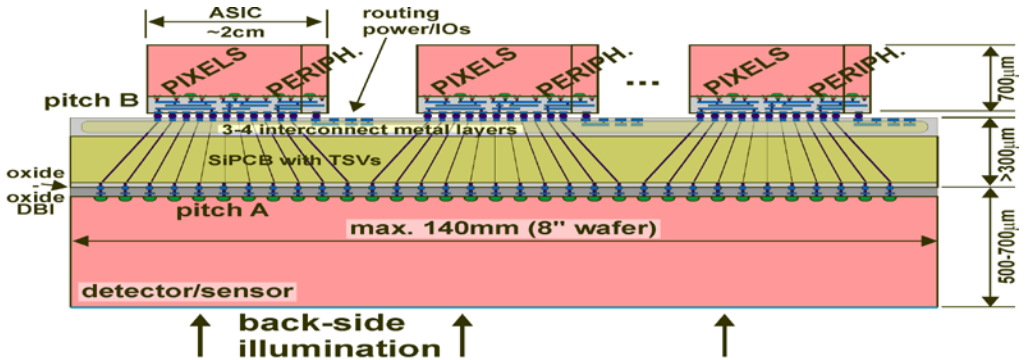
40 MHz dead-timeless operation
Very high dynamic range: 3 fC to 350 pC (~17 bits)
Four ranges
Pseudo-log ADC gives 4 sub-ranges in each range
"Floating point" yields approx. constant resolution
Programmable threshold TDC with 500 ps timing
Many programmable parameters
LVDS outputs
Very successful development based on years of experience



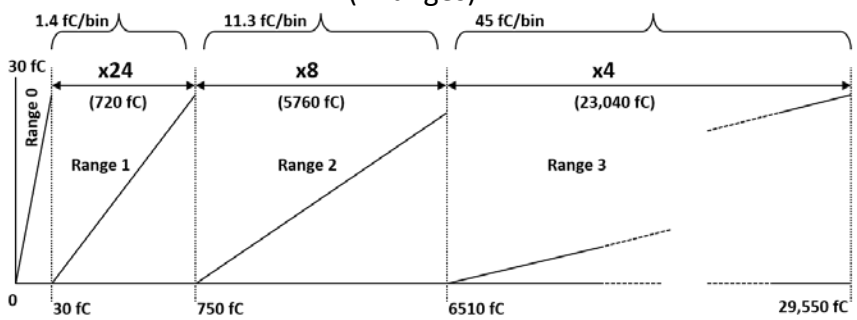
2015 - 2017 ***Translate QIE experience to a dense pixel array application***

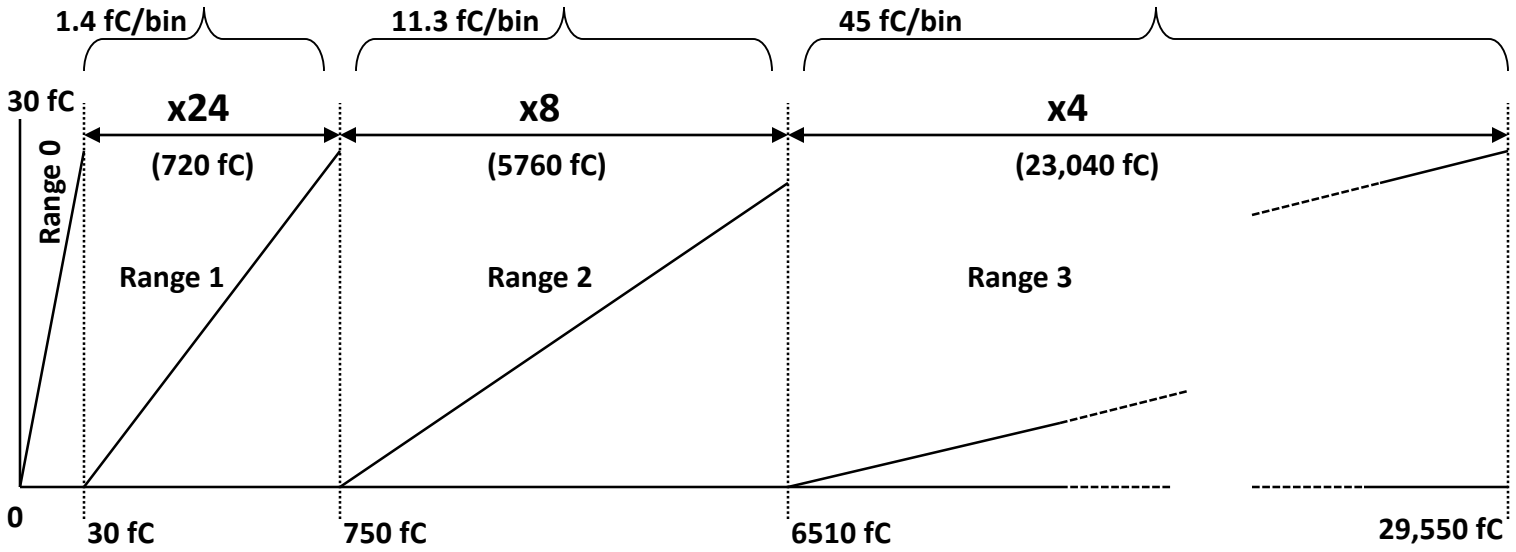
FASPAX: a wafer scale X-ray camera of small pixels with <u>unprecedented dynamic range</u>

Use QIE principles and experience to obtain a dynamic range of 10^5 in a 100u X 100u pixel



(4 ranges)




1.4 fC/bin
11.3 fC/bin
45 fC/bin
30 fC
x24
x8
x4
(720 fC)
(5760 fC)
(23,040 fC)
Range 0
Range 1
Range 2
Range 3
0
30 fC
750 fC
6510 fC
29,550 fC

Abder Mekkaoui

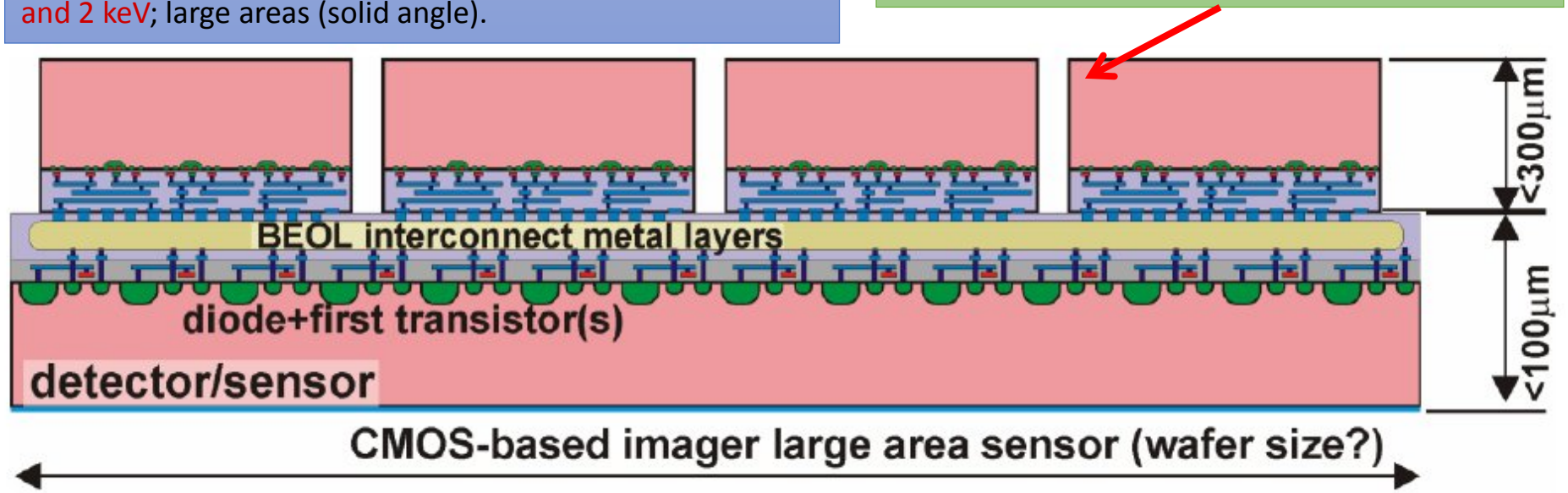
FLORA: A 3D integrated CMOS detector for imaging experiments at LCLS-II

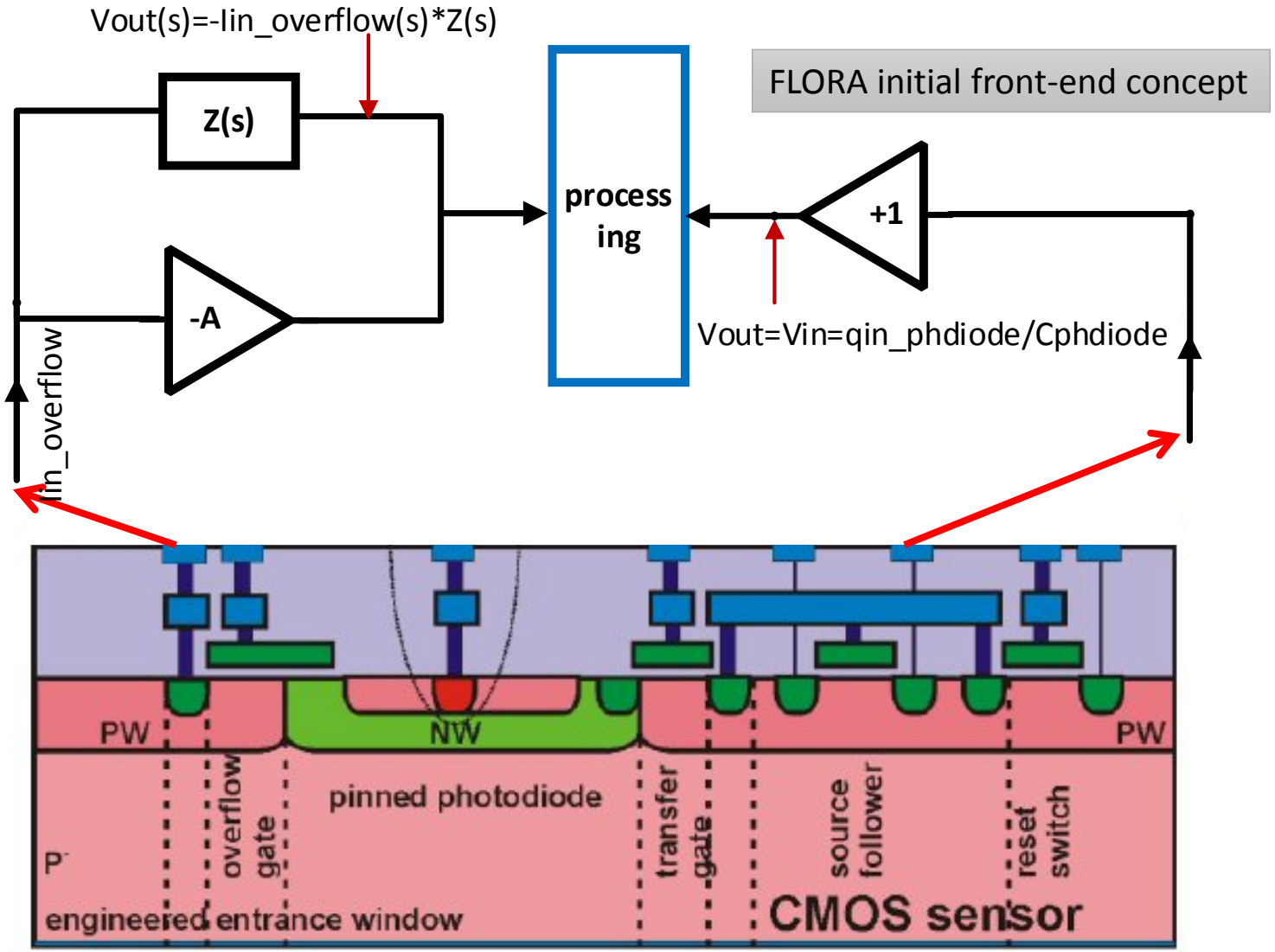
D. Christian, G.W. Deptuch, F. Fahim, R. Lipton, A. Mekkaoui, T. Zimmerman (FERMILAB), Gabriella Carini et al. (SLAC)

LCLS: The SLAC Linac Coherent Light Source (LCLS) is the world's first hard X-ray source produced by free electron laser. With X-ray pulses a billion times brighter than predecessor X-ray sources that last for just femtoseconds, LCLS can measure the properties of ultra-fast processes at the scale of atoms and molecules. The LCLS opened the door to revolutionary experiments in atomic and molecular dynamics.
LCLS-II: LCLS-II will provide a major jump in capability – moving from 120 pulses per second to 1 million pulses per second. This will enable researchers to perform experiments in a wide range of fields that are now impossible. The unique capabilities of LCLS-II will yield a host of discoveries to advance technology, new energy solutions and our quality of life. More info: https://portal.slac.stanford.edu/sites/lcls_public/Pages/Default.aspx

FLORA (Fermilab-LCLS CMOS 3D-integRated detector with Autogain), with very low noise, high dynamic range and fast readout suitable for imaging experiments at the upcoming LCLS-II.
Small pixel size (50µmx50µm pixels); Frame readout > 10 kfps; Built-in adaptive gain; DR from 1 to 1,000 photons per pixel per frame with a single photon resolution; High quantum efficiency in the energy range between 250 eV and 2 keV; large areas (solid angle).

Divide and conquer using a 3D approach: Using a sensing layer (in an imaging CMOS process) to deal with "upfront" issues (Help with the ENC, DR, appropriate entrance window and thickness...) and a *readout layer, implemented in an optimum process, would implement signal processing and communication with the upstream system.*





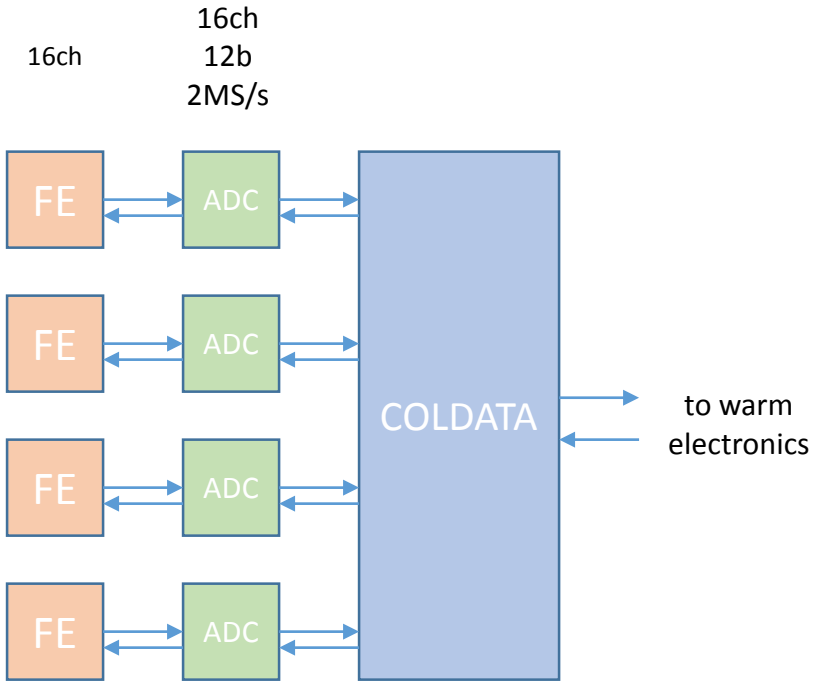
FLORA initial front-end concept

Smallest input charge is 1ph@250eV yielding ~70e-. This requires an ENC (equivalent Noise Charge) of 10e- rms (or less). Largest signal 1000ph@2000eV ~ 0.55 Me-. A low power, small area frontend that deals with an input charge this large (@1.2V) and maintains a 10e- input-referred noise is very challenging. Analog readout @ 10kfps would require very low noise and very fast settling time paths+ system complexity using off the shelf ADC is high. Digital readout would require low power small area in-pixel ADCs + multi Gbps data transmission.

Davide Braga

COLDATA (Cold Digital Data) ASIC for **DUNE**

(*Davide Braga, Jim Hoff, Alpana Shenai*)



- Data concentrator and readout chip for DUNE LAr TPCs
  - 1.5Gbps In , 2x 1.2Gbps Out
  - data readout and control between cold and warm electronics
  - system clock interface

- Digital chip with mixed-signal components

- **Challenges**:
  - Low power/high speed: 65nm CMOS process
  - Reliability: operate at 89°K for >15 years without maintenance
    → custom logic library designed to avoid premature degradation
    → custom models for accurate simulation provided by external company from Fermilab test structure
    → accurate cold timing models provided by UPenn
  - Fully digital chip:
    → new workflow/EDA tools
    → clock domains synchronization
    → test coverage and verification

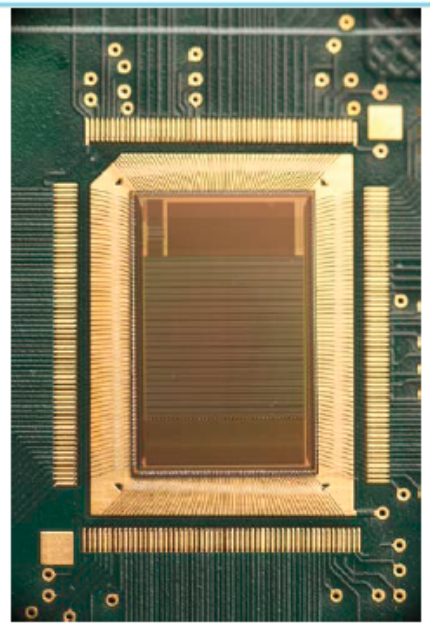
Fermilab ASIC group responsible for most of the chip design, plus top level assembly and verification; collaboration with Southern Methodist University (PLL and Line Driver) and University of Pennsylvania (library characterization).

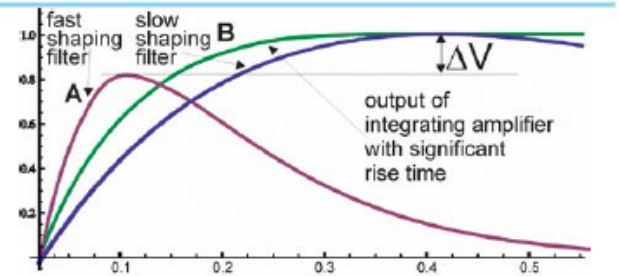
Farah Fahim

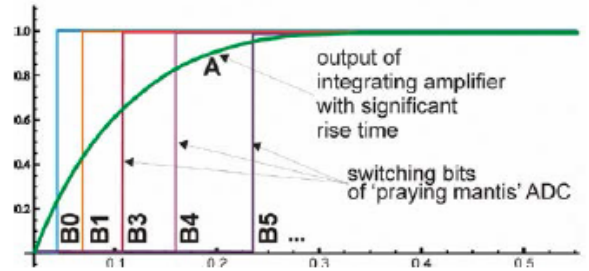
Fermi CMS Pixel (FCP130) – CMS Phase II forward Pixel – Synchronous concept

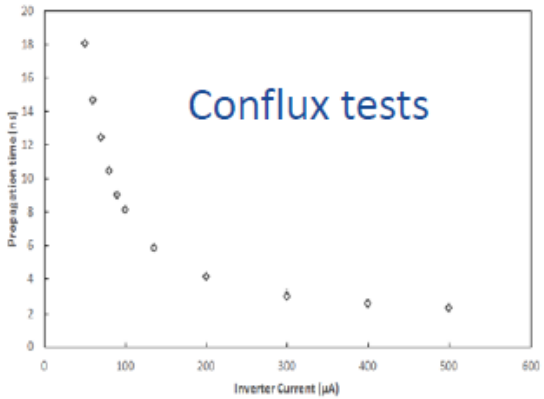
- Novel Synchronous front-end concept for CMS Phase II forward pixel
- Correlated double sampling for noise reduction
- ½ BXClk cycle for reset & ½ for compare
- Version 1- Issues:
  - Unbiased and wrongly Biased Deep N Wells
  - Substrate contacts instead of Antenna Diodes
  - Thresholds are parasitically connected
- However: Successful Preliminary Qualitative analysis
  - Preamplifier response can be monitored; change of current is feedback loop changes the return to baseline.
  - All comparator response times are changing with change in threshold voltage
- Configuration register is able to able to correctly program the pixels
- The serial mode of transfer in FIFO 2 daisy can correctly send data Out
- The Spy signals for last superColumn (Pixel Hit, ADC value and address can be correctly monitored)
- Conflux performance could be measured

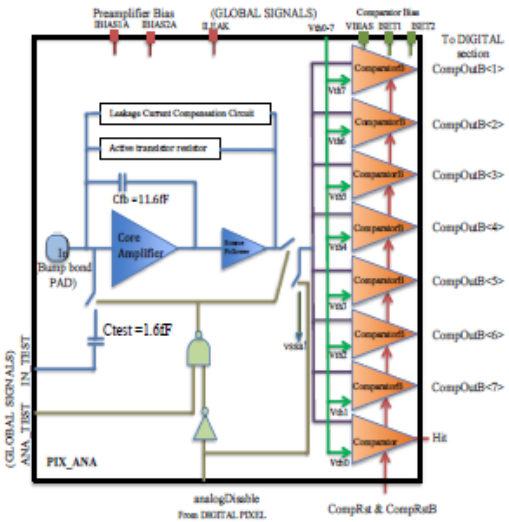
- Version 2- Status
  - Change in Preamp and comparator
  - All other bugs fixed
  - Top Level changed for only 1 design
  - Submission on 6th Nov 2016







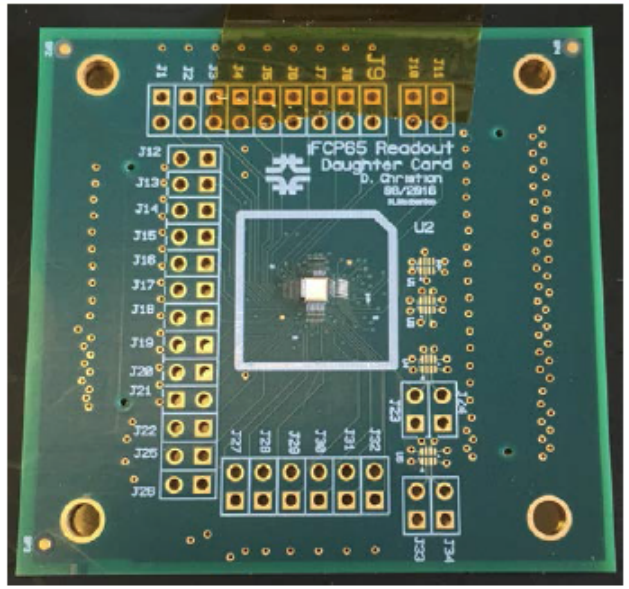


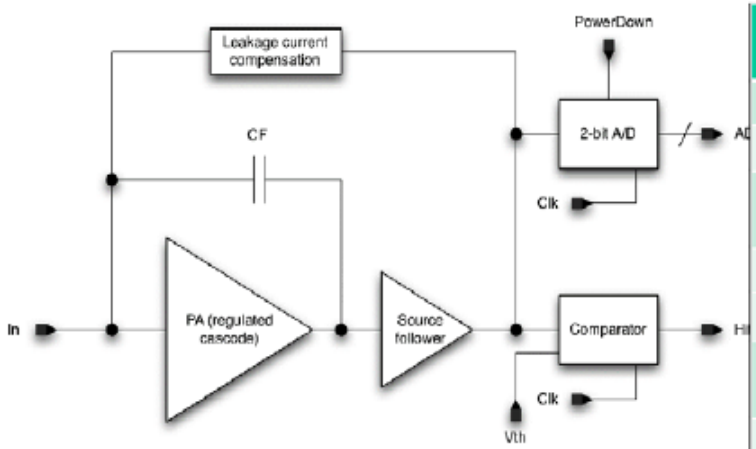


Fermilab

INFN- Fermi CMS Pixel (IFCP65): Translation of FCP130

- Collaboration with INFN (U.Bergamo)
- Front-end with 2 bit ADC redesigned in TSMC 65nm
- Test structure of 16 x 16 matrix submitted in May 2016
- Detailed tests to be carried out both at Fermi and U.Bergamo (Radiation tests at U. Padova)
- Designed to meet constraints set by RD53A chip for submission in Feb –March 2017
- Implemented design has extremely low noise but higher power consumption





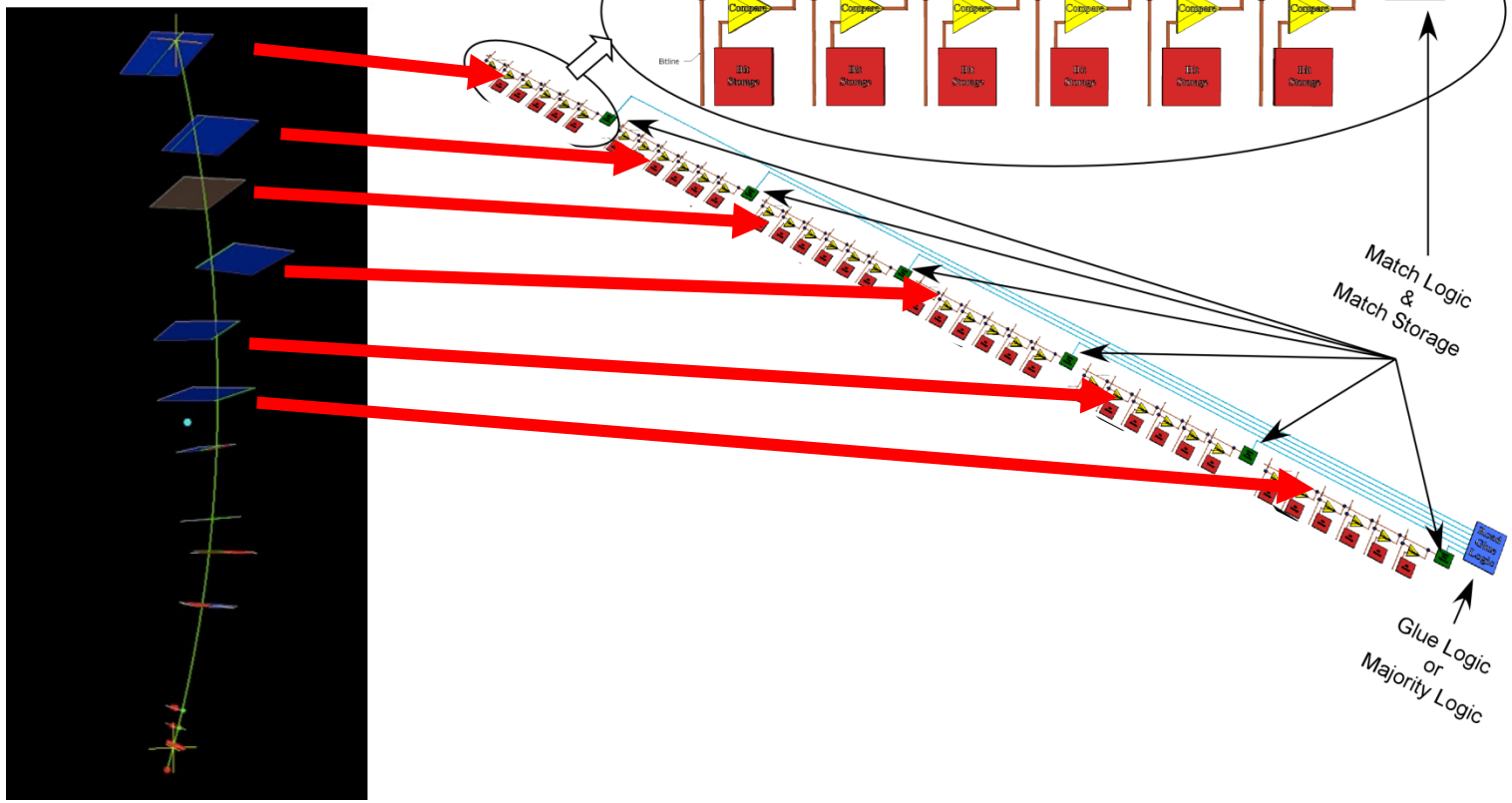
	TT	TT 500 Mrad	SS	FF	FS	SF	spec
Charge sensitivity [mV/ke]	10.3	10.2	9.1	11.7	9.9	10.4	-
ENC rms [e]	79	79	82	76	83	77	-
Threshold dispersion σ(Qth) rms [e]	35						-
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	86						≤126
In-time overdrive [e-]	NOT applicable						≤ 600
Current consumption [μA/pixel]	5*						≤ 4
Delay time [ns]	10.8	12.1	11.0	10.5	10.8	10.9	-
ADC Conversion time [ns]	12.5	12.5	12.5	12.5	12.5	12.5	-

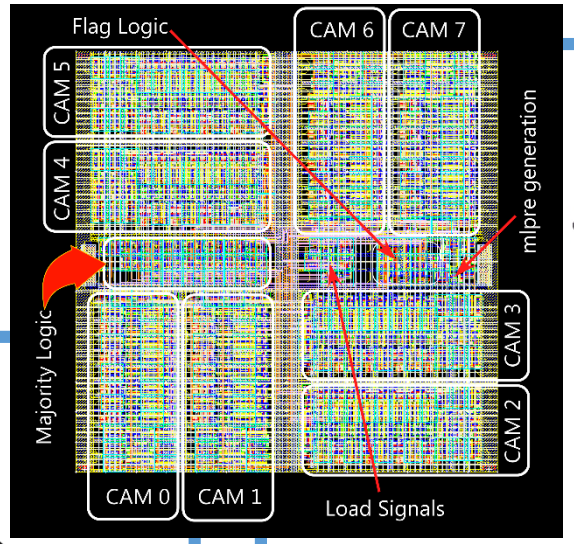
Jim Hoff

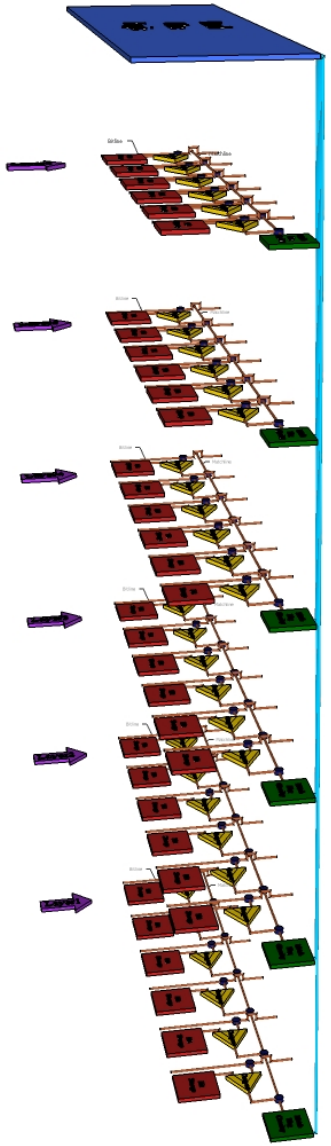
VIPRAM

Jim Hoff
Jamieson Olsen
Alpana Shenai

The PRAM Idea – Track Fitting through Associative Memory Pattern Recognition



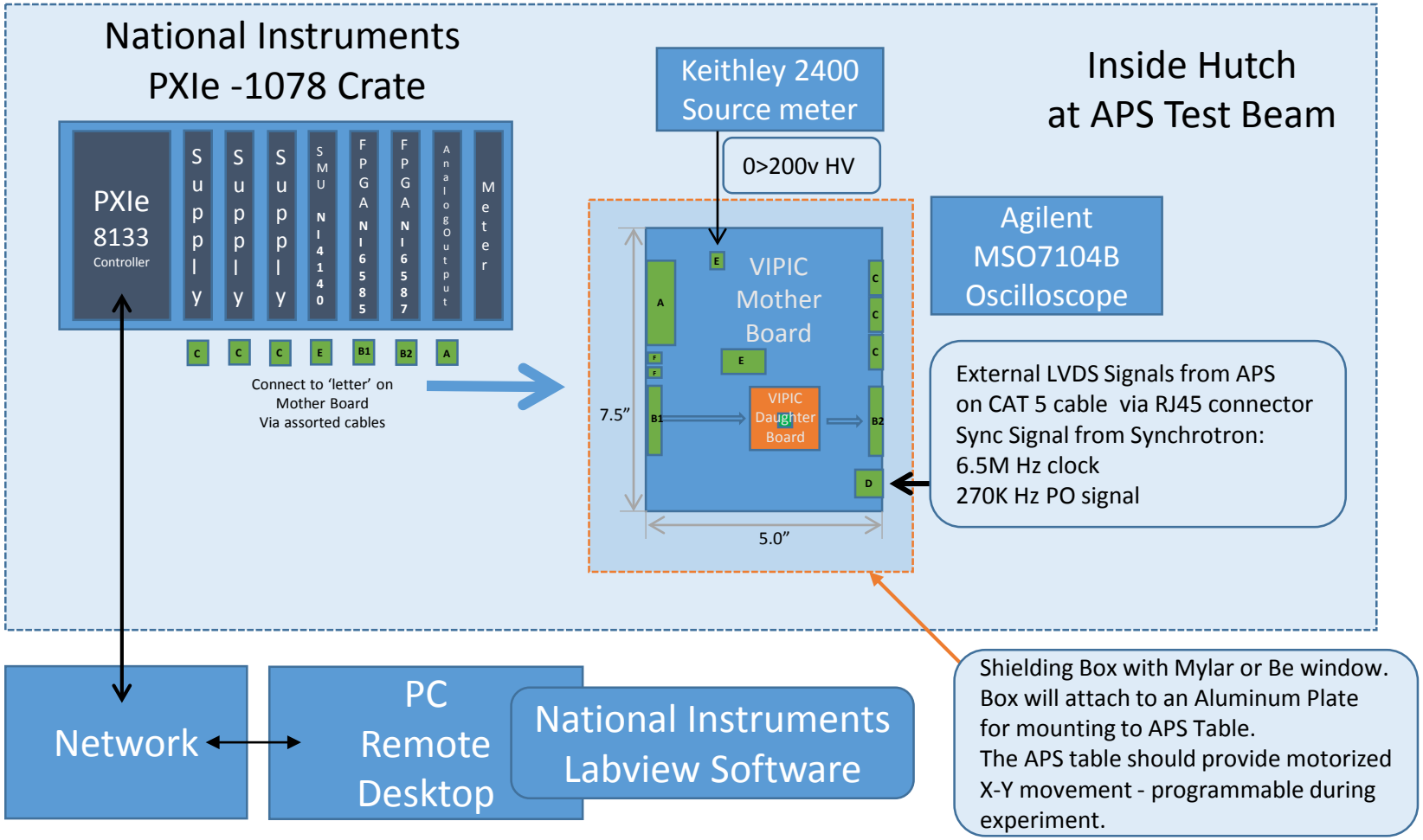


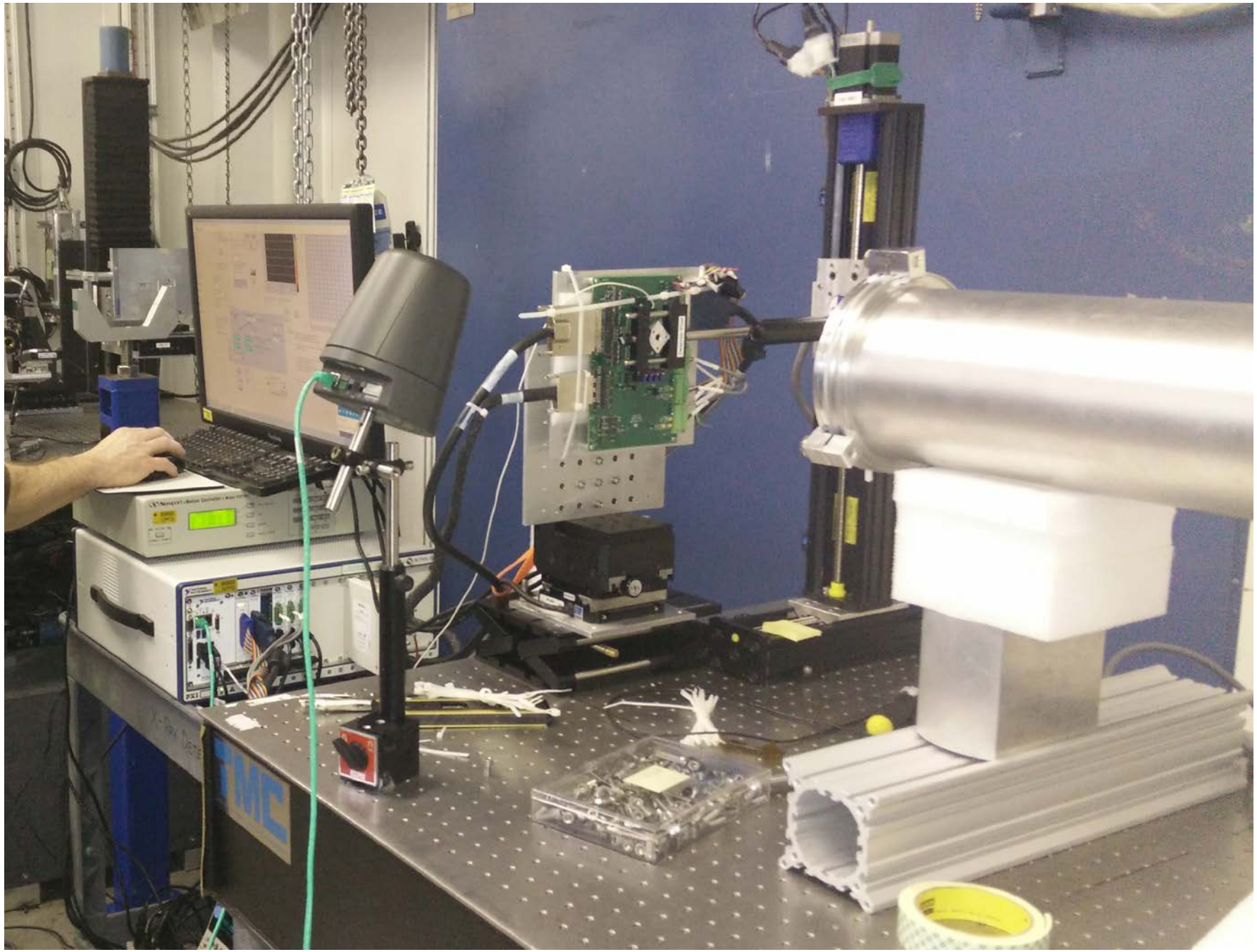


The VIPRAM Idea – Performance Improvement through Vertical Integration

Scott Holm

Crate Dimension : 40cm x 40 cm x 25cm tall
The cables coming out of the modules will extend out of the modules about 10cm before they can bend.
The shortest cables are 1 meter in length(they are custom cables from National Instruments).





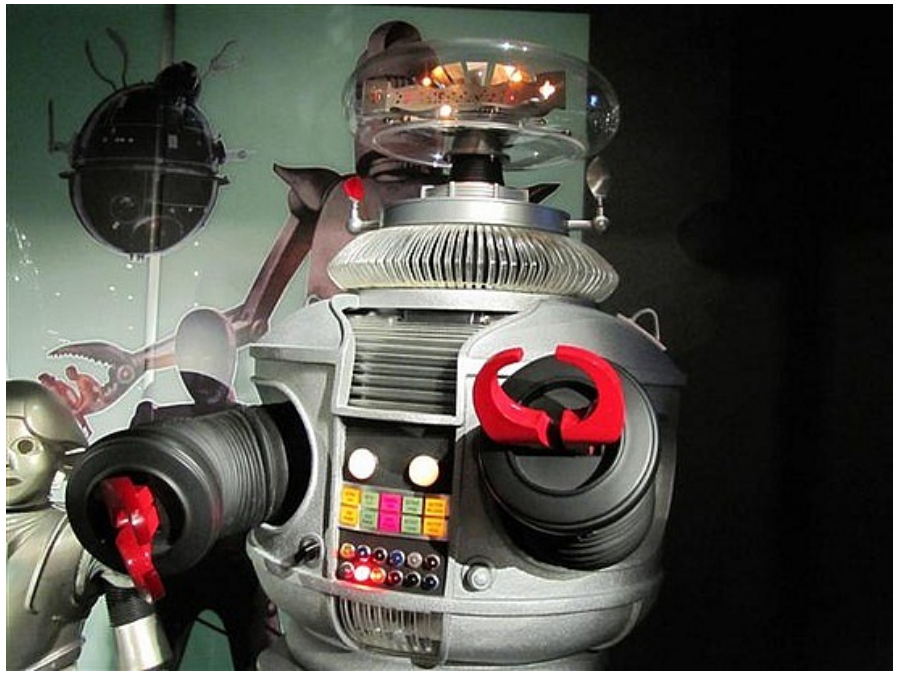
Lou Dalmonte

ASIC Production
Test Robot

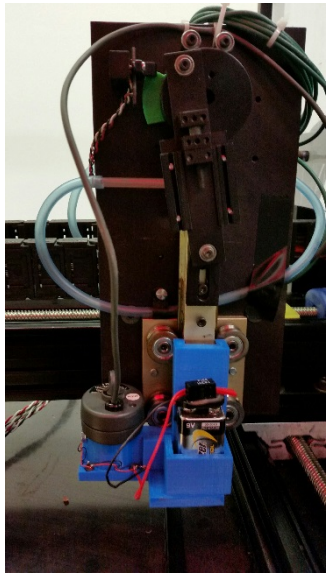
Lou DalMonte – EED ASIC GROUP

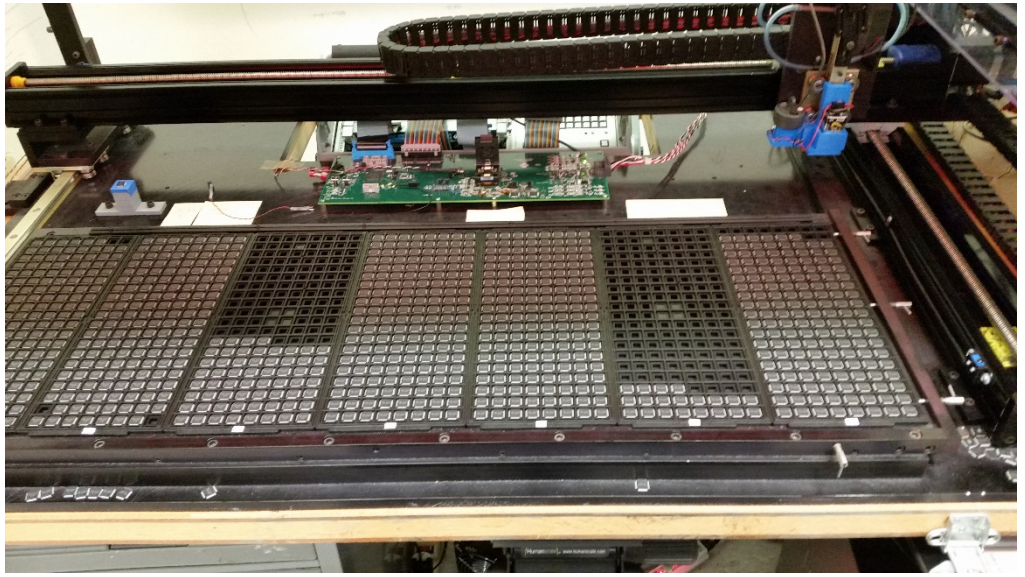
other EED INFRASTRUCTURE

DANGER WILL ROBINSON, DANGER!



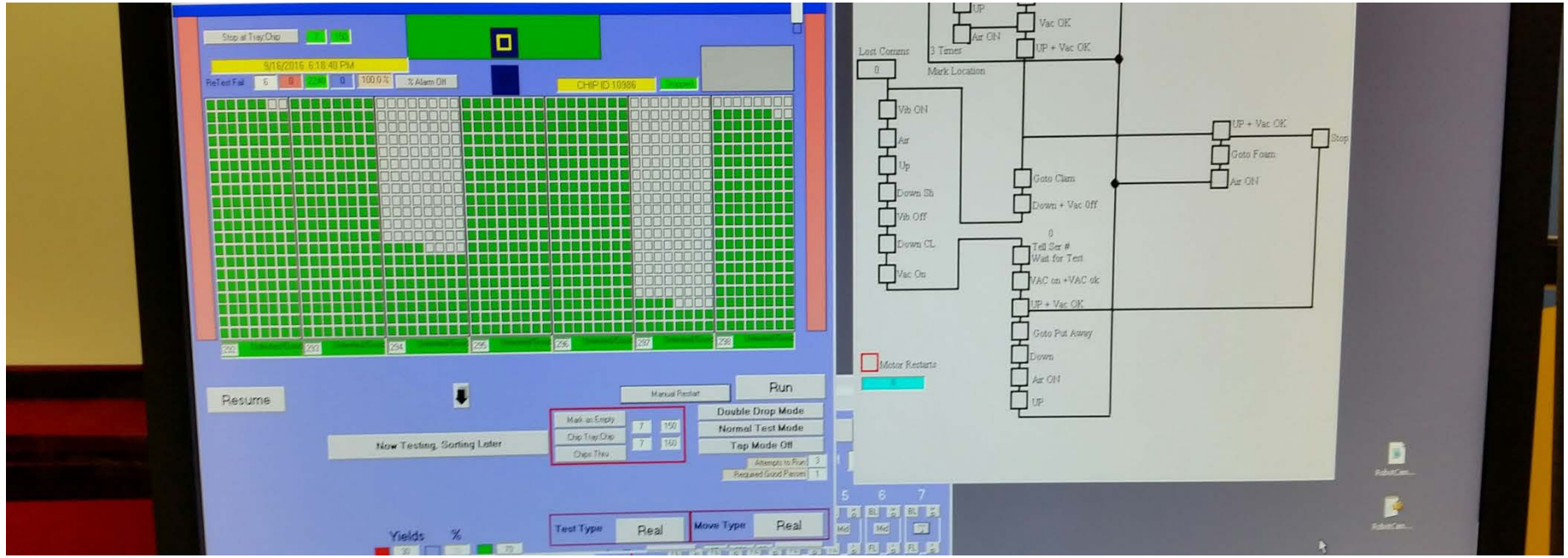
The Robot we wish we had





2016 YEAR REVIEW

- 2016 QIE10 ASIC's Tested - approx. 7600
- 2016 QIE11 ASIC's Tested - approx. 12000
- 2016 QIE11 ASIC's To Be Tested - approx. 23000



- Inauguration date 2009??
- Alan Baumbaugh designer. (Mechanical & Software)
- Final documentation in progress for future support.
- Manpower Requirements
  (Maintenance, Repairs , Operations , Upgrades)
- Second Robot in the works, waiting for FPGA design.
- Upgrade to National Instruments Control is being discussed.

Al Dyer

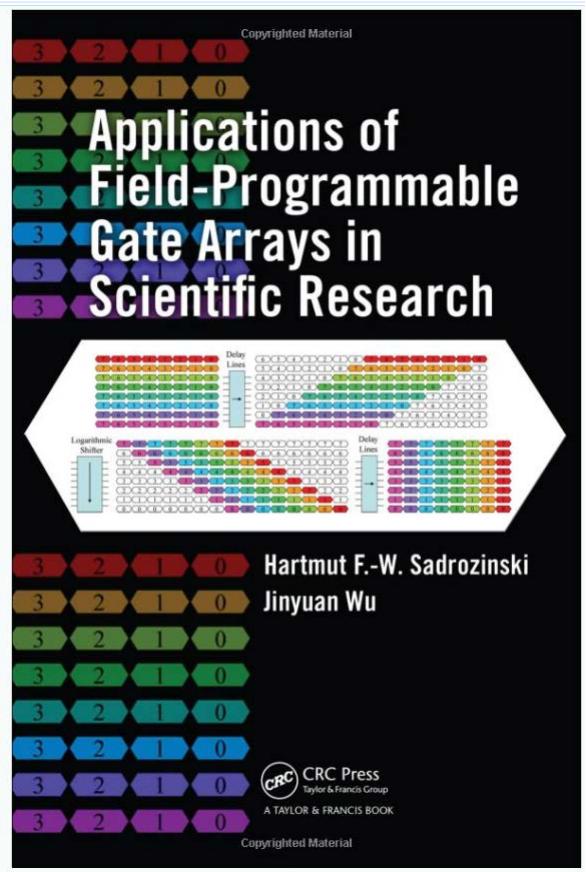
Clean Room

- **Cleanroom** : 2 probe stations for testing silicon wafers, one manual and one automatic. ASIC's storage. Wire Bonding. PCB assembly.
- **Cyro-cooler** : located in a lab area on the northeast side of the floor can provide testing from room temperature down to cryogenic temperatures.
- **Westside Surface Mount Lab** : flexibility to assemble circuit boards as well as any type of re-work required.
- **Albert's Messy Lab Area** : For all things possible!

Jinyuan Wu

Jinyuan Wu

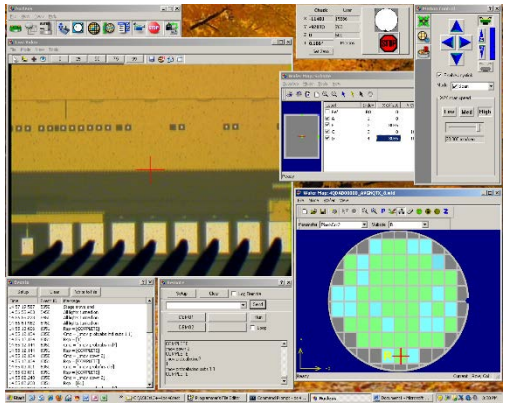
- Short CV:
  - 1997 Fermilab
  - 1995-1997: RA: Colorado
  - 1992-1994: Post Doc: Penn State,
  - 1986-1992: Ph. D. Student: Penn State
- Current Projects:
  - Accelerator Protection System (NML & PIP-II)
  - SeaQuest
- What I can do for other colleagues:
  - FPGA Based TDC
  - RAM-based Histograms
  - Data Organizers …

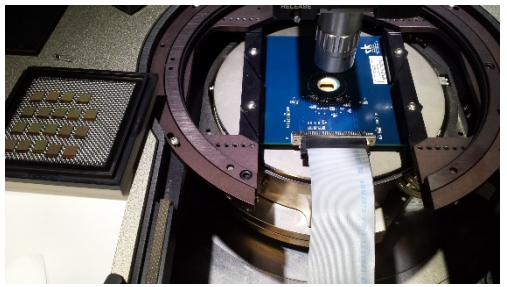


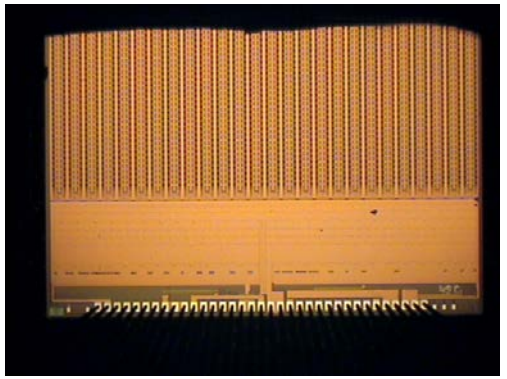
Christian Gingu

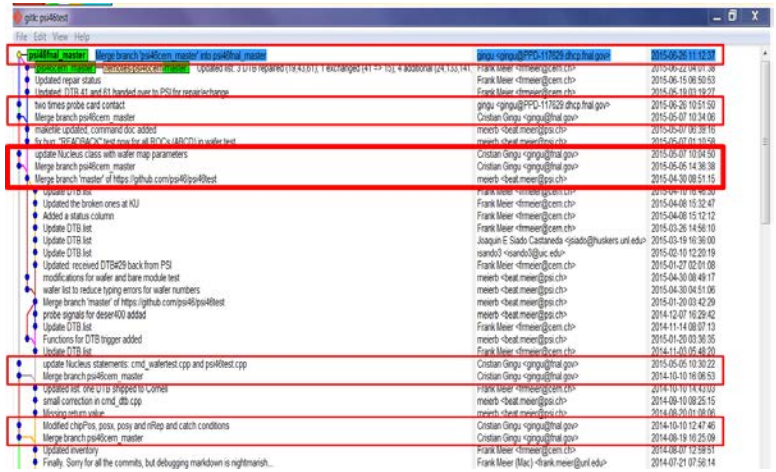
On wafer chip testing using Cascade Probe Station (1)

- Six production batches with 118 wafers for CMS Pixel - ROC PSI46dig tested (2015 and 2016)
- Using DTB hardware (PSI), probe card (FNAL) and C++ software (PSI source code with FNAL modifications for our automatic probe station interface and data base files creation)
- Git repository used for PSI46dig test application
- Creating Xml files for Fermilab data base
- Updating C++ grlog application (PSI) for FNAL wafers maps
- Very good agreement between PSI and FNAL test results
- Detailed reports at https://cms-docdb.cern.ch doc#12279, 12445, 12502, 12634, 12650 and 13085







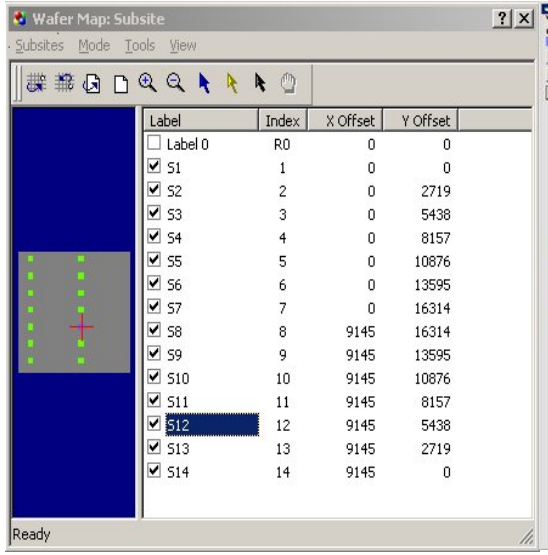


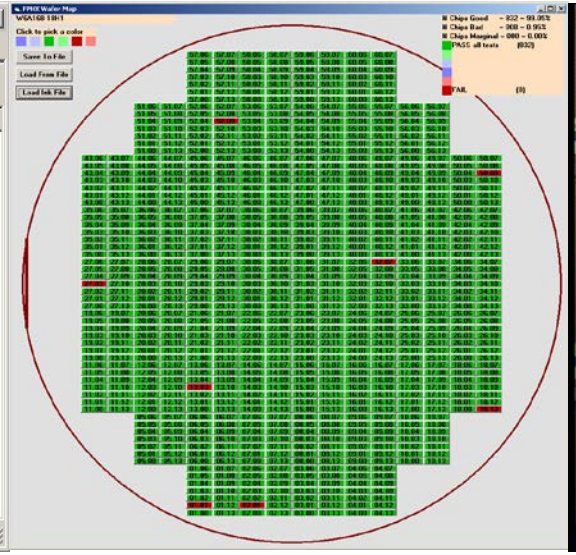
On wafer chip testing using Cascade Probe Station (2)

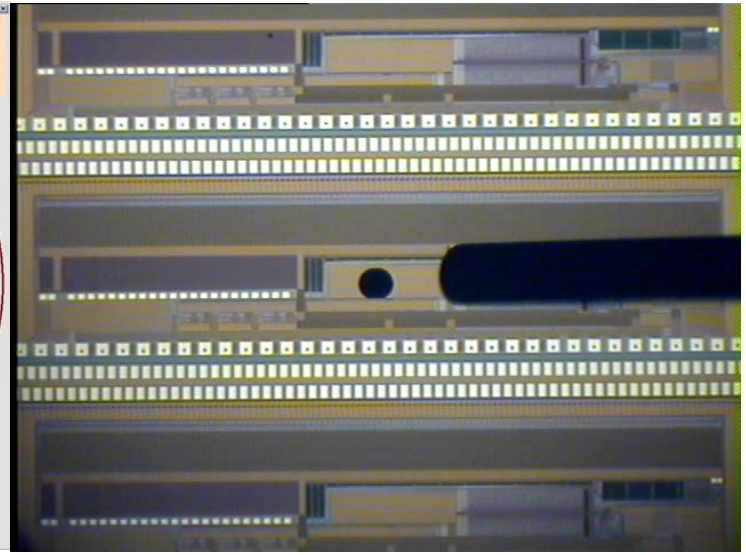
- Testing 8 wafers with FPHX chip for PHENIX Group (BNL) in 2016; more wafers are expected to come.
- Using ASIC Testing System with interface board, probe card and test script program developed at FNAL (*Alan Baumbaugh* and *Louis Dal Monte*) with modifications for our automatic probe station interface and test file reports for every chip.
- Established analog level cuts; provided wafer inking and wafer maps for dicing.

The following is a summary of main tests performed and the FailCode bit they set. The tests are listed in the order they are performed.

1. Power supply test.	Sets bit 00.
2. Sync words.	Sets bit 01.
3. LVDS data levels.	Sets bit 02.
4. Registers.	Sets bit 03.
5. Timestamp.	Sets bit 04.
6. Defaults.	Sets bit 05
7. Chip ID.	Sets bit 06.
8. LVDS scan.	Sets bit 07.
9. Dual data port.	Sets bit 08.
10. Kill inject mask.	Sets bit 09.
11. Internal DAC hits.	Sets bit 10.
12. External gain.	Sets bit 11.
13. Internal DAC ADCs.	Sets bit 12.
14. Channel test – the Drake.	Sets bit 13.

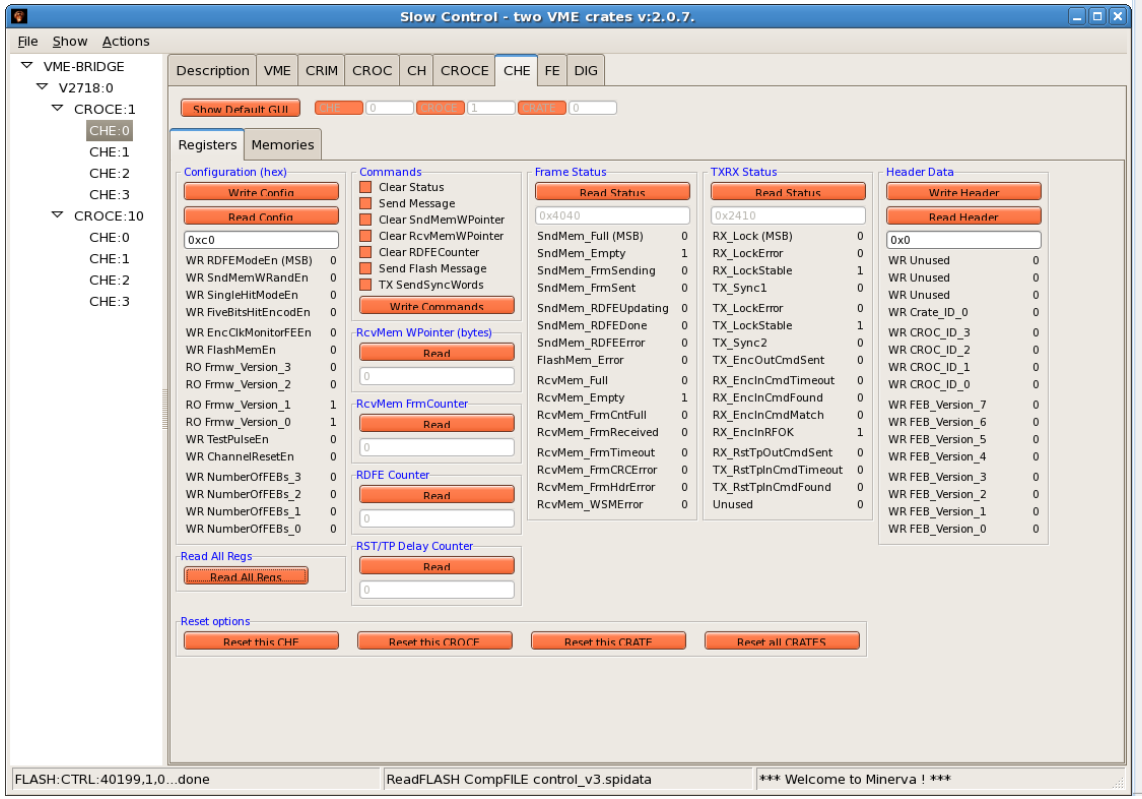


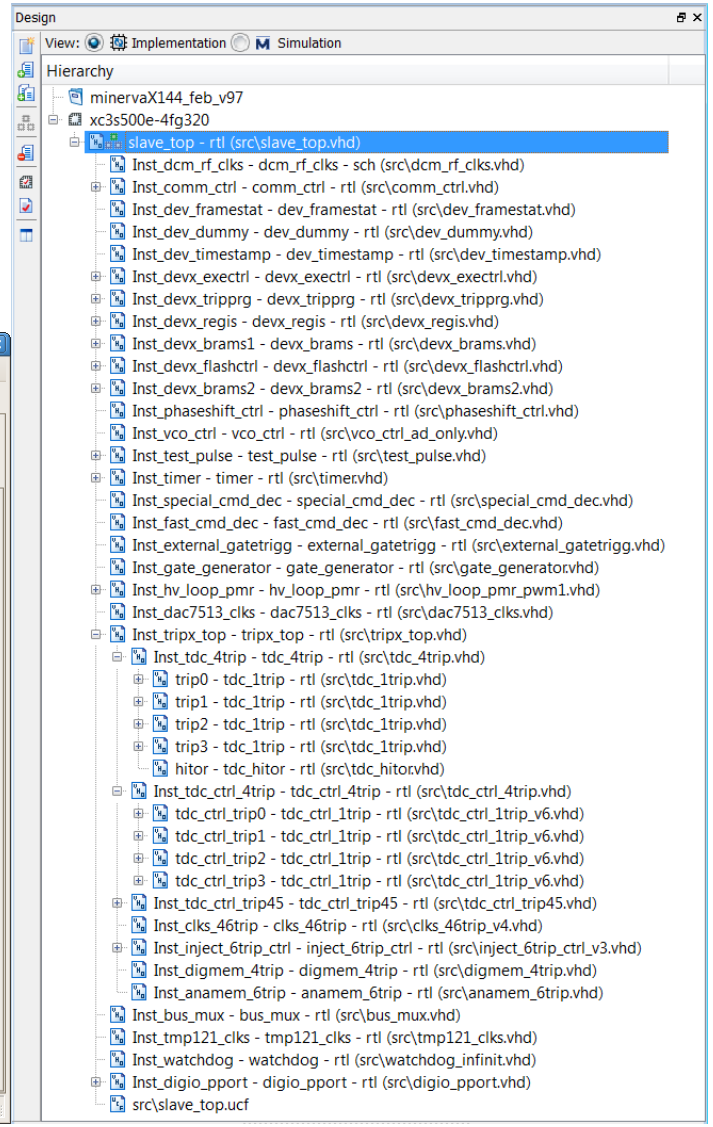




Contributions to Minerva (high luminosity, 2015-2016)

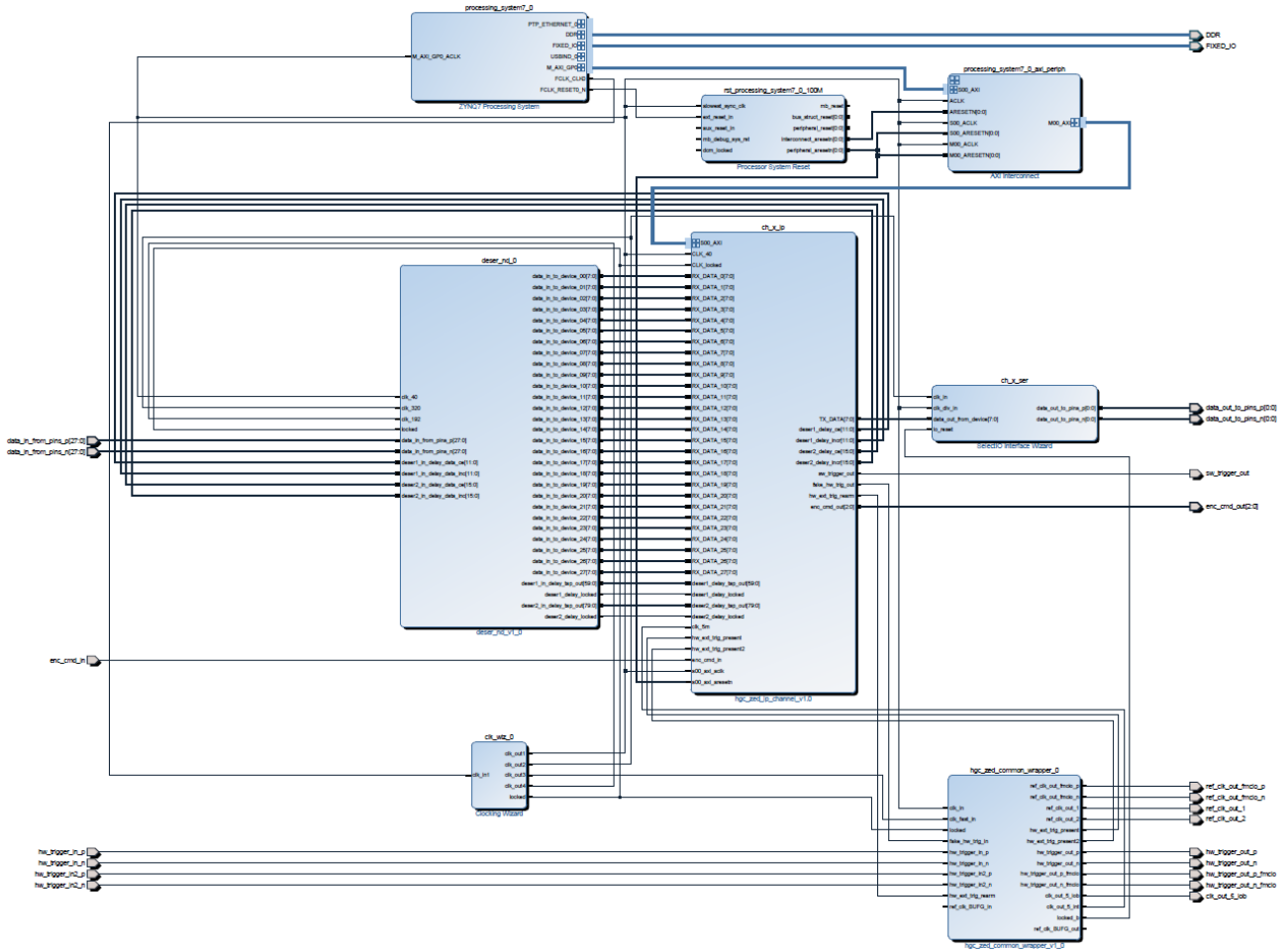
- FEB firmware update (v97, Xilinx) includes: new sequencer features, 20 hits readout, TRIPTs chips push independent or in pair, 4-modes digitization
- CROCE firmware updates (v4-5, Lattice, Diamond)
- Slow Control (Python)





Contributions to HGC (2016)

- Started with *Paul Rubinov* ; wrote firmware for the commercial Zed Board (Xilinx ZYNQ) and for the custom readout board FMCIO (Xilinx ARTIX) using Vivado IP driven environment

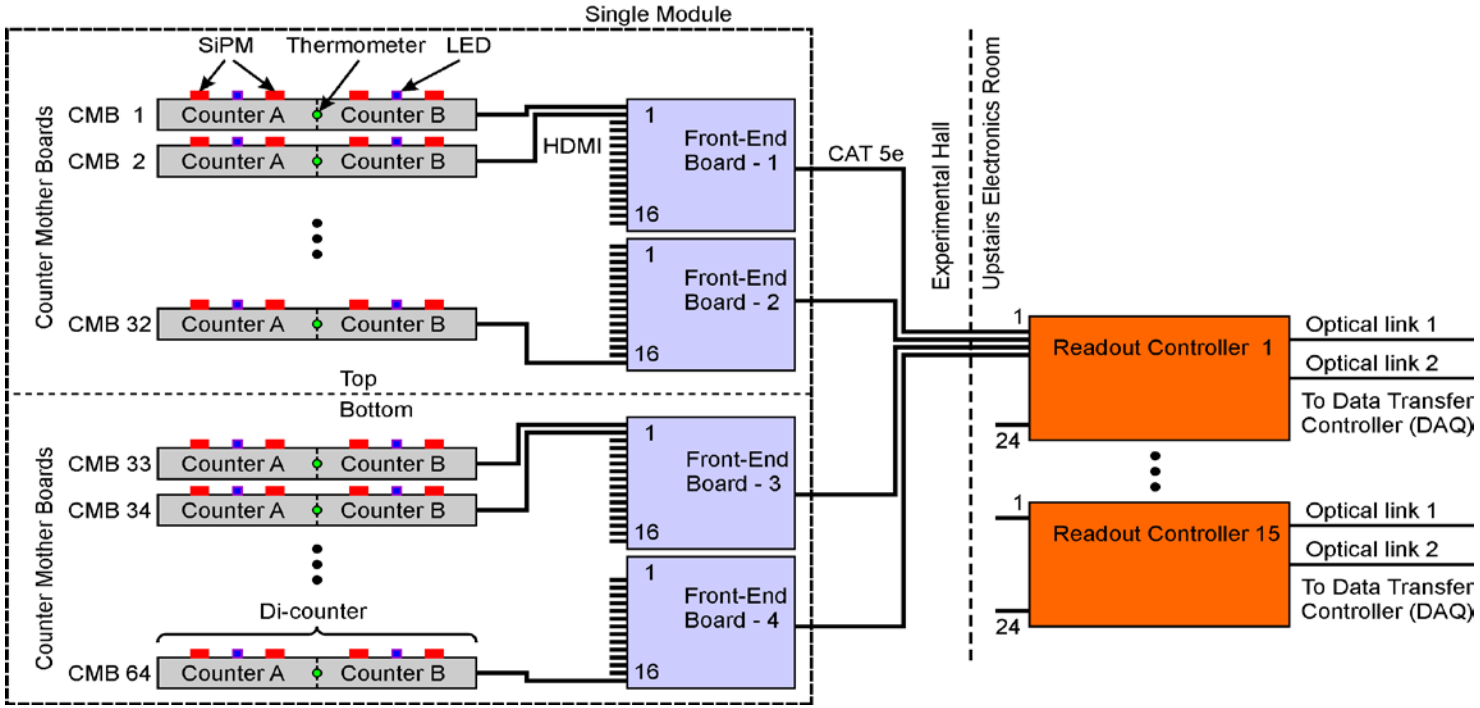


Sten Hansen

Detector Electronics Sub-group (Terry + Sten)

1. Mu2e: Cosmic ray tagger electronics consisting of three parts:

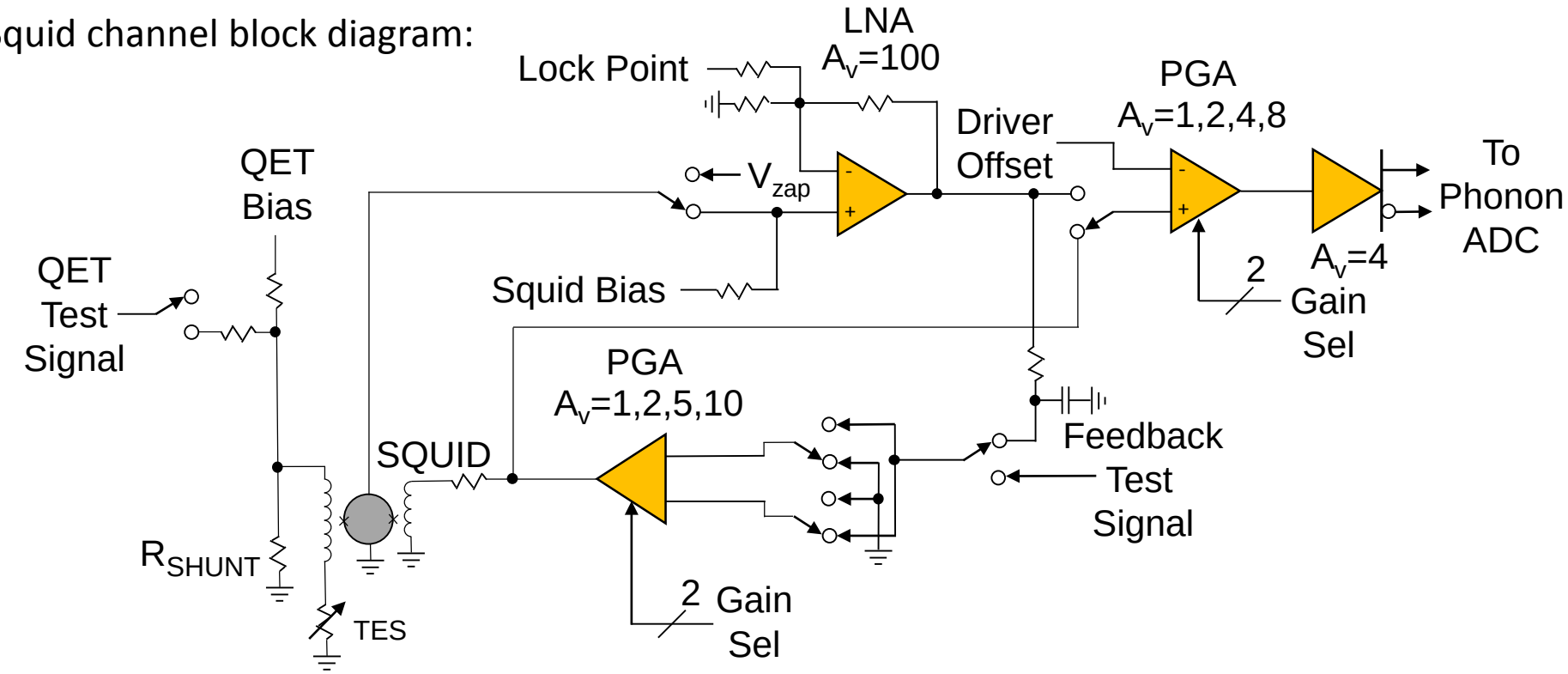
- Counter motherboard. Mounted on end of a scintillating extrusion servicing four SiPM photodetectors.
- Front end board mounted on the side of the extrusion panel digitizing 64 SiPM signals coming from the CMBs.
- Readout controller. Installed in the electronics room. Collects data form 24 FEBs.
- 5000 CMBs, 325 FEBs, 15 controllers in the system.



2. CDMS: Warm electronics consisting of three parts:

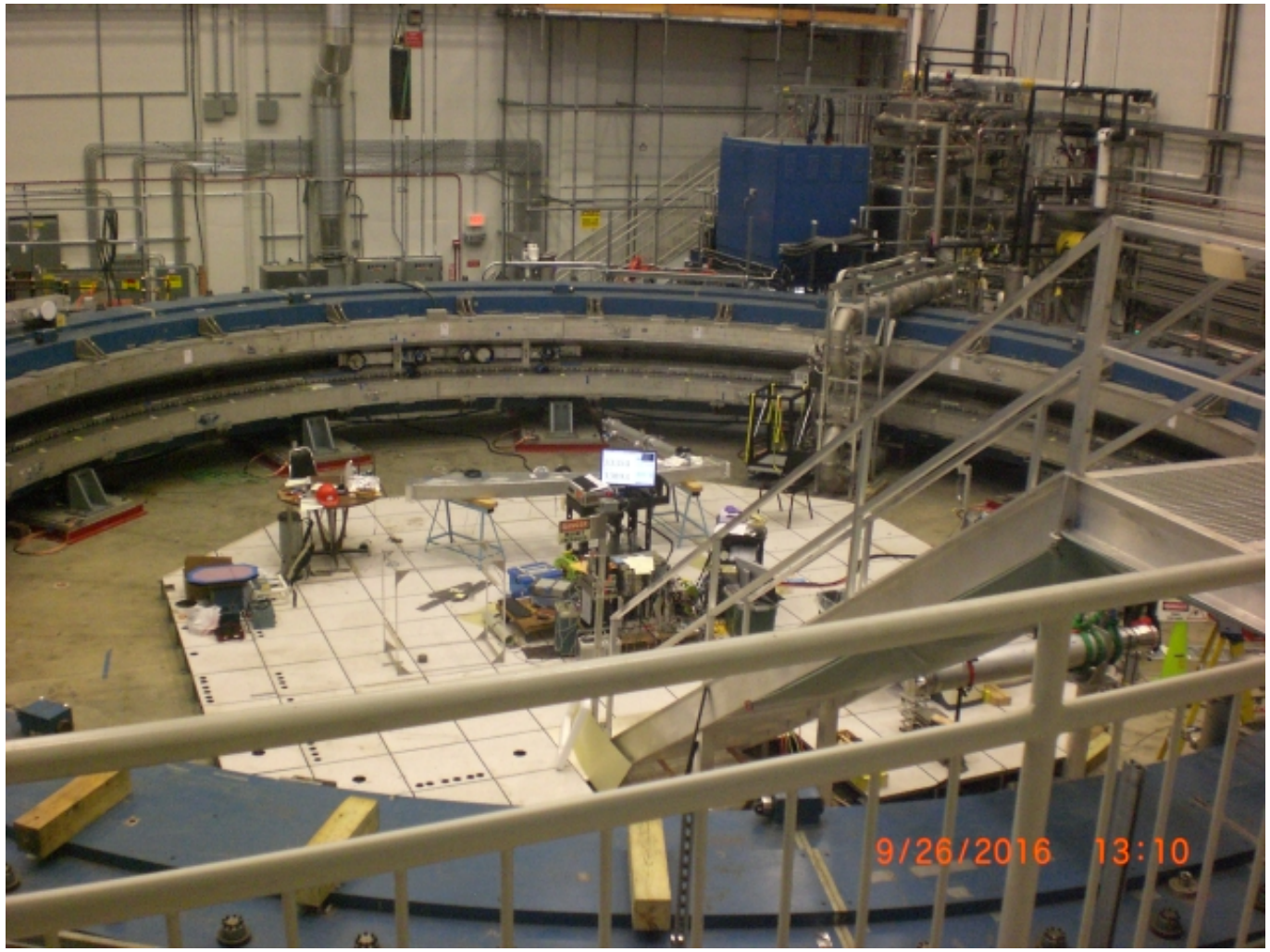
- Digital control and readout card. Controls and reads out 12 Squids and four charge amplifiers. 65 DACs, 110 switches.
- Signal distribution unit. Synchronizes the DCRCs, digitizes acoustic signals for mechanical vibration monitoring.
- Vacuum interface board. Feedthrough board for 600 signals into the vacuum space.
- 30 DCRCs, eight VIBs, 4 SDUs.

Squid channel block diagram:



Steve Chappa

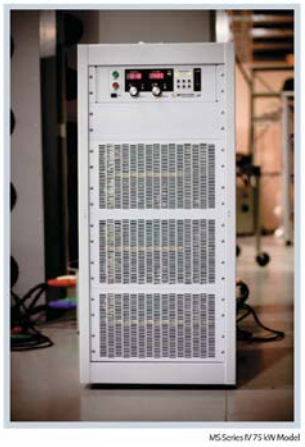
Muon g-2 Project Electrical Engineer



Muon g-2 Project Electrical Engineer

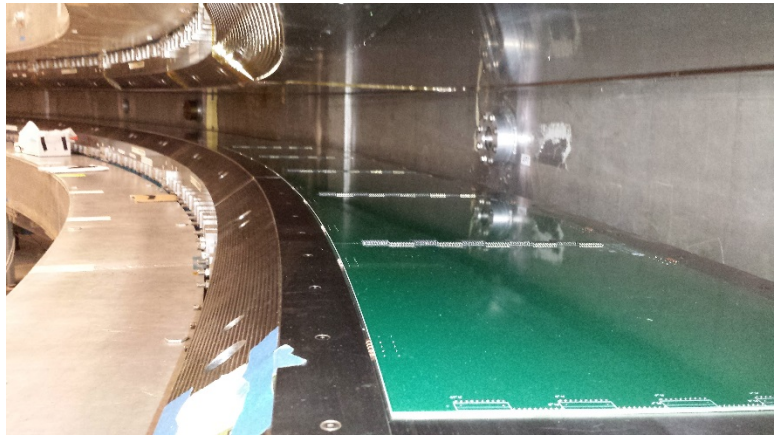
Main Ring Power Supply and Quench Protection

Inflector Power Supply and Quench Protection



AC Power and Grounding Infrastructure

Main Ring Active Shim Coils



Muon g-2 Project Electrical Engineer

Main Ring Beam Systems Installation

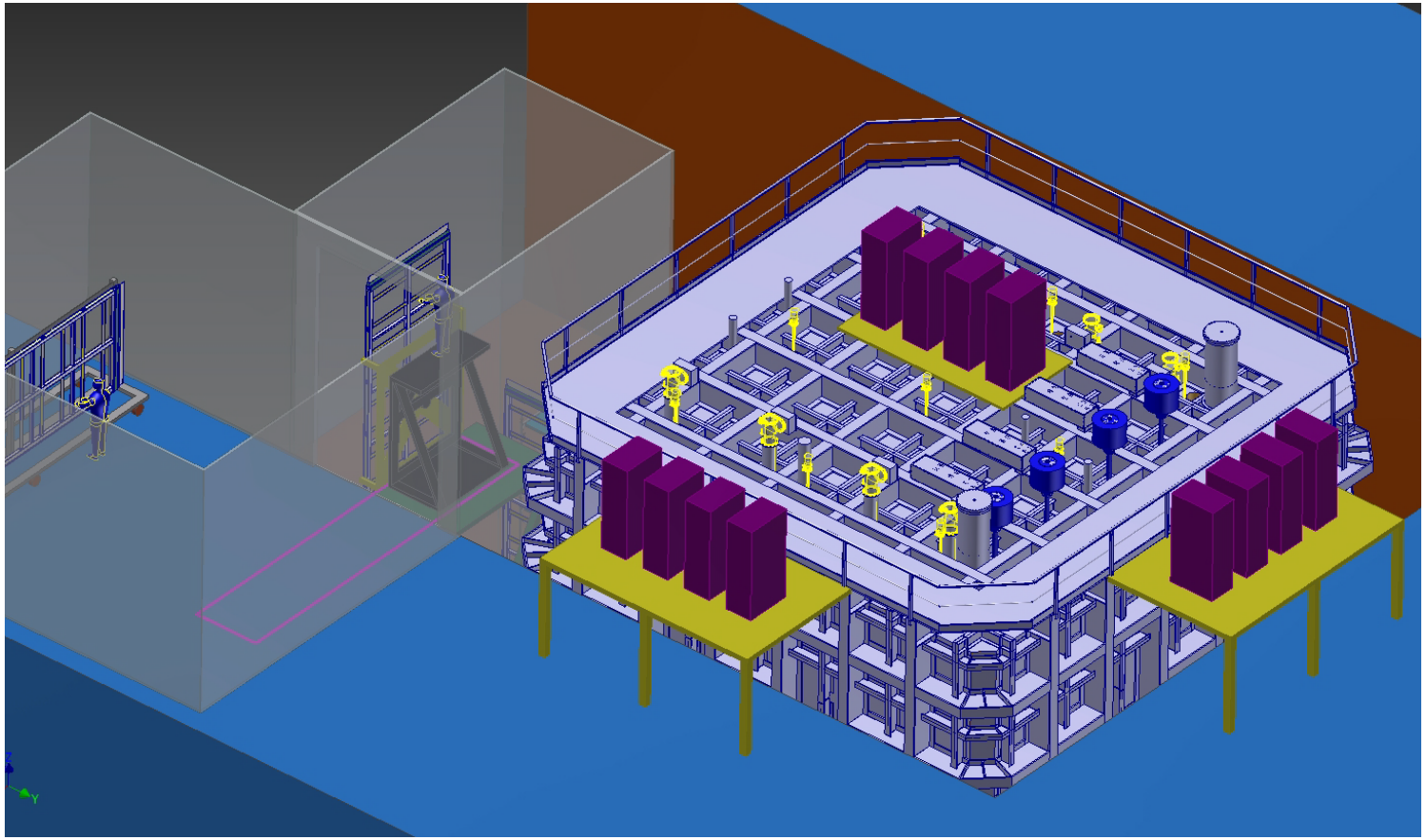
Cable Tray Management

Overseeing Detector Installations

Organizing for and Conducting Electrical Safety Reviews

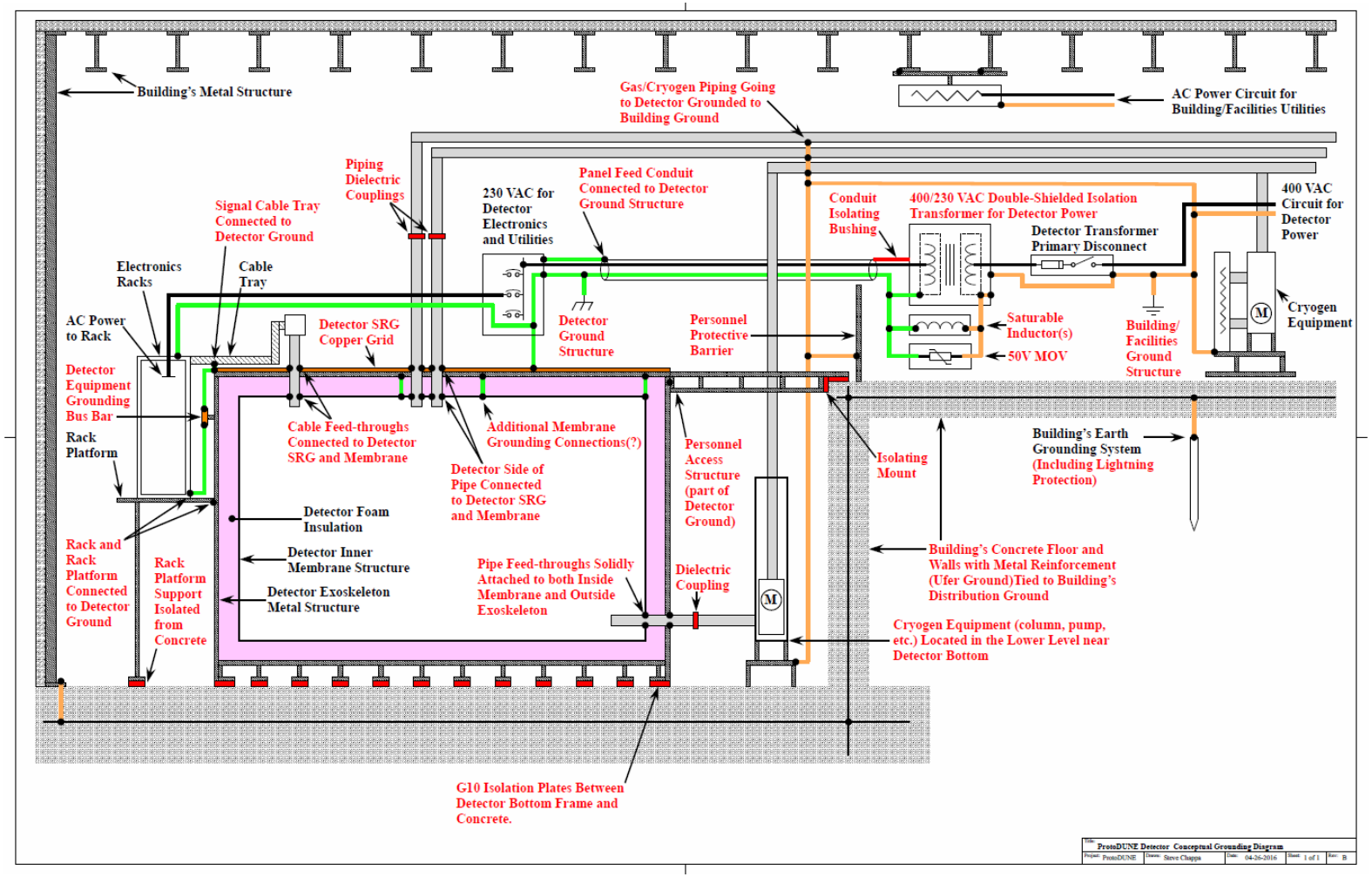
DUNE/ProtoDUNE Electrical and Grounding

At present, developing the grounding and electrical requirements for a DUNE test vessel, or ProtoDUNE. This detector is located at CERN and construction is underway for the service building addition that will house this detector.



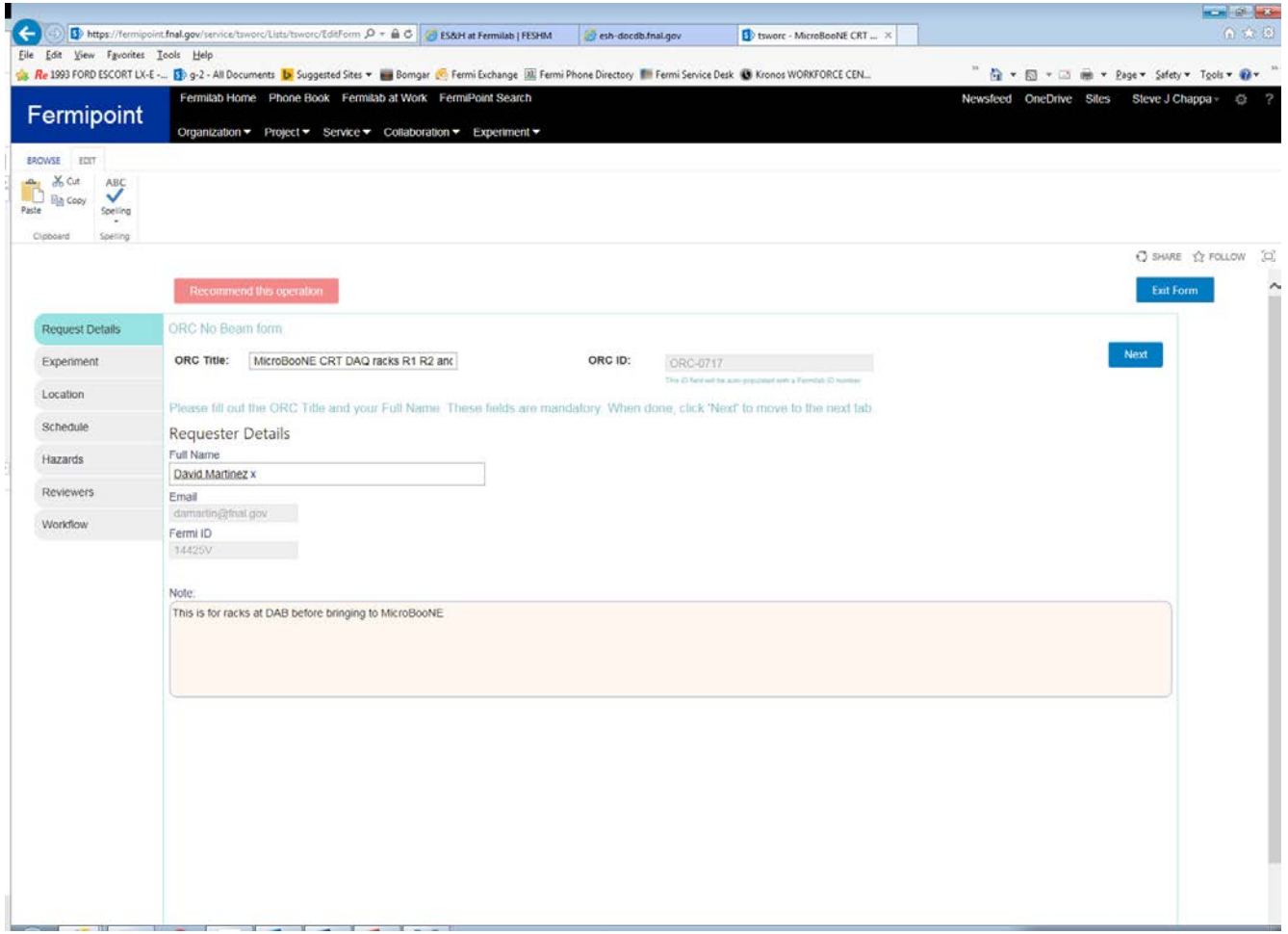
DUNE/ProtoDUNE Electrical and Grounding

In the process, we develop diagrams that provides an easily understandable picture that depicts these requirements. Then, from these diagrams, engineering drawings and documents are generated.



PPD ORCs and Electrical Safety

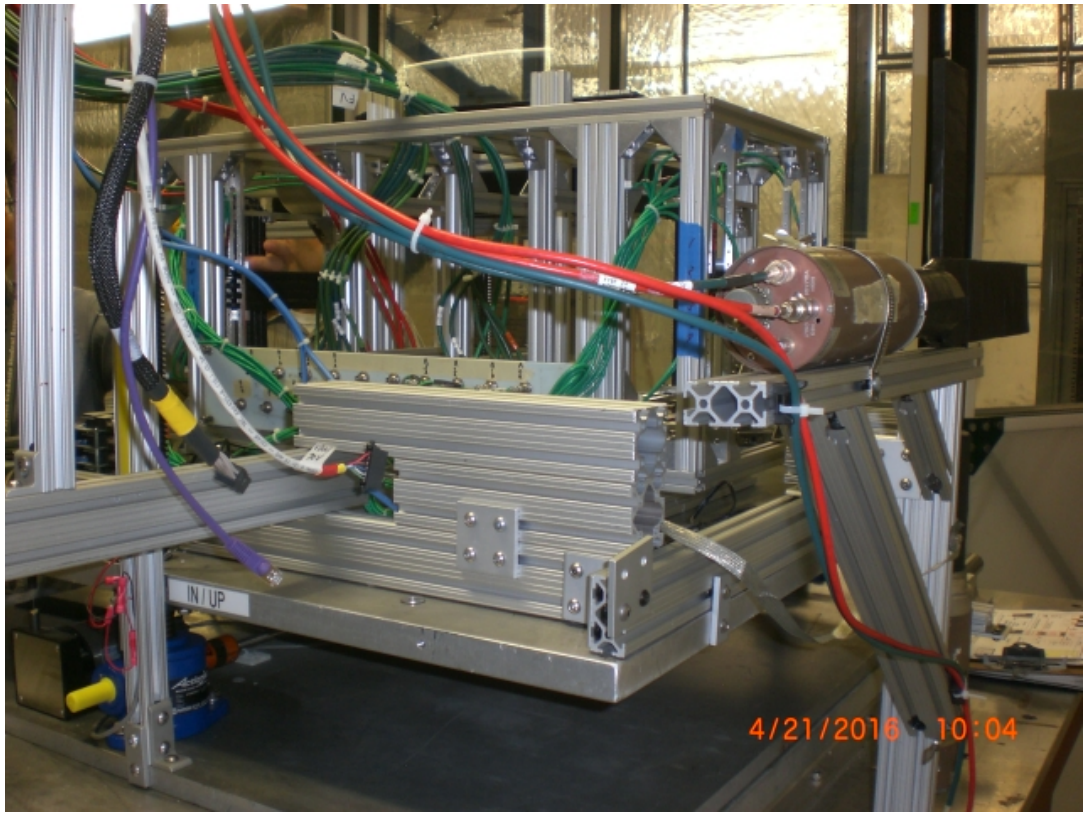
ES&H has developed an interactive webpage where ORCs (Operational Readiness Clearance) for experimental and test installations can be tracked.



PPD ORCs and Electrical Safety

As part of the PPD Electrical Safety subcommittee, serve as a reviewer in the field to examine electrical equipment to be installed for safety and for sufficient mitigation of electrical hazards:

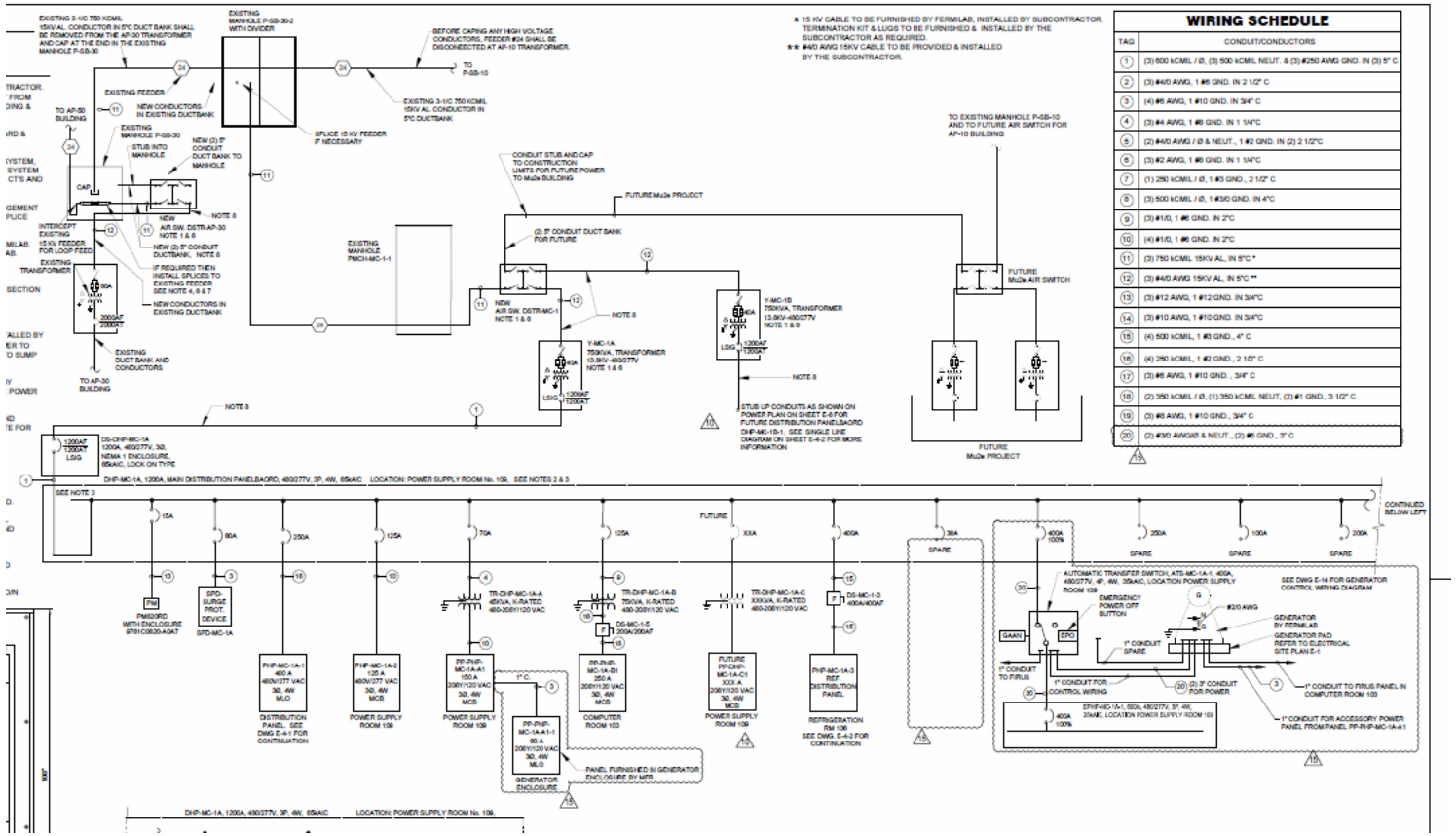
1. Will it shock anybody? (exposed live circuits with high voltage)
2. Will it start a fire? (insufficient overcurrent protection/mitigation)



For example, examine this installation (in the Fermi Test Beam Facility), done by an experimenter or user. Using supplied documentation and by examining it in the field as it is to be used, determine that it is safe for operation.

Hmm…let's see now…

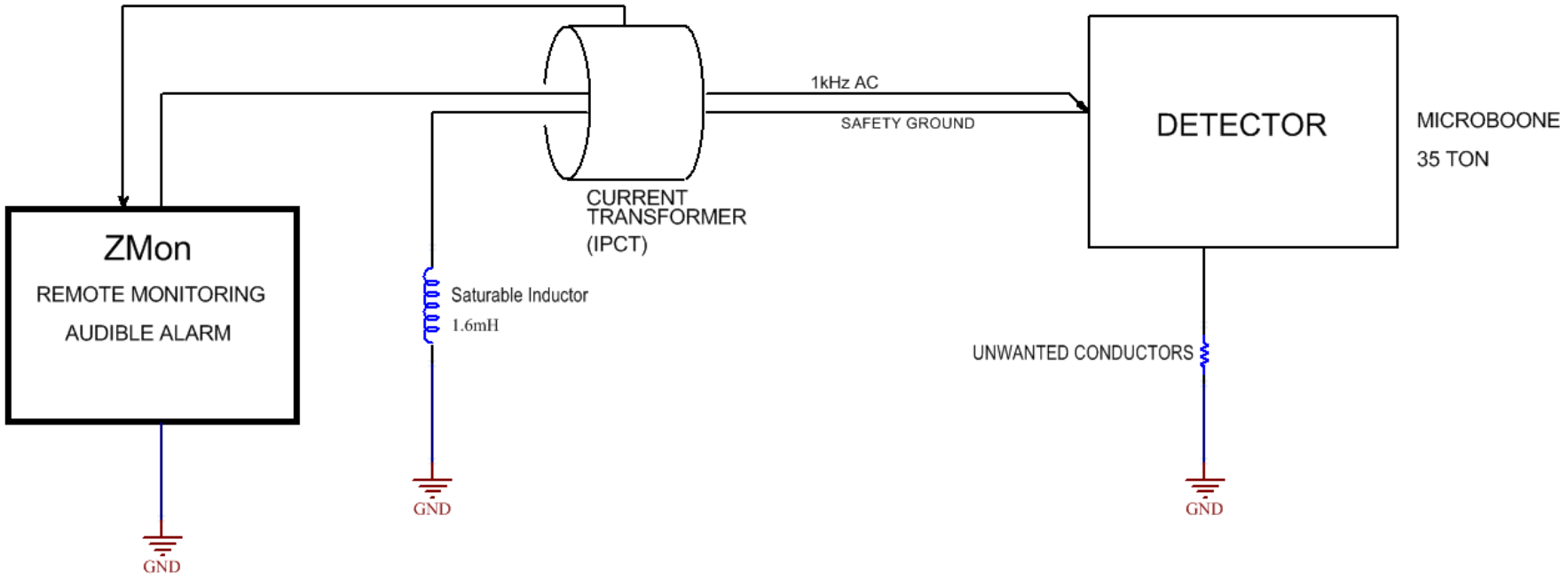
PPD Electrical Installations



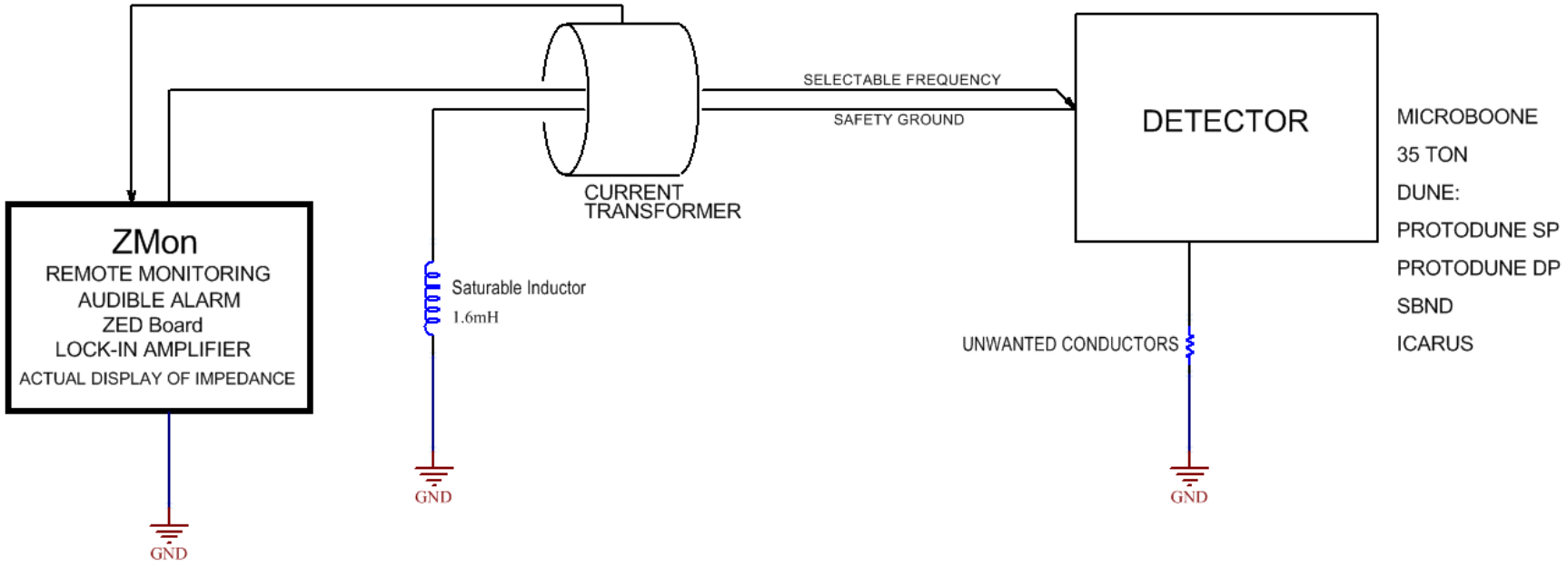
- **Provide engineering support and task management for PPD electrical installations:**
  - Determine electrical load requirements, panel and switchgear requirements, etc.
  - Maintain and update installation Single Line Electrical Drawings (SLEDs)
  - Maintain and update electrical panel schedules (individual circuit assignments)
  - Evaluate installations for safety according to NFPA-70E (arc-flash calculations)

Mike Utes

Impedance Monitor for New Detectors



Impedance Monitor for New Detectors



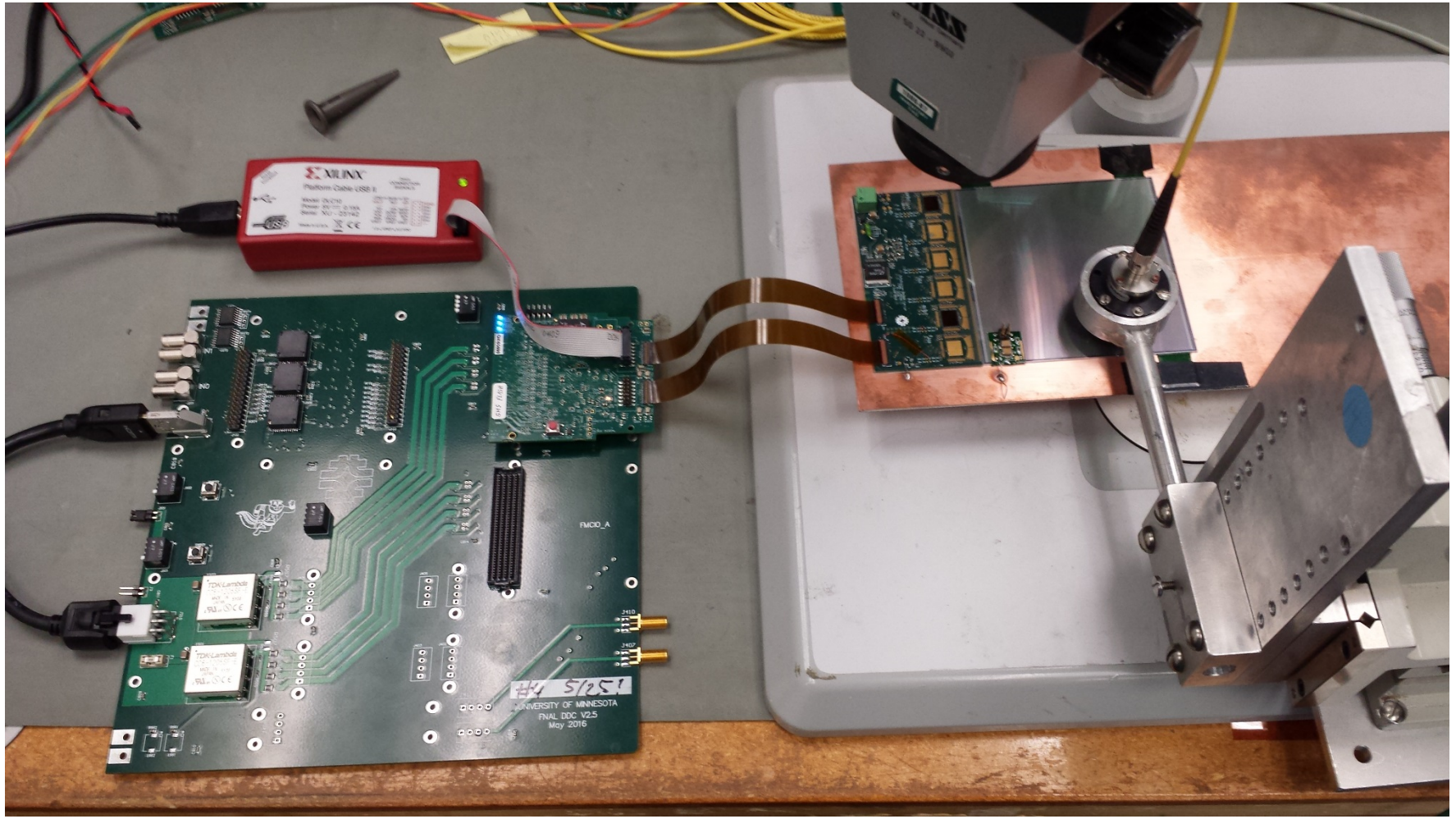
Impedance Monitor for New Detectors

Silicon Scanner for Muon Tomography

R&D for NSTec (National Security Technologies)
Nevada Test Site

Main application is for nuclear material imaging
for homeland security.

Silicon Scanner for Muon Tomography



Thanks for coming!