PPD EED Department Meeting

27 September 2016

EED Department

• Department News

- Lots of retirements, some new hires
 - Welcome to Vadim Rusu Duty Head of EED
 - Welcome to Brian Hess Technician
 - Welcome back to Abder Mekkaoui
- Department Org Chart can be found online at EED website

http://ppd.fnal.gov/eed/

| Electrical Engineering Department |
|-----------------------------------|
| T. Shaw, Head |
| V. Rusu, Deputy Head |
| M. Matulik, Associate Head |
| |
| |

Administration Support C. Johnson

| | Asic Development | |
|--------------|------------------|--------------|
| | G. Deptuch, Ldr. | |
| Analog | Digital | Test |
| A. Mekkaoui | J. Hoff | A. Baumbaugh |
| F. Fahim | D. Braga | |
| T. Zimmerman | A. Shenai | S. Holm |
| | | L. Dal Monte |
| | | A. Dyer |
| | | L. Scott |
| | | B. Hess |
| | | |

| [| Detector Electronics |
|-----------|----------------------|
| | P. Rubinov, Ldr. |
| S. Hansen | C. Gingu |
| T. Kiper | K. Kuk |
| S. Los | M. Utes |
| J. Wu | J. Olsen |
| | |
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| Infrastruc | ture & Support | |
|----------------------|----------------|--|
| M. Matulik, Ldr. | | |
| S. Chappa D. Huffman | | |
| D. Featherston | M. Cherry | |
| W. Jaskierny | T. Cunneen | |
| J. Noyola | | |
| | | |
| C. Danner | J. Green | |
| P. Lippert | R. Klein | |
| V. Martinez | N. Moibenko | |
| | | |

EED Department continued

• Department News

- Please keep up with required training!
- Lots of general clean up on the floor as we try to make space for lab areas and new people; need to continually work to reduce clutter
- FY2016 Performance Reviews will be available for viewing through Fermiworks early October
- Task Code Guidance can be found at <u>http://ppd.fnal.gov/PPD%20Charging%20Practices.pdf</u>
- CAD tools an Altium Task Force/Users Group is forming in the department to map out a likely transition to PCB schematic capture and board layout using ONLY Altium in the future (phase out of Mentor)

PPD Charging Practices

Program Support (PS)

- General Training
 - Training common across the lab
 - o Examples: Traffic safety, computer security
- Division Activities
 - o Management of group, department, division
 - o Quality assurance
 - Performance review
 - o All-CRO, division, department all-hands meetings
- Charge to department PS code (see table below)

General and Administrative (GA)

- · Services on review of Fermilab or non-Fermilab projects/programs/activities
- General outreach/education services
- Fermilab All Hands
- Service on Lab Committees
- Charge to 40PD.40.01.05

Common Site Support (CSS)

- Building Maintenance/Management
- Vehicle Maintenance
- Facility Infrastructure
- Licenses for software not directly associated with projects or operations
- Charge code depends on the task

Conference Travel/attendance/presentations

Charge to activity or project supporting the work

Training Associated with Job Function

- · Examples: Working from heights, beryllium handling, crane operation
- Charge to home code

Program Support Task Codes

| Department | PS Code |
|------------|---------------|
| AMD | 40PD.08.03 |
| Astro | 40PD.70.01.07 |
| CMS | 40PD.30.08 |
| DDOD | 40PD.80.01.01 |
| EED | 40PD.50.01.01 |

EED Department continued

• Department News

Carolyn is working to set up a group lunch (courtesy of PPD!) at Chez Leon in October

Details will be announced soon.

• Questions?

Terri Shaw

Dune Far Detector Project Electrical Engineer

http://www.dunescience.org/







Gregory Deptuch



1.2M-pixel, single module camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays, Funded by DOE Office of Science Office of Basic Energy Sciences (1M\$ for Fermilab manpower) (FWP started in Oct. 2014, completion planned for Sept. 2017)

- VIPIC-L ASIC is a two tier 3D ASIC 1.25 × 1.25 cm² with ~120M transistor (largest ASIC built by a US national lab) and 65μm pixel pitch and is configurable in sparsification or imaging mode (up to 78kfps)
- 1 Mpixel = 3 slabs of 2 × 6 VIPIC-L LTD-bonded directly to a Si sensor wafer
- 1FPGA per VIPIC-L (in its footprint) for on the fly data processing (up to 0.72 Tbps of raw data produced)
- Multi-layer (>20 routing layer LTCC) suports b-bonded detector structure

Alpana Shenai

Custom IC Design Tools



Tom Zimmerman

QIE: a multi-decade development effort in high dynamic range floating-point readout chips for HEP

1989: original idea (Bill Foster)
 1995: QIE5 for KTeV
 1996: QIE6 for CDF
 1997: QIE6 for CDF
 2002: QIE7 for MINOS

 2003: QIE8 for CMS
 2004: QIE9 for BTeV
 2016: QIE10 and QIE11 for CMS, QIE12 for ATLAS



FASPAX: a wafer scale X-ray camera of small pixels with <u>unprecedented dynamic range</u>

Use QIE principles and experience to obtain a dynamic range of 10^5 in a 100u X 100u pixel





Abder Mekkaoui

FLORA: A 3D integrated CMOS detector for imaging experiments at LCLS-II

D. Christian, G.W. Deptuch, F. Fahim, R. Lipton, A. Mekkaoui, T. Zimmerman (FERMILAB), Gabriella Carini et al. (SLAC)

LCLS: The SLAC Linac Coherent Light Source (LCLS) is the world's first hard X-ray source produced by free electron laser. With X-ray pulses a billion times brighter than predecessor X-ray sources that last for just femtoseconds, LCLS can measure the properties of ultra-fast processes at the scale of atoms and molecules. The LCLS opened the door to revolutionary experiments in atomic and molecular dynamics. LCLS-II: LCLS-II will provide a major jump in capability – moving from 120 pulses per second to 1 million pulses per second. This will enable researchers to perform experiments in a wide range of fields that are now impossible. The unique capabilities of LCLS-II will yield a host of discoveries to advance technology, new energy solutions and our quality of life. More info: https://portal.slac.stanford.edu/sites/lcls_public/Pages/Default.aspx

FLORA (Fermilab-LCLS CMOS 3D-integRated detector with Autogain), with very low noise, high dynamic range and fast readout suitable for imaging experiments at the upcoming LCLS-II.

Small pixel size (50µmx50µm pixels); Frame readout > 10 kfps; Built-in adaptive gain; DR from 1 to 1,000 photons per pixel per frame with a single photon resolution; High quantum efficiency in the energy range between 250 eV and 2 keV; large areas (solid angle). Divide and conquer using a 3D approach: Using a sensing layer (in an imaging CMOS process) to deal with "upfront" issues (Help with the ENC, DR, appropriate entrance window and thickness...) and a readout layer, implemented in an optimum process, would implement signal processing and communication with the upstream system.





Smallest input charge is 1ph@250eV yielding ~70e-. This requires an ENC (equivalent Noise Charge) of 10e- rms (or less). Largest signal 1000ph@2000eV ~ 0.55 Me-. A low power, small area frontend that deals with an input charge this large (@1.2V) and maintains a 10e- input-referred noise is very challenging. Analog readout @ 10kfps would require very low noise and very fast settling time paths+ system complexity using off the shelf ADC is high. Digital readout would require low power small area in-pixel ADCs + multi Gbps data transmission.

Davide Braga

COLDATA (Cold Digital Data) ASIC for **DUNE**

(Davide Braga, Jim Hoff, Alpana Shenai)

- Data concentrator and readout chip for DUNE LAr TPCs
 - 1.5Gbps In , 2x 1.2Gbps Out
 - data readout and control between cold and warm electronics
 - system clock interface
- Digital chip with mixed-signal components
- Challenges:
 - Low power/high speed: 65nm CMOS process
 - Reliability: operate at 89°K for >15 years without maintenance
 - ightarrow custom logic library designed to avoid premature degradation
 - ightarrow custom models for accurate simulation provided by external company from Fermilab test structure
 - \rightarrow accurate cold timing models provided by UPenn
 - Fully digital chip:
 - ightarrow new workflow/EDA tools
 - ightarrow clock domains synchronization
 - ightarrow test coverage and verification

Fermilab ASIC group responsible for most of the chip design, plus top level assembly and verification; collaboration with Southern Methodist University (PLL and Line Driver) and University of Pennsylvania (library characterization).



16ch

Farah Fahim

Fermi CMS Pixel (FCP130) – CMS Phase II forward Pixel – Synchronous concept

- Novel Synchronous front-end concept for CMS Phase II forward pixel
- Correlated double sampling for noise reduction
- ½ BXClk cycle for reset & ½ for compare
- Version 1- Issues:
 - Unbiased and wrongly Biased Deep N Wells
 - Substrate contacts instead of Antenna Diodes
 - Thresholds are parasitically connected
- However: Successful Preliminary Qualitative analysis
 - Preamplifier response can be monitored; change of current is feedback loop changes the return to baseline.
 - All comparator response times are changing with change in threshold voltage
- Configuration register is able to able to correctly program the pixels
- The serial mode of transfer in FIFO 2 daisy can correctly send data Out
- The Spy signals for last superColumn (Pixel Hit, ADC value and address can be correctly monitored)
- Conflux performance could be measured
- Version 2- Status
 - Change in Preamp and comparator
 - All other bugs fixed
 - Top Level changed for only 1 design
 - Submission on 6th Nov 2016



INFN- Fermi CMS Pixel (IFCP65): Translation of FCP130

- Collaboration with INFN (U.Bergamo)
- Front-end with 2 bit ADC redesigned in TSMC 65nm
- Test structure of 16 x 16 matrix submitted in May 2016
- Detailed tests to be carried out both at Fermi and U.Bergamo (Radiation tests at U. Padova)
- Designed to meet constraints set by RD53A chip for submission in Feb –March 2017
- Implemented design has extremely low noise but higher power consumption





9/26/2016

Jim Hoff



Scott Holm

Crate Dimension : 40cm x 40 cm x 25cm tall The cables coming out of the modules will extend out of the modules about 10cm before they can bend. The shortest cables are 1 meter in length(they are custom cables from National Instruments).





Lou Dalmonte

ASIC Production Test Robot

Lou DalMonte – EED ASIC GROUP

other EED INFRASTRUCTURE

DANGER WILL ROBINSON, DANGER!





The Robot we wish we had





2016 YEAR REVIEW

- 2016 QIE10 ASIC's Tested approx. 7600
- 2016 QIE11 ASIC's Tested approx. 12000
- 2016 QIE11 ASIC's To Be Tested approx. 23000



- Inauguration date 2009??
- Alan Baumbaugh designer. (Mechanical & Software)
- Final documentation in progress for future support.
- Manpower Requirements
 - (Maintenance, Repairs , Operations , Upgrades)
- Second Robot in the works, waiting for FPGA design.
- Upgrade to National Instruments Control is being discussed.

Al Dyer



Clean Room

- **Cleanroom** : 2 probe stations for testing silicon wafers, one manual and one automatic. ASIC's storage. Wire Bonding. PCB assembly.
- **Cyro-cooler** : located in a lab area on the northeast side of the floor can provide testing from room temperature down to cryogenic temperatures.
- Westside Surface Mount Lab : flexibility to assemble circuit boards as well as any type of re-work required.
- Albert's Messy Lab Area : For all things possible!

Jinyuan Wu

Jinyuan Wu

- Short CV:
 - 1997 Fermilab
 - 1995-1997: RA: Colorado
 - 1992-1994: Post Doc: Penn State,
 - 1986-1992: Ph. D. Student: Penn State
- Current Projects:
 - Accelerator Protection System (NML & PIP-II)
 - SeaQuest
- What I can do for other colleagues:
 - FPGA Based TDC
 - RAM-based Histograms
 - Data Organizers ...





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Christian Gingu

On wafer chip testing using Cascade Probe Station (1)

- Six production batches with 118 wafers for CMS Pixel ROC PSI46dig tested (2015 and 2016)
- Using DTB hardware (PSI), probe card (FNAL) and C++ software (PSI source code with FNAL modifications for our automatic probe station interface and data base files creation)
- Git repository used for PSI46dig test application
- Creating Xml files for Fermilab data base
- Updating C++ grlog application (PSI) for FNAL wafers maps
- Very good agreement between PSI and FNAL test results
- Detailed reports at https://cms-docdb.cern.ch doc#12279, 12445, 12502, 12634, 12650 and 13085

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| Q-psi46fnal_manter_ Merge branch bsi46cen_master into psi46fnal_master | gingu soingu@PPD-117629 dhop thai gove | 2015-06-26 11 12 3 |
| Concern manner Matchastics concernment - Updated list 3 D/IB repared (19(45/01), 1 exchanged (41 -> 10), 4 accional | (24.135,141, Hark Neel 41Treet@cett.ch> | 2015-00-22 04 01.3 |
| Updated repair status | Frank Meier <tmeier@cem.ch></tmeier@cem.ch> | 2015-06-15 06 50 5 |
| Updated: DTB 41 and 61 handed over to PSI for repair/echange | Frank Neier stmeierißcem ch> | 2015-05-19/03 19/2 |
| two times probe card contact | gingu <gingu@ppd-117629.dhcp.fnal.gov></gingu@ppd-117629.dhcp.fnal.gov> | 2015-06-26 10:51:5 |
| Merge branch psi46cem master | Cristian Gingu <gingu@thal.gov></gingu@thal.gov> | 2015-05-07 10:34.0 |
| maketie updated, command doc added | meerb teat meerbdps.ch> | 2015-05-07 06 39 1 |
| for hum "READBACK" test now for all ROCs (ABCD) in water test. | might their mighting cha | 2015/05/07 01 10:5 |
| update Nucleus class with wafer map parameters | Cristian Gingu <ginguiĝthal.gov></ginguiĝthal.gov> | 2015-05-07 10:04 5 |
| Merge branch psi48cem master | Cristian Gingu <gingu@fnal.gov></gingu@fnal.gov> | 2015-05-05 14:38:3 |
| Merge branch 'master' of https://github.com/psi46/psi46/est | meierb <beat meier@psi.ch=""></beat> | 2015-04-30 08:51.1 |
| V Update U T D Xox | Flammeer Nimbergoen un? | 2010-04-10 10 40.5 |
| Updated the broken ones at KU | Frank Meier <frmeier@cern.ch></frmeier@cern.ch> | 2015-04-08 15:32-4 |
| Added a status column | Frank Meier <frmeier@cern.ch></frmeier@cern.ch> | 2015-04-08 15:12:1 |
| Update DTB list | Frank Meier <fmeier@cem.ch></fmeier@cem.ch> | 2015-03-26 14:56:1 |
| Update DTB list | Joaquin E Siado Castaneda <isiado@huskers.unl.edu></isiado@huskers.unl.edu> | 2015-03-19 16:36:0 |
| Update DTB list | isando3 <isando3buc edu=""></isando3buc> | 2015-02-10 12:20:1 |
| Updated: received DTB#29 back from PSI | Frank Meier <frmeien@cern.ch></frmeien@cern.ch> | 2015-01-27 02:01 0 |
| modifications for wafer and bare module test | meierb <beat meier(2psi.ch=""></beat> | 2015-04-30 08 49 1 |
| water list to reduce typing errors for water numbers | meierb deat meer@psi.ch> | 2015-04-30 04:51 0 |
| Merce branch 'master' of https://github.com/psi48/psi48/est | meierb <best meier@psi.ch=""></best> | 2015-01-20.03 42 2 |
| probe signals for deser400 addad | meierb <beat meier@psi.ch=""></beat> | 2014-12-07 16:29:4 |
| Update DTB list | Frank Meier <frmeien@cem.ch></frmeien@cem.ch> | 2014-11-14 08:07:1 |
| Functors for DTB trigger added | meierb <beat meier@psi.ch=""></beat> | 2015-01-20 03 36 3 |
| Update DTB ist | Frank Meier <frmeien@cern.ch></frmeien@cern.ch> | 2014-11-03 05 48 2 |
| update Nucleus statements: cmd_walertest.cpp and psikRest.cpp | Cristian Gingu <ginguiĝtrial gov=""></ginguiĝtrial> | 2015-05-06 10:30 2 |
| Merge branch psi48cem_master | Cristian Gingu <gingu@thal.gov></gingu@thal.gov> | 2014-10-10 18:06 5 |
| Updated list one UTB shipped to Comell | Hark Neer Ameergcen.ch> | 2014-10-10 14:431 |
| small correction in cmd_db cpp | meierb <beat meier@psi.ch=""></beat> | 2014-09-10 08:25:1 |
| Mosing return value | meinth steat meintigesi cho | 2014-08-20-01-08-0 |
| Modified chipPos, posy, posy and nRep and catch conditions | Cristian Gingu <gingu@thal.gov></gingu@thal.gov> | 2014-10-10 12:47:4 |
| Merge branch ps-40cem_master | Cristian Gingu Kgingu@thal.gov> | 2014-08-19 16:25:0 |
| Updated inventory | Frank Meer Immeergcen.ch> | 2014-08-07 12 59 5 |
| Finally Some for all the commits but debugging markdown is notifimarish | Frank Meier (Mac) -frank meier(Buri) edu- | 2014-07-21 07:58:1 |

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| - <rout></rout> | |
| - <header></header> | |
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| <extension_table_name>FPIX_ROC_ON_WAFER_TEST<td>2</td></extension_table_name> | 2 |
| <name>FPIX ROC On-Water Test</name> | |
| | |
| - <run></run> | |
| <run_name>PS146V2 SNSDPGT</run_name> | |
| <run_begin_timestamp>2014-10-14 15:30:46</run_begin_timestamp> | |
| <comment_description>ROC On-Wafer Test</comment_description> | |
| <initiated_by_user>Cristian Gingu</initiated_by_user> | |
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| - <daia_sei></daia_sei> | |
| <comment_description>Test results from FNAL for SNSDPGT<td>DN ></td></comment_description> | DN > |
| <data_file_name>SNSDPGT.txt</data_file_name> | |
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Cristian Gingu| PPD/EED All Hands Meeting

On wafer chip testing using Cascade Probe Station (2)

- Testing 8 wafers with FPHX chip for PHENIX Group (BNL) in 2016; more wafers are expected to come.
- Using ASIC Testing System with interface board, probe card and test script program developed at FNAL (<u>Alan Baumbaugh</u> and <u>Louis Dal Monte</u>) with modifications for our automatic probe station interface and test file reports for every chip.
- Established analog level cuts; provided wafer inking and wafer maps for dicing.

| The following is a summary | of main tes | ts performed | and the | FailCode | bit they | set. | The |
|---|-------------|--------------|---------|----------|----------|------|-----|
| tests are listed in the order they are pe | erformed. | | | | | | |

| 1. | Power supply test. | Sets bit 00. |
|-----|---------------------------|--------------|
| 2. | Sync words. | Sets bit 01. |
| 3. | LVDS data levels. | Sets bit 02. |
| 4. | Registers. | Sets bit 03. |
| 5. | Timestamp. | Sets bit 04. |
| 6. | Defaults. | Sets bit 05 |
| 7. | Chip ID. | Sets bit 06. |
| 8. | LVDS scan. | Sets bit 07. |
| 9. | Dual data port. | Sets bit 08. |
| 10. | Kill inject mask. | Sets bit 09. |
| 11. | Internal DAC hits. | Sets bit 10. |
| 12. | External gain. | Sets bit 11. |
| 13. | Internal DAC ADCs. | Sets bit 12. |
| 14. | Channel test – the Drake. | Sets bit 13. |
| | | |



Contributions to Minerva (high luminosity, 2015-2016) Design

8

1

-

- FEB firmware update (v97, Xilinx) includes: new sequencer features, 20 hits readout, TRIPTs chips push independent or in pair, 4-modes digitization
- CROCE firmware updates (v4-5, Lattice, Diamond) ۲
- Slow Control (Python)

| Stow Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Be Show Action Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. V ME: BRIOCE V V2:18.0 Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. V V2:18.0 V V2:18.0 Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Register Memories Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. CHE: 1 Stow Crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. CHE: 3 V CROCC: 1 Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. CHE: 3 V ME Crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. CHE: 3 V ME Crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. CHE: 3 V ME Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - two VME crates v;2:07. Image: Control - t | | | | | 🖶 强 Inst_devx_regis - devx_regis - rtl (src\devx_regi |
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| V CROCE:10 Read Eardin Core 3 model membrane Core 3 model membrane </td <td>CHE:3</td> <td>Write Config</td> <td>Read Status Read Status</td> <td>Write Header</td> <td>Inst_fast_cmd_dec - fast_cmd_dec - rtl (src\fast_cmd_dec - rtl)</td> | CHE:3 | Write Config | Read Status Read Status | Write Header | Inst_fast_cmd_dec - fast_cmd_dec - rtl (src\fast_cmd_dec - rtl) |
| CHE:0 (9x:0) | | Read Config Clear SndMemWPointer | 0x4040 0x2410 | Read Header | 🔜 Inst_external_gatetrigg - external_gatetrigg - |
| CHE:1 WR RDFEModeEn (MSB) Geer RDFECounter SndMem_Emry 1 R K_LockEmr WR Unused WR Unused CHE:2 WR SingleHiMdodE WR SingleHiMdodE WR SingleHiMdodE WR Unused WR WR WR WR WR UNUSED WR W | CHE:0 | 0xc0 Clear RcvMemWPointer | SndMem_Full (MSB) 0 RX_Lock (MSB) | 0 0x0 | 🛛 🔁 Inst_gate_generator - gate_generator - rtl (src |
| CHE:2 CHE:3 WR SndtemwRands no WR SingleHitModefn o WR FingleHitModefn o WR FingleHitMode | CHE:1 | WR RDFEModeEn (MSB) 0 Clear RDFECounter | SndMem_Empty 1 RX_LockError | 0 WR Unused 0 | 🕀 强 Inst hy loop pmr - hy loop pmr - rtl (src\hy lo |
| CHE:3 WR SingleHildedEn WR Howstehl WR Howstehl WR Howstehl WR Howstehl WR EnclikMonitorEEn WR Hewitshiftencoden SndMem. RDFEUpdating TX_LockEnor TX_LockEnor WR RCBC_ID_3 WR EnclikMonitorEEn WR Heisthiftencoden Read SndMem. RDFEUpdating TX_LockEnor WR RCBC_ID_2 WR RCBC_ID_3 RO Firmw_Version_2 Read Read RX_EnclicmdFound WR RCBC_ID_0 WR RCBC_ID_0 WR RCBC_ID_0 WR RCBC_ID_1 RO Firmw_Version_1 RX_EnclicmdFound RX_EnclicmdFound WR RCBC_ID_0 WR RCBC_ID_0 <td< td=""><td>CHE:2</td><td>WR SndMemWRandEn 0 TX SendSyncWords</td><td>SndMem_rrmSent 0 TX Sync1</td><td>WR Unused 0</td><td>🔚 Inst dac7513 clks - dac7513 clks - rtl (src\dac</td></td<> | CHE:2 | WR SndMemWRandEn 0 TX SendSyncWords | SndMem_rrmSent 0 TX Sync1 | WR Unused 0 | 🔚 Inst dac7513 clks - dac7513 clks - rtl (src\dac |
| WR Russhicht Goden 0 WR Russhicht Goden 0 WR Russhicht Goden 0 WR Rachter (bytes) SndMem RDFEbone WR Rachter (bytes) SndMem RDFEbone Rof Fmw, Version 3 0 Ro Fmw, Version 1 RevMem FmmCounter Rof Fmw, Version 1 RevMem FmmCounter RovMem FmCounter RevMem FmmCounter RovMem FmReetived RX_EnclorMdfound RvMem FmRefets_2 o WR FEB_Version_3 <td>CHE:3</td> <td>WR SingleHitModeEn 0 WR SingleHitModeEn 0 Write Commands</td> <td>SndMem BDEEUpdating 0 TX LockError</td> <td>WR Unused 0</td> <td>E Inst tripx top - tripx top - rtl (src\tripx top.vho</td> | CHE:3 | WR SingleHitModeEn 0 WR SingleHitModeEn 0 Write Commands | SndMem BDEEUpdating 0 TX LockError | WR Unused 0 | E Inst tripx top - tripx top - rtl (src\tripx top.vho |
| WK R1columoniturFein 0 WK R1columoniturFein 0 Ro Firms, Version 3 0 RO Firms, Version 1 Read RO Firms, Version 1 Read RO Firms, Version 1 Read RO Firms, Version 2 Read WK R1columoniturFein 0 Rowmen, Firms, Version 1 Read Rowmen, Firms, Version 2 Read WK R2columoniturFein 0 Rowmen, Firms, Version 2 Read WK R2columoniturFein 0 Rowmen, Firms, Version 2 Read WK R2columoniturFein 0 Rowmen, Firms, Version 2 Read WK R2columoniturFein Read WK R2columonitur Read | | WR FiveBitsFitchCodeFit | SndMem_RDFEDone 0 TX_LockStable | | Inst tdc 4trip - tdc 4trip - rtl (src\tdc 4trip) |
| R0 firms_Version_3 0 Read FlashMem_Error 0 TX_EncOutCrddSent 0 R0 firms_Version_2 0 RevMem_Fruil 0 RX_EncInCmdTimeout 0 R0 firms_Version_0 1 RevMem_frmineout RX_EncInCmdMatch 0 R0 firms_Version_0 1 RevMem_frmineout RX_EncInCmdMatch 0 WR Rest_Prise 0 RX_RetR_Version_7 0 WR FEB_Version_7 0 WR Rest_Prise 0 RX_RatTpOutCmdSent 0 WR FEB_Version_4 0 WR NumberOfFEBs_1 0 RevMem_frmiReceived RX_RatTpOutCmdSent 0 WR FEB_Version_3 0 WR RumberOfFEBs_1 0 RevMem_frmiReceived RX_RatTpInCmdTimeout 0 WR FEB_Version_3 0 WR RumberOfFEBs_1 0 RevMem_frmiReceived 0 WR FEB_Version_1 0 WR FEB_Version_2 0 WR RumberOfFEBs_2 0 RevMem_frmiReceived 0 WR FEB_Version_2 0 WR FEB | | WR FlashMemEn 0 Recommendation | SndMem_RDFEError 0 TX_Sync2 | 0 WR CROC ID 2 0 | trip0 - tdc 1trip - rtl (src)tdc 1trip ybd) |
| R0 frmw_Version 2 0 RcvMem_Full 0 RX_EnclnCmdTimeout 0 WR CROC_ID_0 0 R0 frmw_Version 1 RcvMem_Empty Rx_EnclnCmdTimeout 0 RX_EnclnCmdTimeout 0 WR CROC_ID_0 0 WR TestPulse Revidem_frmCounter RcvMem_frmReceived RX_EnclnCmdMatch 0 WR FEB_Version 7 0 WR TestPulse Revidem_frmReceived RX_EnclnCmdMatch RX_EnclnCmdMatch 0 WR FEB_Version 5 0 WR NumberOfFEBs 2 0 RcvMem_frmTimeout 0 RX_RatTplonCmdFound Unused WR FEB_Version 2 0 WR FEB_Version 2 0 WR NumberOfFEBs 2 0 Revidem_frmReceived Rx_RatTplonCmdFound 0 WR FEB_Version 2 0 WR NumberOfFEBs 2 0 WR FEB_Version 1 0 WR FEB_Version 2 0 WR FEB_Version 2 0 WR RumberOfFEBs 2 0 Read Read Rest Rest 0 WR FEB_Version 2 0 WR RumberOfFEBs 2 0 WR FEB_Version 2 0 WR FEB_Version 2 0 WR FEB_Version 2 0 WR RumberOfFEBs 2 0 | | RO Frmw_Version_3 0 | FlashMem_Error 0 TX_EncOutCmdSen | 0 WR CROC_ID_1 0 | Trip trip the strip trip trip trip trip trip trip trip |
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| R0 Frmw_Version_0 1 Read RevMem_frmmLendum_rev 0 WR FEB_Version_1 0 WR FEB_Version_5 0 WR FEB_Version_6 0 WR NumberOfFEBs_3 0 RovMem_frmmLRedum_rev RX_EnclnRFOX IRX_RETP/Usersion_1 0 WR NumberOfFEBs_1 0 RovMem_frmmLRedum_rev RX_EnclnRFOX IRX_EnclnRFOX WR FEB_Version_3 0 WR NumberOfFEBs_1 0 RovMem_frmmLRedum_rev 0 TX_RastrpinCmdTimeout 0 TX_RestrpinCmdTimeout 0 WR NumberOfFEBs_1 0 Reved Reversion_1 0 WR FEB_Version_2 0 WR NumberOfFEBs_2 0 Reversion_1 0 WR FEB_Version_1 0 WR FEB_Version_1 0 WR NumberOfFEBs_0 0 Reset all Reversion_2 0 WR FEB_Version_0 0 WR FEB_Version_1 0 Read All Regs Read Read Read Read Reset all CRATES Reset all CRATES WR FEB_Version_0 0 WR FEB_Version_0 0 Reset options Reset this CROCE Reset this CRATE Reset all CRATES Reset all CRATES Reset all CRATE | | RO Frmw_Version_1 1 RcvMem FrmCounter | RCVMem_Empty 1 RX_EncinCmdFound | 0 WR FEB_Version_7 0 | The second secon |
| WR Rest options Revert this CRED | | RO Frmw_Version_0 1 Read | RcvMem FrmReceived 0 RX EncInRFOK | WR FEB_Version_6 0 | trip3 - tac_1trip - rti (src\tac_1trip.vna) |
| WR NumberOFEEBs 3 WR NumberOFEEBs 2 WR NumberOFEEBs 2 WR NumberOFEEBs 2 WR NumberOFEEBs 2 WR NumberOFEEBs 2 WR NumberOFEES 1 WR NumberOFEES 2 WR NumberOFEES 2 WR FEB Version 2 WR | | WR (happelResetEn 0 | RcvMem FrmTimeout 0 RX RstTpOutCmdSr | nt 0 WR FEB Version 4 0 | hitor - tdc_hitor - rtl (src\tdc_hitor.vhd) |
| WR NumberOfFEBs 2 0 Revel Revel TX_RstPinCmdFound 0 WR NumberOfFEBs 1 0 0 Unused 0 WR FEB_Version 2 0 WR NumberOfFEBs 1 0 0 WR FEB_Version 1 0 WR FEB_Version 2 0 WR NumberOfFEBs 2 0 0 WR FEB_Version 1 0 WR FEB_Version 2 0 WR NumberOfFEBs 2 0 0 WR FEB_Version 1 0 WR FEB_Version 2 0 Read All Regs Read 0 Reset options NR FEB_Version 2 0 WR FEB_Version 2 0 Reset options Reset this CROCE Reset this CRATE Reset all CRATES WR FEB_Version 2 0 | | WR NumberOfFEBs 3 0 RDFE Counter | RcvMem_FrmCRCError 0 TX_RstTpInCmdTim | out 0 WR FEB Version 3 0 | Inst_tdc_ctrl_4trip - tdc_ctrl_4trip - rtl (src\td |
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| Reset options | | | | | 🛯 🔚 Inst_clks_46trip - clks_46trip - rtl (src\clks_4 |
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| | | Reset this CHE Reset this CROCE | Reset this CRATE Reset all CRATE | | 🛛 强 Inst_digmem_4trip - digmem_4trip - rtl (src |
| Inst anamem 6trip - anamem | | | | | 🔚 Inst anamem 6trip - anamem 6trip - rtl (sr |
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| ■ S Inst tmp121 clks - tmp121 | | | | | Inst tmp121 clks - tmp121 clks - rtl (src\tmp1 |
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Cristian Gingu PPD/EED All Hands Meeting

Contributions to HGC (2016)

• Started with <u>Paul Rubinov</u>; wrote firmware for the commercial Zed Board (Xilinx ZYNQ) and for the custom readout board FMCIO (Xilinx ARTIX) using Vivado IP driven environment



Sten Hansen

Detector Electronics Sub-group (Terry + Sten)

- 1. Mu2e: Cosmic ray tagger electronics consisting of three parts:
- Counter motherboard. Mounted on end of a scintillating extrusion servicing four SiPM photodetectors.
- Front end board mounted on the side of the extrusion panel digitizing 64 SiPM signals coming from the CMBs.
- Readout controller. Installed in the electronics room. Collects data form 24 FEBs.
- 5000 CMBs, 325 FEBs, 15 controllers in the system.



- 2. CDMS: Warm electronics consisting of three parts:
- Digital control and readout card. Controls and reads out 12 Squids and four charge amplifiers. 65 DACs, 110 switches.
- Signal distribution unit. Synchronizes the DCRCs, digitizes acoustic signals for mechanical vibration monitoring.
- Vacuum interface board. Feedthrough board for 600 signals into the vacuum space.
- 30 DCRCs, eight VIBs, 4 SDUs.



Steve Chappa

Muon g-2 Project Electrical Engineer



Muon g-2 Project Electrical Engineer

Main Ring Power Supply and Quench Protection



AC Power and Grounding Infrastructure



Inflector Power Supply and Quench Protection



Main Ring Active Shim Coils



Muon g-2 Project Electrical Engineer

Main Ring Beam Systems Installation



Cable Tray Management



Overseeing Detector Installations Organizing for and Conducting Electrical Safety Reviews

DUNE/ProtoDUNE Electrical and Grounding

At present, developing the grounding and electrical requirements for a DUNE test vessel, or ProtoDUNE. This detector is located at CERN and construction is underway for the service building addition that will house this detector.



DUNE/ProtoDUNE Electrical and Grounding

In the process, we develop diagrams that provides an easily understandable picture that depicts these requirements. Then, from these diagrams, engineering drawings and documents are generated.



PPD ORCs and Electrical Safety

ES&H has developed an interactive webpage where ORCs (Operational Readiness Clearance) for experimental and test installations can be tracked.

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| Request Details | ORC No Beam form | |
| Experiment | ORC Title: MicroBooNE CRT DAQ racks R1 R2 and ORC ID: ORC-0717 | Next |
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| Contraction of the second s | Requester Details | |
| Hazards | David Martinez x | |
| Reviewers | Email | |
| Workflow | damartin@finat.gov Ferm ID | |
| | 144250 | |
| | Note | |
| | This is for racks at DAB before bringing to MicroBooNE | |
| | | |

PPD ORCs and Electrical Safety

As part of the PPD Electrical Safety subcommittee, serve as a reviewer in the field to examine electrical equipment to be installed for safety and for sufficient mitigation of electrical hazards:

- 1. Will it shock anybody? (exposed live circuits with high voltage)
- 2. Will it start a fire? (insufficient overcurrent protection/mitigation)



For example, examine this installation (in the Fermi Test Beam Facility), done by an experimenter or user. Using supplied documentation and by examining it in the field as it is to be used, determine that it is safe for operation.

PPD Electrical Installations



- Provide engineering support and task management for PPD electrical installations:
 - Determine electrical load requirements, panel and switchgear requirements, etc.
 - Maintain and update installation Single Line Electrical Drawings (SLEDs)
 - Maintain and update electrical panel schedules (individual circuit assignments)
 - Evaluate installations for safety according to NFPA-70E (arc-flash calculations)

Mike Utes

Impedance Monitor for New Detectors



Impedance Monitor for New Detectors



Impedance Monitor for New Detectors



Silicon Scanner for Muon Tomography

R&D for NSTec (National Security Technologies) Nevada Test Site

Main application is for nuclear material imaging for homeland security.

Silicon Scanner for Muon Tomography



Thanks for coming!