3D and SOI Integrated Circuit Design at Fermilab for HEP and Related Applications

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Fermilab

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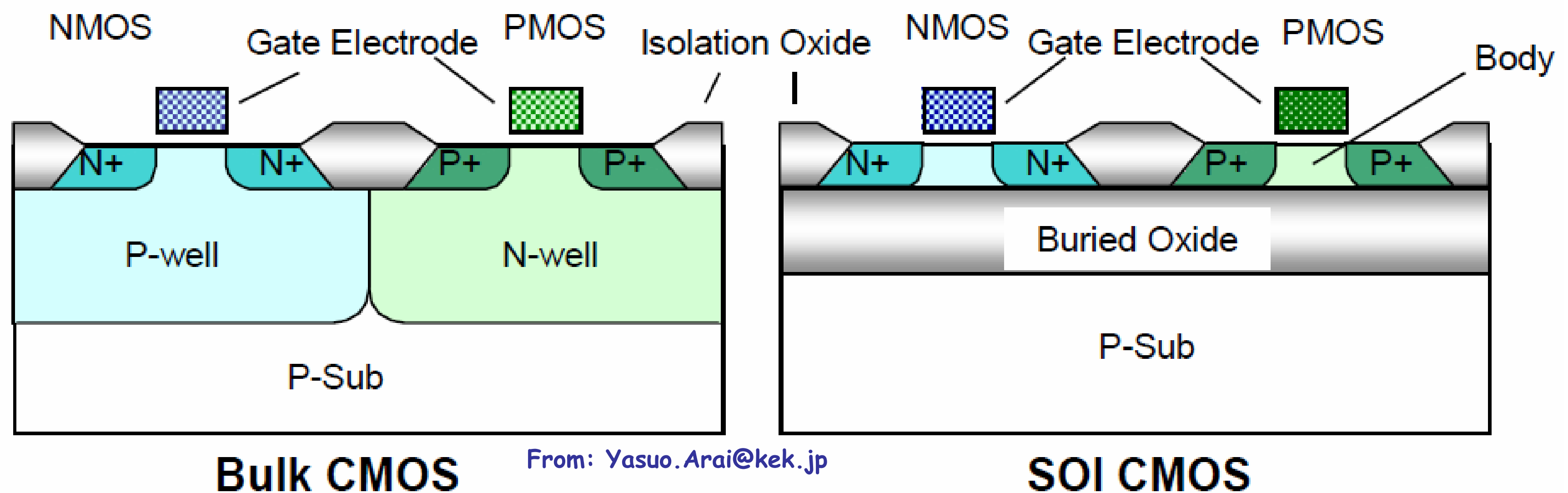
Overview

- Fermilab is pursuing the development of detectors and readout electronics using some of the latest technologies available.
- Over the last two years, Fermilab has been involved with the design and fabrication of 3D integrated circuits and MAPS like devices built in SOI technology.
- This presentation will provide an overview of some of the work in these two areas.
- Because of the large amount of material, I will cover some slides very quickly but have included them so that they can be studied more carefully at a later time.

What is SOI Technology?

Features of SOI (Silicon-on-Insulator)

- Transistors are built in a thin layer of Si (50-100 nm) and are isolated from each other by SiO_2 (each transistor is built in its own isolated island, no source-bulk, drain-bulk junctions, low capacitance)
- Transistors sit on top of a buried oxide layer (BOX) that is usually 200-400 nm thick.
- Can obtain transistor with different threshold voltages by selective implantation of islands to different resistivities – N or P wells are usually blanket implantations.
- SOI transistor characteristics are somewhat different than bulk CMOS



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Fermilab SOI MAPS

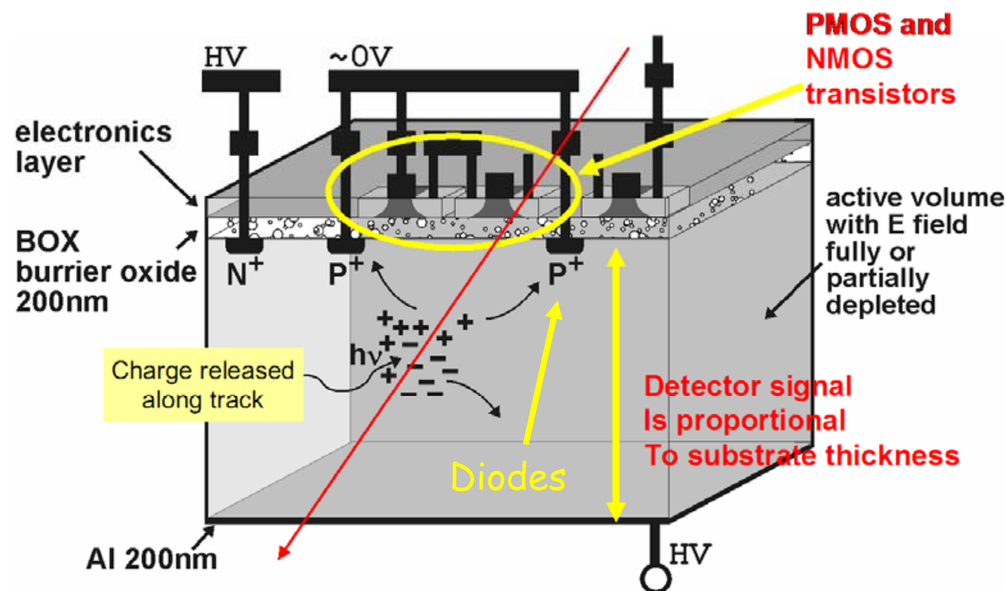
- Design objectives
  - Explore OKI 0.15 um and 0.20 um SOI CMOS processes
    - Add vias to allow charge collection from diodes implanted in the substrate below the BOX
  - Design of pixel electronics suitable for small size pixels and ultra low power consumption
- Applications
  - Direct digital imaging of electrons in electron microscopes
  - Soft X-ray imaging in synchrotron radiation experiments and medical applications
  - Vertex detectors and tracking in HEP

Active Pixel Sensor in SOI

SOI detectors are a first step toward 3D integration since it uses many of the same processes (oxide bonding, wafer thinning, via formation) as 3D integration.

- Thin top layer with silicon islands in which PMOS and NMOS transistors are built.
- A buried oxide layer (BOX) which separates the top layer from the substrate.
- High resistivity substrate which forms the detector volume.
- Diode implants are formed beneath the BOX and connected by vias to CMOS circuitry.

The raw SOI wafers which have the CMOS layer bonded to the substrate layer are procured from commercial vendors such as SOITEC in France.

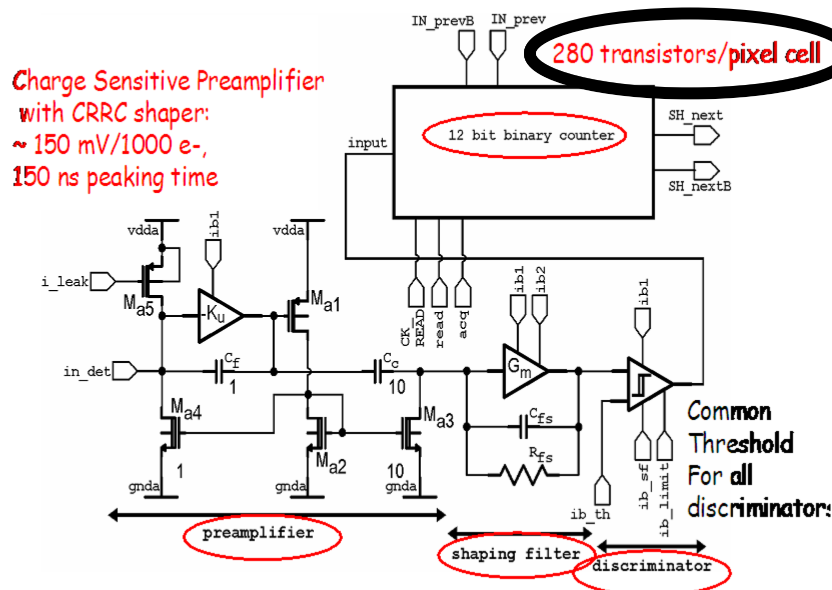


Advantages:
* 100% fill factor in pixel
* NMOS + PMOS transistors
* Large signal
* Faster charge collection
* Less charge spreading
* SOI features:
  - No latch up
  - Low power

Fermilab Pixel Sensor in SOI Process

First design done in OKI 0.15 um multi-project run coordinated by Y. Arai at KEK. [1]
MAMBO1 – Monolithic Active pixel Matrix with Binary Output. [2]
Imaging detector for direct detection in electron microscopy (TEM), and soft X-rays.
Designed for counting applications

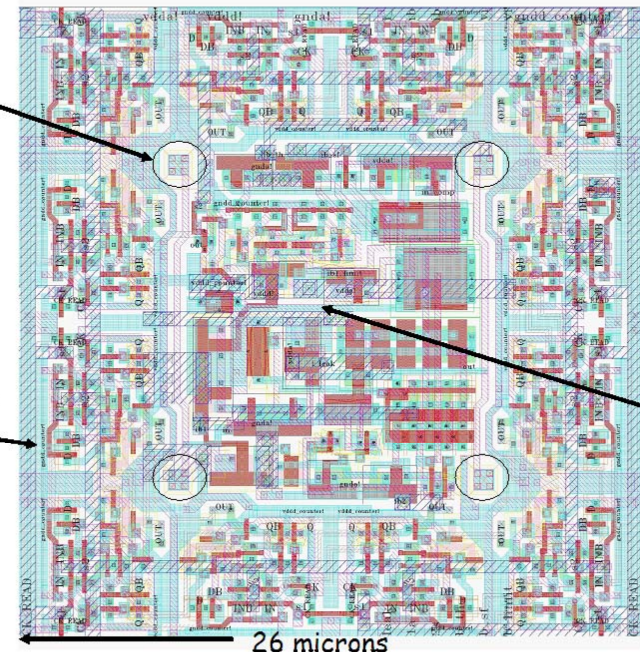
- 64 x 64 pixel array, 26 µm pitch, 4 parallel diodes/pixel (spaced 13 µm apart).
- Each pixel has CSA, CR-RC2 shaper, discriminator + 12 bit binary counter.
- The counter is reconfigurable as a shift register for serial readout of all pixels.



Single pixel schematic

One of four detector diodes

One of twelve D flip-flops arranged around perimeter of pixel cell



All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

Single Pixel Layout

Test results

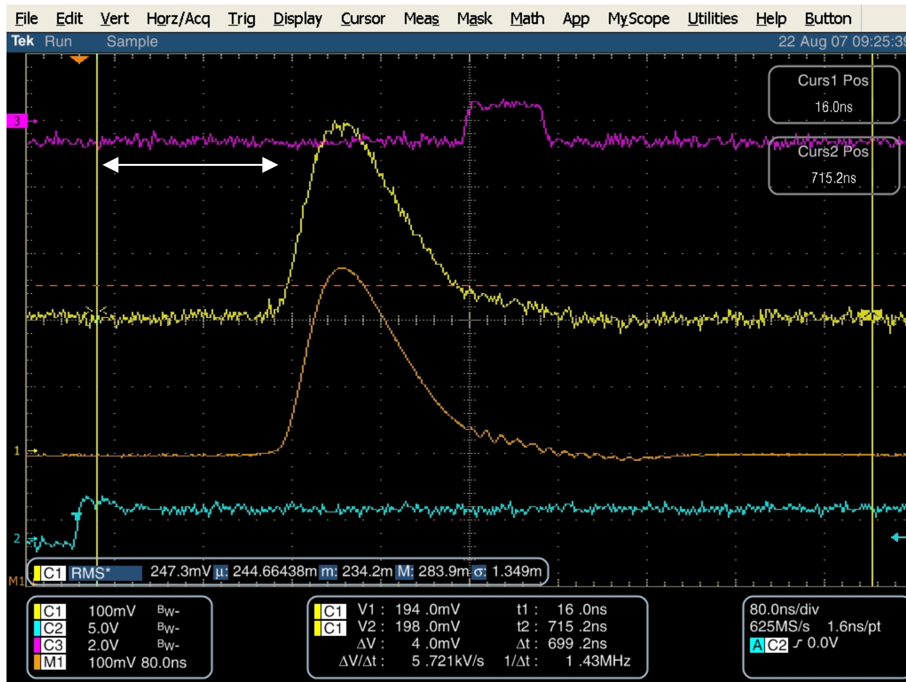
Analog section working with charge injection circuit

Gain lower and shaping faster than expected

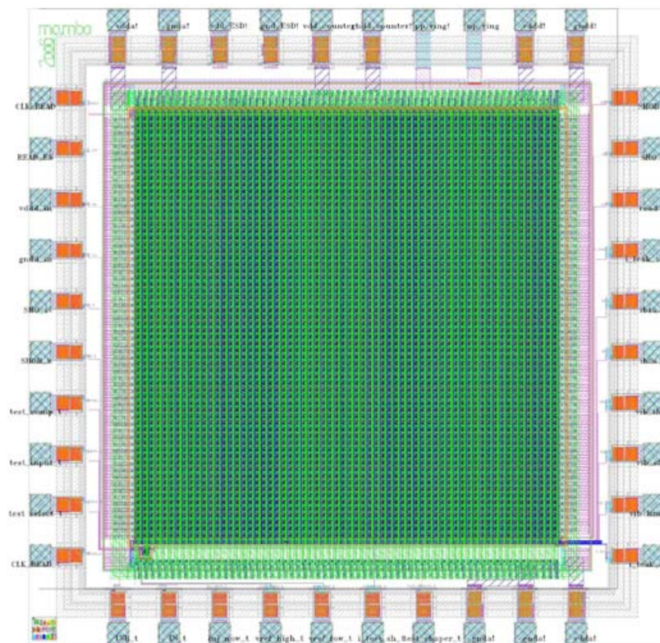
Counter/shift register working (needs back gate voltage for proper operation)

Discriminator working

Backgate voltage problems have prevented simultaneous operation of the front end and back end electronics.



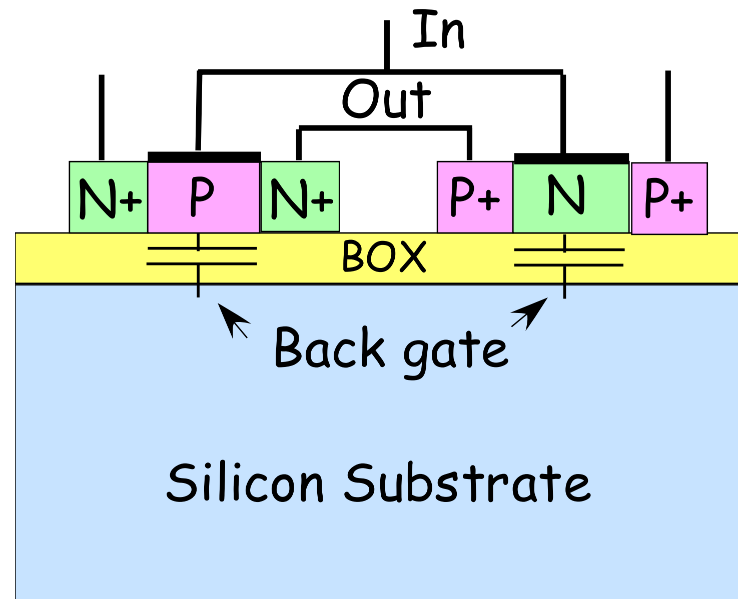
Preamp, shaper, discriminator response



64 x 64 array in pad frame

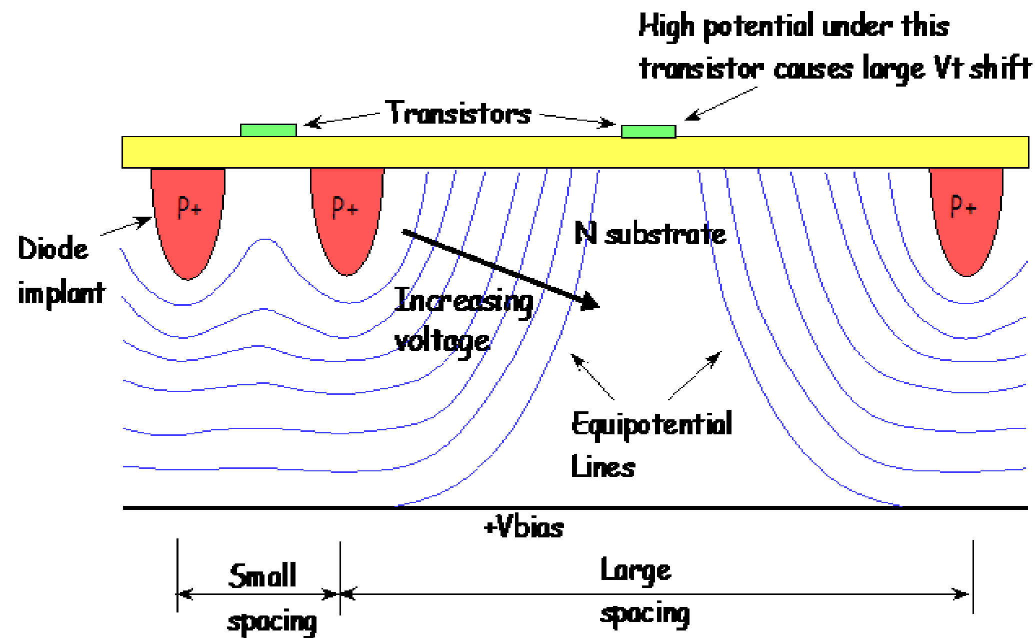
Issues with SOI Detectors

1) A The BOX (Buried Oxide) acts as a back gate for the NMOS and PMOS transistors.



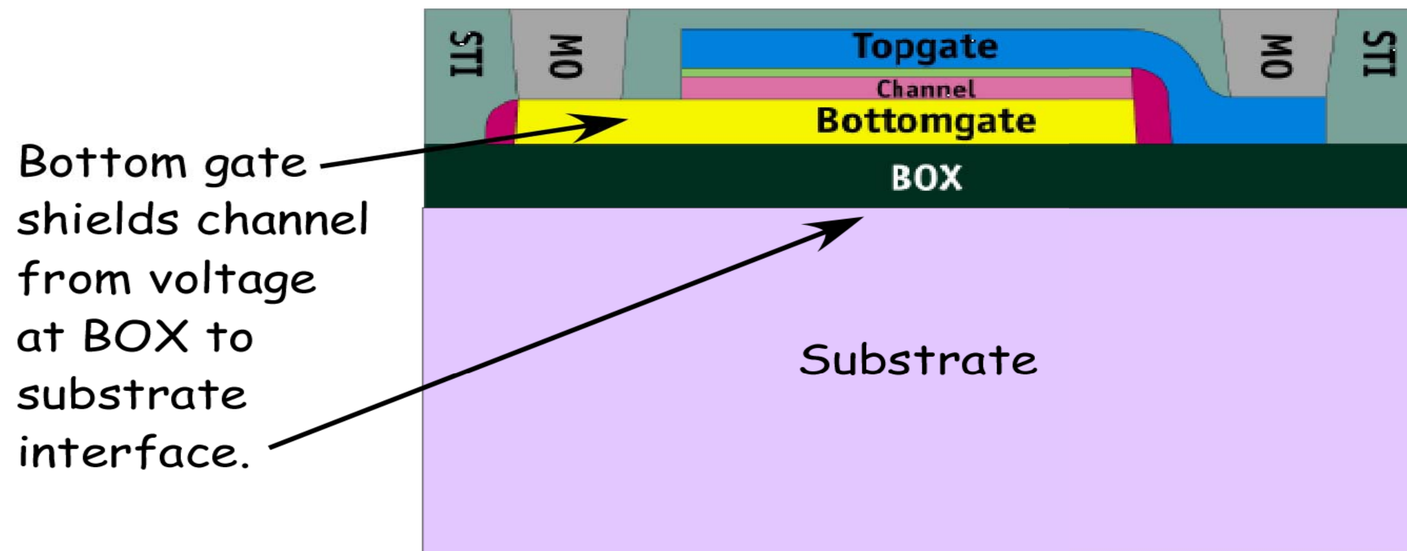
The BOX is thick enough (200 nm) to trap charge from ionizing radiation and cause Vth shifts. (Fortunately the Vth shifts can be fully corrected by adjusting the substrate/back gate potential). 3

2) The back gate voltage affects the transistor threshold voltage in a manner similar to the top gate. The voltage on the back gate of transistors and hence Vth is affected by the distribution of the diode contacts which affects back gate potential.



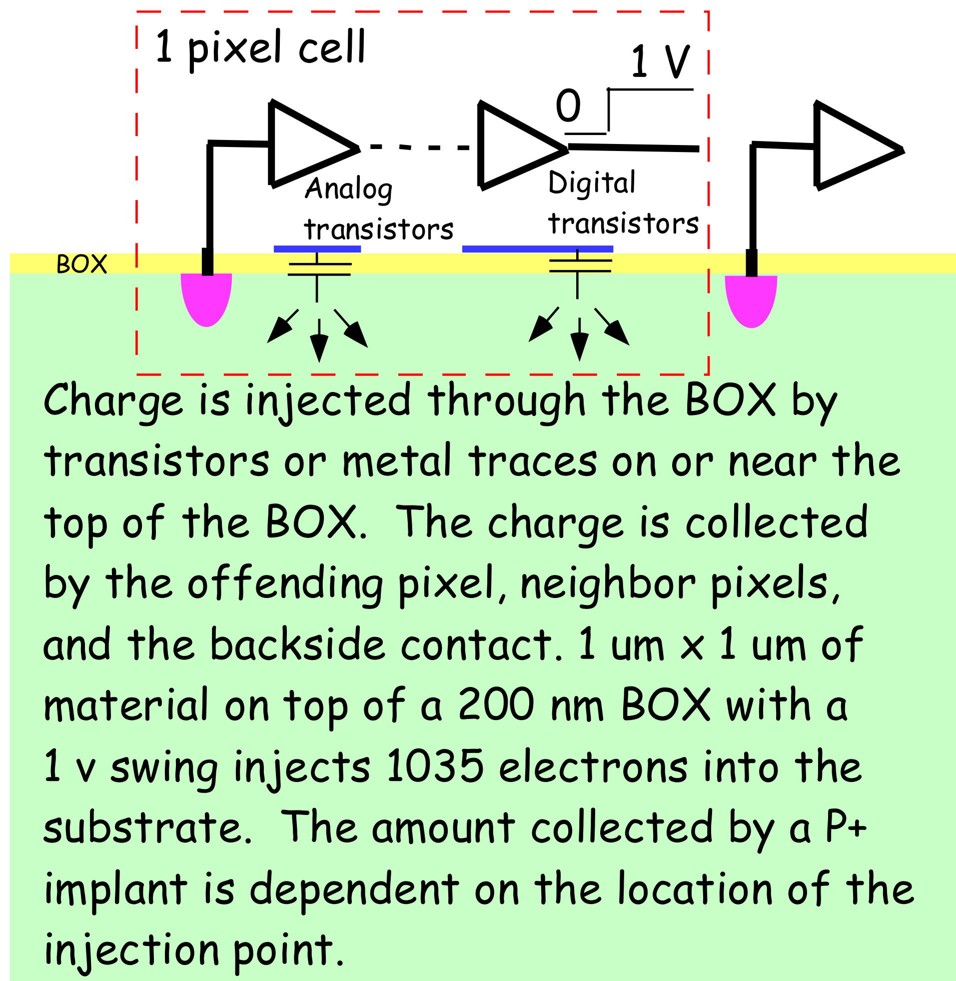
This problem can be solved by placing p+ implants relatively close together or by use of Flexfet transistors as shown on the next slide.

- ASI (American Semiconductor Inc.) has a process based on dual gate transistor called a Flexfet.[4]
  - Flexfet has a top and bottom gate.
  - Bottom gate shields the transistor channel from voltage on the substrate and thus removes the back gate voltage problem.
  - Bottom gate also shields the transistor channel from charge build up in the BOX caused by radiation.



Fermilab has an SBIR with ASI to characterize diodes in the substrate that are connected through the BOX to electronics in the thin top layer

3) The Box is relatively thin, permitting the circuit to capacitively inject charge into the substrate which is collected by the sensing diodes.



Charge is injected through the BOX by transistors or metal traces on or near the top of the BOX. The charge is collected by the offending pixel, neighbor pixels, and the backside contact. 1 um x 1 um of material on top of a 200 nm BOX with a 1 v swing injects 1035 electrons into the substrate. The amount collected by a P+ implant is dependent on the location of the injection point.

Note: capacitive coupling should be considered whenever layers are very close to the detector. (Bump bond spacing is helpful.)

Problem can be mitigated by

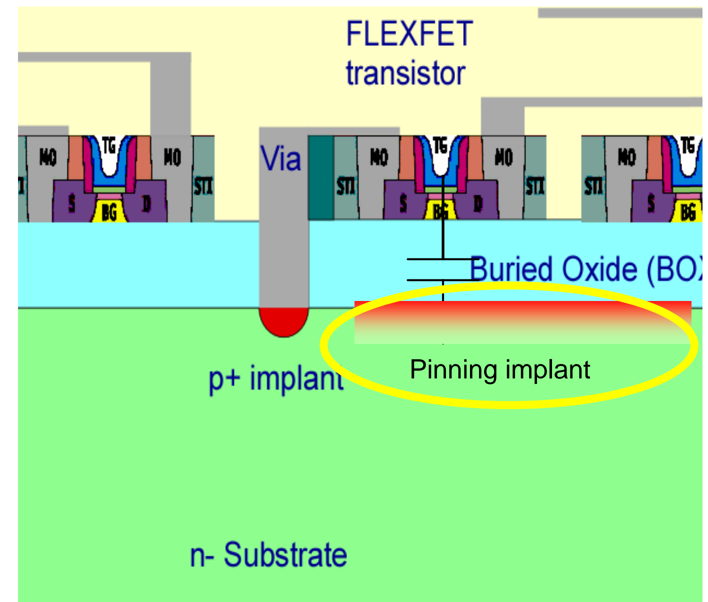
a) Using thicker BOX
b) Using differential signals
c) Dividing circuit design into two tiers such that there is no electrical activity above the BOX during the signal acquisition period.
d) Add a pinning layer as shown on the next slide.

Pinning Layer

- SOI detectors are sensitive to capacitive coupling of CMOS signals to the pixel diode.

    Adding a "pinning" layer at the surface of the substrate, between pixels, tied to a fixed potential can reduce the problem.

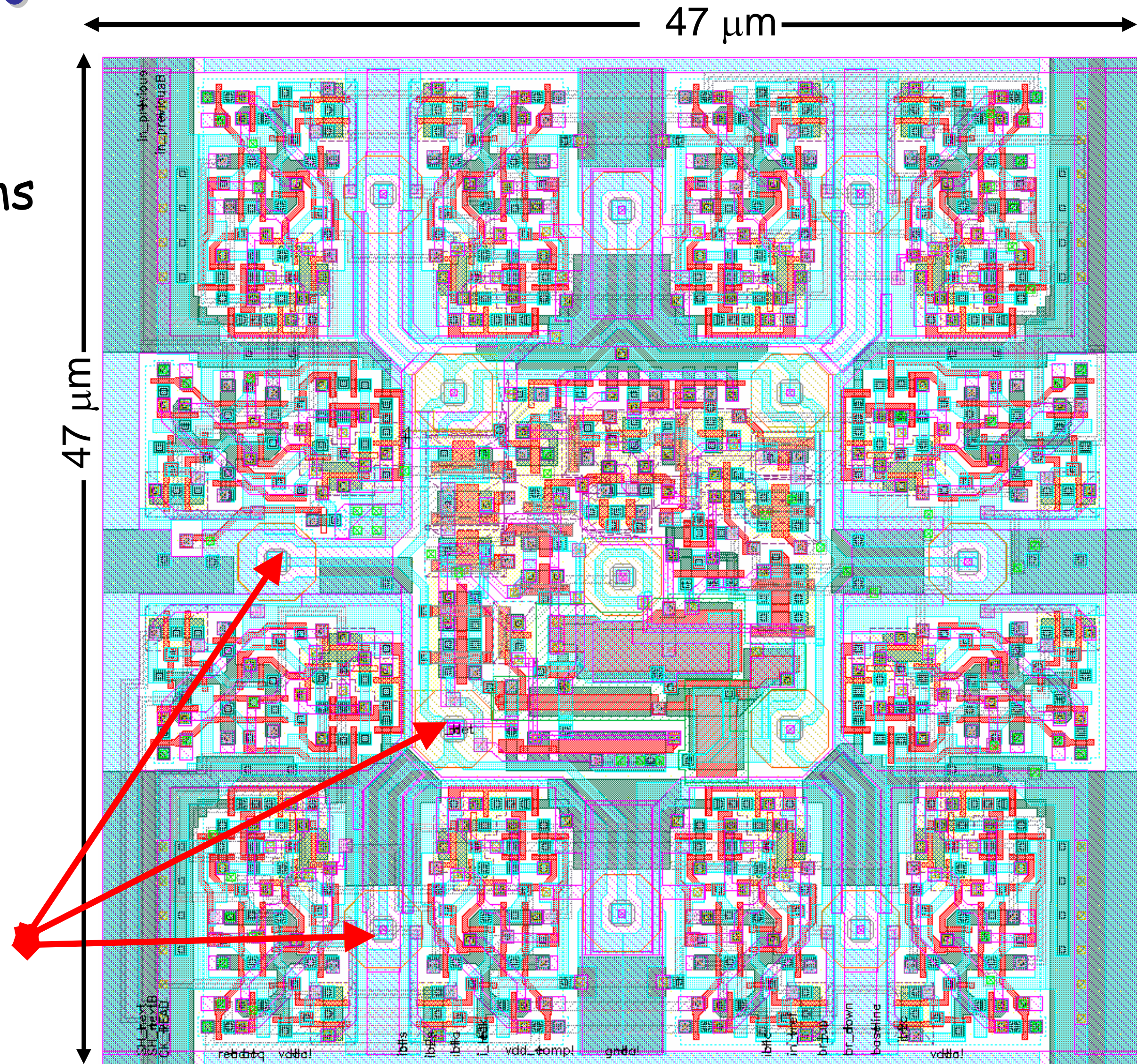
- 2D / 3D Silvaco device simulations confirm effectiveness of pinning layer.
- However, pinning layer can also increase capacitance, make depletion harder, and trap charge. More study needed.
- Available in ASI



MAMBO2 Project

Architecture changed to correct for problems identified in MAMBO1

BOX reduced from 400 nm in 0.15um process to 200 nm in 0.20 um process – not good for charge injection problem.



13 charge collecting diodes

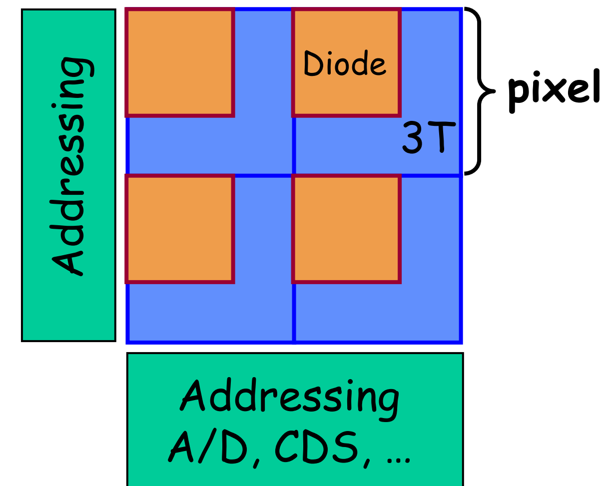
Further SOI Work

- Test MAMBO2 when it arrives
  - Chip was due in April
  - Due to a via fabrication problem, a second run has been started. Chip due end of May.
- Continue work with ASI on development and characterization of SOI detectors.
- Fermilab is part official US-JP program for "Development of Advanced Pixel Sensors in SOI Technology" with funding coming from Japan.

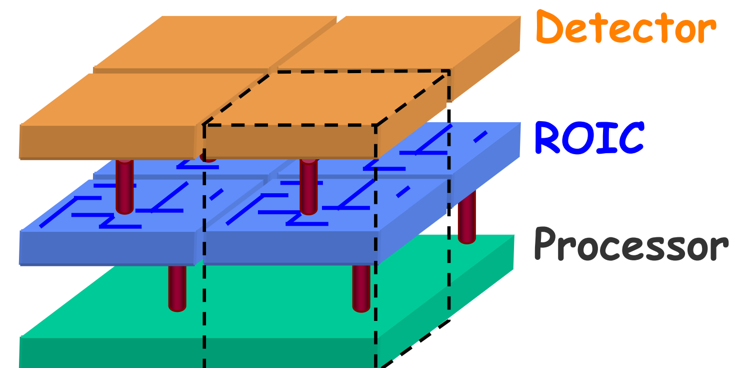
3D or Vertical Integration

- Conventional MAPS
  - Pixel electronics and detectors share pixel area
    - Fill factor loss
    - Fabrication of diodes and ROIC is not optimized
  - Control and support electronics placed outside of imaging area
- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
    - Fabrication optimized for each layer
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable
- 3D Technology driven by industry
  - Reducing trace length reduces R, L, C for higher speed
  - Reduces chip I/O pads
  - Provides increased functionality
  - Reduces interconnect power, crosstalk

Conventional MAPS



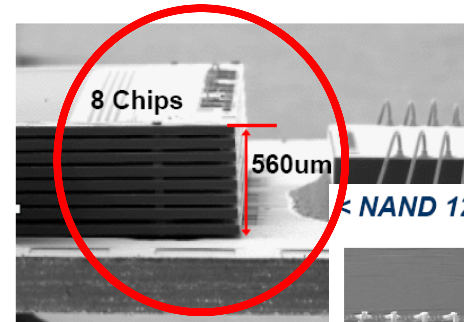
3-D Pixel



Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - Both IBM and Samsung could be in production this year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix [5,6,7]
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >



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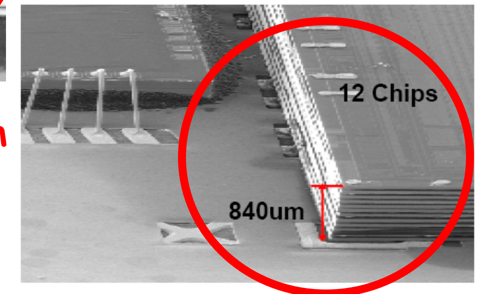
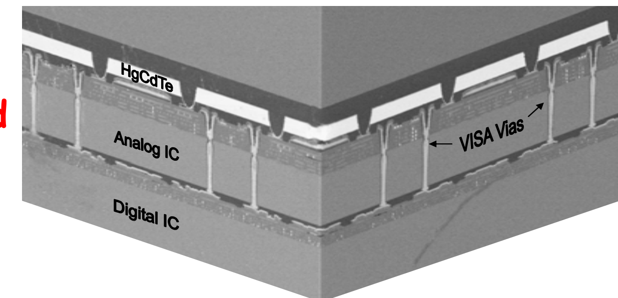


Samsung – 30 um laser drilled vias in 70um chips

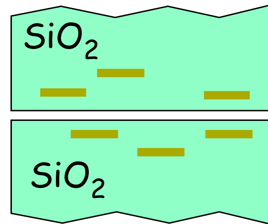
RTI Infrared Imager

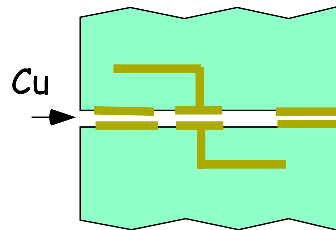


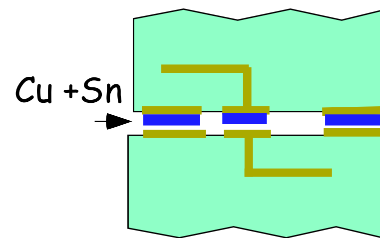
Four Key Technologies for 3D ICs [8]

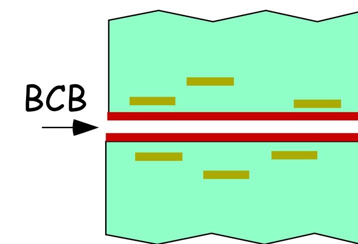
- Bonding between layers
  - Oxide to oxide fusion
  - Direct copper fusion
  - Copper/tin bonding
  - Polymer bonding
- Wafer thinning
  - Grinding, lapping, etching, and CMP
- Through wafer via formation and metallization
  - With isolation
  - Without isolation
- High precision alignment
  - Less than 1 micron

Bonding Techniques









Direct silicon fusion bonding

Mechanical bond

Exceptionally flat and clean surfaces are necessary.

Pressure and temperature used to fuse wafers.

Plasma treated surfaces reduce bonding temperature to 300 ^{0}C.

Copper to copper fusion bonding

Electrical + mech.

Very high degree of planarity is needed.

Full contact is necessary

Large area of copper generally used to mate surfaces.

Bonding done at 400 ^{0}C

Copper-tin eutectic bonding

Electrical + mech.

Tin is added to form eutectic bond at a lower temperature (250 ^{0}C).

Large area of copper generally used.

Can be used to encapsulate bonds.

Adhesive (BCB) bonding

Mechanical bond

Typical adhesive polymer used is BCB.

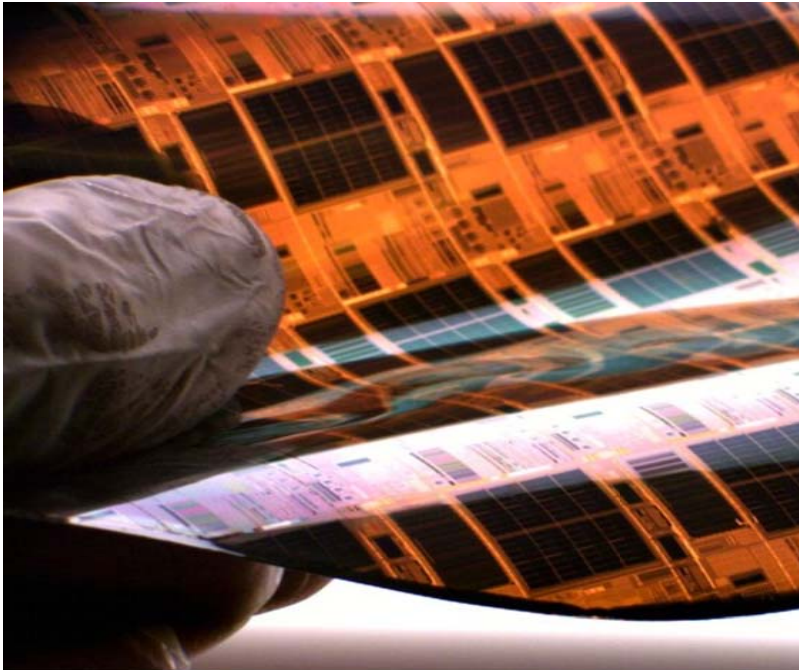
Most tolerant of uneven bonding surfaces such as non-planarized surfaces.

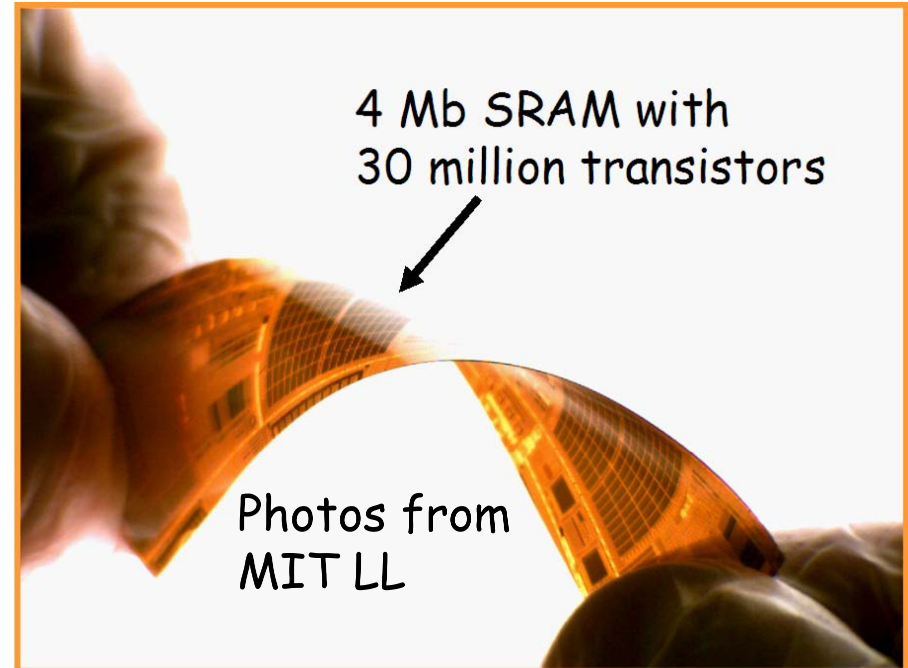
Low adhesive temperature may affect later procesing steps.

Wafer Thinning

Through wafer vias typically have an 8 to 1 aspect ratio for etched vias. Thus, in order to keep the area associated with the vias as small as possible, the wafers should be as thin as possible. This is critical for small pixel designs.

Thinned SOI wafer from MIT Lincoln Laboratory

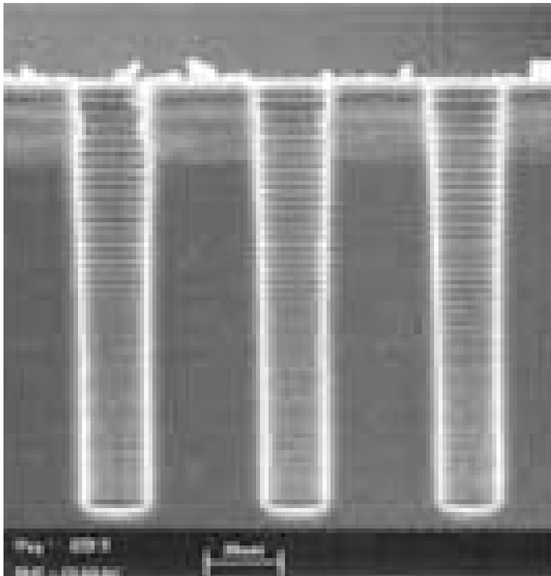




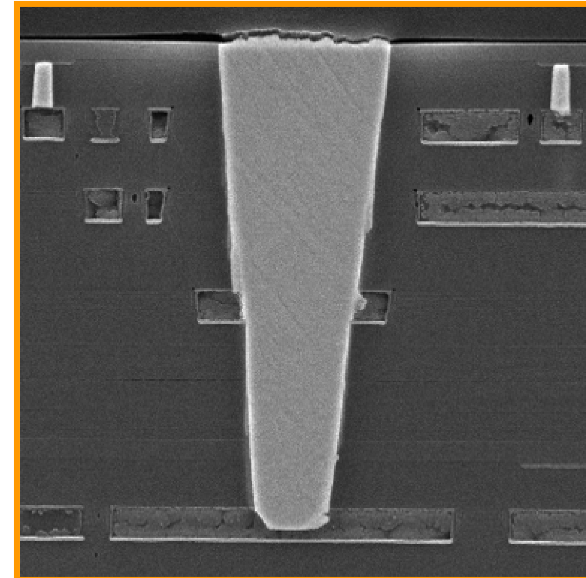
Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

Through Wafer Vias and Metallization

- Small diameter vias are critical for high circuit density circuits.
- Passsivation
  - Vias in CMOS must have via holes passivated (extra step) to prevent short circuits.
  - Vias in SOI require no passivation before metallization.



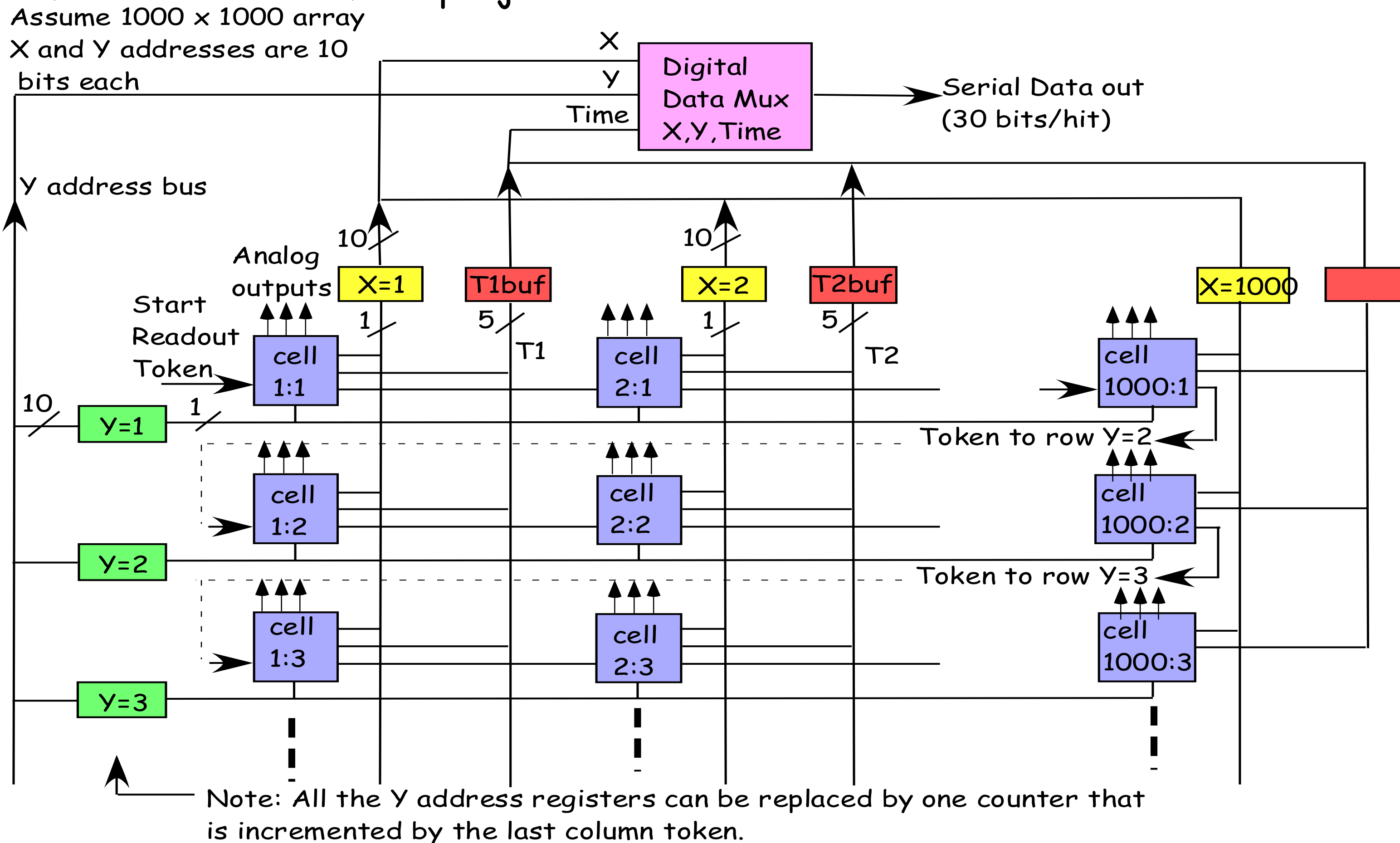
SEM of 3 vias In CMOS using Bosch Process[9]



Filled via using oxide etch process in SOI (Lincoln Labs)

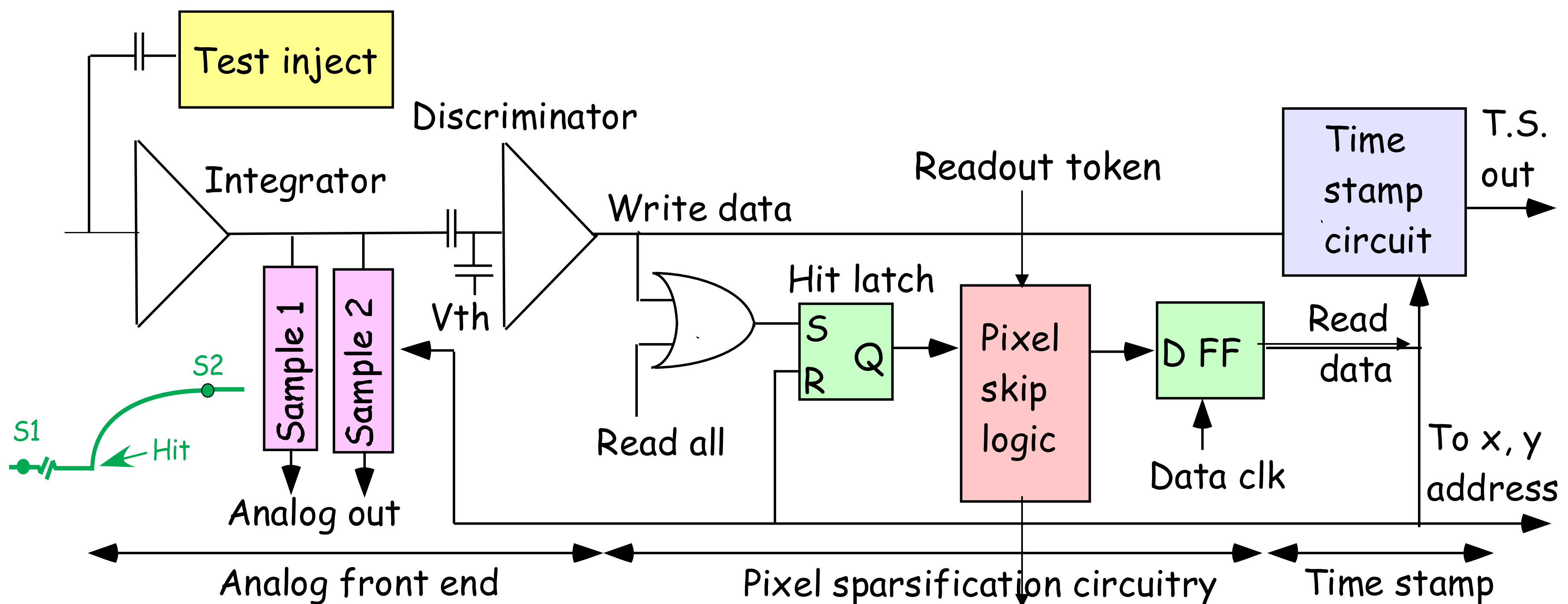
VIP1 - A 3D Pixel Design for ILC Vertex[10]

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
  - Key features: Readout between bunch trains, analog pulse height, sparse readout, high resolution time stamps (~1us), test inputs, 20 um pixels. - <u>Meets all ILC critical requirements.</u>
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- 64 x 64 pixel demonstrator version of 1k x 1K array.
- Submitted to 3 tier multi project run. Sensor to be added later.

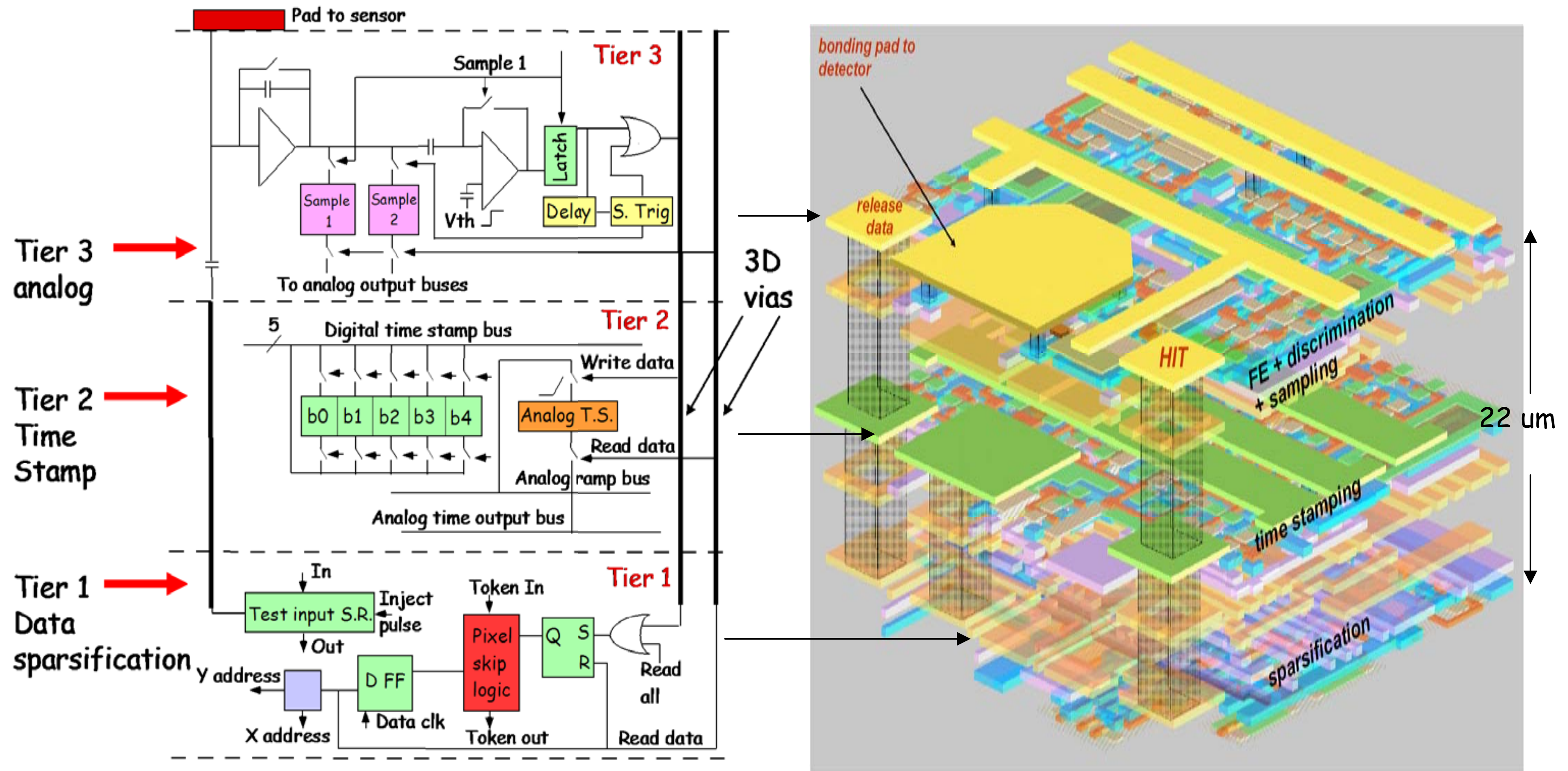


Simplified Pixel Cell Block Diagram

- When a Hit occurs, the Hit pixel stores Sample 1 & 2 and the Time Stamp, and sets the Hit Latch in sparse readout circuit.
- During readout, when the read out token arrives, the time stamp and analog values are read out, and pixel points to hit address found on perimeter of chip.
- While outputting data from one pixel, the readout token is passed ahead looking for next pixel that has been hit.

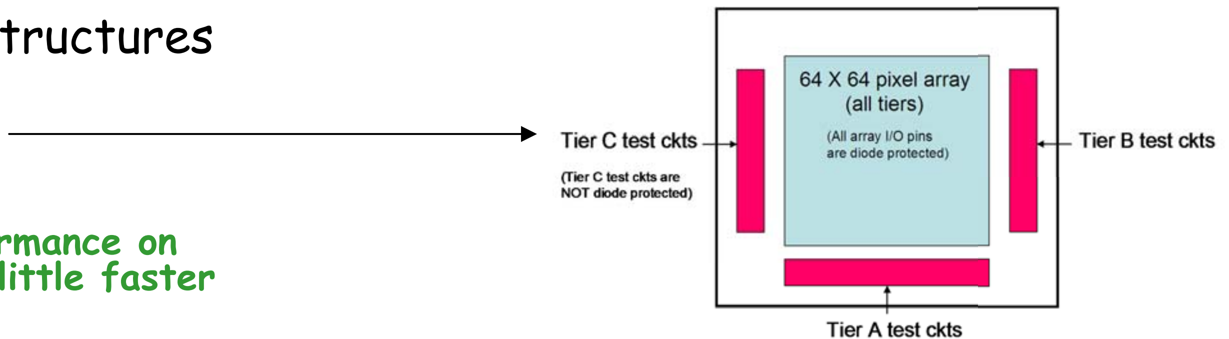


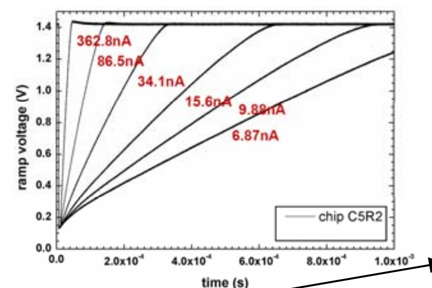
3D Three Tier Arrangement for ILC Pixel

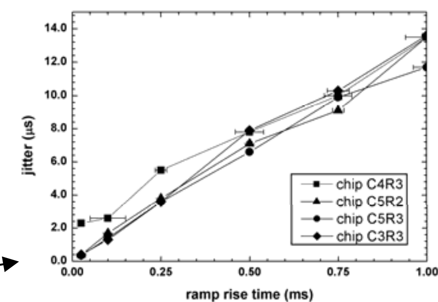


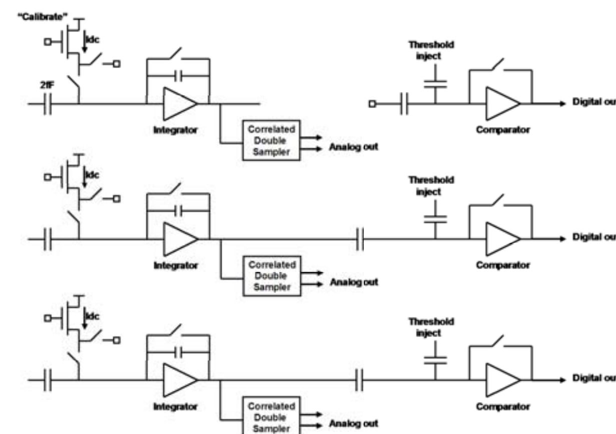
VIP1 Test Results

- Chip is divided into test structures and 64 x 64 array
- Test structure results
  - Bottom tier (tier 1)
    - Simple buffer – performance on one working part is a little faster than simulations
    - Dynamic FF (used for inject in full array) – T_r and T_f should be less than 5 ns for proper operation
  - Middle tier (tier 2)
    - Time stamp ramp test
      - Ramp circuit works but…
        - » Current mirror on different chips gives very different ramp currents
        - » Noise on ramp may be ~~due~~ to protection diodes causing jitter in ramp timing
  - Top tier (tier3) analog ckts
    - Integrators work on some chips
    - Discriminators work on other chips
    - Analog circuits when working are a little faster than simulations.
    - Noise performance appears close to simulations on the few circuits that work



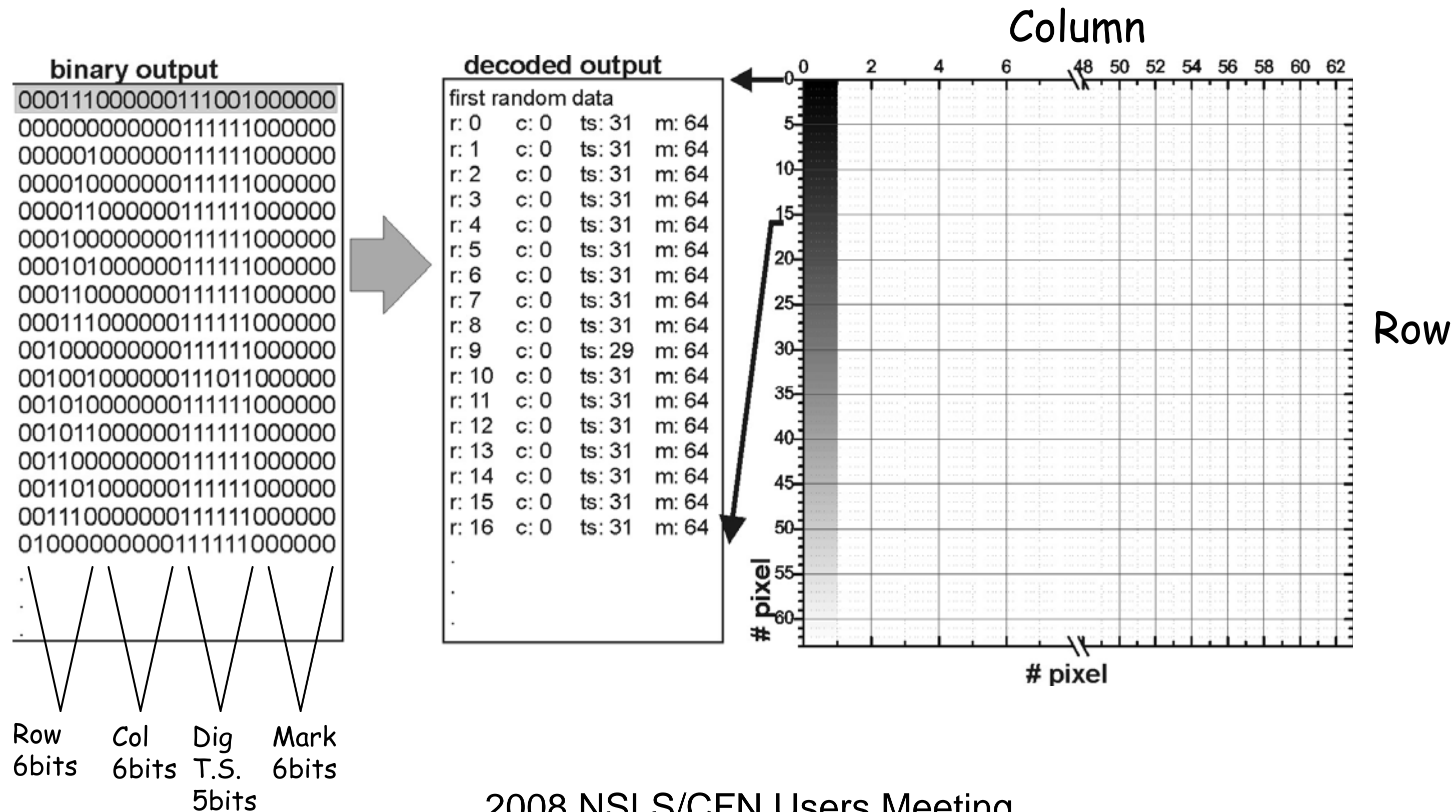






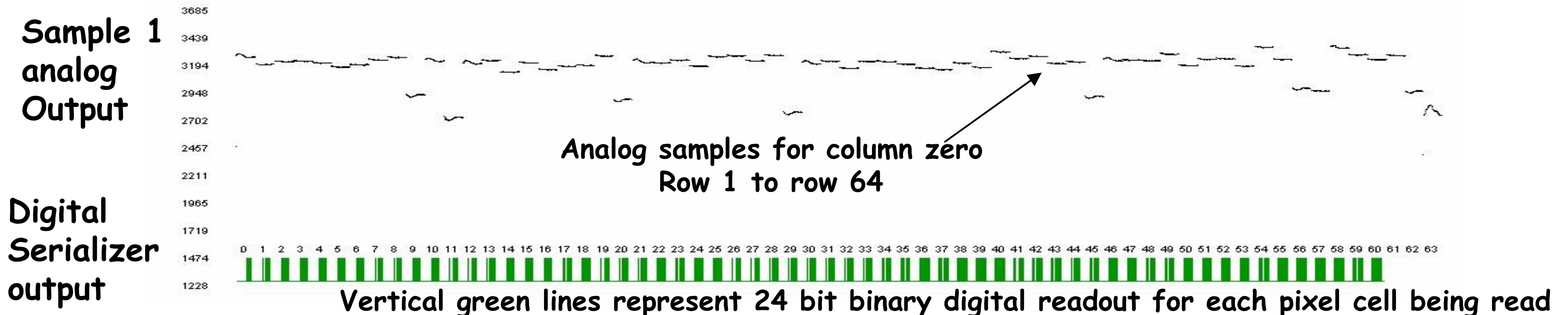
VIP1 Test Results

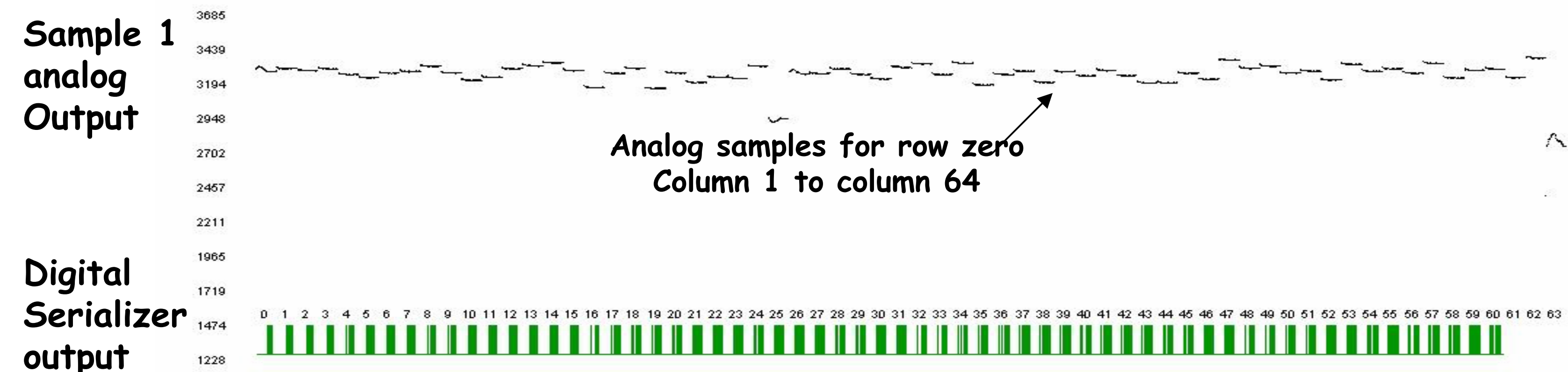
- Preliminary full array results – data acquisition still under development
  - Digital Results
    - Serial readout for address partially working on some chips for $0.9<V_{dd}<1.3$ V. Circuits do not work at nominal voltage.
    - Serial Shift Register for charge injection works on some chips for $1.0<V_{dd}<1.2$V.
    - Feature needed for large arrays (read all cells in column 1) works as shown below



VIP1 Test Results

- *Analog test results*
  - Data acquisition system used to measure analog pedestals on Sample 1 output
  - Double correlated sample results in dramatic reduction in pedestal variation.
  - The full 64 x 64 array has subarrays with different transistor sizes and input capacitances to help evaluate noise performance.
    - Array noise tests not yet done



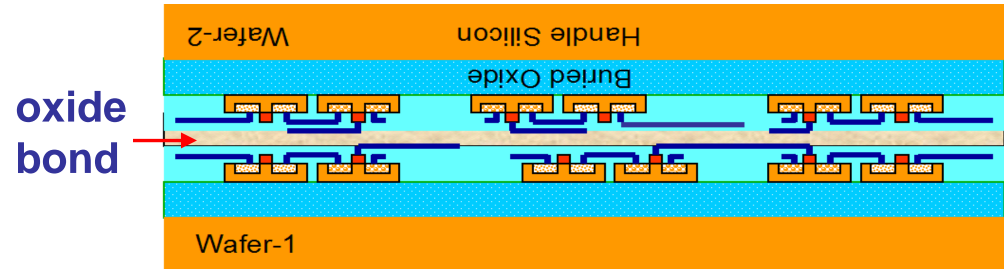


MIT LL 3DM2 Vertical Integration Process Flow

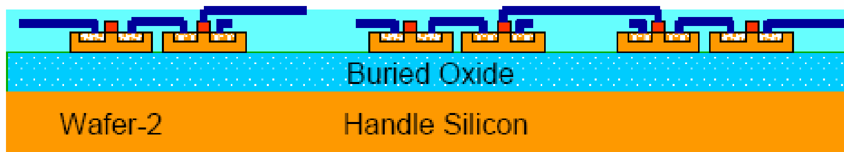
"Via last" process – vias are formed after FEOL and BEOL processing is completed

Step2: Invert, align, and bond wafer 2 to wafer 1

oxide bond



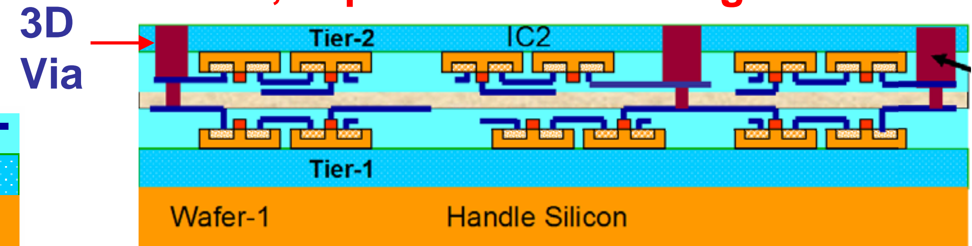
Step 1: Fabricate individual tiers



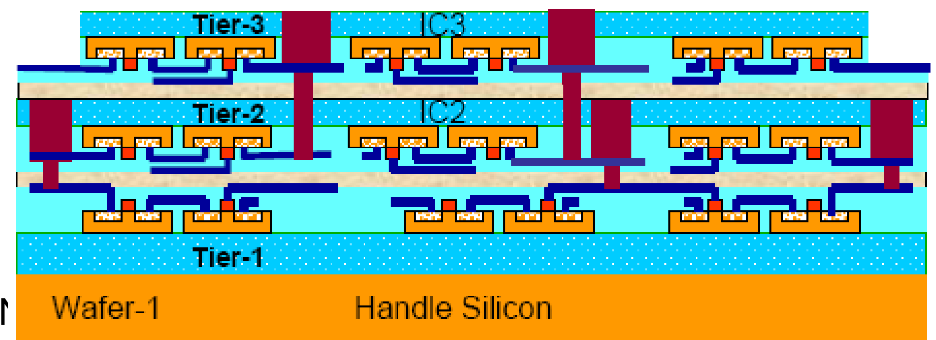
In principle wafer 1 could also be bulk

Step 3: Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via



Step 4: Invert, align and bond wafer 3 to wafer 2/1, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3, etch bond pads



VIP1 Problems

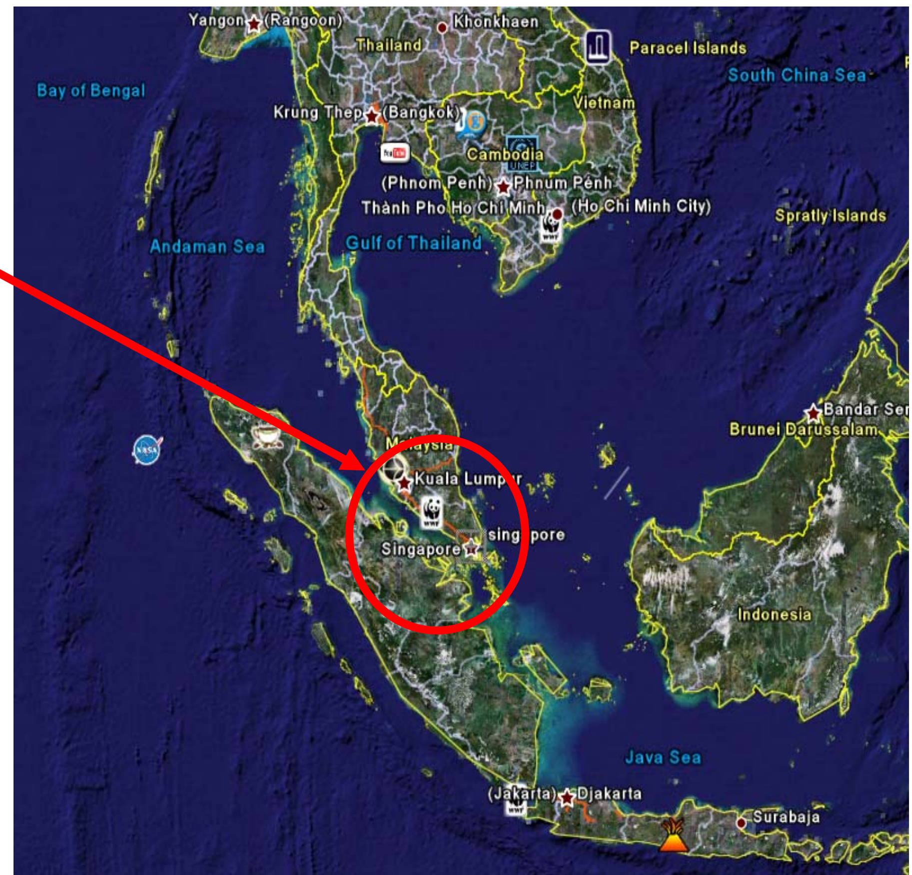
- VIP1 took one year to fabricate
- Trapped charge between tiers 2 and 3 during fabrication caused NMOS transistor thresholds to shift from 500 mv to 200 mv.
  - Attempts are being made by vendor to correct the problem after the fact with UV radiation
  - Backup lot being processed with different tier2-tier3 bonding conditions to remove threshold shift problem.
- ESD protection diodes are very leaky causing serious problems for circuits with analog inputs.
- Current mirrors used for biasing are not working properly - problem thought to be due to leakage path in the current mirror circuits – still investigating.
- There are significant variation between chips resulting in low yields - reasons unknown at this time.
  - Testing will continue with parts from a different wafer
  - Discussions are ongoing with other users
- VIP2a will be submitted later in 2008

A Program to Use Commercial Vendors for 3D Circuits

- To avoid difficulties in using a non commercial foundry such as MIT LL and difficulties in developing a via technology such as with OKI or ASI, our interest has shifted toward looking for commercial vendors for 3D
- There are 3 vendors that I know have commercially available (external) 3D processes.
  - Tezzaron – uses CuCu thermocompression for bonding
  - Ziptronix- uses Direct Bond Interconnect (oxide bonding)
  - Zycube – uses adhesive and In-Au bumps for bonding
- Fermilab is working with Tezzaron to fabricate 3D integrated circuits using CuCu bonding.
  - Others developing CuCu bonding include IBM, RPI, MIT, IMEC
- Fermilab is also working with Ziptronix to do low mass bonding with DBI to detectors as a replacement for conventional bump bonds. (Have order to bond FPIX chips to 50 um thick sensors.)

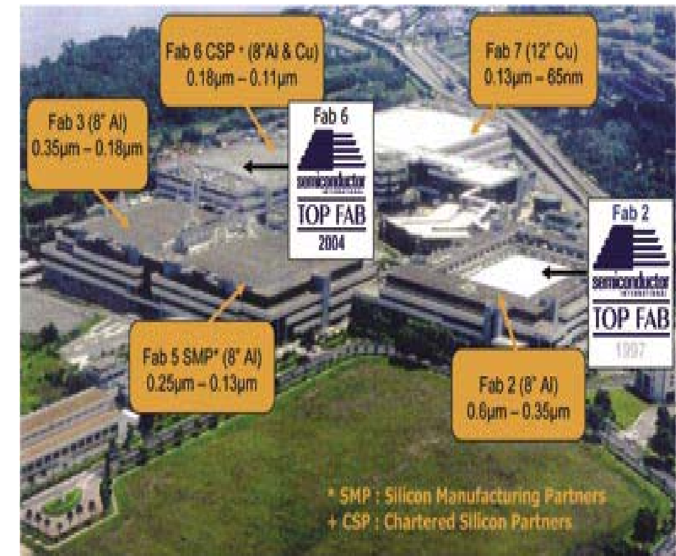
Tezzaron Background

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



Chartered Semiconductor

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Tezzaron chose the Chartered 0.13 um mixed signal CMOS process for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Working on extending 3D to 300mm wafers and 45nm process
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic



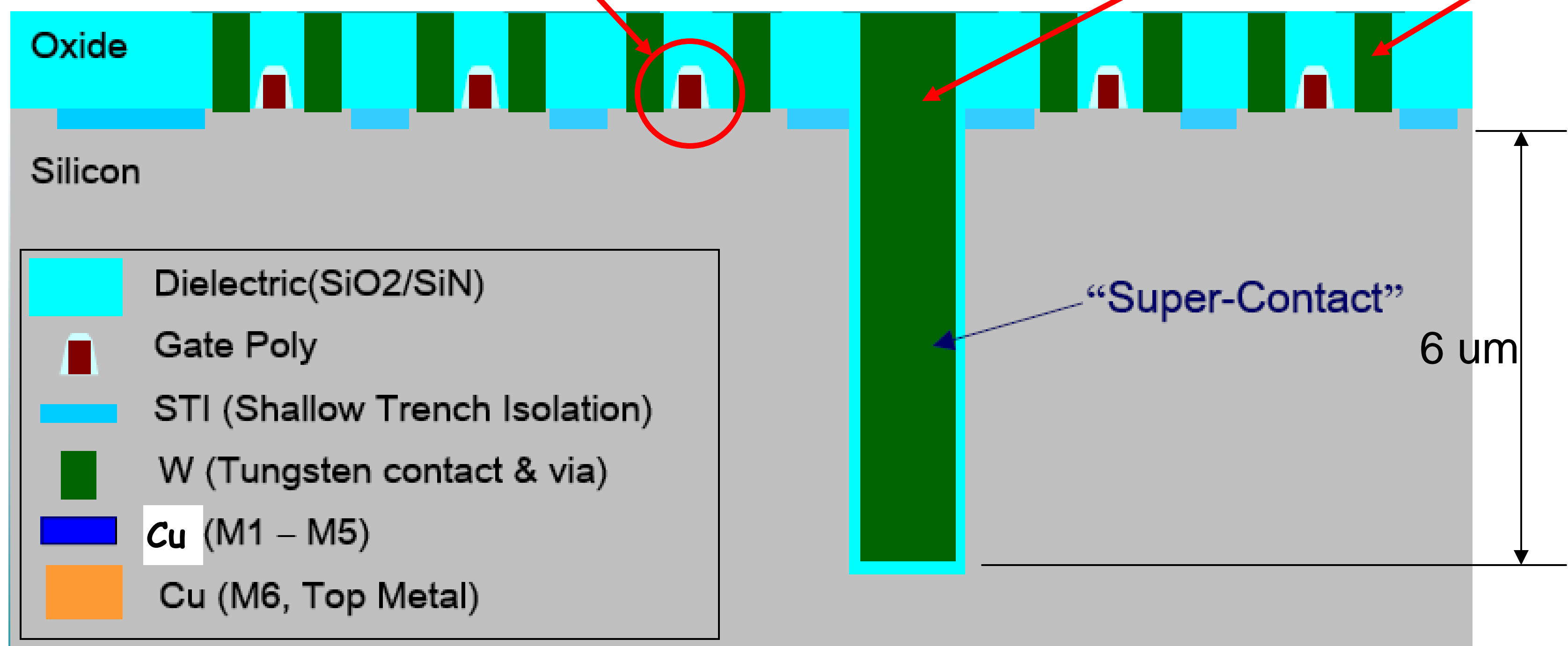
Chartered Campus

Chartered 0.13 um Process

- 8 inch wafers
- Large reticule – 26 mm x 31 mm
- Features
  - Deep N-well
  - MiM capacitors – 1 fF/um^2
  - Single poly
  - 8 levels of metal
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously
    - Nominal
    - Low voltage
    - High performance
    - Low power
  - 8-12 ohm cm non-epi substrate for possible use in MAPS

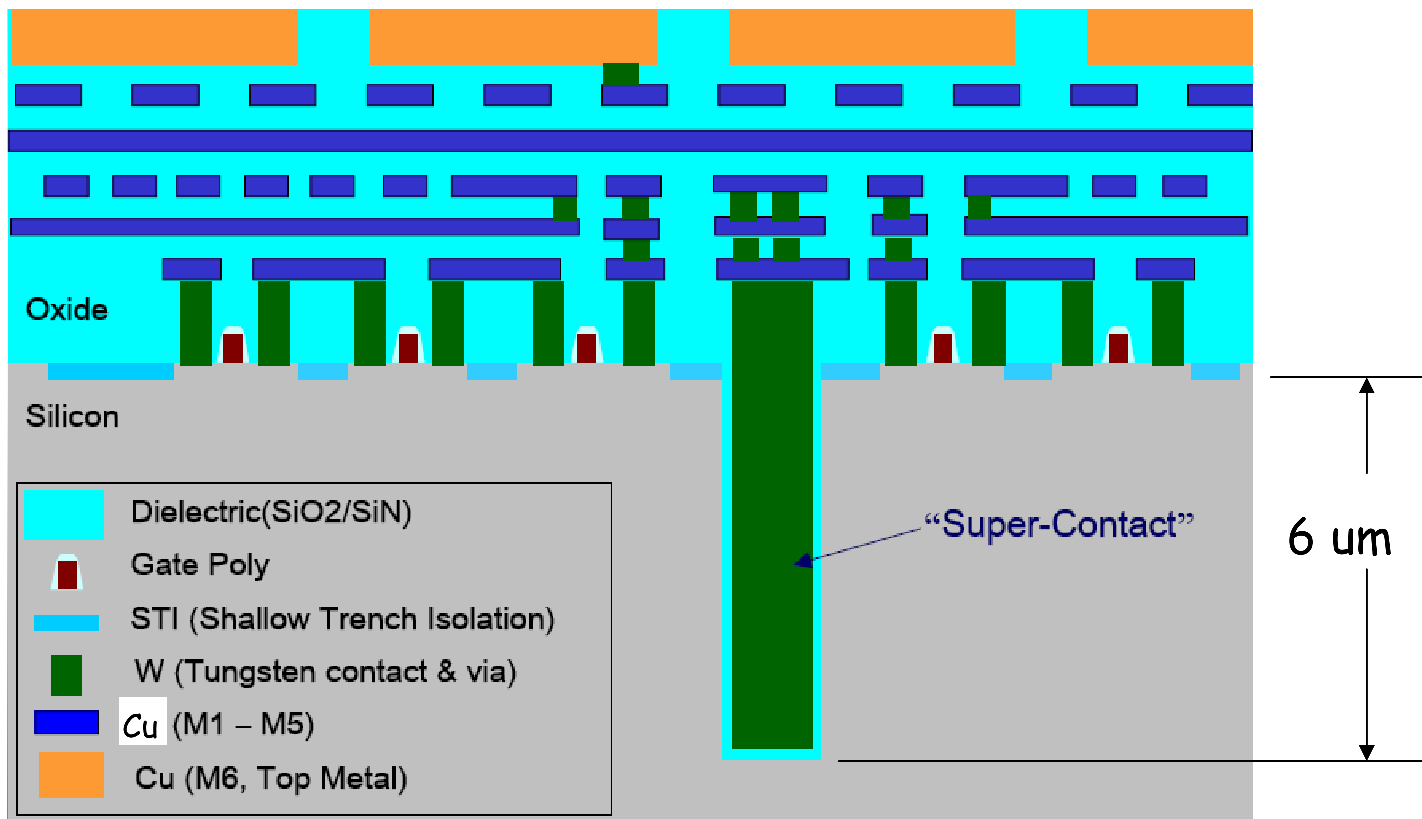
Tezzaron 3D Process[11]

- Through silicon vias are fabricated as a part of the foundry process. "Via first" approach.
- Complete FEOL (transistor fabrication) on all wafers to be stacked
- Form and passivate super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors



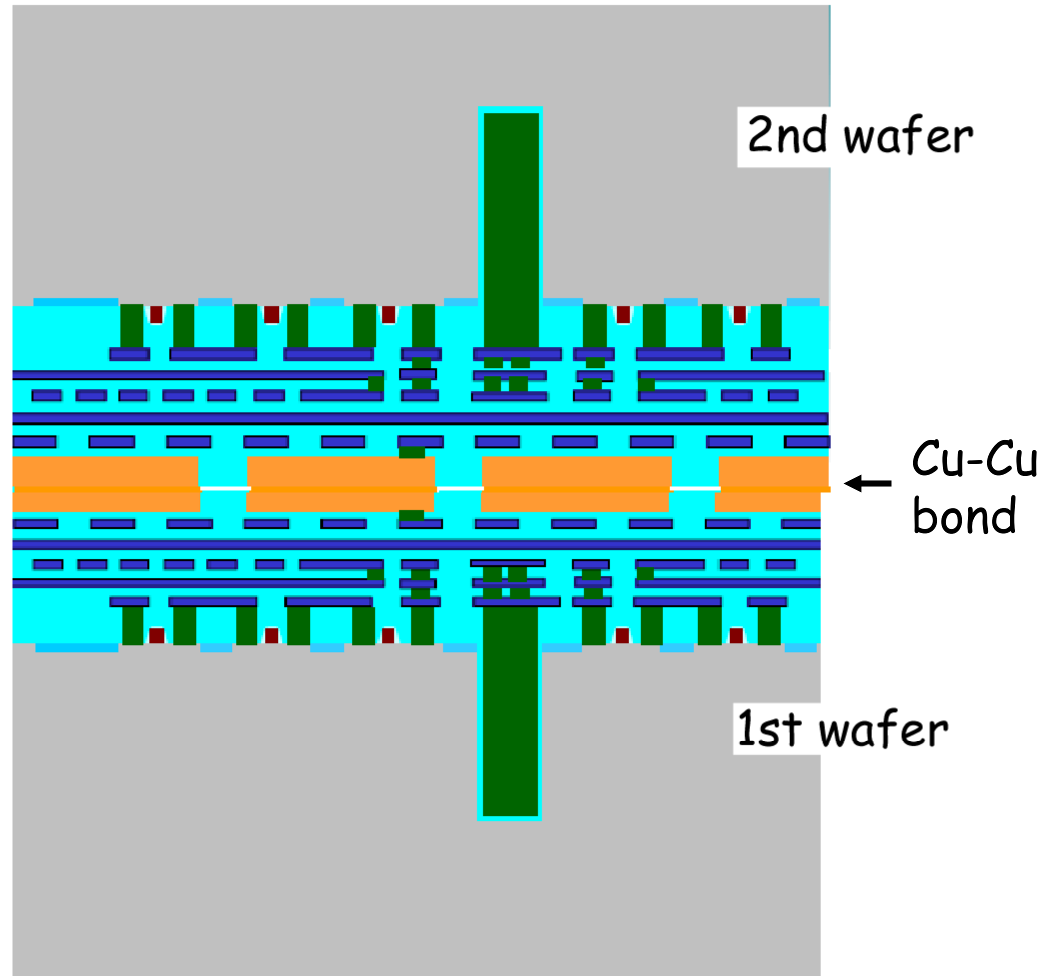
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)



Tezzaron 3D Process

- Bond second wafer to first wafer using Cu-Cu thermo-compression bond

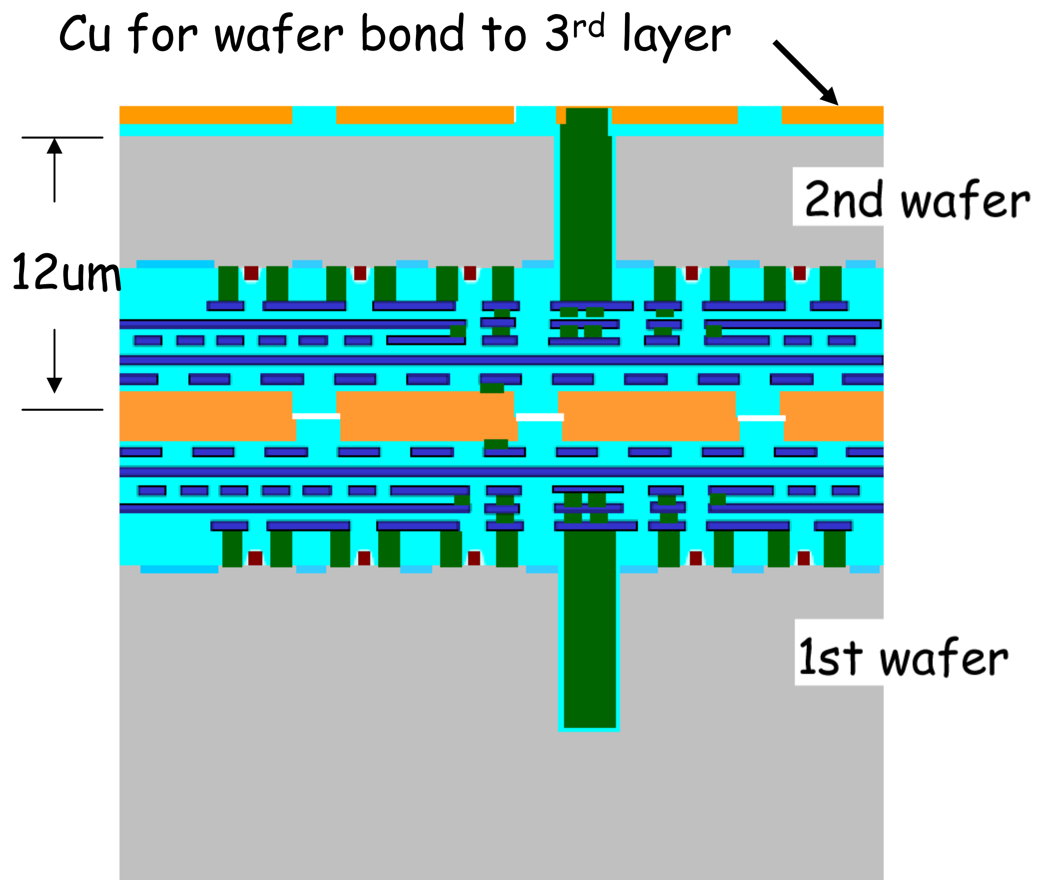


Tezzaron 3D Process

- Thin the second wafer to about 12 um total thickness to expose super via.
- Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer

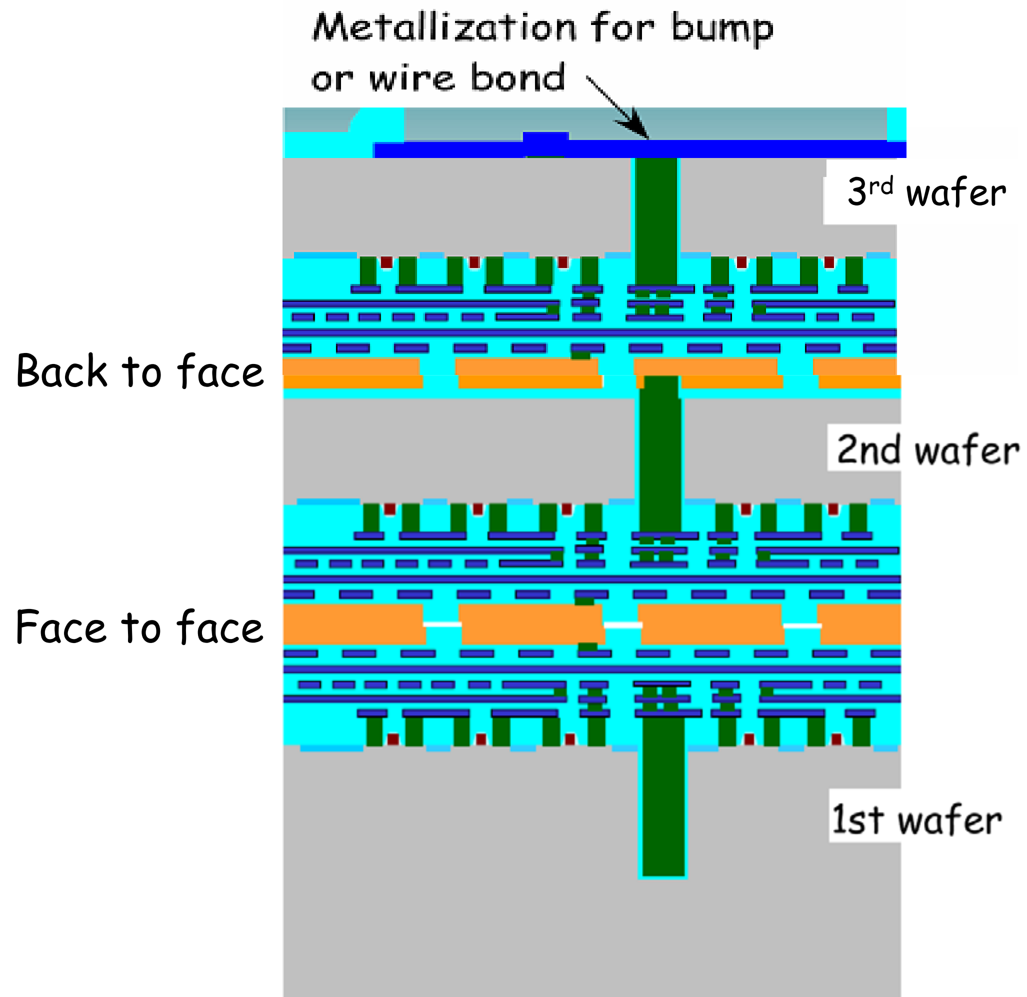
  OR

  add metallization on back of 2nd wafer for bump bond or wire bond.

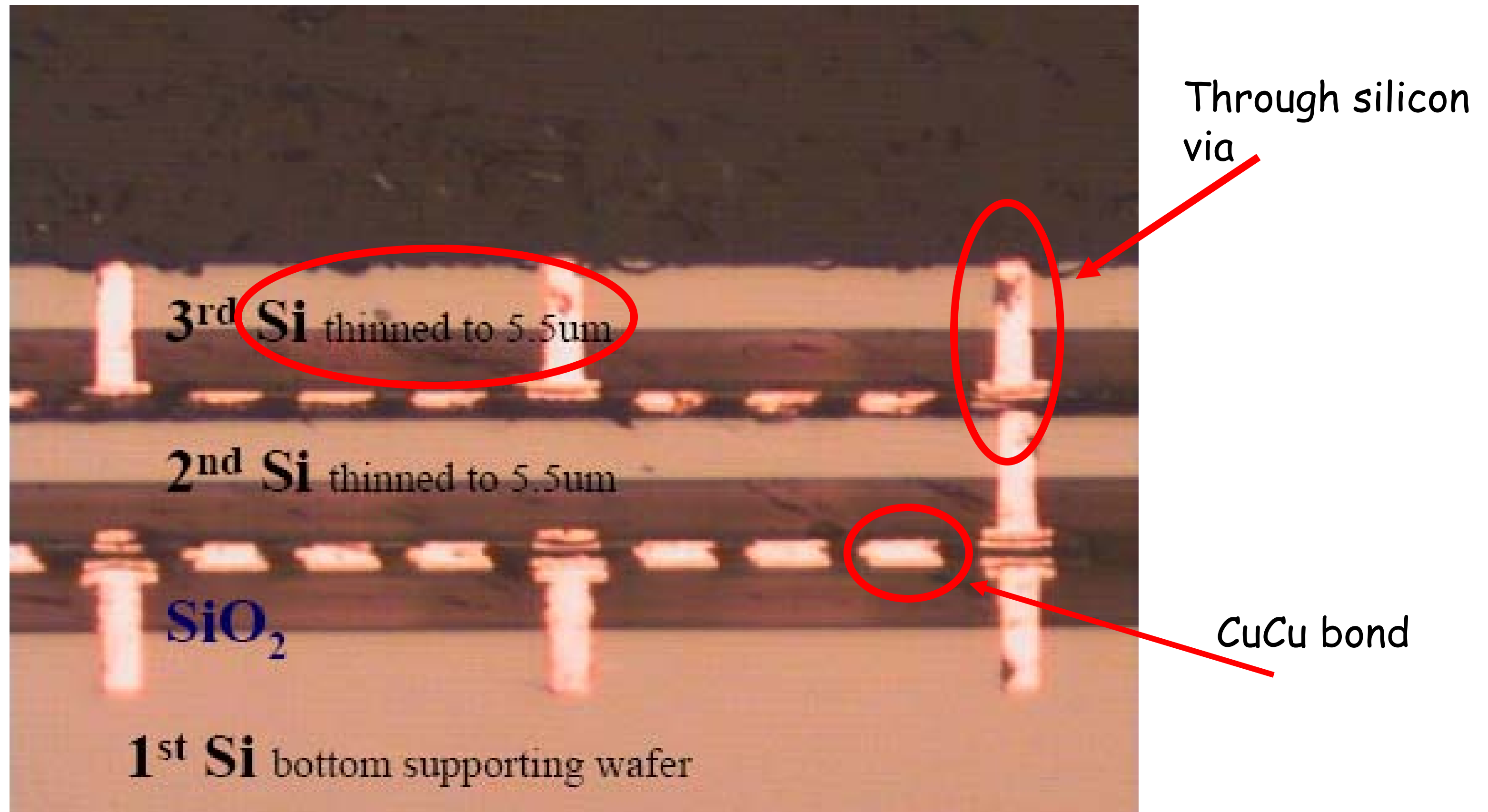


Tezzaron 3D Process

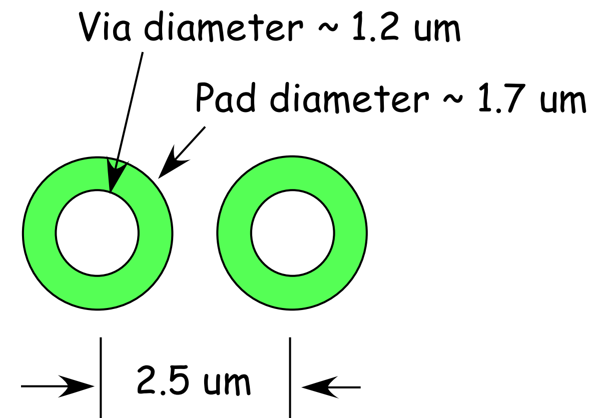
- Stack 3rd wafer
- Thin 3rd wafer (course and fine grind to 20 um and finish with CMP to expose W filled vias)
- Add final passivation and metal for bond pads



Cross section of Tezzaron 3 Layer Stack[11]



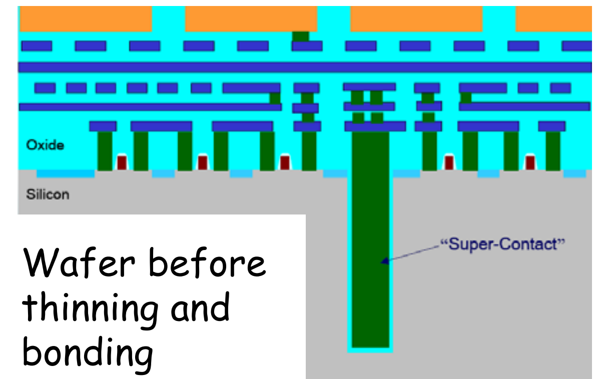
Tezzaron Vias and Bonding

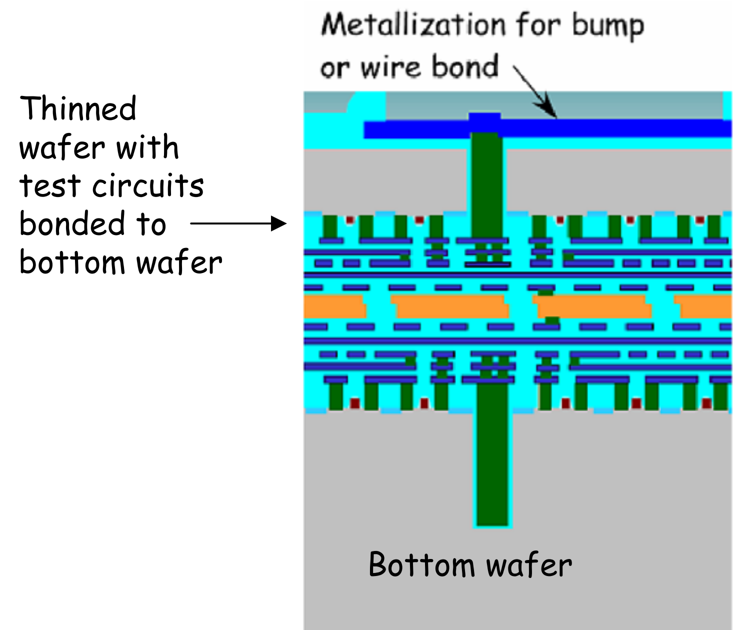


- Via size plays an important role in high density pixel arrays
- Tezzaron has small vias that can be placed close together
- Wafer bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 um
- Missing bond connections = 0.1 PPM
- Temp cycling of bonds from -65 to + 150 C
  - 100 devices, 1500 cycles, 2 lots, no failures

Circuit Performance

- Circuits tested with full substrate thickness and then after bonding and thinning to 12 um
  - No change in performance between thinned and bonded devices and unthinned/unbonded devices.
    - Bandgap circuit
    - Sense Amplifier
    - Charge pump
  - No change in performance between thinned and bonded devices before and after temperature cycling.
- Transistor measurements on same devices before and after thinning have been completed
  - No noticeable difference in characteristics except small increase in PMOS speed due to strain in silicon as expected



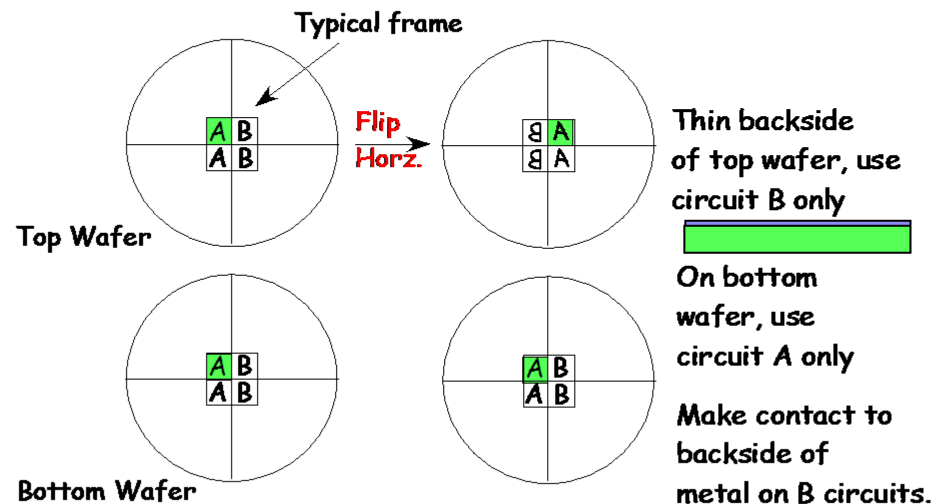


Advantages

- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Good models available for Chartered transistors
- Thinned transistors have been characterized
- Process supported by commercial tools and vendors
- Fast assembly
- Lower cost

Fermilab 3D Multi-Project Run

- Fermilab will be submitting a 3D multi project run using Tezzaron.
- There will be only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 15.5 x 26 mm)
- The wafers will be bonded face to face.
- Bond pads will be fabricated for bump bonding to be done later at Ziptronix



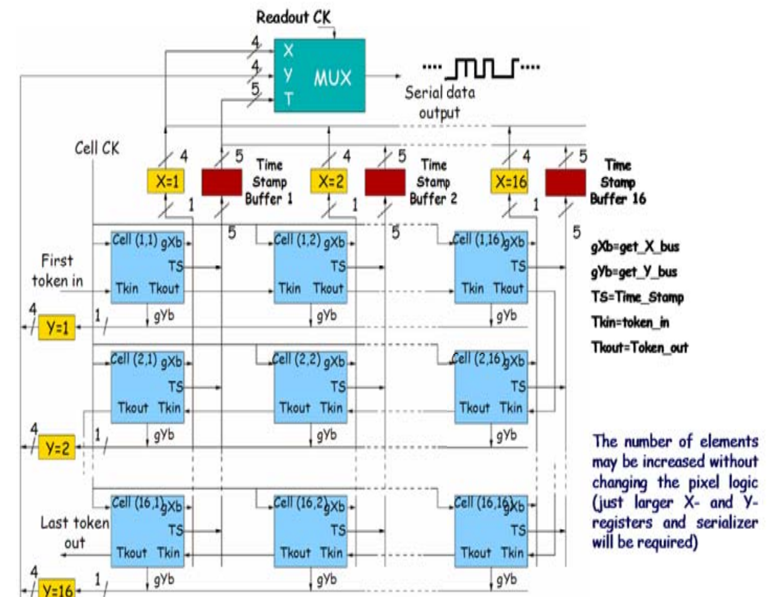
Face to Face Bonding

3D Collaboration Forming

- Recently 4 French laboratories have received funding to perform 3D electronics development
  - Strasbourg - IPHC
  - Orsay - LAL
  - Paris - LPNHE
  - Marseille - CPPM
  - Received LOI from CNRS/In2P3 to join Fermilab MPW run
- INFN has received funding for study of MAPS, including 3D circuit design
  - Received LOI from Universita di Bergamo to join Fermilab MPW run
- Submission expected at the end of 2008 or beginning of 2009 with delivery of 3D parts 12 weeks later

ILC Projects in Tezzaron MPW Run

- Marc Winter (Strasbourg) is intending to work with Fermilab to develop a simple 3D MAPS device with 7 bits of time stamping for the ILC.
- Valerio Re (Bergamo) has designed and built a MAPS device using a deep N-Well, for the ILC with sparsification and 5 bit time stamping.
  - Valerio will work with Fermilab to develop a 3D version of the chip to improve fill factor and pitch and to add features such as expanded time stamping and digitization of analog information



Fermilab VIP2b Design

- VIP2b design essentially the same as MIT VIP2a.
- Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
- Radiation tolerance of Chartered 0.13 um process is currently being studied by another group.
- Going from 3 layers in 0.18 um technology to 2 layers in 0.13 um technology should reduce pixel size below 20 um.
- Using the via first process at Chartered eliminates the wasted area needed for vias in the MIT LL process.
- Chartered provides fully characterized process and models at commercial foundry along with standard cell libraries.
- VIP2b requires significantly less 3D processing than VIP2a

SLHC Projects in Tezzaron MPW Run

- Jean-Claude Clemens and Alexandre Rozanov (CPPM) have expressed interest in converting the current 0.25 um ATLAS pixel design to a 3D structure with 2 tiers in the Chartered 0.13 um process.[12]
- Fermilab intends to develop a 3D chip with 2 tiers of electronics to explore the advantages of 3D for the Super CMS pixel detector.
  - Going from 1 layer of circuitry in a 0.25um process to 2 layers in a 0.13 um process can increase circuit density by a factor of 7.
  - Circuit density can by traded for smaller pixel size.
  - Features to consider for parallel processing
    - In pixel digitization
    - Large digital storage
    - Triggering capability
    - Sparsification
    - Reduction of peripheral circuitry

Summary

- New technologies for detector development are becoming available to scientific community every year.
- Fermilab is exploring SOI detector development and 3D integrated circuit design for application in a variety of areas.
- Industry is making rapid progress in the development of 3D circuits. Our community should closely follow these developments and be prepared to take advantage of them.

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