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3D-IC technology for future detectors

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on behalf of the FERMILAB ASIC design group

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- **OUTLINE:**
  1) *History and introduction*
  2) *Why 3D-IC?*
  3) *Key components for 3D-IC technology*
  4) *3D-IC at Fermilab*
  5) *Roadmaps and summary*

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History and introduction

First electronic components allowing performing nonlinear funnctions were vacuum tubes

Construction of vacuum tubes was complex, their cost was high, but above all they were bulky (not good candidates for miniaturization)D

They are still loved by audiphiles for highest fidelity in sound

But 3D-IC belongs to solid state transistors

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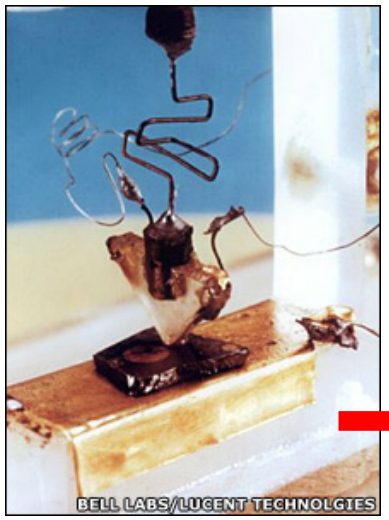
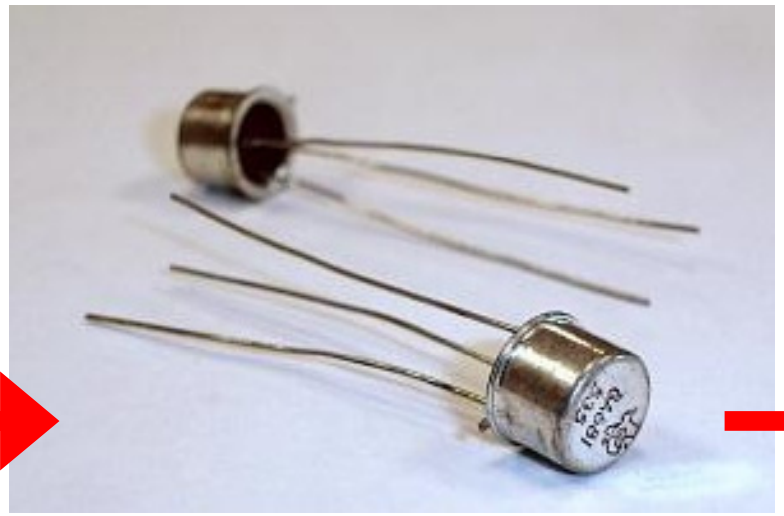
History and introduction

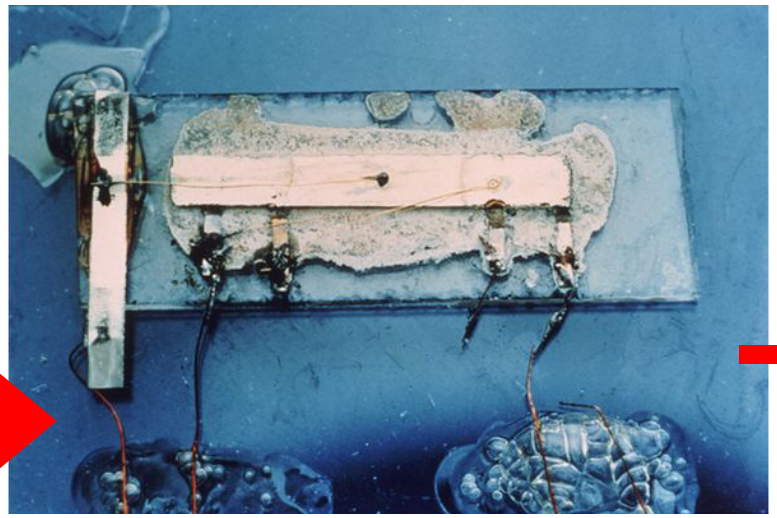


First transistor
(Bell Labs 1947)



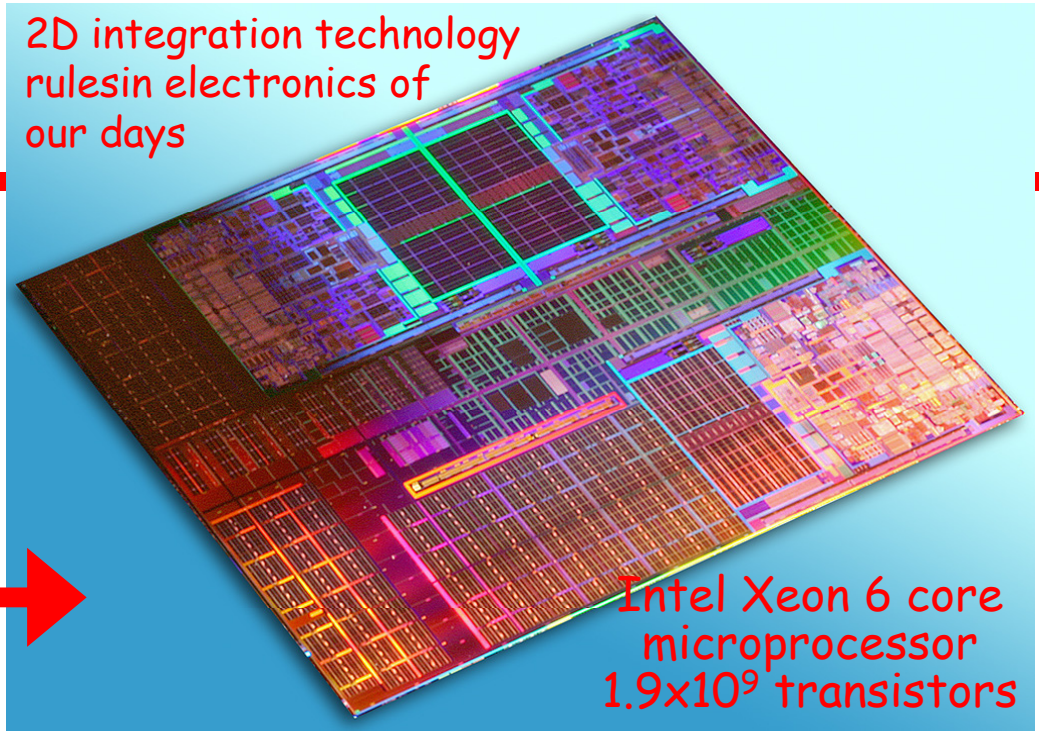
Very soon we have two
and more transistors

First integrated circuit
(Texas Instruments 1958)



More and more components, more and
more functions, growing complexity

2D integration technology
rulesin electronics of
our days



Intel Xeon 6 core
microprocessor
1.9×10^9 transistors

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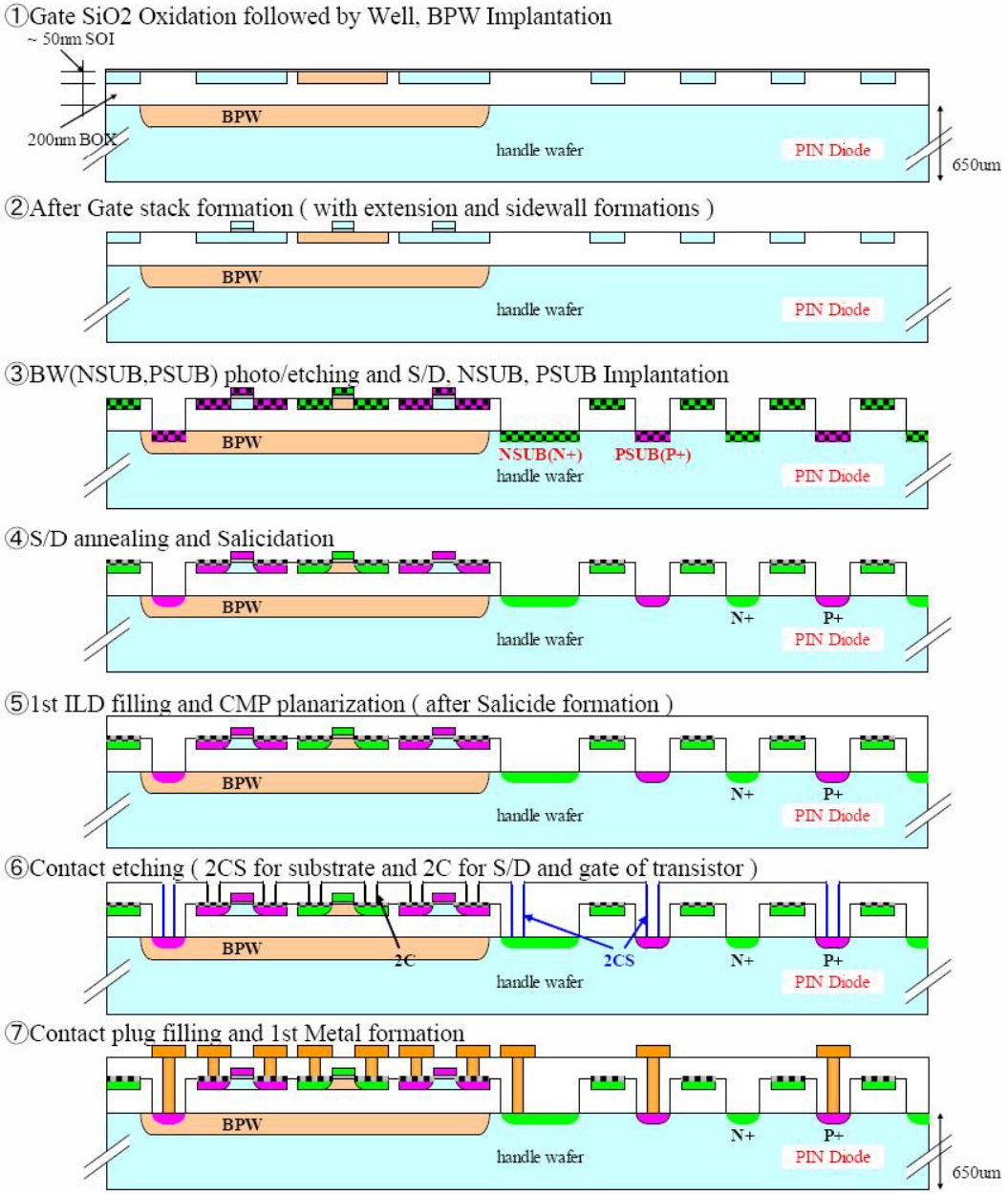
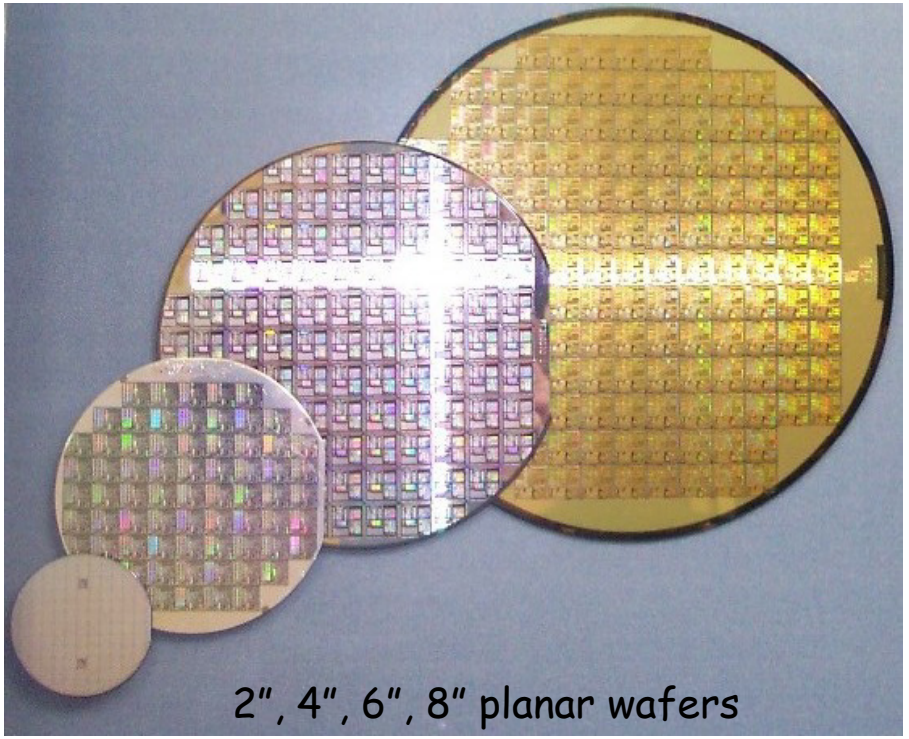
History and introduction

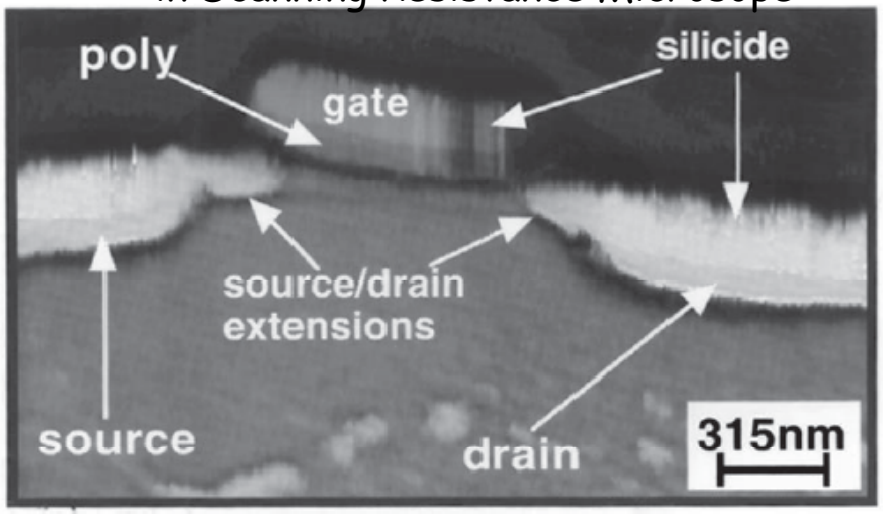


Example of a planar process flow



2", 4", 6", 8" planar wafers

X-section of NMOS transistor seen in Scanning Resistance Microsope



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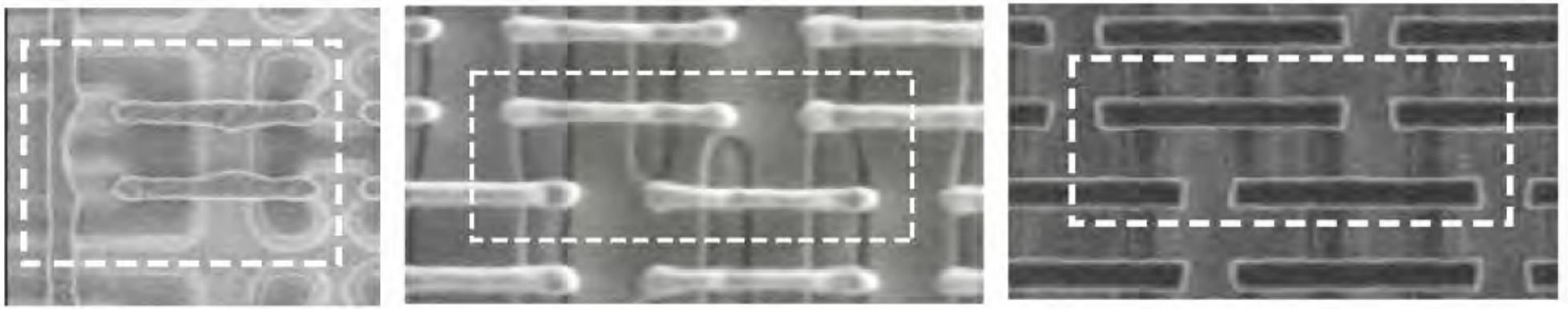
History and introduction

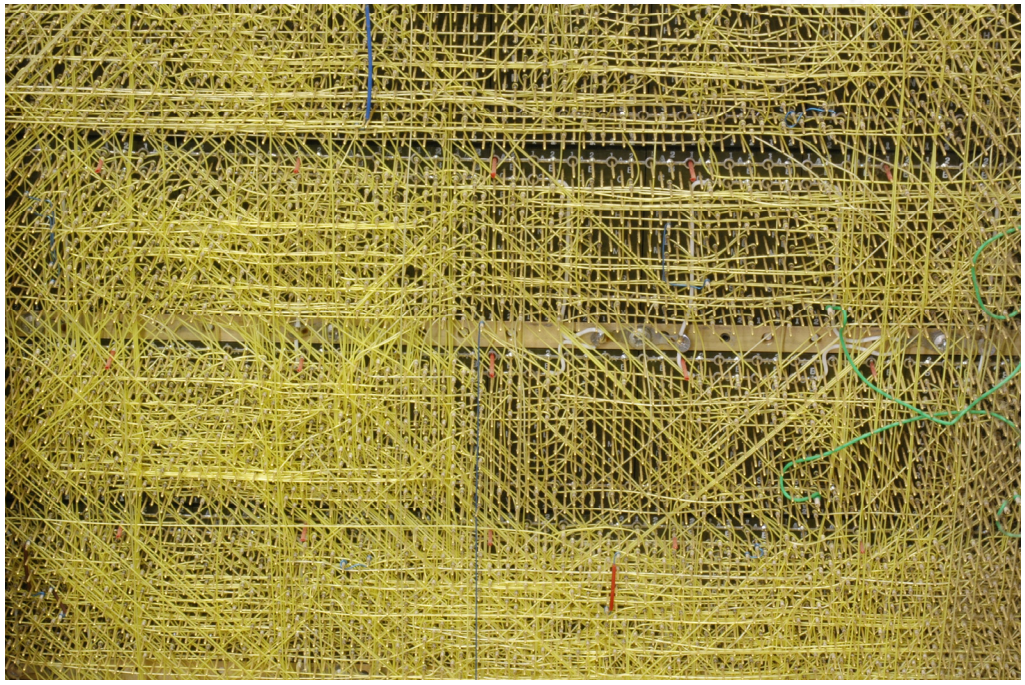
View of the same simple SRAM cell in 90nm, 65nm and 45nm process node



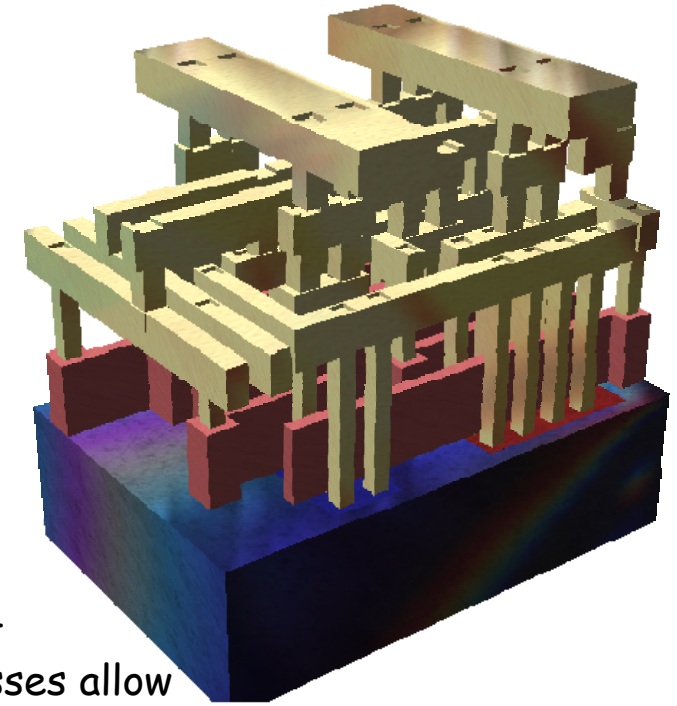
90nm – tall
1.0 μm²

65nm – wide
0.57 μm²

45nm – wide
w/ patterning enhancement 0.346 μm²



Interconnectivity is THE ISSUE!!!
Backplane of PDP-8I machine wire-wrapped



recent processes allow up to 10 interconnection metal layers

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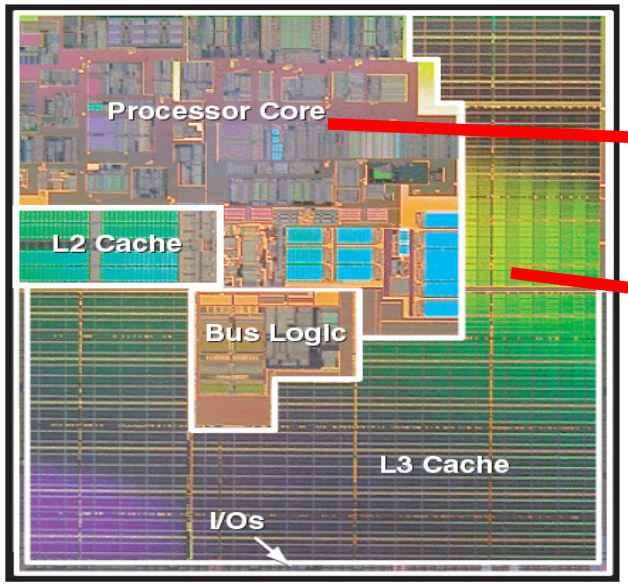
Why 3D-IC?

Die Photograph of the Itanium 2 MPU
(~2/3 of Area is Cache Memory)



Source: Intel

BEFORE

Intel Photo used as proxy

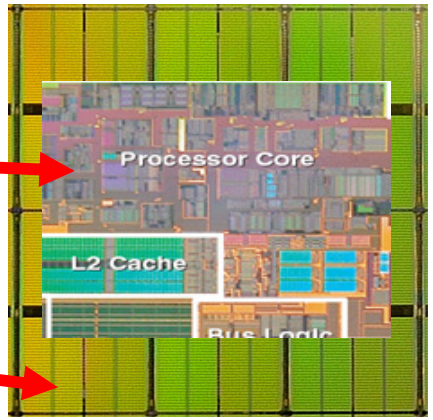
Only memory directly compatible with logic process (virtually no choice!)

maps to logic only die

maps to memory die array

AFTER: 3D IC

rendering of 3D IC



14× increase in memory density
4× Logic Cost Reduction
29× → 100× memory cost reduction (choice!)

Single Die~ 430 mm^2 2D IC "All or Nothing"
Wafer Cost ~ $6,000
Low yield ~ 15%, ~ 10 parts per wafer
memory costs ~ $44/MB

128MB not 9MB
memory costs ~ $1.50/MB → $0.44/MB

Operation	Energy
32-bit ALU operation	5 pJ
32-bit register read	10 pJ
Read 32 bits from 8K RAM	50 pJ
Move 32 bits across 10mm chip	100 pJ
Move 32 bits off chip	1300 to 1900 pJ

Calculations using a 130nm process operating at a core voltage of 1.2V
(Source: Bill Dally, Stanford)

From Bob Patti Tezzaron

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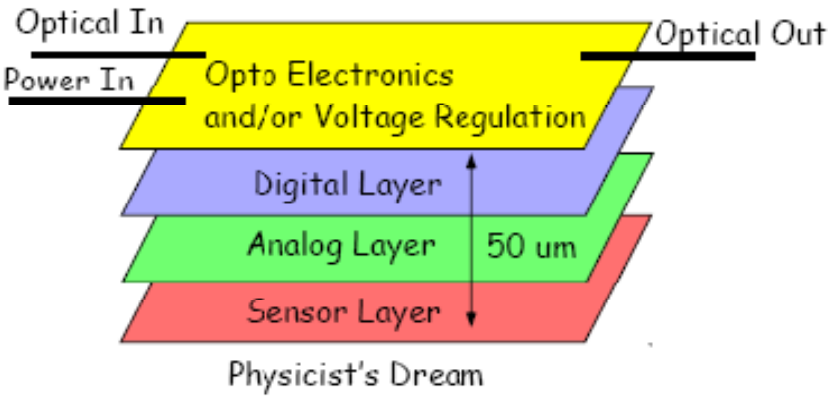
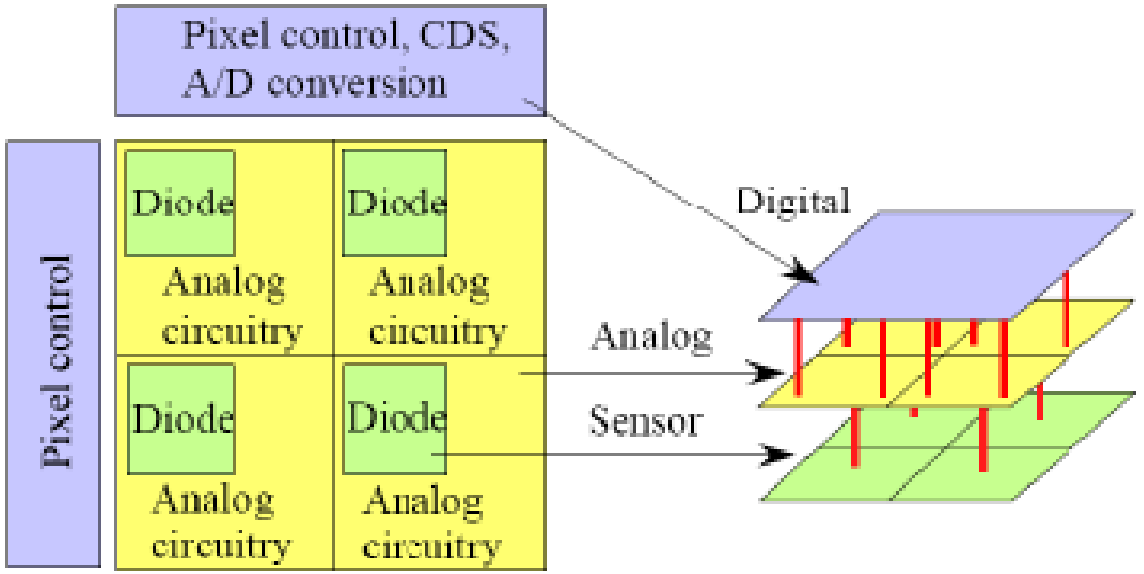
Why 3D-IC?

improvements to achieve using 3D-IC :

- reduced interconnect delays (R, L, C), higher clock rates,
- reduced interconnect capacitance (I/O pads), lower power dissipation,
- higher integration density, may go heterogeneous
- high bandwidth μ-processors
- merging different process technologies, mixed materials, system integration,
- advanced focal planes



Optimal repartition of functions



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

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Why 3D-IC?

Real estate analogy

How much time, effort and energy (gas) is needed to communicate with your neigbors in 2D assembly?

2D

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Key components of 3D-IC technology

3D-IC definition

A chip in three-dimensional integrated circuit (3D-IC) technology is composed of two or more layers of active electronic components, integrated both vertically and horizontally

3D-IC methods

Agressive wafer thinning, through wafer/chip connectivity, back-side metalization and patterning, oxide or metal bonding (W-W, C-W, C-C)

Fermilab position in 3D-IC

Fermilab began exploring the technologies for 3D circuits in 2006.

Fermilab is leading an Int'l Consortium (15 members) on 3D-IC for scientific applications, mainly HEP

http://3dic.fnal.gov

Importance of 3D-IC in detectors

Not only more 'transistors/μm^2', but 3D-IC methods lead to replacement of typical bump bonds and open new frontiers for detectors architectures

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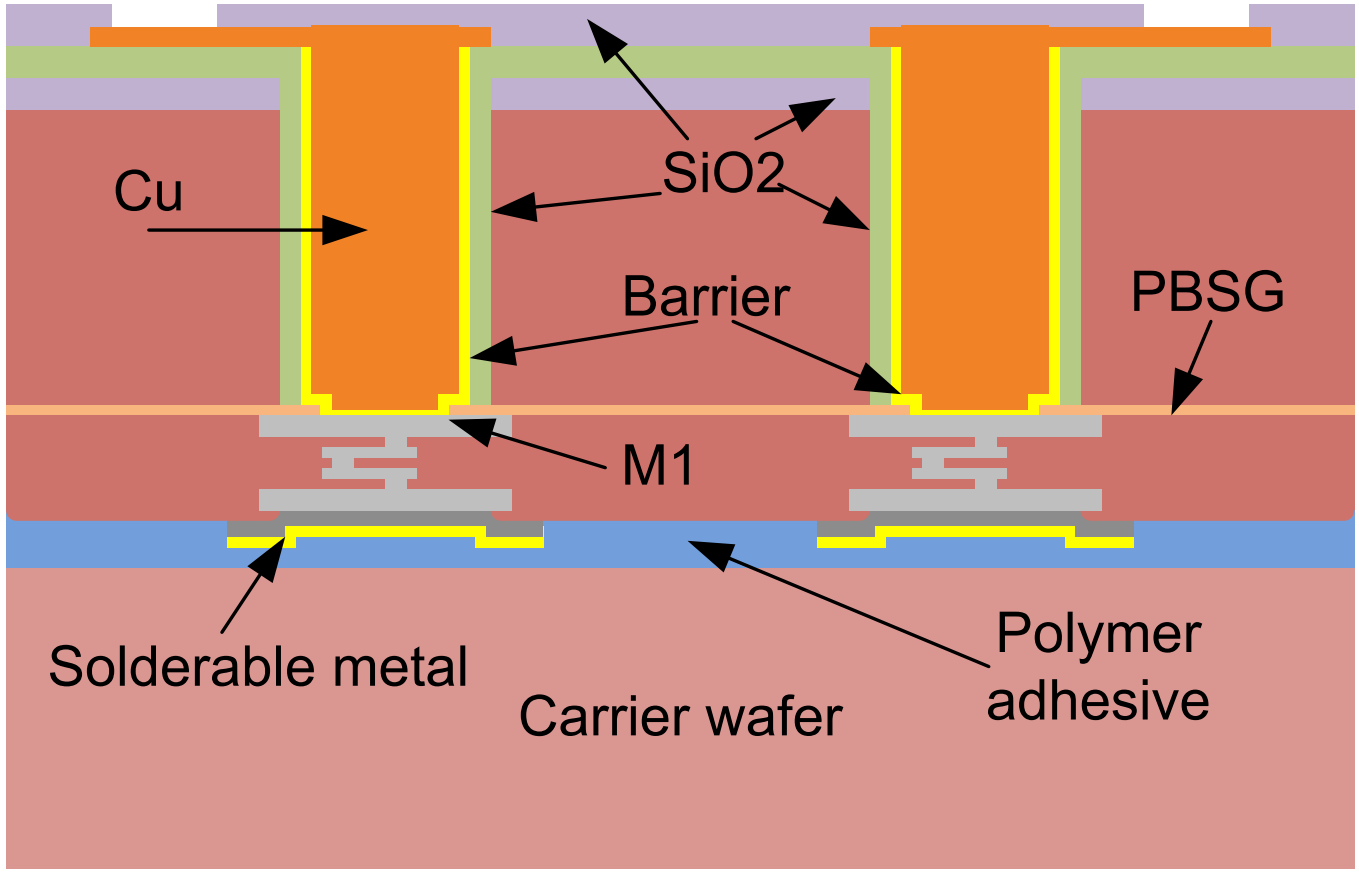
Key components of 3D-IC technology

THROUGH SILICON VIAS (TSV)



proxy picture

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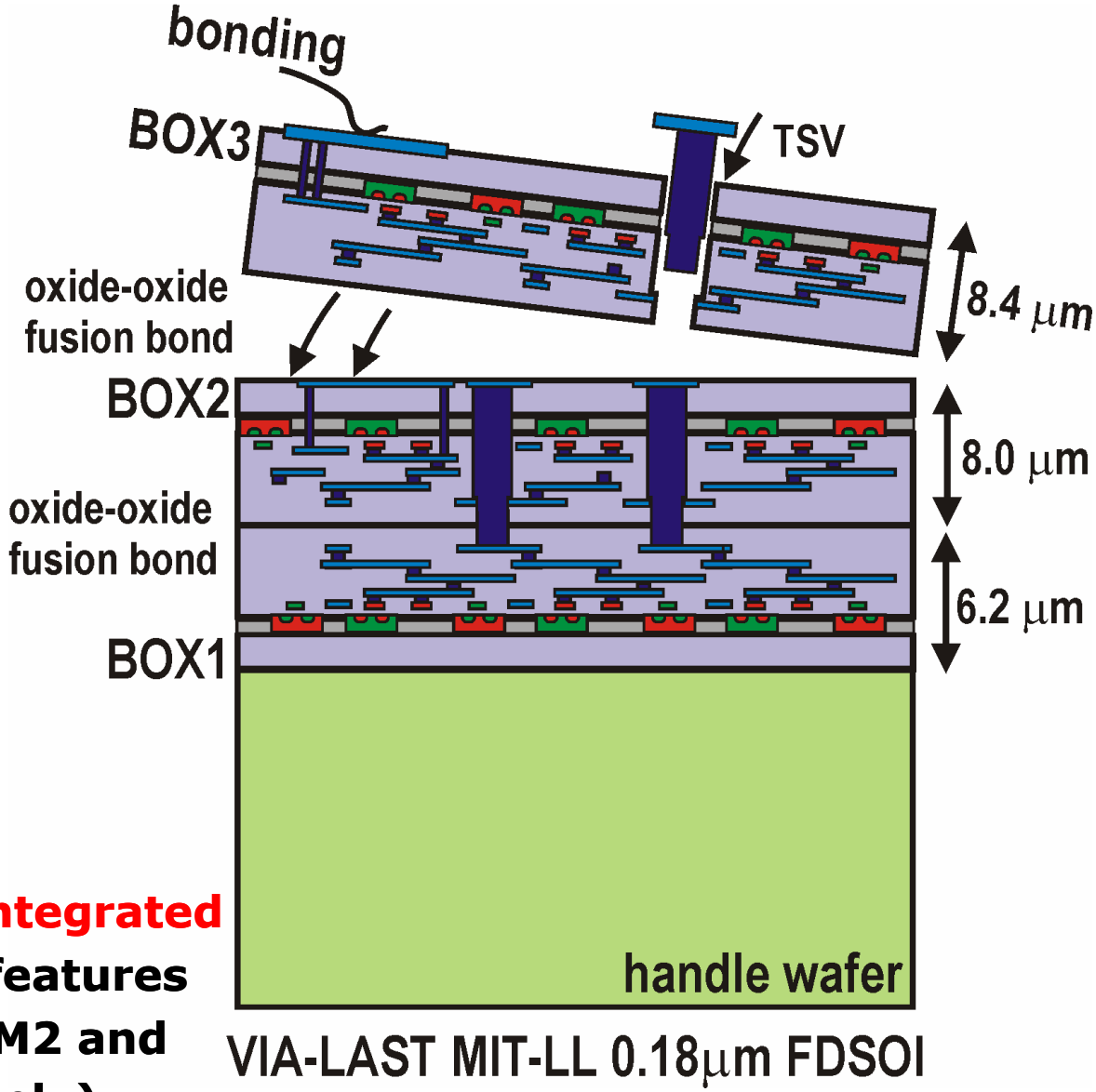
3D-IC at Fermilab

Via Last

Features:

- VIA-LAST process (*vias added to wafers after bonding and thinning*) – excludes large area for local interconnect in TSV locations
- Readily based on Silicon-on-Insulator process where presence of natural oxides acts as etch stoppers and bonding surfaces
- potential use of heteregenous wafers



VIA-LAST MIT-LL 0.18μm FDSOI

Submissions:

Two generations of Vertically Integrated Pixel (VIP) readout chips with features for ILC detector vertex (run 3DM2 and 3DM3, 2006 and 2008 respectively)

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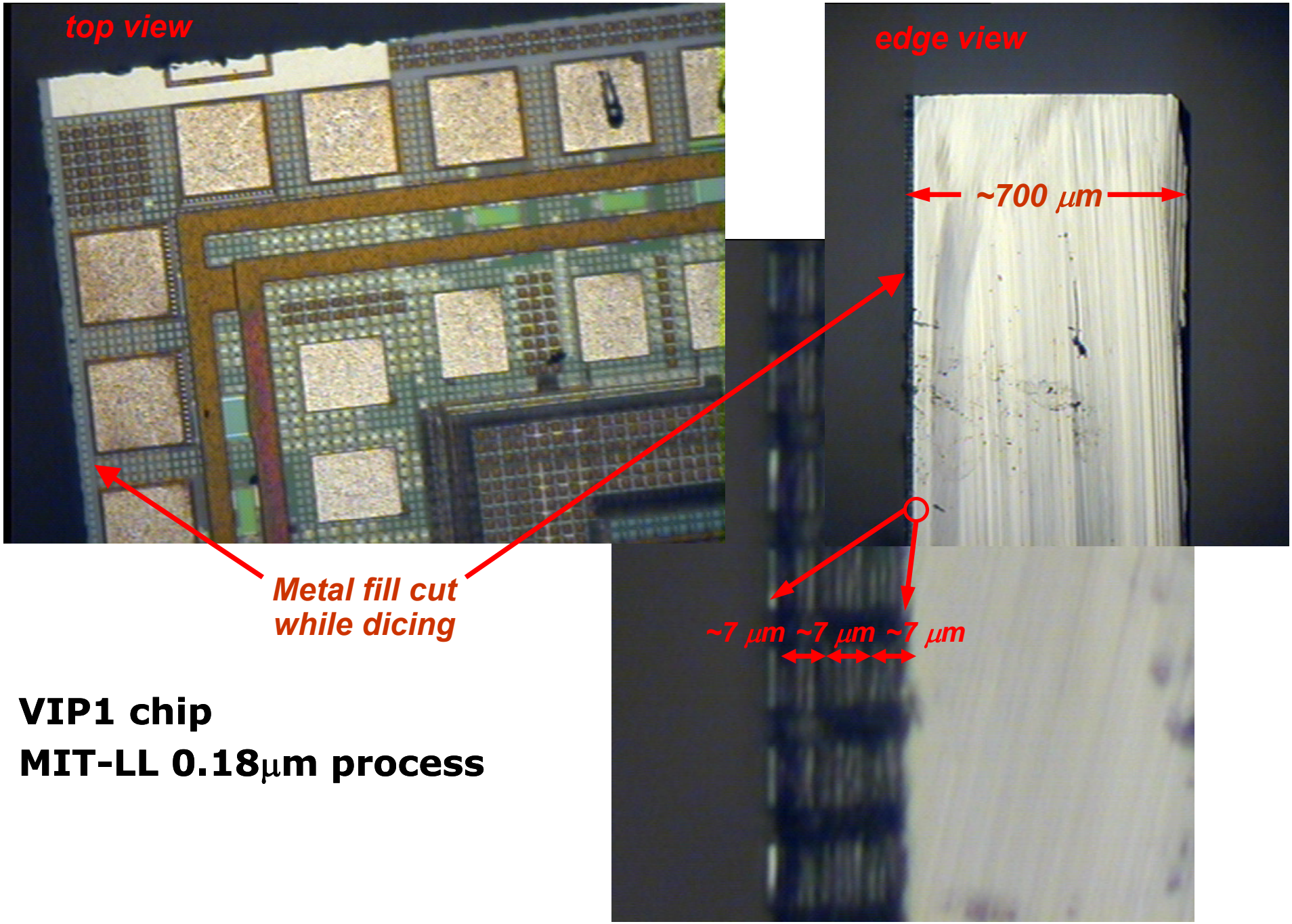
3D-IC at Fermilab



VIP1 chip

MIT-LL 0.18μm process

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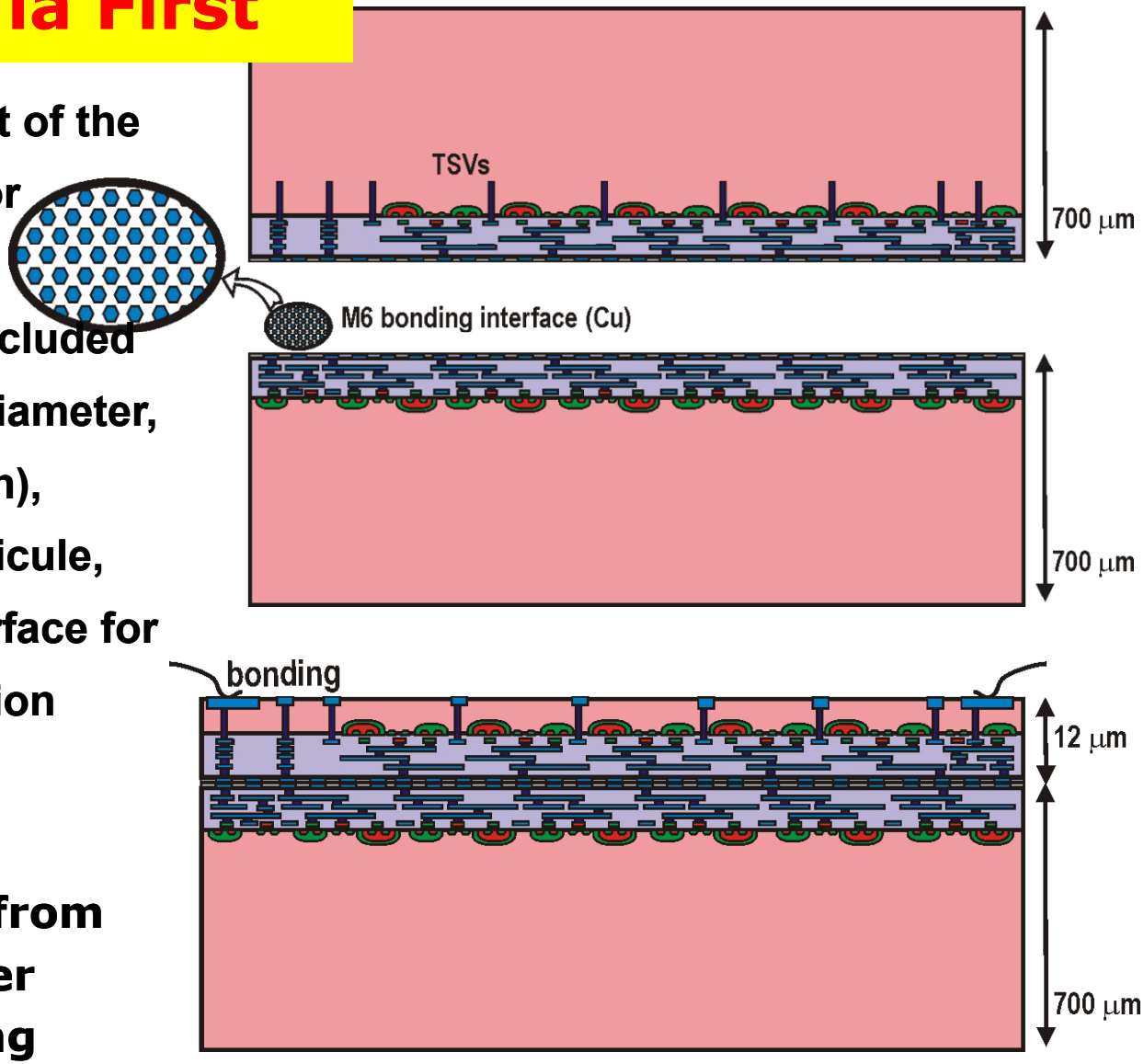
3D-IC at Fermilab

Via First

Features:

- VIA-FIRST process (vias are part of the wafer processing inserted before or right after forming transistors) – metal interconnect lines are not excluded over TSV locations (TSVs 1.3 μm diameter, 3.8 μm rec. spacing and 6 μm depth),
- 8" wafers, large ~26×31 mm^2 reticule,
- W 6th metal used as a bond interface for face-face Cu-Cu thermo-compression bonding



Submissions:

3 fully functional prototypes from Fermilab together with 9 other subreticules from participating institutions submitted on a Fermi MPW run in 2009; currently 'in fab'

0.13 μm bulk CMOS by Chartered with Tezzaron 3D via-first technology

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3D-IC at Fermilab

- Access to the first commercially available 3D-IC process through Tezzaron excited creation of a consortium centered on Fermilab in late 2008. The consortium groups international laboratories and universities with interest in High Energy Physics for the development of 3D integrated circuits.

Consortium presently comprised of 15 members from 5 countries

- University at Bergamo
- University at Pavia
- University at Perugia
- INFN Bologna
- INFN at Pisa
- INFN at Rome
- CPPM, Marseilles
- IPHC, Strasbourg
- IRFU Saclay
- LAL, Orsay
- LPNHE, Paris
- CMP, Grenoble
- University of Bonn
- AGH University of Science &Technology, Poland
- Fermilab, Batavia

- Others contributing to first MPW
  - BNL, Brookhaven
  - LBNL, Berkeley

http://3dic.fnal.gov

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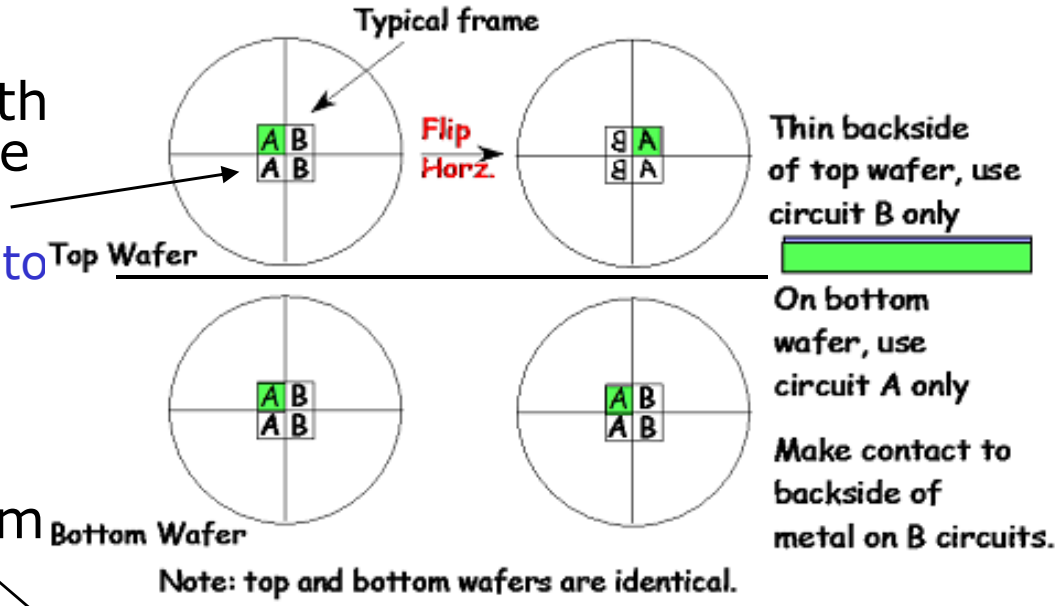
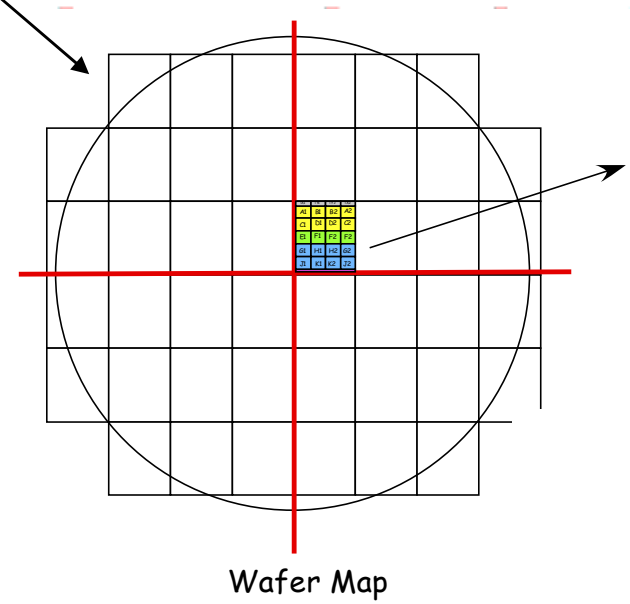
3D-IC at Fermilab

- 3D chip has two tiers
- One set of masks used for both top and bottom tiers to reduce mask cost.
  - Identical wafers bonded face to face by Tezzaron.
  - Backside metallization by Tezzaron.
- Frame divided into 12 subreticules among consortium members
- More than 25 two-tier designs (circuits and test devices)
  - CMS strips, ATLAS pixels
  - ILC pixels
  - B factory pixels
  - X-ray imaging
  - Test circuits
    - Radiation
    - Cryogenic operation
    - Via and bonding reliability
    - SEU tolerance





TXL	TYL	TYR	TXR
AL	BL	BR	AR
CL	DL	DR	CR
EL	FL	FR	ER
GL	HL	HR	GR
IL	JL	JR	IR

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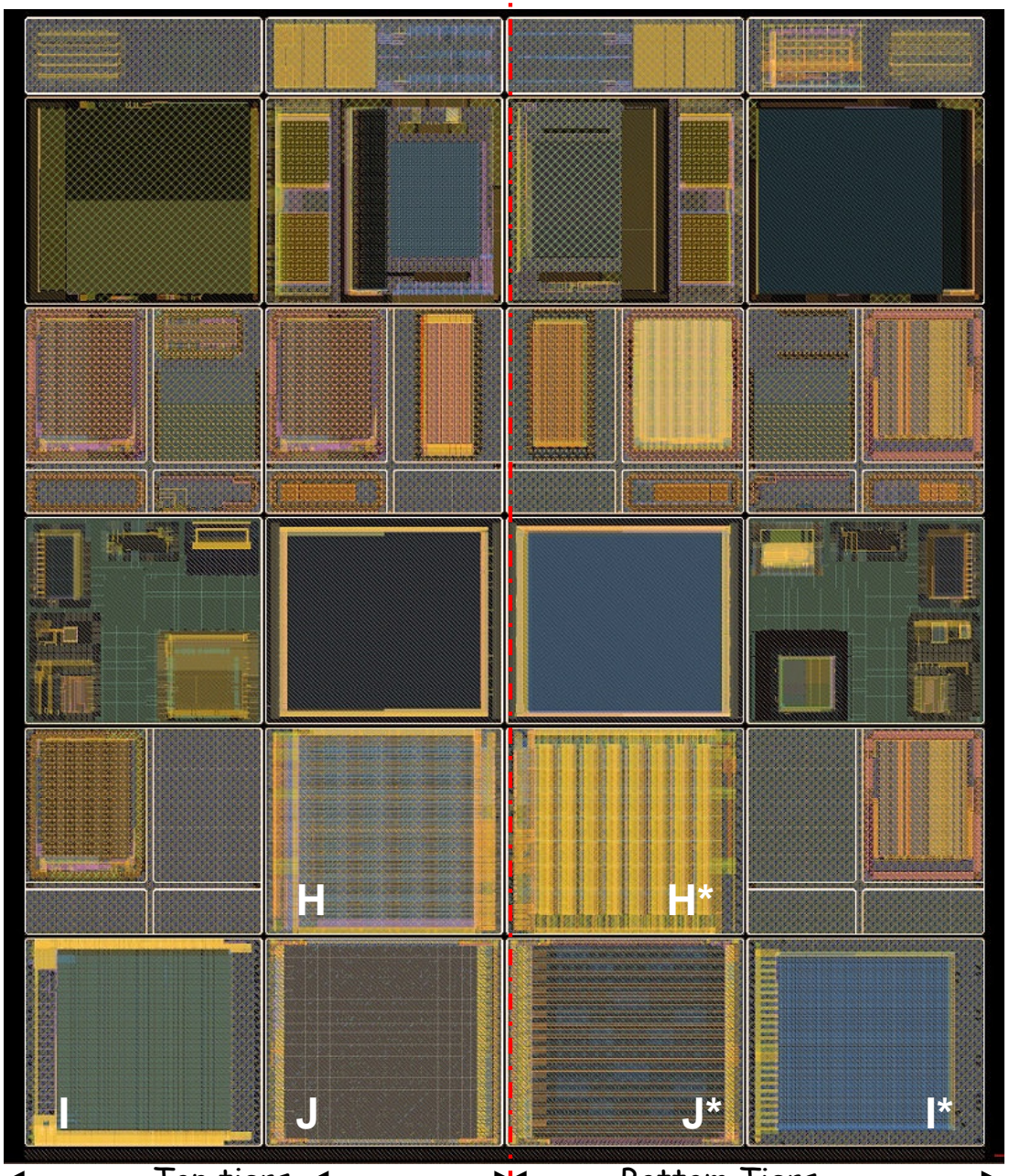
3D-IC at Fermilab

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D, E,
F, G, H, I, J
5.5 x 6.3 mm

Full frame
0.13 μm
Chartered



– **frame organization:**

- Top and bottom tiers fabricated on the same frame; vertical symmetry about the center of the frame for flipping one wafer over another and obtaining matching of circuits in 3D assembly,
- All designs initially submitted by mid-May 2009

– **Fermilab designs**

- **H** = VICTR; short pixel readout chips realizing pt cut for implementation of L1 trigger embedded in tracker for CMS @ SLHC
- **I** = VIP2b; time stamping pixel readout chip for vertex detector @ ILC
- **J** = VIPIC; very high frame rate with sparsification pixel readout chip for X-ray Photon Correlation Spectroscopy @ light source

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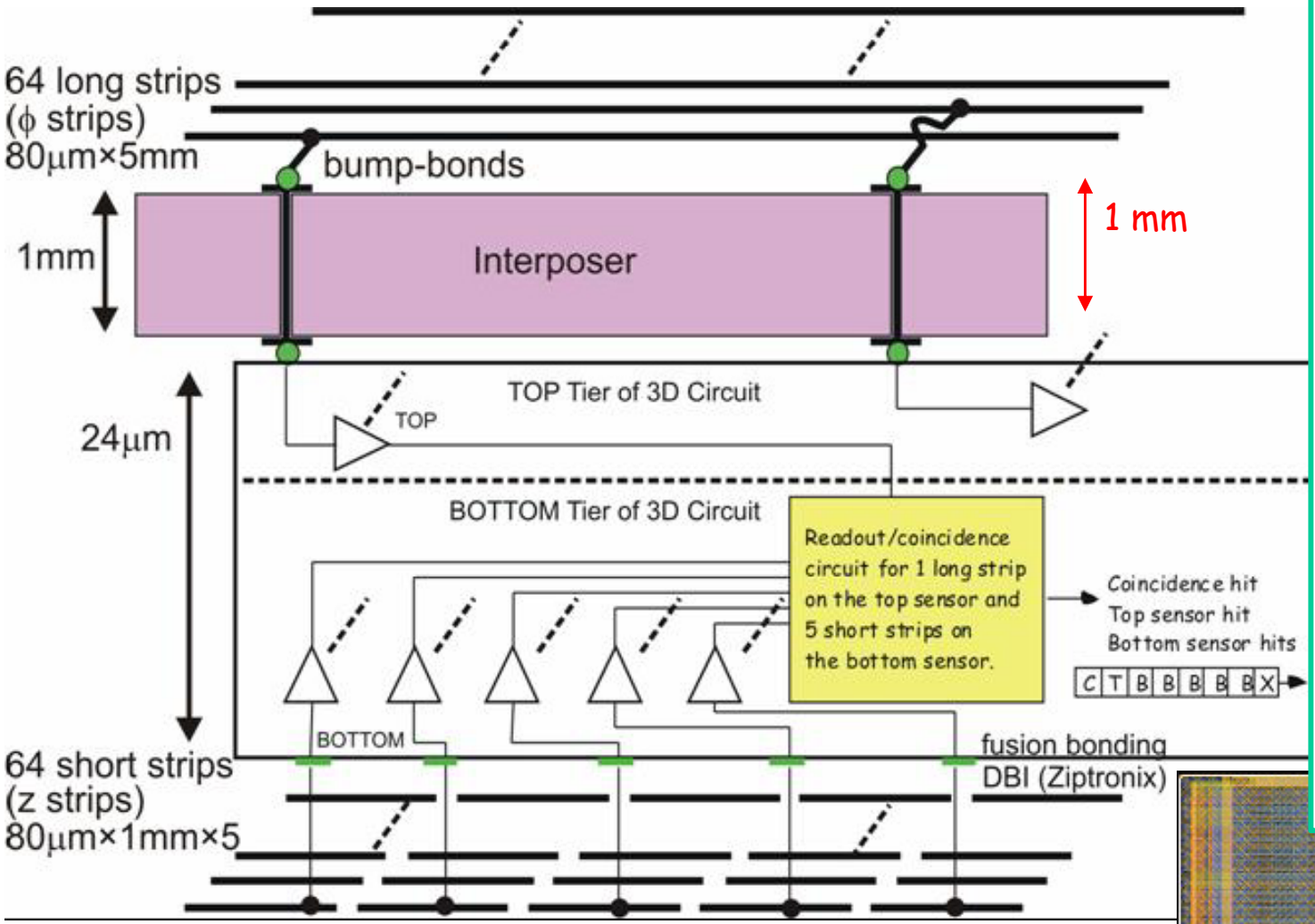
3D-IC at Fermilab

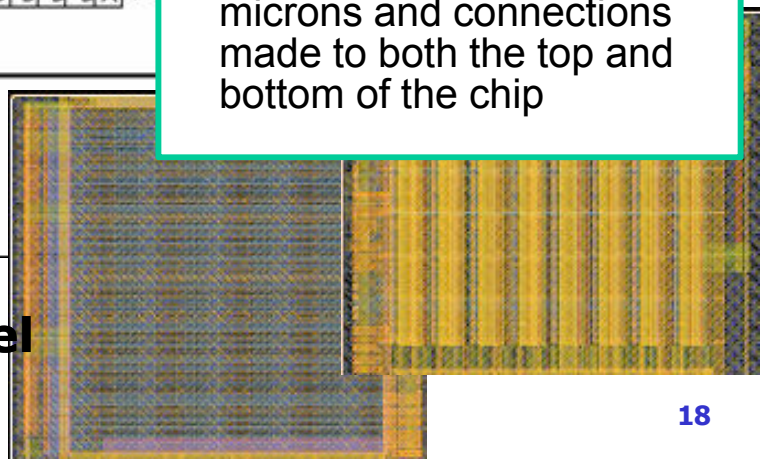
VICTR **FNAL/CPPM/LBNL**

Vertically Integrated CMS Tracker



– **How it works:**

- Design employing the FEI4 ATLAS pixel front-end
- Top tier looks for hits from long ϕ strips and bottom tier looks for coincidence between ϕ strips and shorter z strips connected to bottom tier.
- Designed for 80 μm pitch sensors
- Serial readout of all top and bottom strips along with coincidence information
- Downloadable hit patterns
- Fast OR outputs
- Circuit to be thinned to 24 microns and connections made to both the top and bottom of the chip



Processes signals from 2 closely spaced parallel silicon strip sensor planes (ϕ and Z planes).

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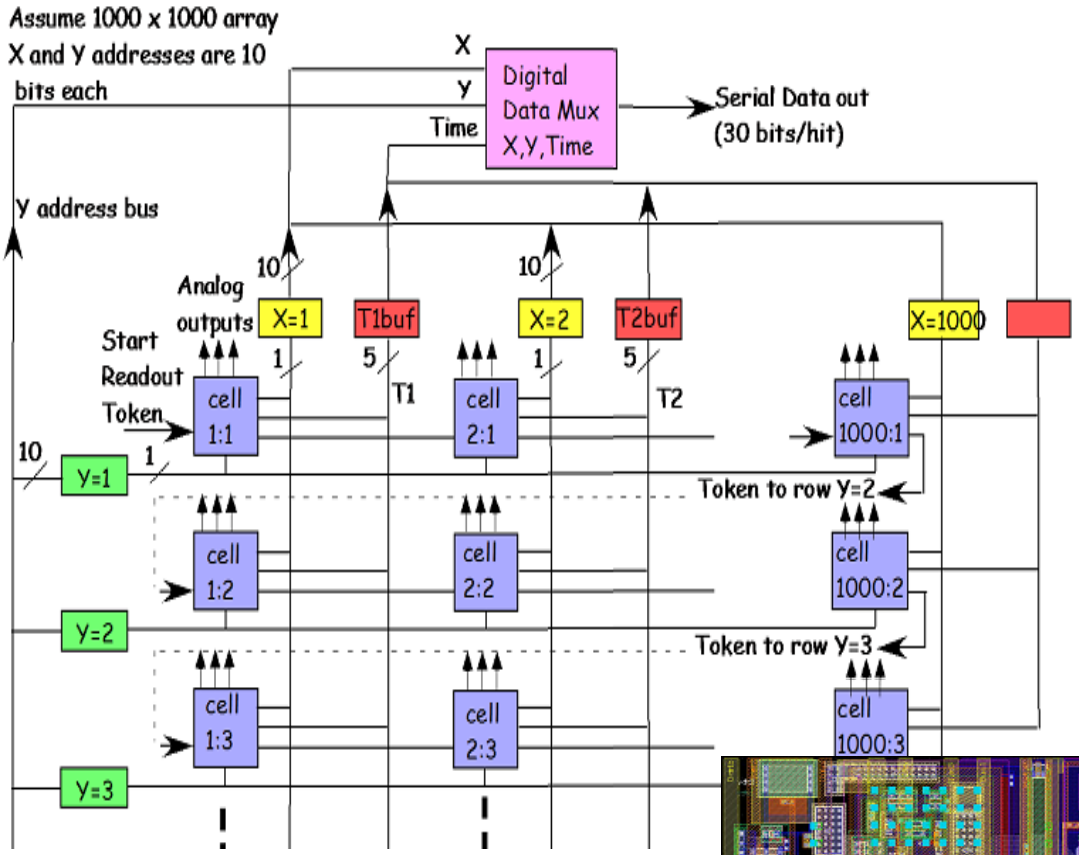
3D-IC at Fermilab
Vertically Integrated Pixel

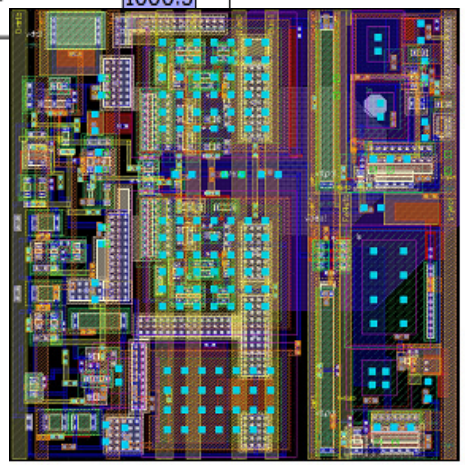
VIP2B

– **How it works:**

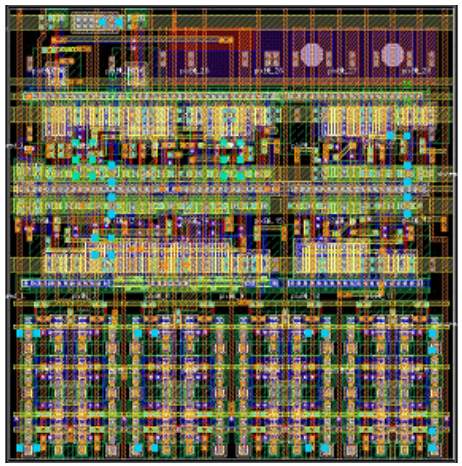
- Adapted from earlier MITLL designs in FDSOI technology
- 192 × 192 array of 24 μm^2 pixels
- 8 bit digital time stamp (Δt=3.9 μs)
- Readout between ILC bunch trains of sparsified data
- Sparsification based on token passing scheme
- Single stage signal integrating front-end with 2 S/H circuits for analog signal output with CDS
- Analog information available for improved resolution
- Separate test input for every pixel cell
- Serial output bus
- Polarity switch for collection of e^- or h^+



signals are accumulated and time stamped using global Grey code counter



Pixel Top Tier (analog)



Pixel Bottom tier (digital)

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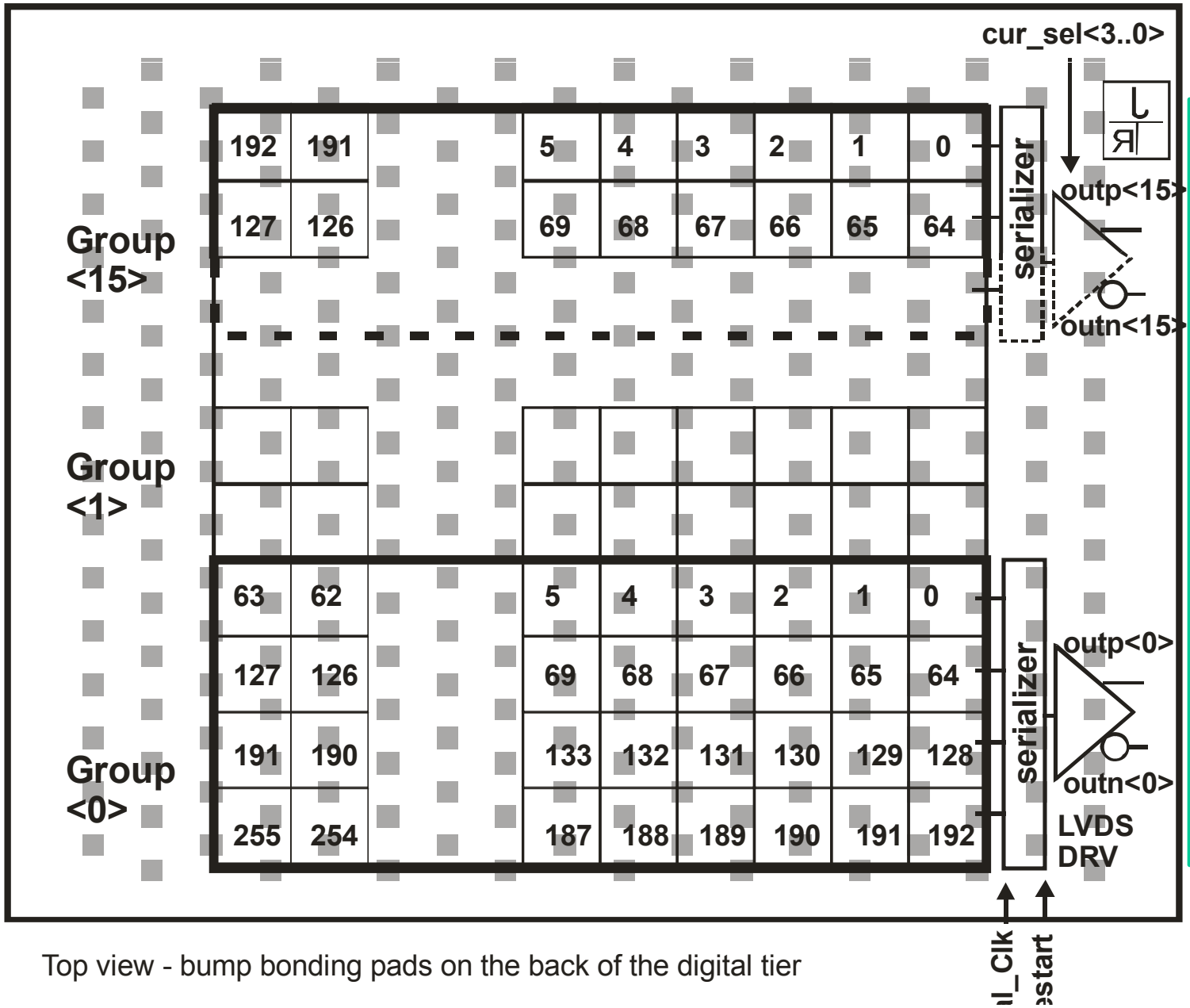
3D-IC at Fermilab

VIPIC

Vertically Integrated Photon Imaging Chip

Common effort of: FNAL/BNL and UST-AGH Poland



- **How it works:**
- X-ray Photon Correlation Spectroscopy (XPCS) is a technique that is used at X-ray light sources to generate speckle patterns for the study of the dynamics in various equilibrium and non-equilibrium processes
- The chip is divided in 16 group of 256 pixels read out in parallel but through separate LVDS serial ports
- Data sparsification is performed in each group

Top view - bump bonding pads on the back of the digital tier

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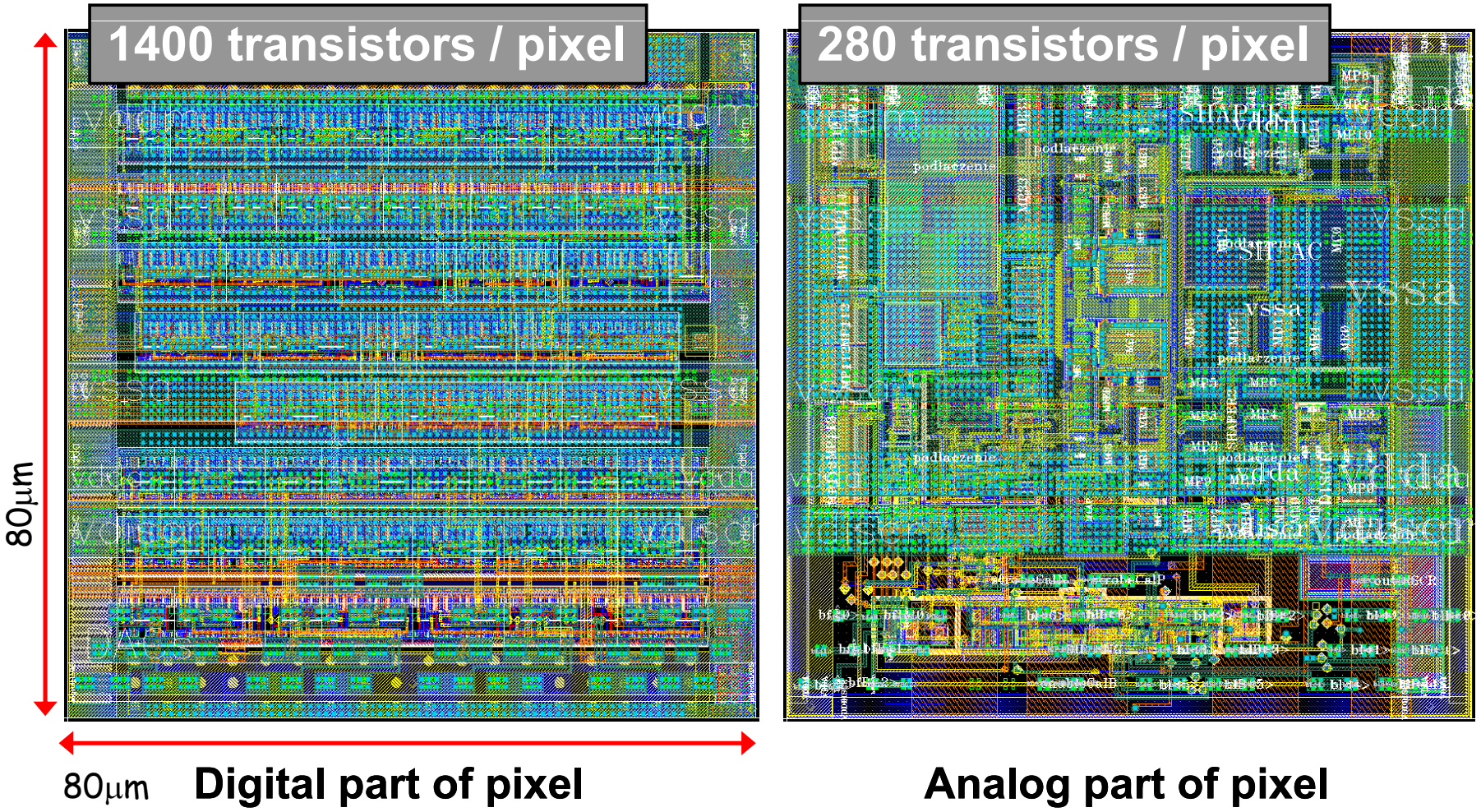
3D-IC at Fermilab

Full separation of analog and digital achieved by dividing functionalities between tiers



Power supplies transferred between tiers; 25 connections between tiers for signals in each pixel

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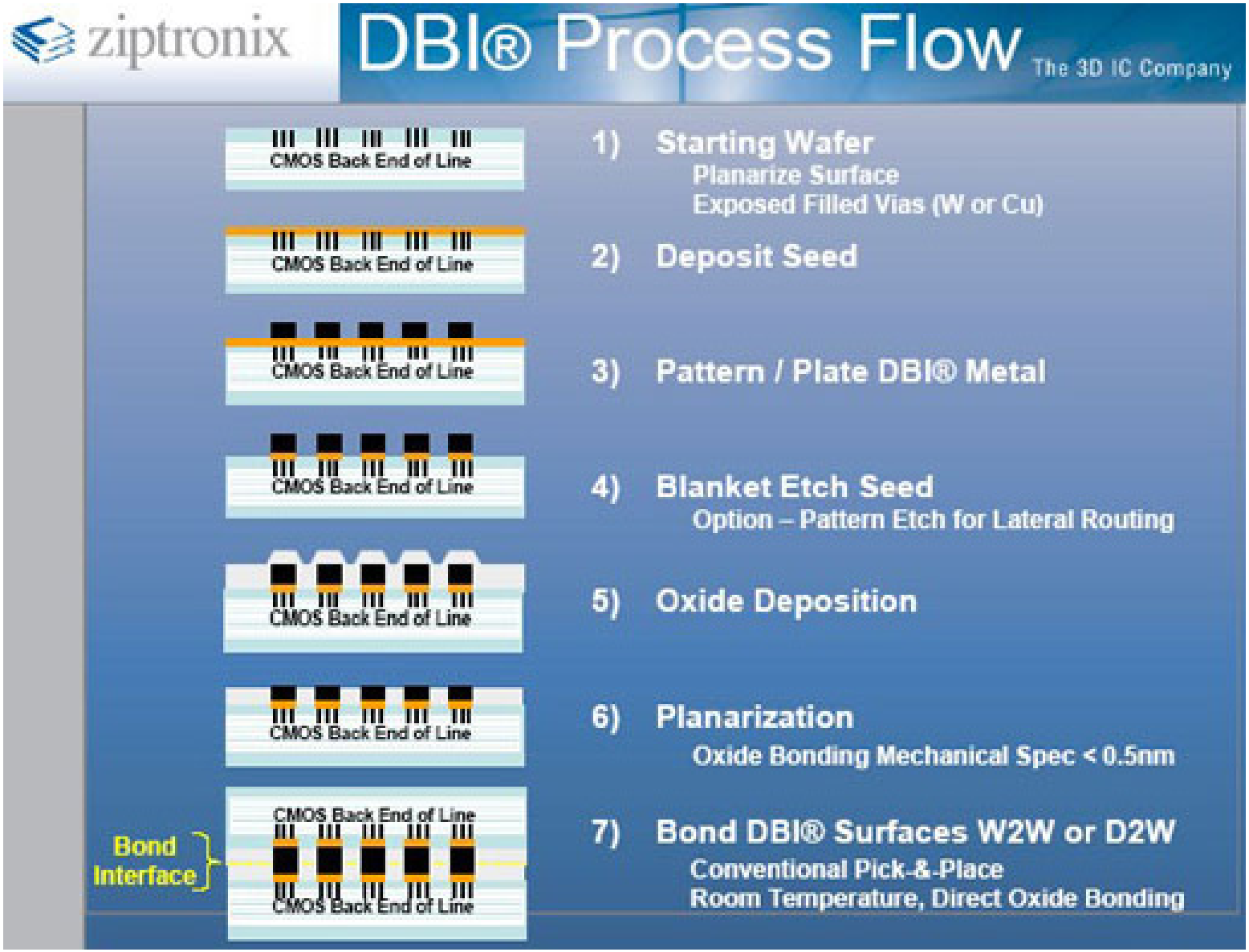

- detector/ROIC bonding; with Ziptronix low mass DBI bonding
- Conventional bumps or CuSn are expensive and not low mass fine pitch

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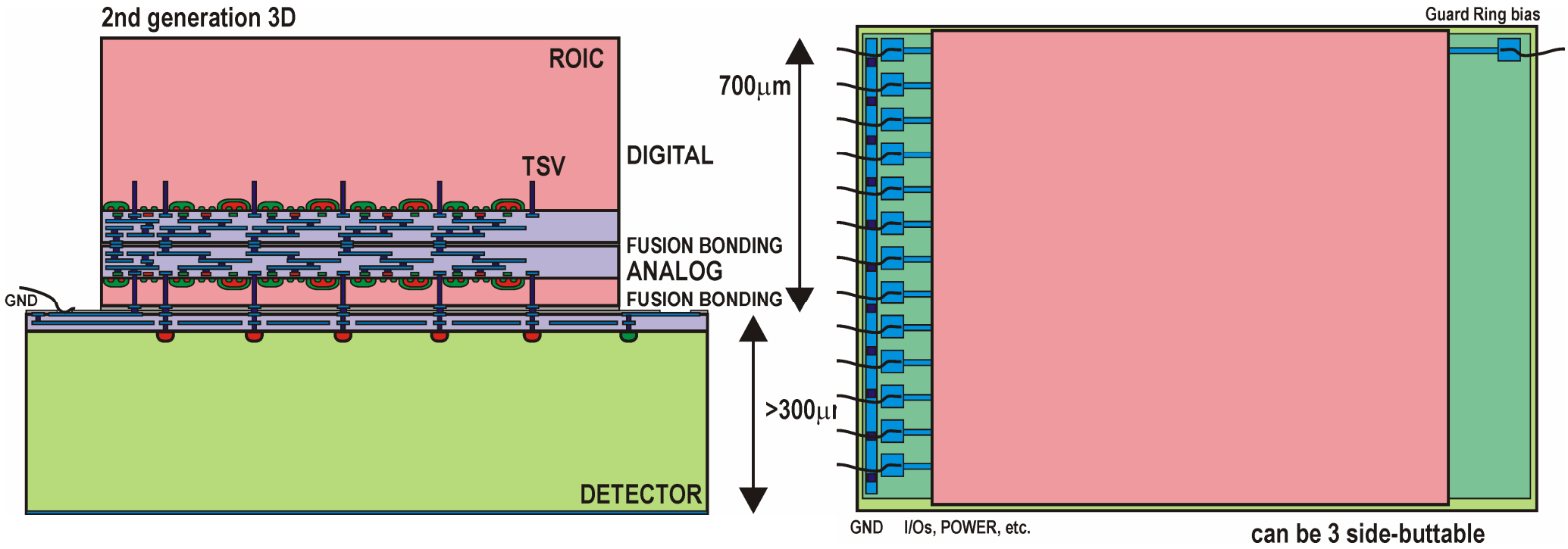
3D-IC at Fermilab

Less aggressive mounting option



- fanout/routing on the detector; pads created on the detector, wire bonding to the pads on the detector to mount in the system

DBI bonding with Ziptronix (a form of oxide bonding)

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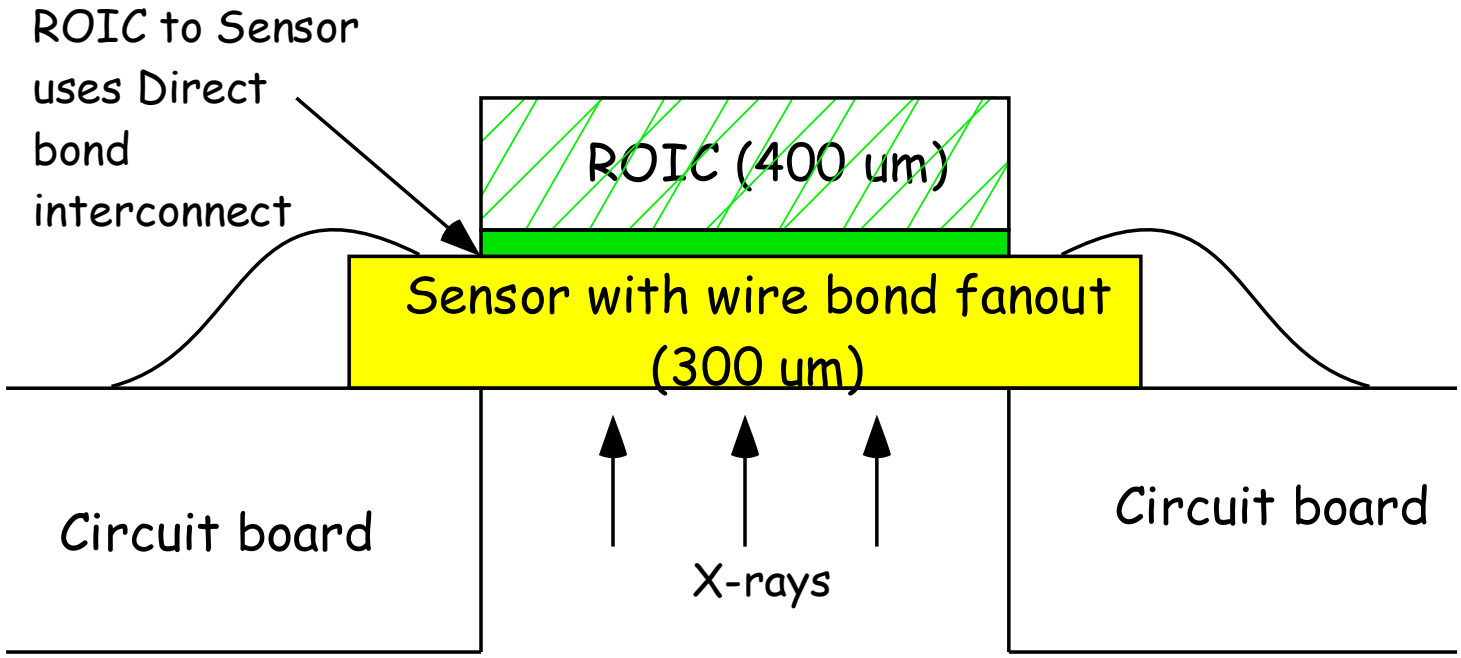

Option 1 - Less Aggressive Mounting

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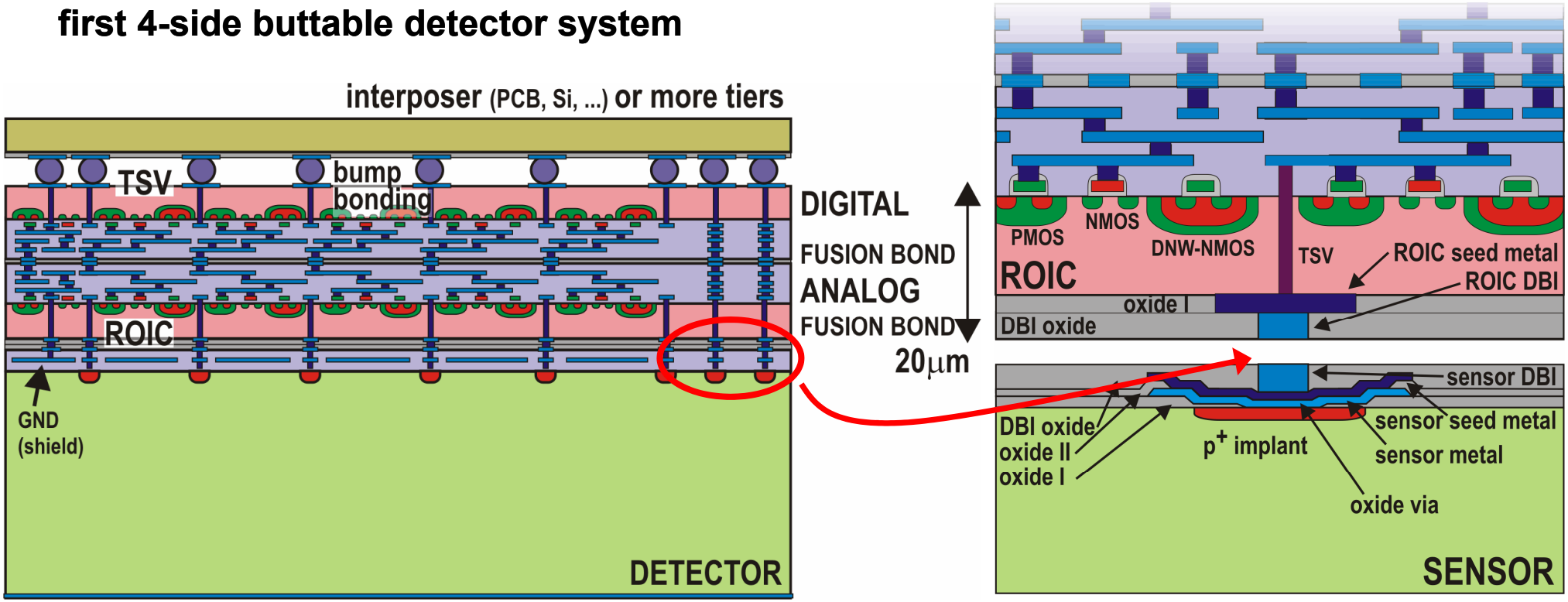
3D-IC at Fermilab

aggressive mounting option – essence of 3D-IC

Ultimate goal is:

first 4-side buttable detector system



- **low density array of I/O pads available on the side of the readout chip - opposite to the detector; one side of the readout chip connected to the detector using DBI or similar bonding technique, second side used to mount the device on the support PCB with bump or stud bonding technique**

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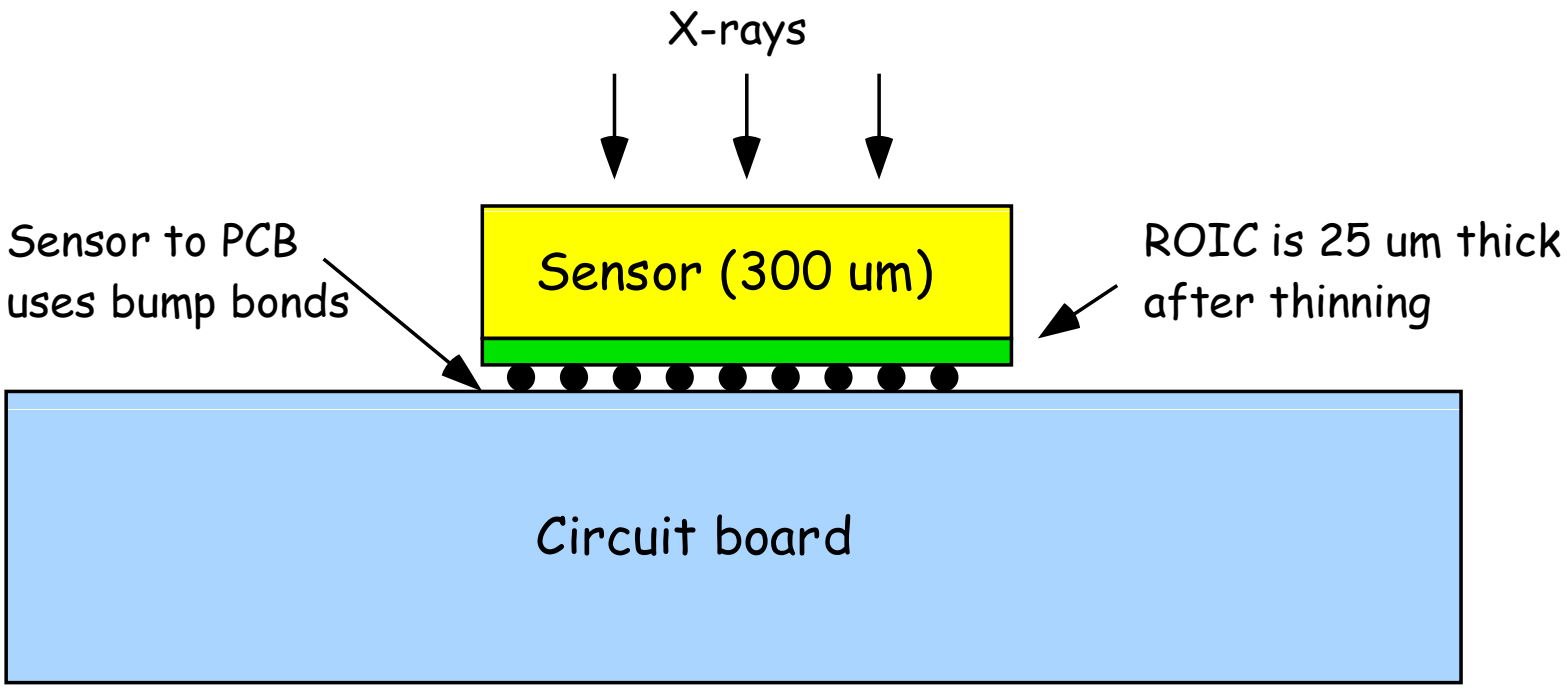
3D-IC at Fermilab



Option 2 - More Aggressive Mounting for four side buttable sensor arrays

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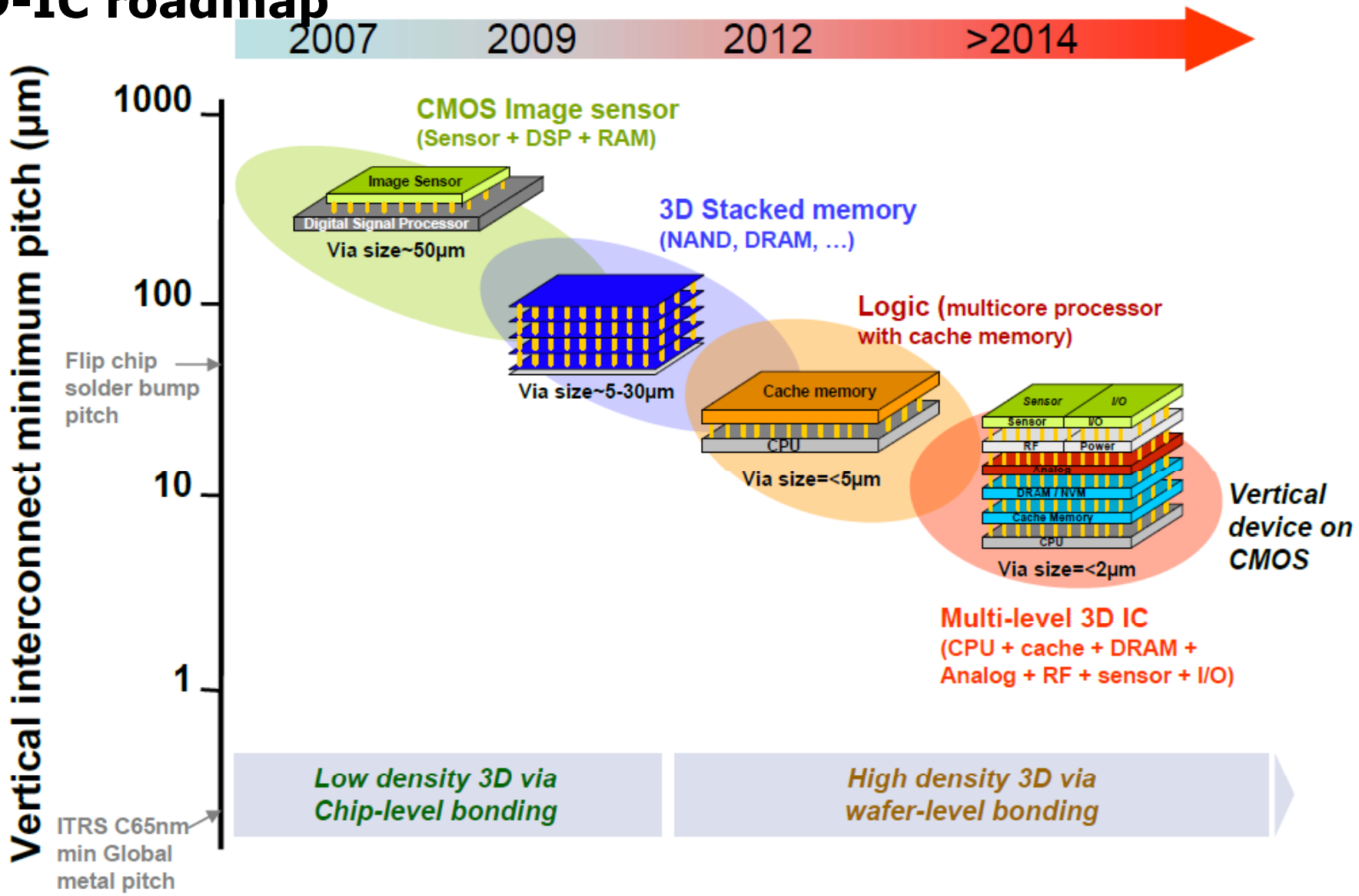
3D-IC roadmap



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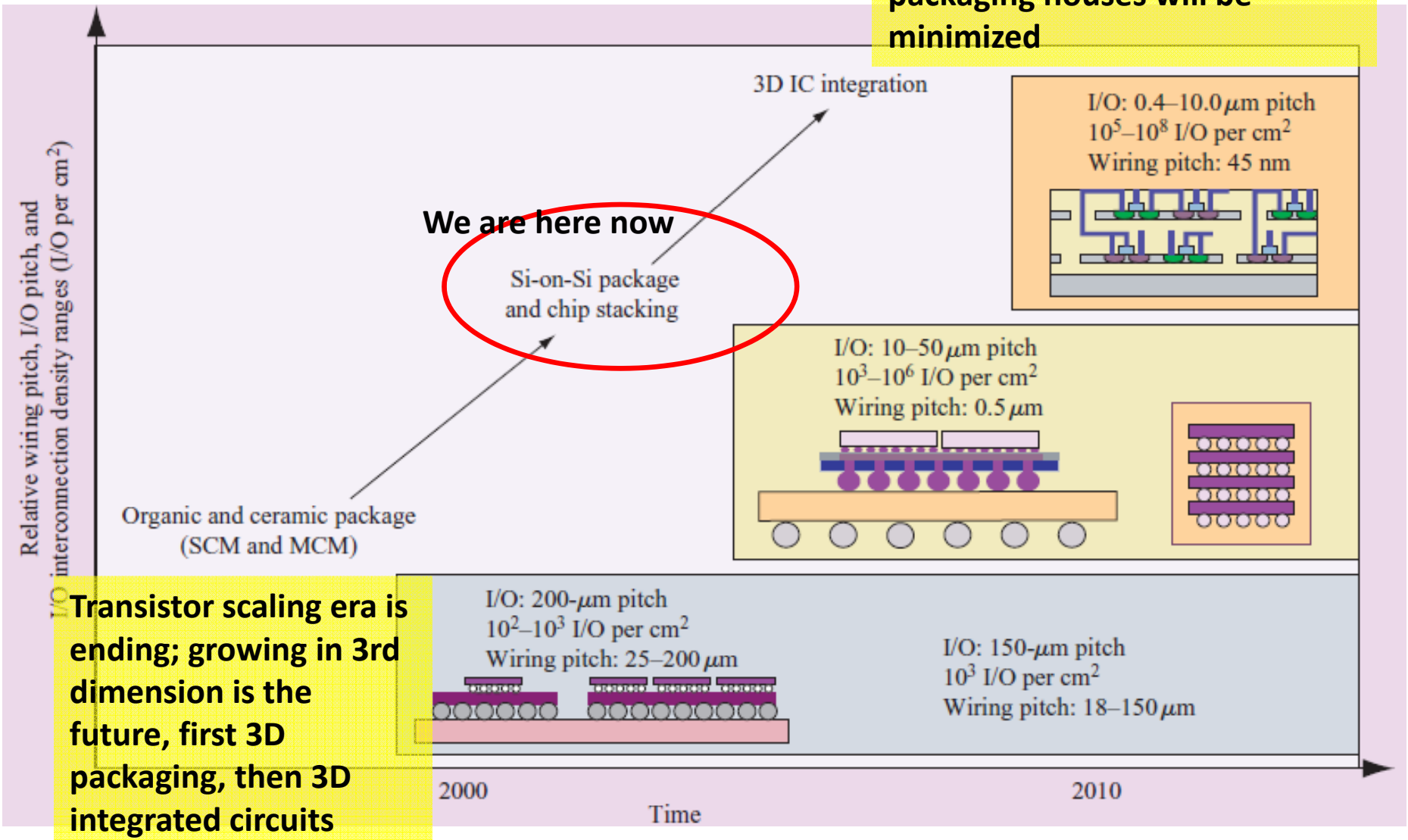
High-density I/O roadmap

3D-IC chips must be fabricated at wafger foundries, the role of packaging houses will be minimized



Transistor scaling era is ending; growing in 3rd dimension is the future, first 3D packaging, then 3D integrated circuits

Source: Knickerbocker,IBM Journal of Research and Development. Vol. 52 No. 6 2008

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Summary

3D-IC offers new approaches to old problems in detector development. New high density circuit bonding techniques, wafer thinning, and sub-μm size TSVs provide new opportunities for the detector designer.

Fermilab has been working with two different vendors for 3D chip fabrication. MIT LL is a via last SOI process using oxide wafer bonding. Tezzaron is a via first CMOS process using Cu-Cu wafer bonding.

Recently a new (third) 3D-IC technique has been explored with a new pixel chip submission to the OKI-SOI run within the SOIPIX collaboration that is based in KEK, Japan. The new bonding is based on ZyCube.

Chips are still in fab, except the first device, VIP1, that was fabricated in 2007; The prototype was tested and despite poor yield actual functionality was demonstrated

The 3D-IC seems to be the avenue for future development in μelectronics industry we hope to be able to maintain our R&D program

Packaging industry is under revolution because of the transistor scaling era is ending and 3D-IC era with TSVs is beginning.

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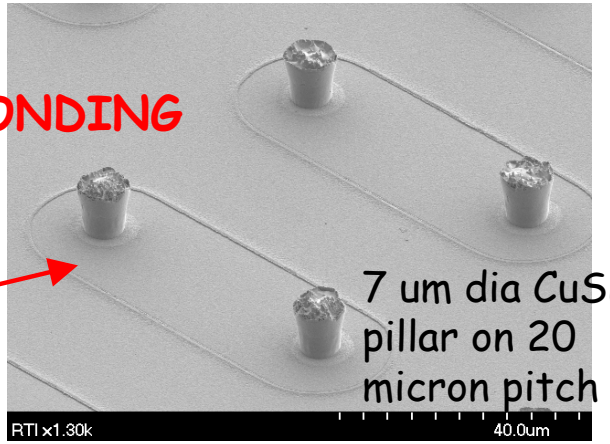
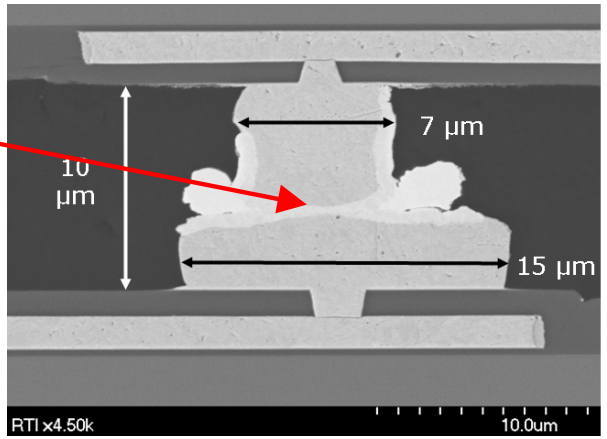
Backup1:

- 3D bonding technology to replace bump bonds in hybrid pixel assemblies.
- Bonding options being explored by Fermilab:
  - CuSn eutectic with RTI
  - Direct bond interconnect (DBI) using "magic metal" with Ziptronix. 3um pitch possible
  - CuCu fusion with Tezzaron
- Excellent strength and yield obtained with 7 um CuSn pillar on a 20 micron pitch. However 10 um of CuSn covering 75% of bond area would represents Xo=0.075. Too high for some HEP applications.
- CuCu fusion and DBI offer the lowest mass bond required by many HEP experiments.

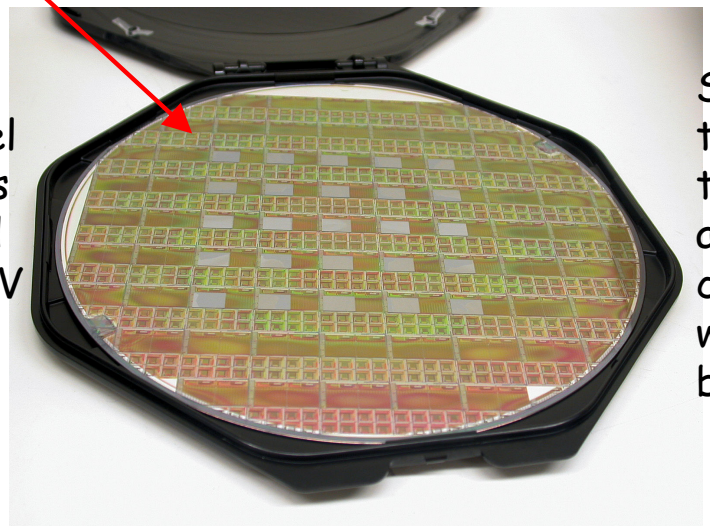
FUSION BONDING



7 um dia CuSn pillar on 20 micron pitch



CuSn bond cross section



25 Pixel sensors bonded to BTEV ROIC wafer

Sensors thinned to 100 um after chip to wafer bonding

Fermilab

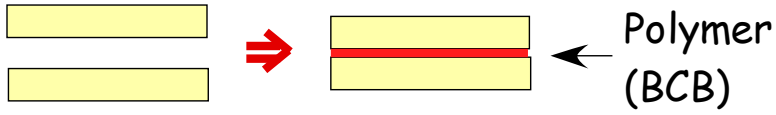
Backup2:

- Electrical and mechanical bonds

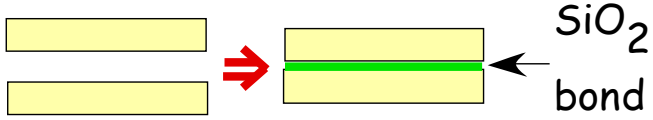
Fermilab experience

1) Bonding between Die/Wafers

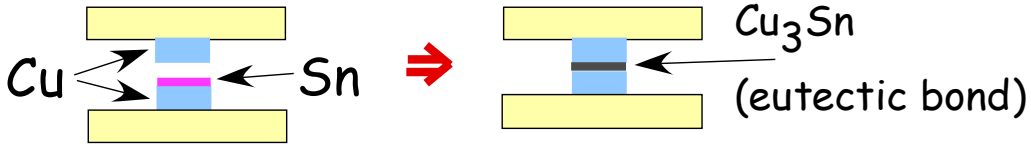
a) Adhesive bond



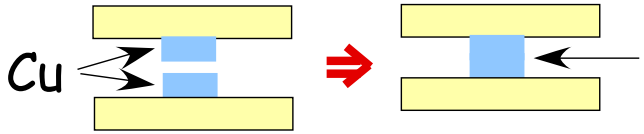
b) Oxide bond (SiO2 to SiO2) (MIT LL)



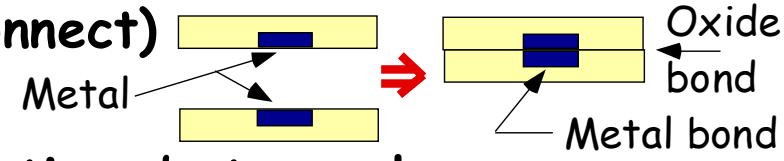
c) CuSn Eutectic (RTI)



d) Cu thermocompression (Tezzaron)



e) DBI (Direct Bond Interconnect) (Ziptronix)



For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

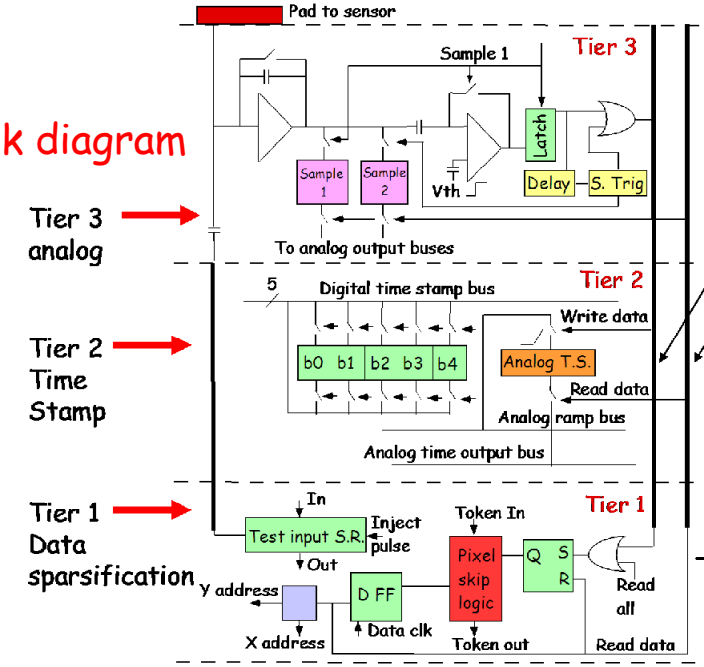
Fermilab

Backup3

VIP1 / VIP2a

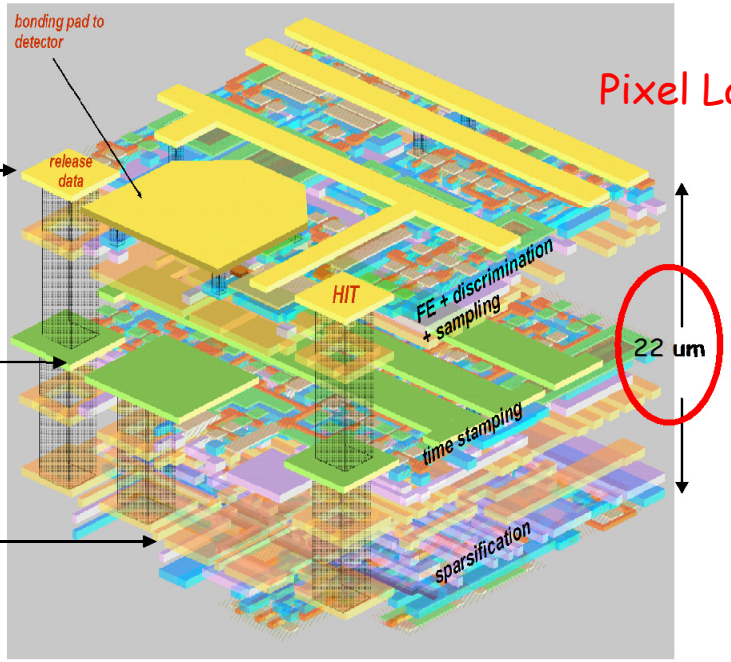
- VIP1 designed in 3 tier MIT-LL 0.18 μm SOI process
- no sensor

Pixel block diagram



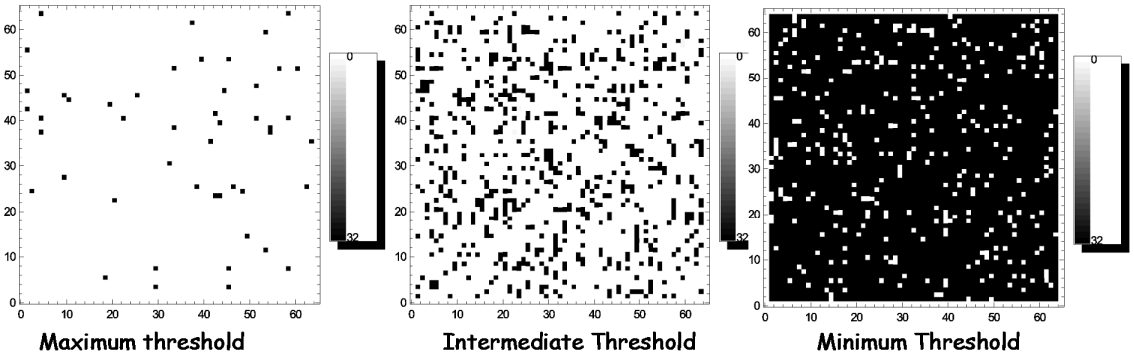
3D vias

Pixel Layout



Data readout out using data sparsification scheme.

VIP1 Test Result



VIP1 found to be functional.
Architecture proven but:
VIP1 Yield was low.
VIP2a designed to improve yield through: increased sizes of FD SoI transistors, improved power distribution, wider traces and redundant vias among other things at expense of larger, 30 um, pixel size
VIP2a is in fabrication
Focus has shifted from working in FD SOI to bulk CMOS processes