FPIX2: A Pixel Readout Chip with 840 Mb/s IO bandwidth

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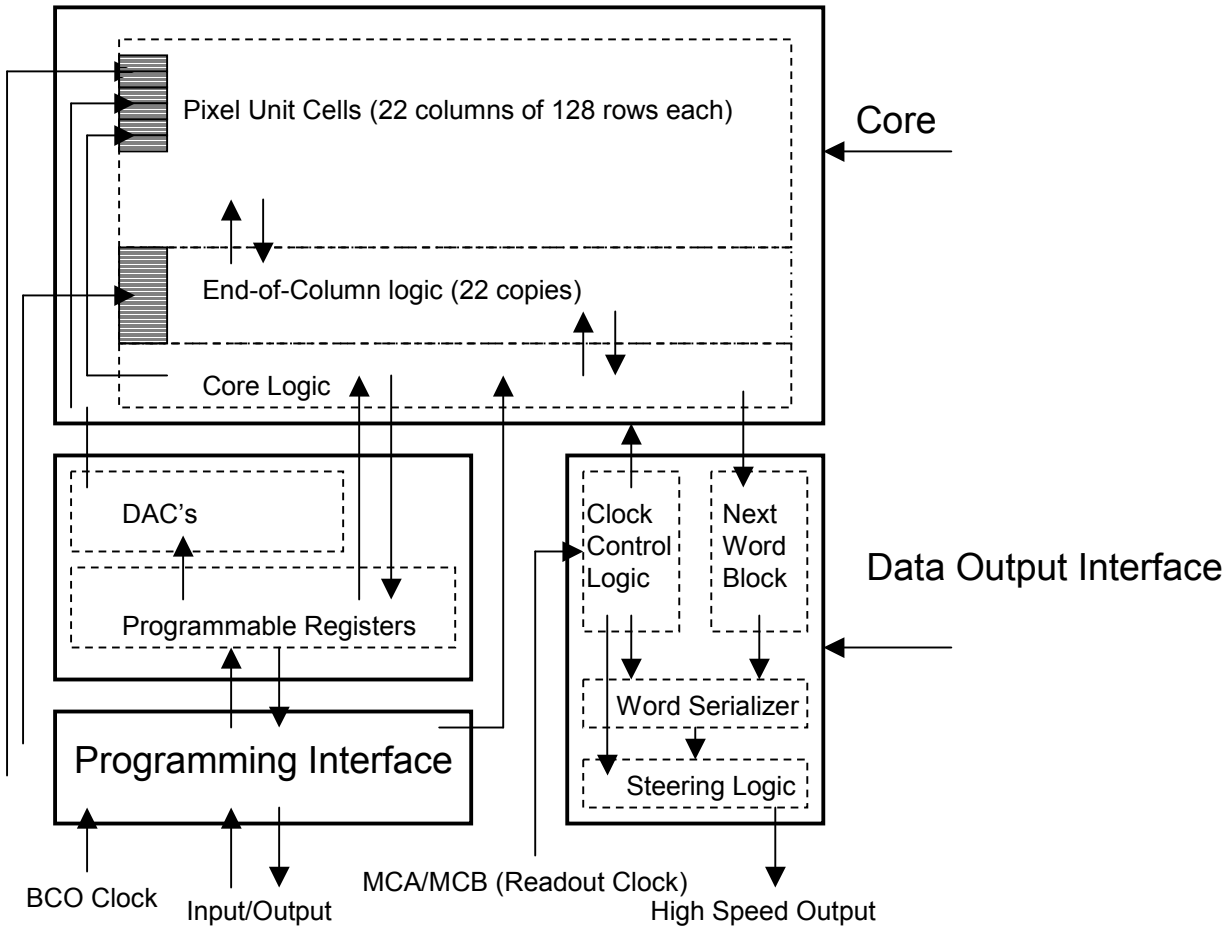
FPIX2 Overview

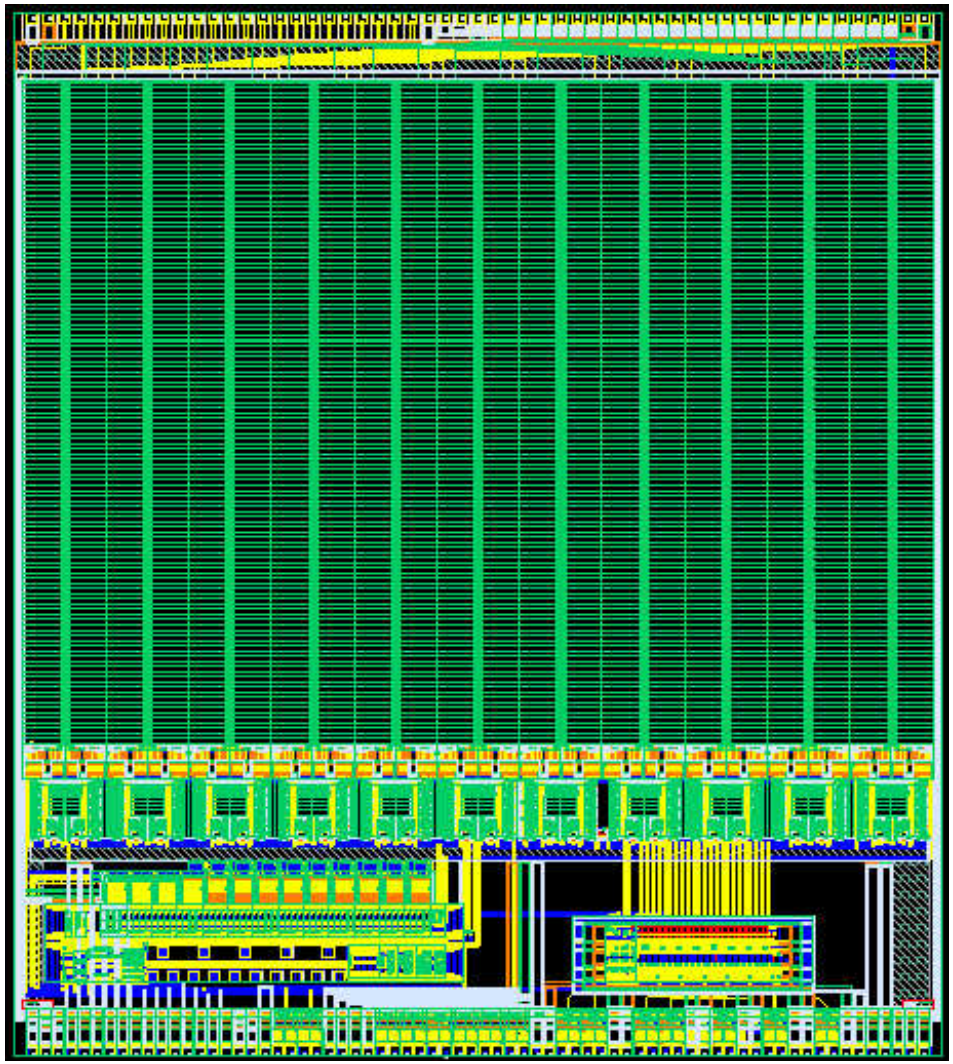
- 0.25µ CMOS, using radiation tolerant layout.
- 128 rows x 22 columns – 50µ x 400µ pixels.
- The only supply voltages required are 2.5V and ground; all other bias voltages, bias currents, and threshold voltages are generated by programmable DAC's.
- Very high speed, data driven, zero-suppressed readout – **no trigger; every hit is read out**.
- Readout off chip is point-to-point, using a configurable number of 140 Mb/s serial links (1,2,4, or 6). A 10m cable length is expected.
- Because of the large disparity in occupancy, a programmable number of IO line will result in a large reduction in system cost and complexity (less cables, less power, smaller DAC system).
- LVDS I/O is used throughout, including "Resets" and slow control; a single row of pads is used.

FPIX2 Block Diagram

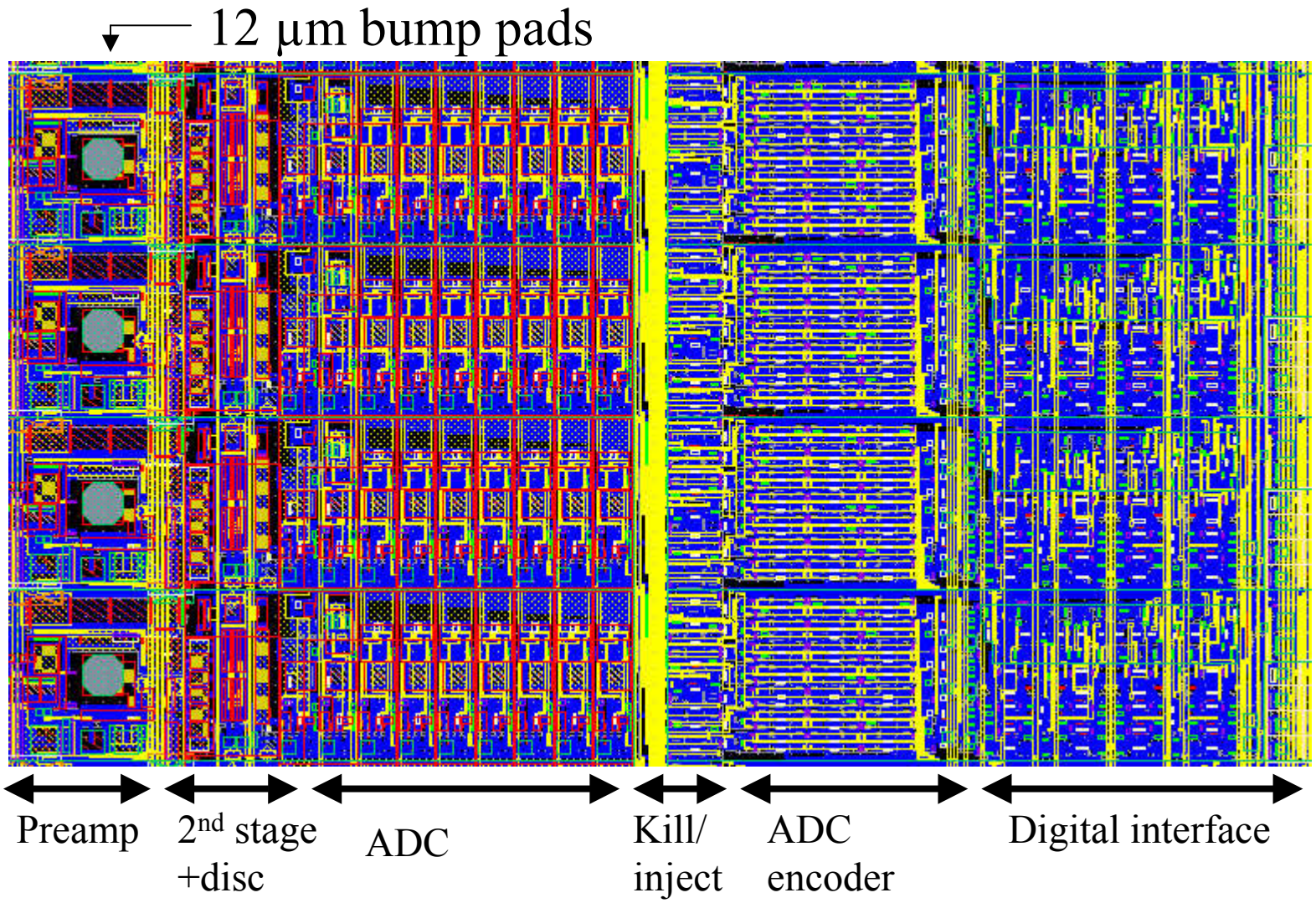
All circuit blocks have been tested in a series of small chips.



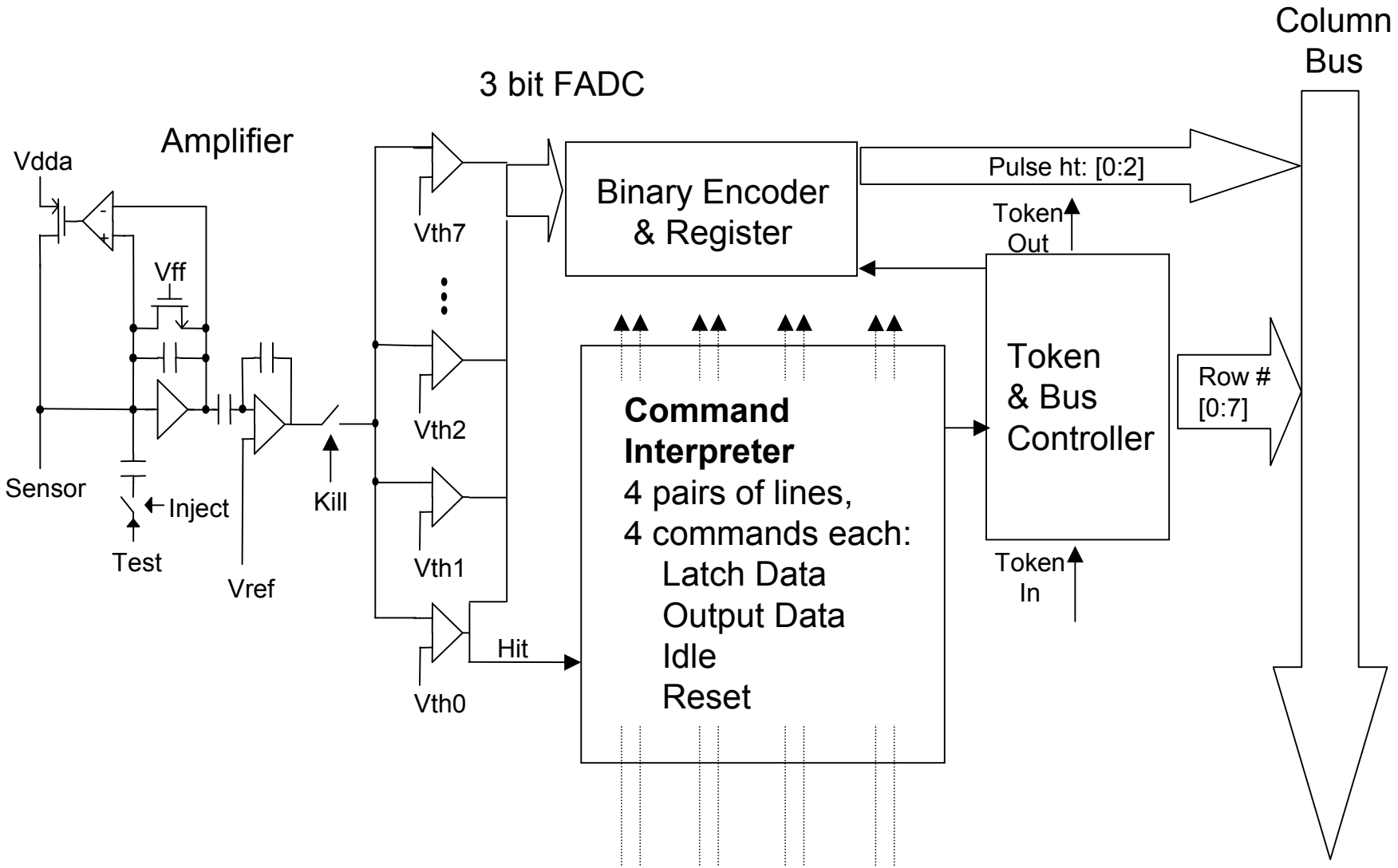
FPIX2 Layout



Pixel Cells (four 50 x 400 um cells)



Pixel Unit Cell



FPIX2: Version A,B and C

We exploited the opportunity of an Engineering run to implement 2 different flavors of our original front-end cell. The original was designed to work in 2 different processes. Modifications were aimed at optimizing the design for the TSMC process.

Version A:

⇒ Base line design.
⇒ Successfully tested
⇒ Radiation hardness beyond 30 Mrad(Si).
⇒ Exists as a 32X18 array in 2 different 0.25µ processes.

Version B:

⇒ Same preamplifier as in version A.
⇒ Modified second stage and discriminator.

Version C:

⇒ Modified Preamplifier with higher gain (lower Cf).
⇒ Added unity buffer between 1st and 2nd stage.
⇒ Modified 2nd stage and discriminators as in Ver. B

Results at a glance

=> Version A worked as expected.

⇒ Version B and C worked almost as expected except for some oscillation problems when biased at nominal conditions. Origin of problem still under investigation.

⇒ Readout and control performed as expected in all versions.

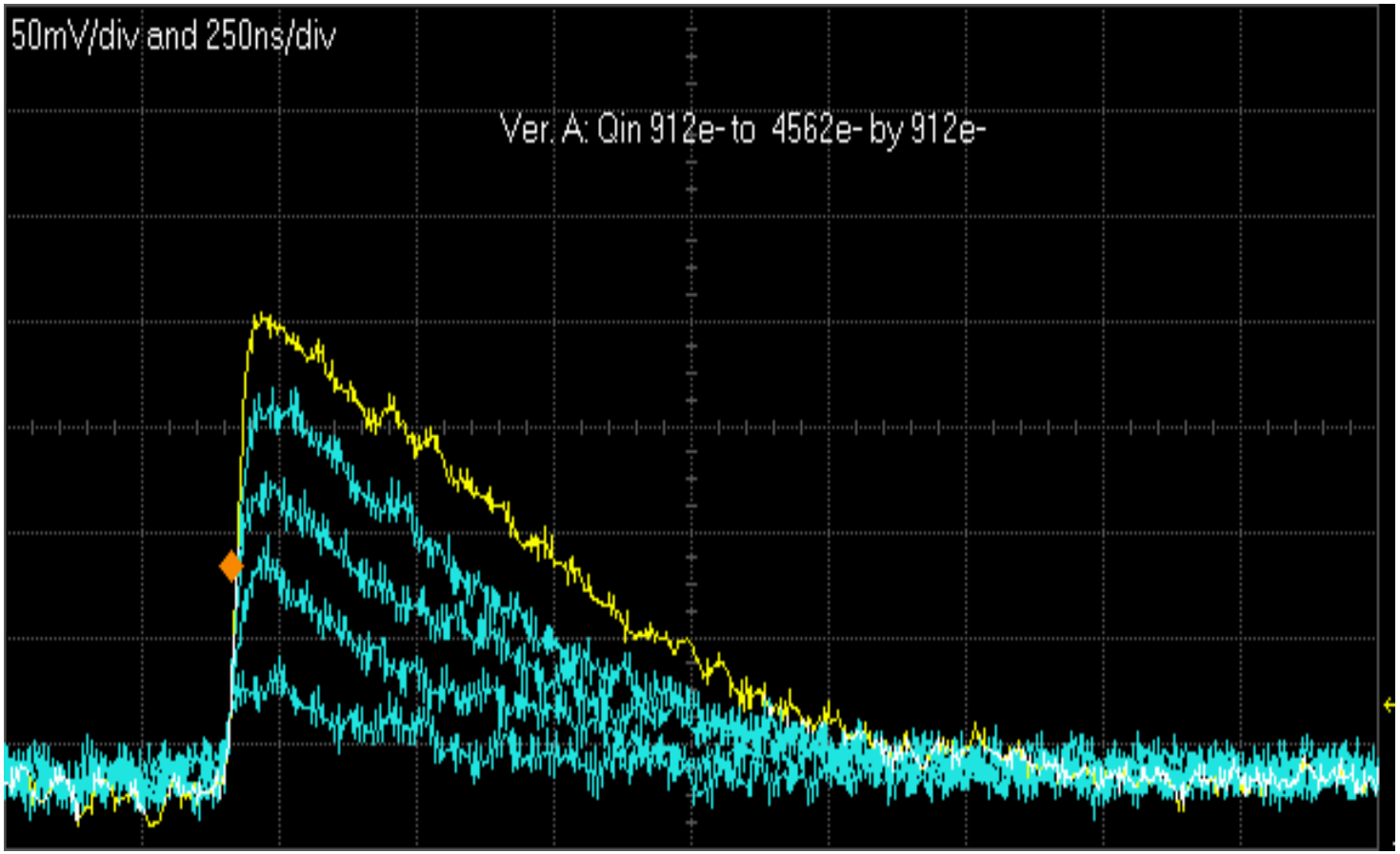
⇒ Readout bandwidth of more than 840Mb/s achieved.

⇒ No Xtalk observed. Analog performance independent of number of communication lines used (1,2,4 or 6).

⇒ The following test results are for non-hybridized chips (0 input cap).

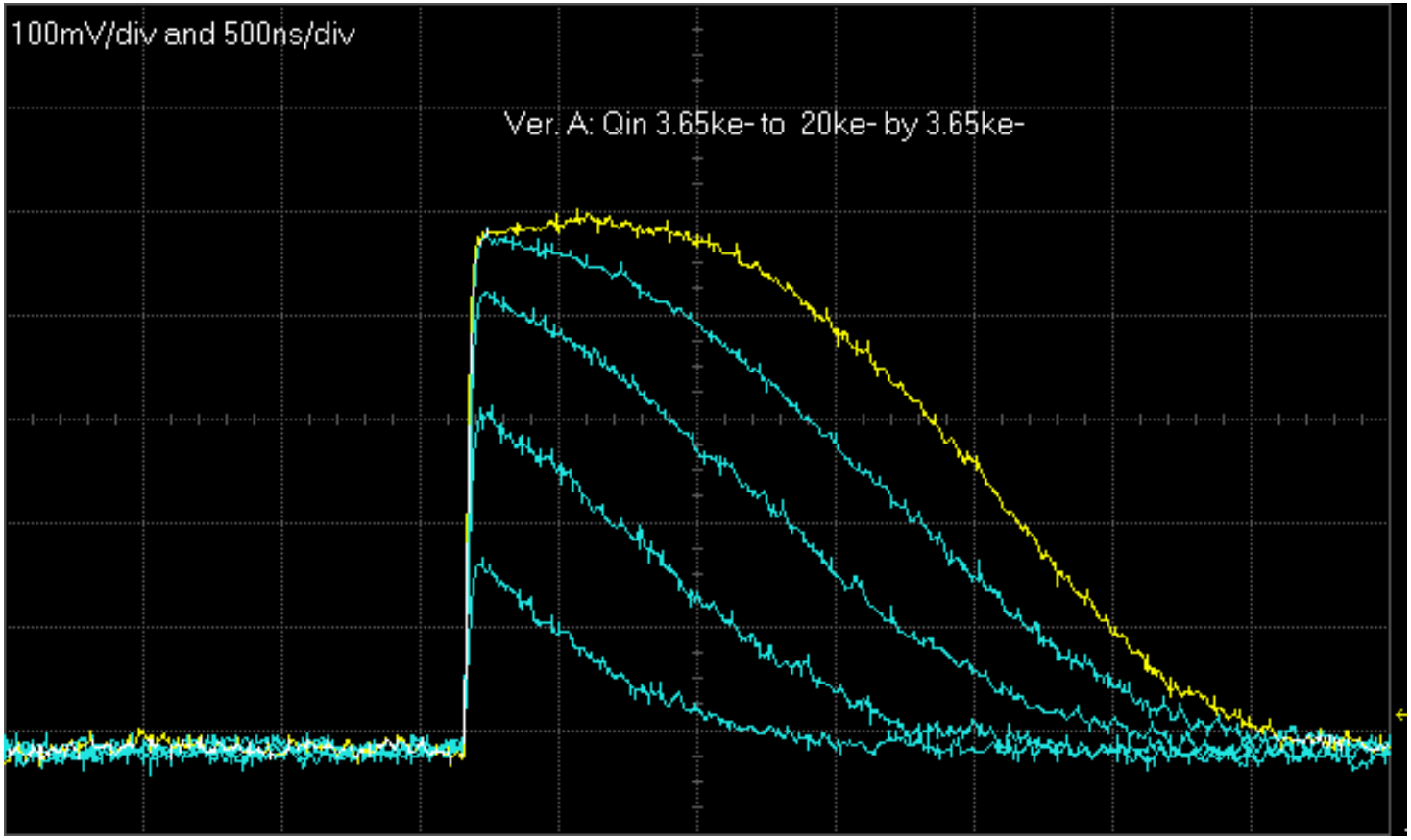
⇒ Hybridized chips expected end of June.

Version A low signal response



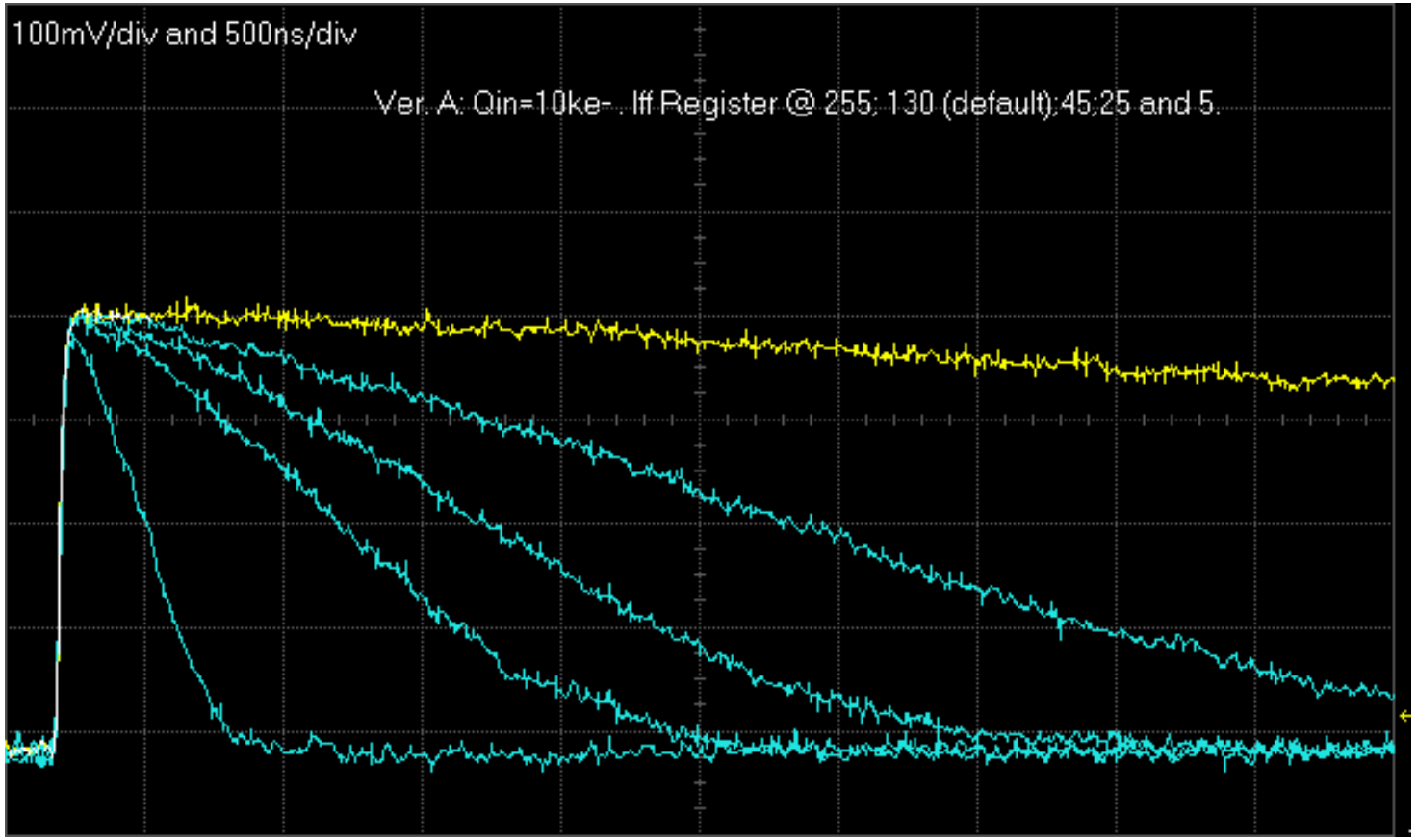
Default setup. Buffered second stage output

Version A: large signal response



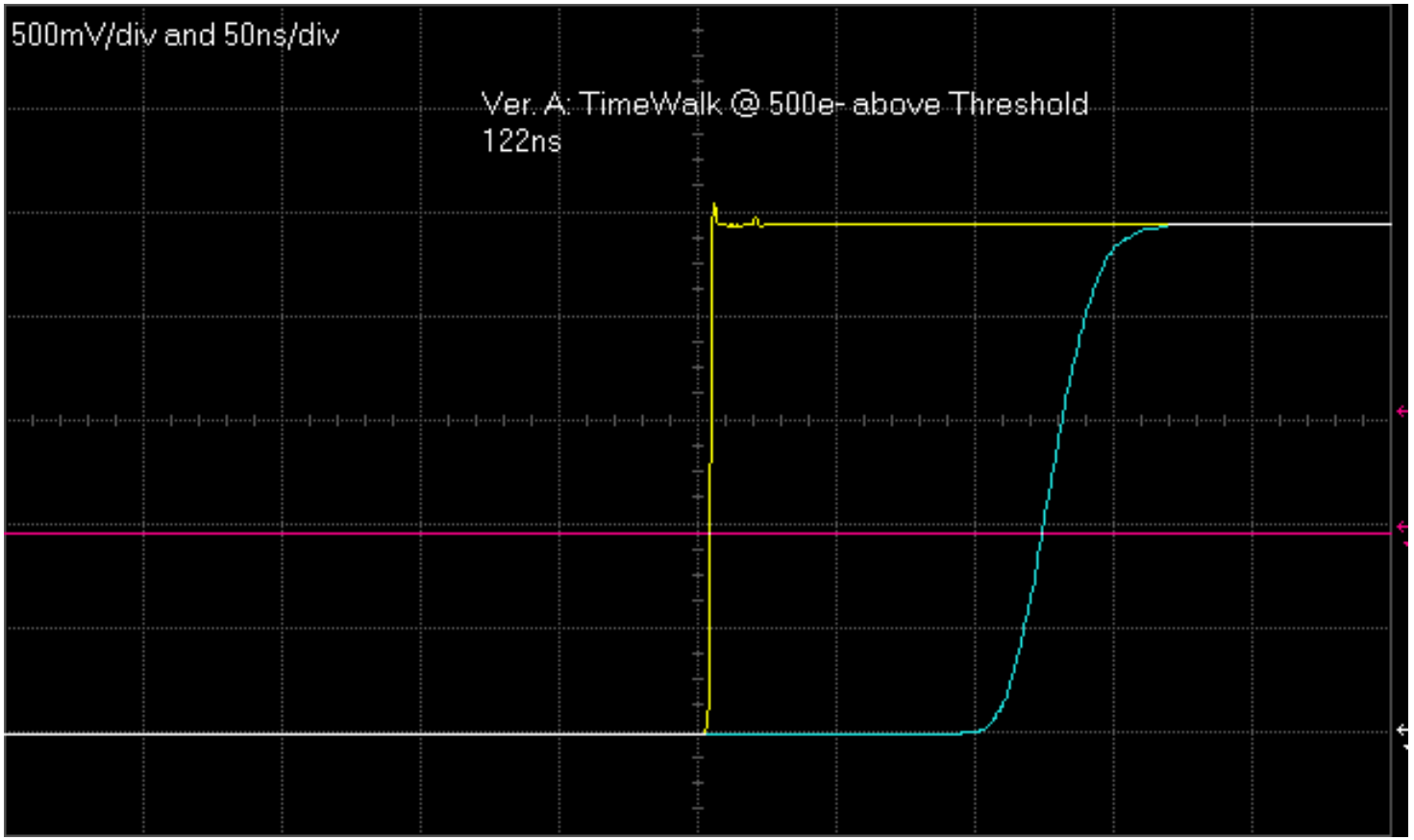
=> Dynamic range can be increased by increasing Vref (at the expense of timewalk). No averaging.

Ver. A: Return to baseline control



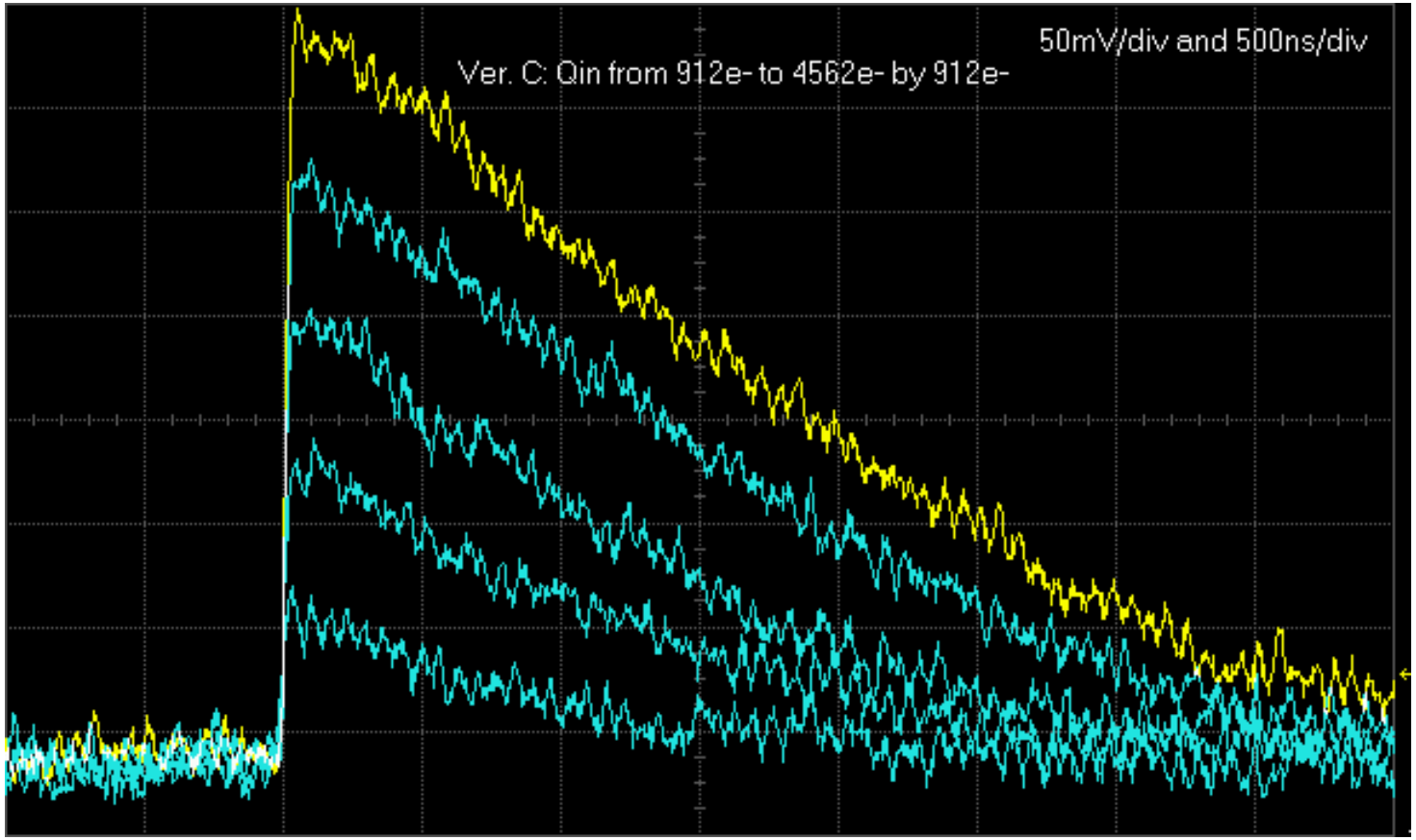
⇒ Feature used to decrease “analog” dead time for very high occupancy chips.

Version A: Time-Walk

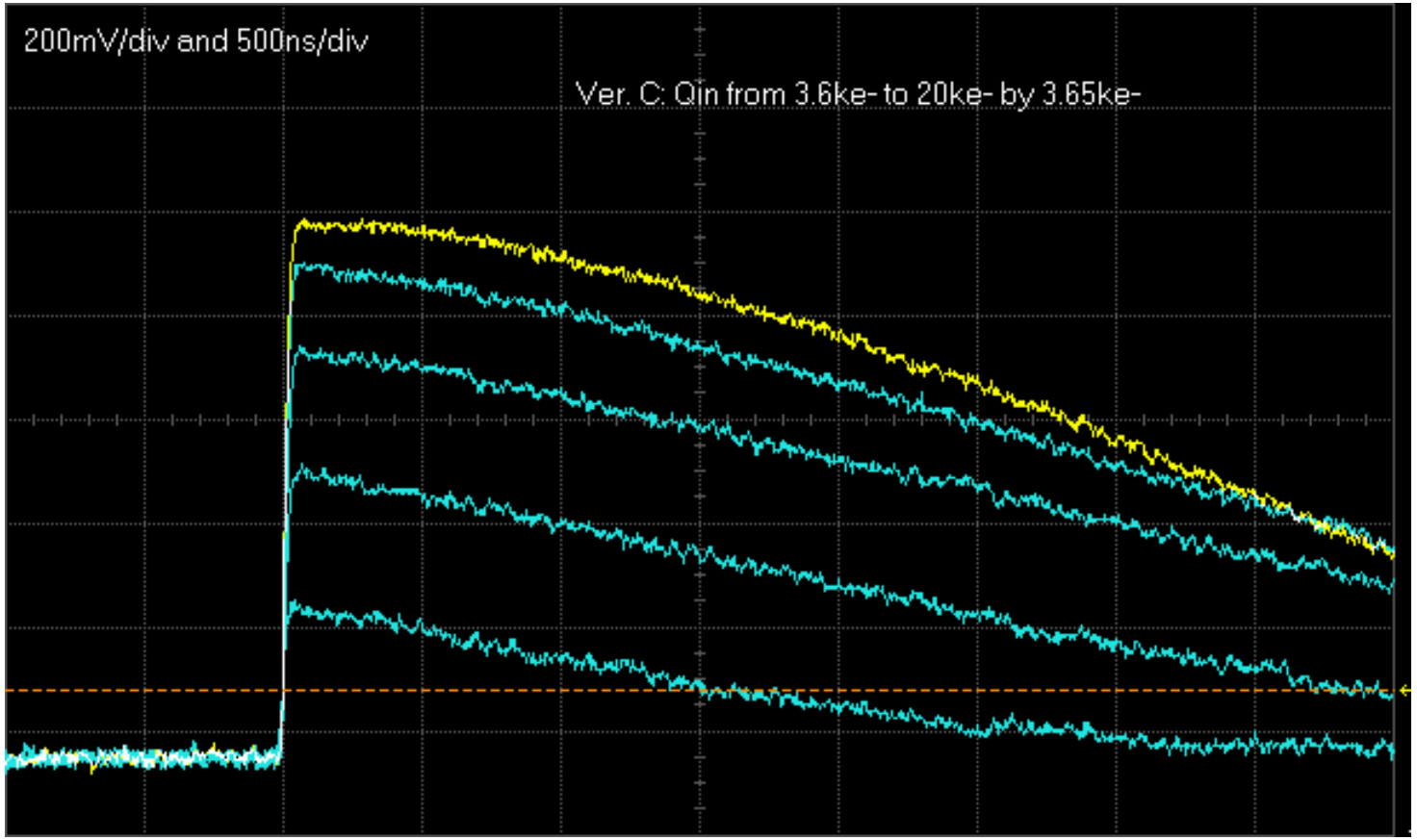


⇒ Required TimeWalk < 132ns. Can be decreased at the expense Of more power.

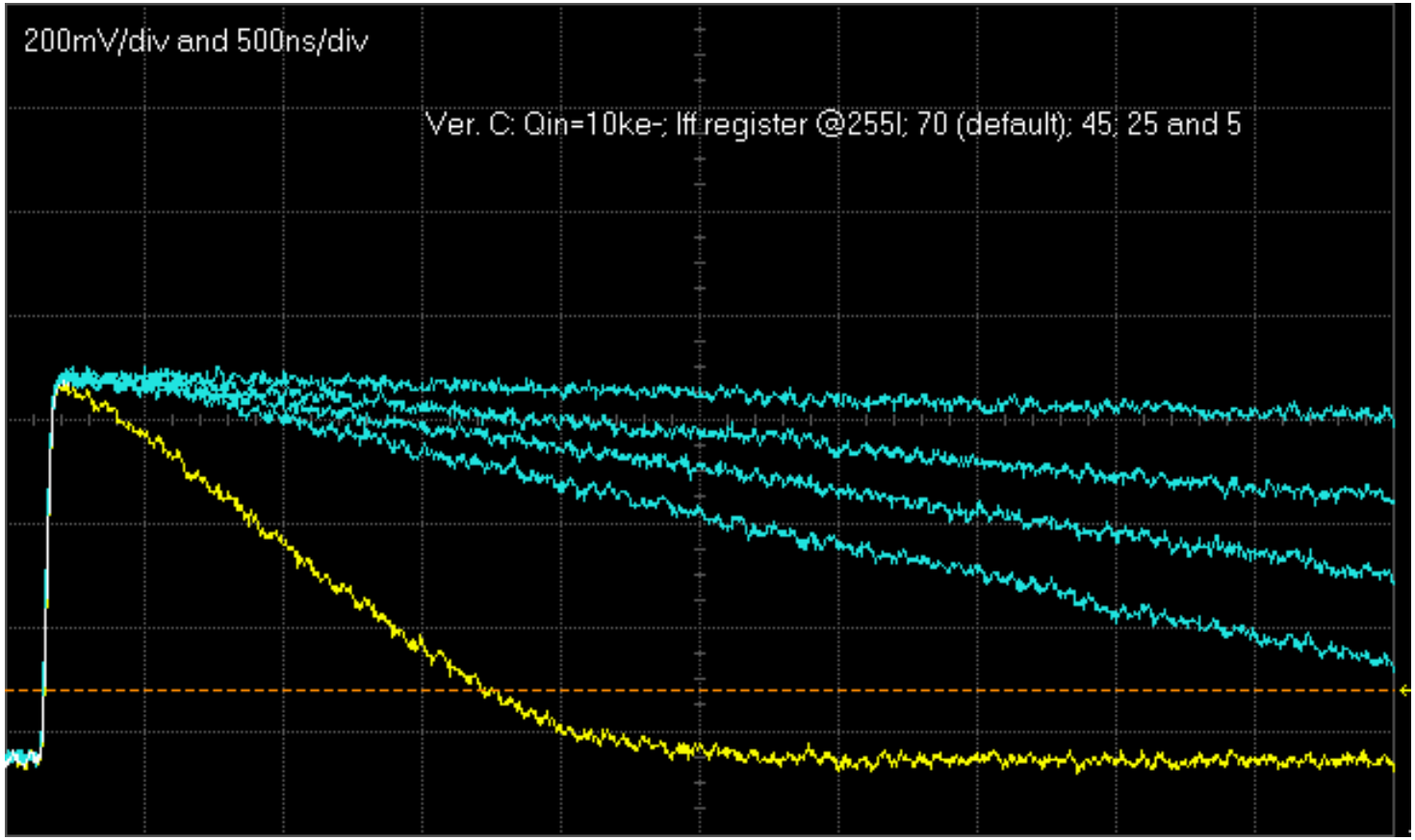
Version C low signal response



Version C: large signal response

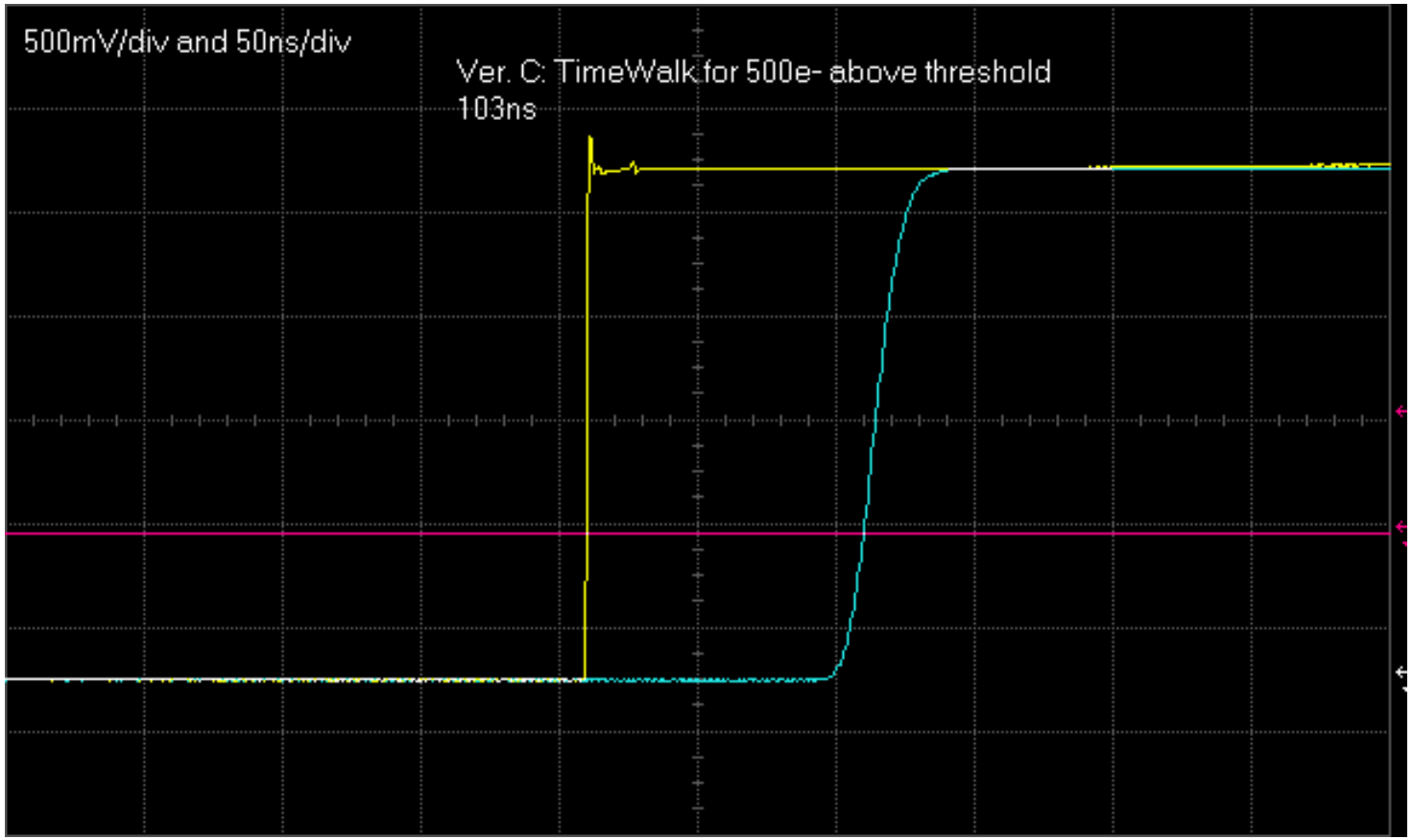


Ver. C: Return to baseline control



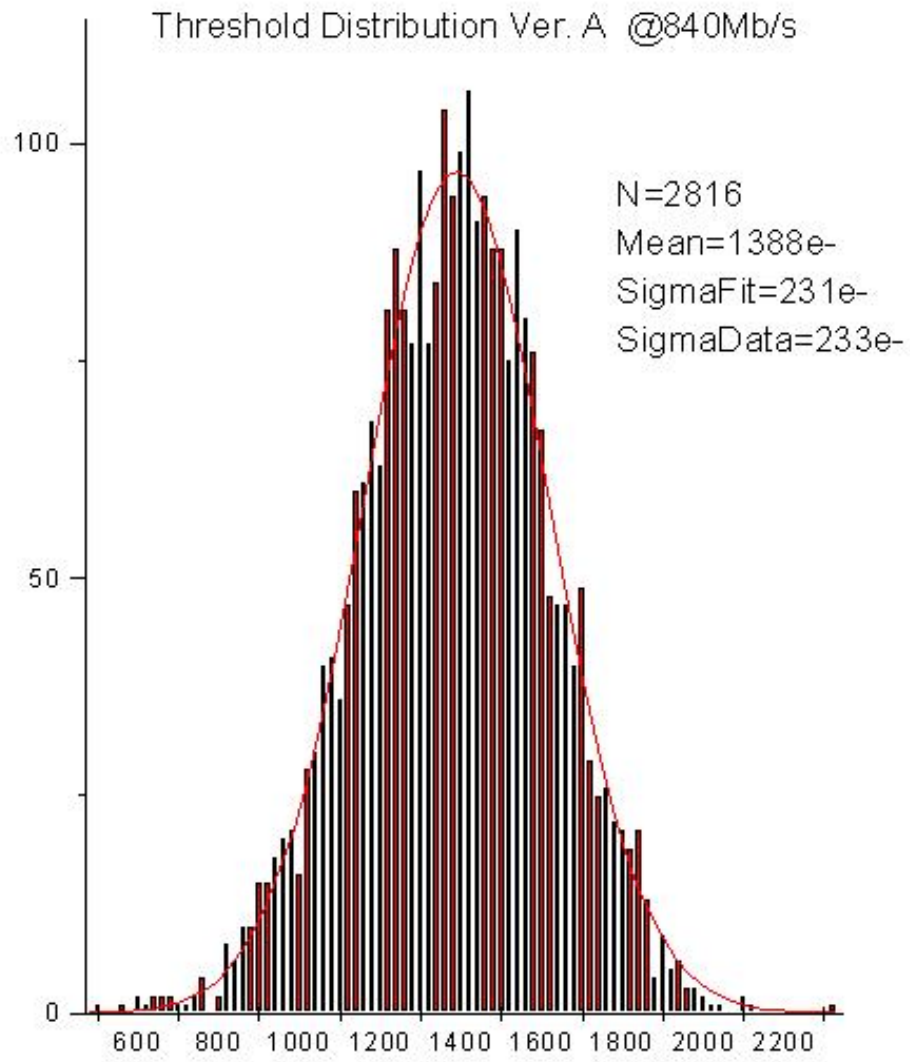
=> Less control range than in A. This is due to non-optimum bias conditions.

Version C: Time-Walk

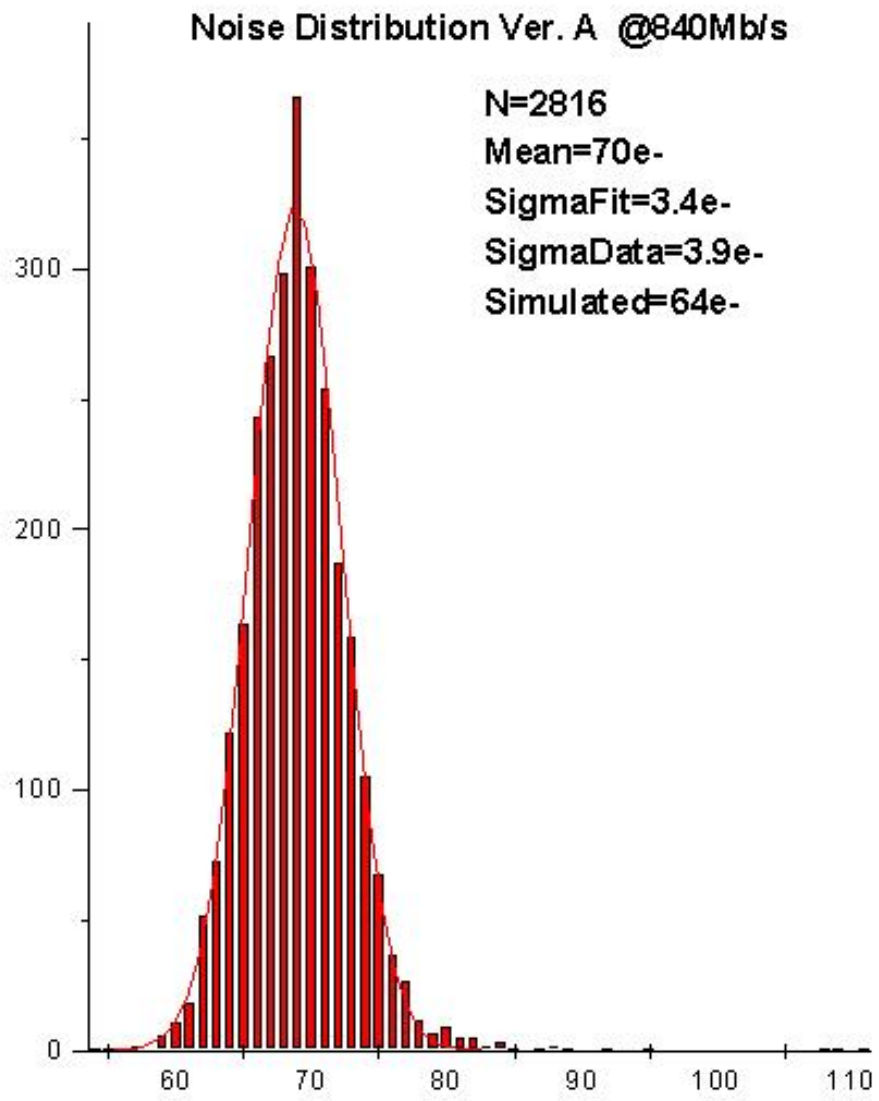


TimeWalk=103ns. Higher than expected because of non optimal bias conditions

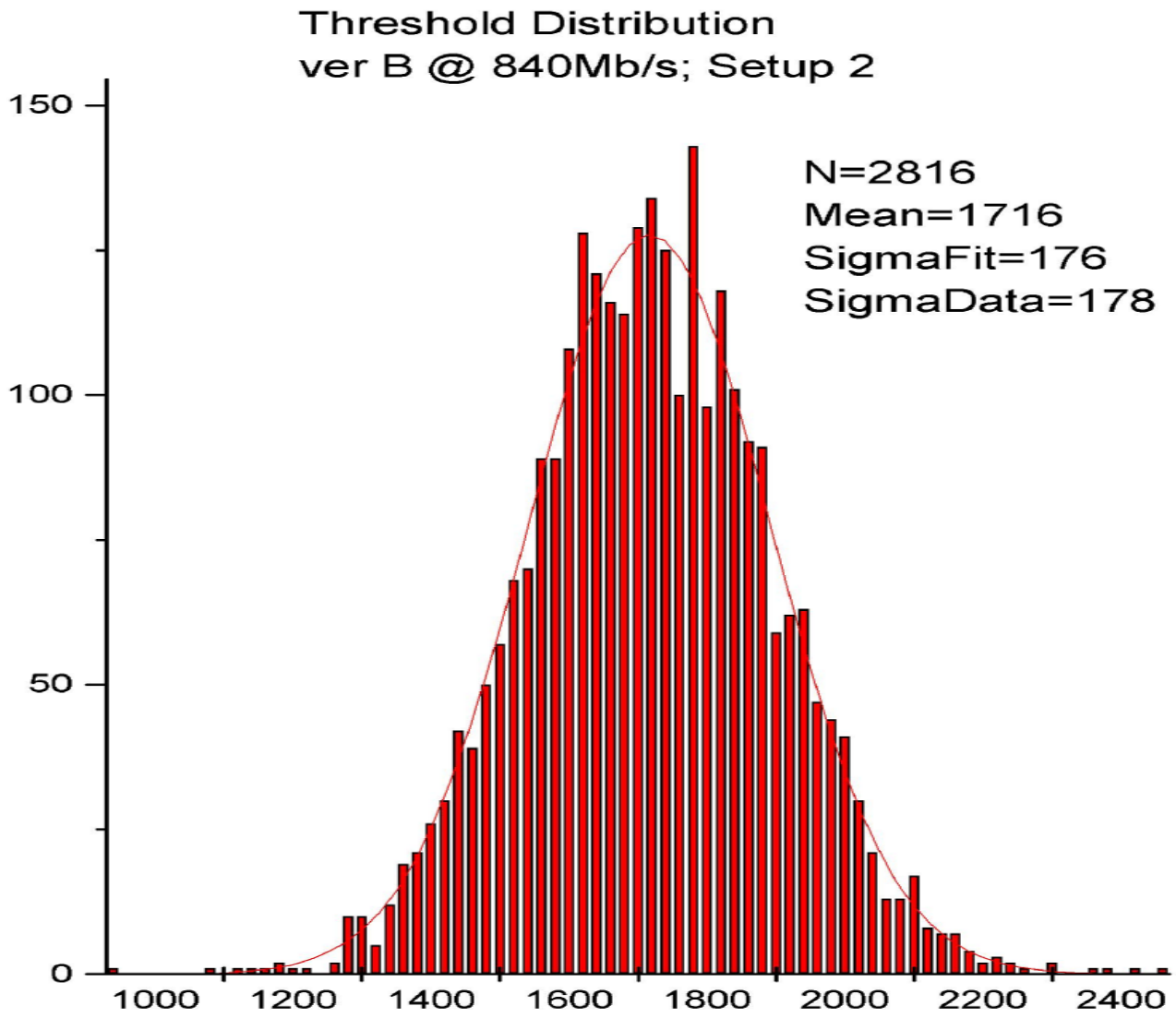
Version A: Threshold distribution



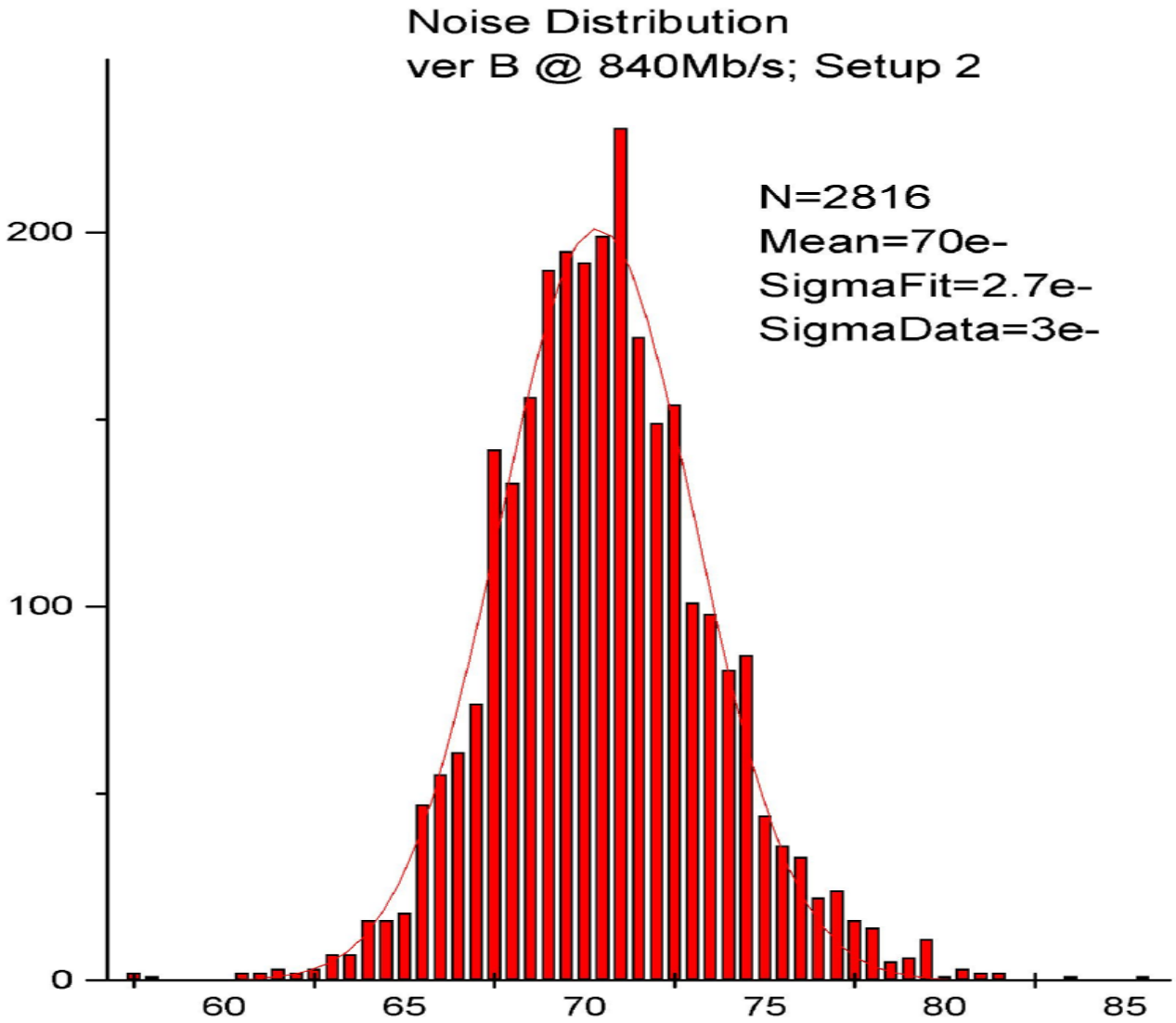
Version A: Noise distribution



Version B: Threshold distribution

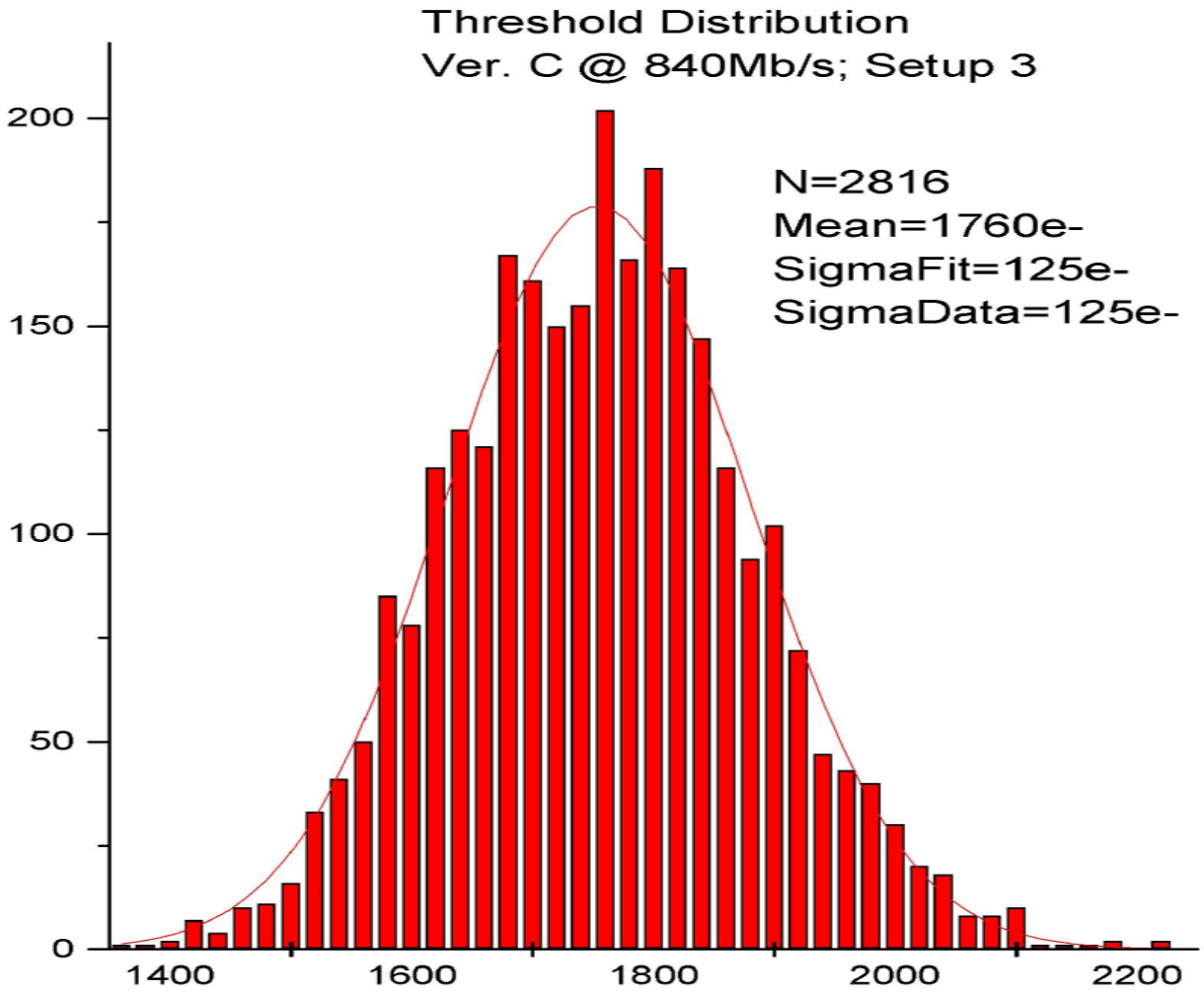


Version B: Noise distribution



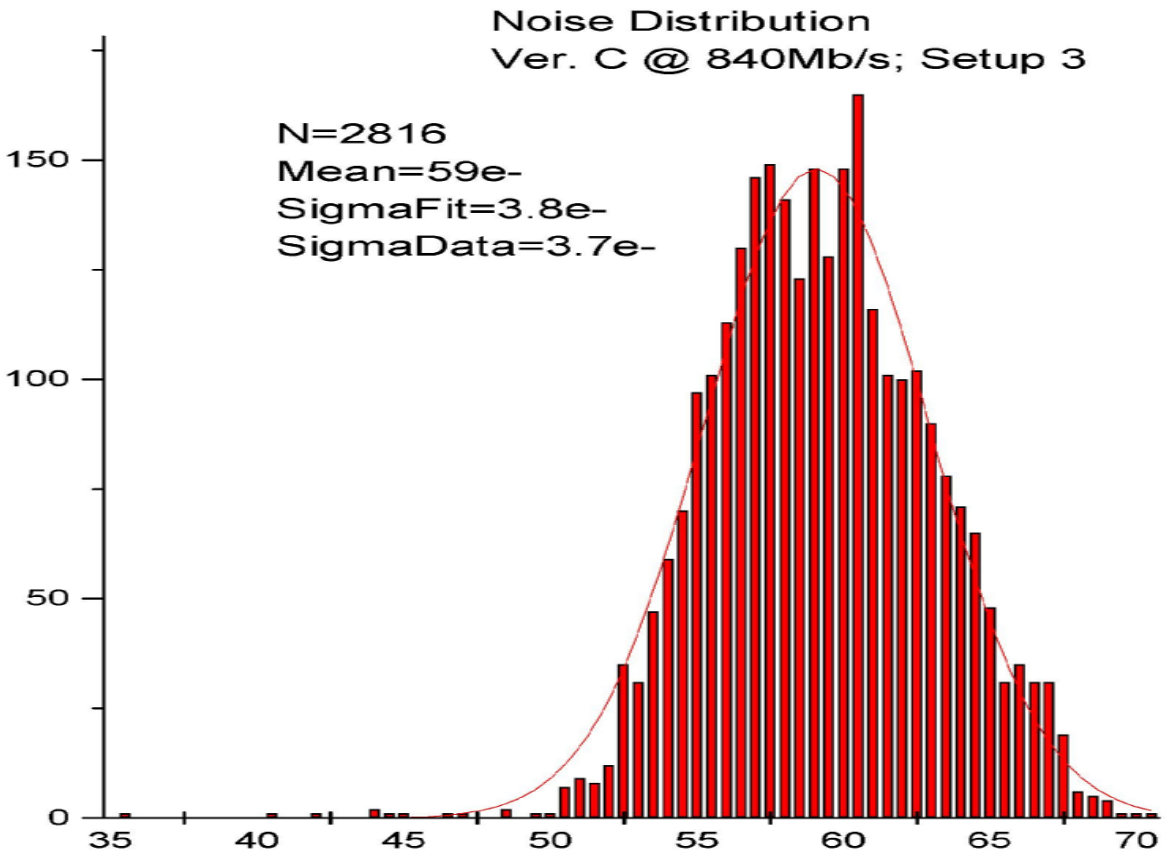
=> Noise Same as in A (same preamp).

Version C: Threshold distribution



=> Close to a factor of 2 improvement over Version A.

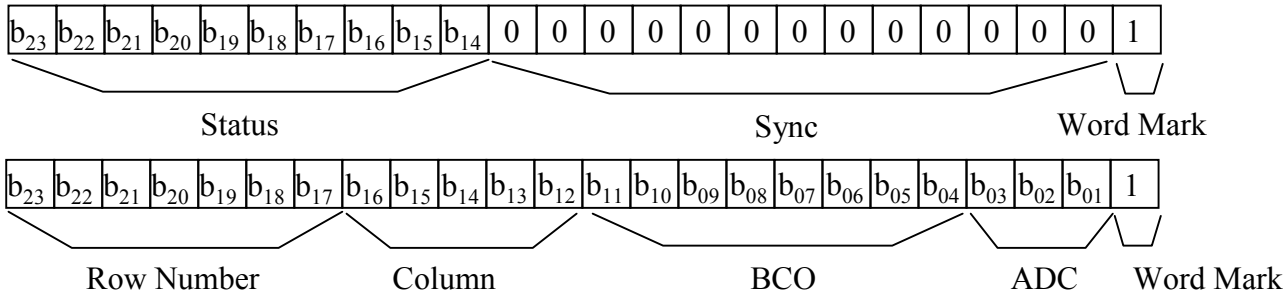
Version C: Noise distribution



A different subject: Data Output

- Data is driven off of a hit pixel onto the Core output bus, which is 23 bits wide. The data word consists of the information generated in the pixel unit cell (7 bit row number, and 3 bit ADC value), plus a 5 bit column number and an 8 bit BCO number, which are added by the end of column logic.
- The Data Output Interface latches data from the Core output bus on the *rising* edge of the readout clock, serializes the data, and drives it off chip.

Output Data Format

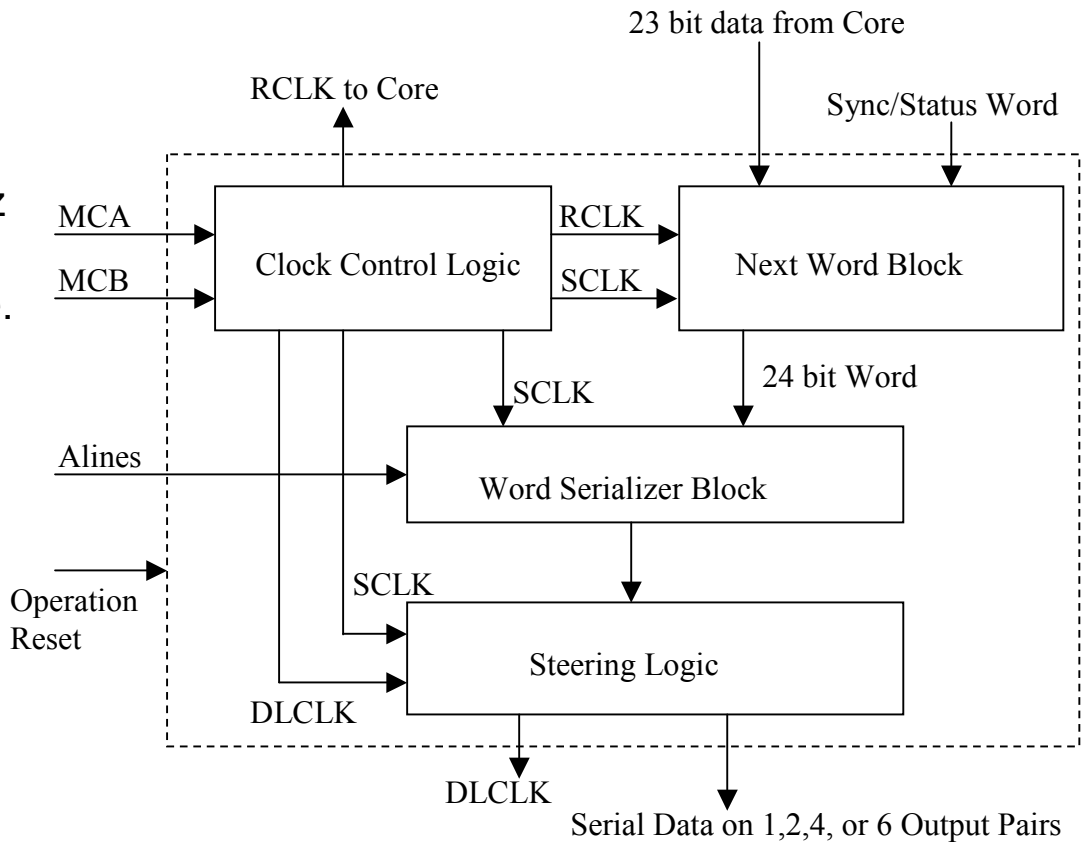


• Five bits are used to encode 22 columns. The column numbering scheme has no column number ending in 00. This ensures that a data word can never have 0's in b_{01} – b_{13}. This feature distinguishes a data word from a sync/status word.

•Synchronization between the FPIX2 and the Pixel Data Combiner Board is established and maintained using the "sync/status" word. Whenever no data is available for output, the FPIX2 transmits the sync/status word. At least two sync/status words are guaranteed to be output every time the column number decreases. In addition, 23 bit hit data is transferred using a 24 bit word. The PDCB uses the word mark bit as a sync check on every word transfer.

Data Output Interface

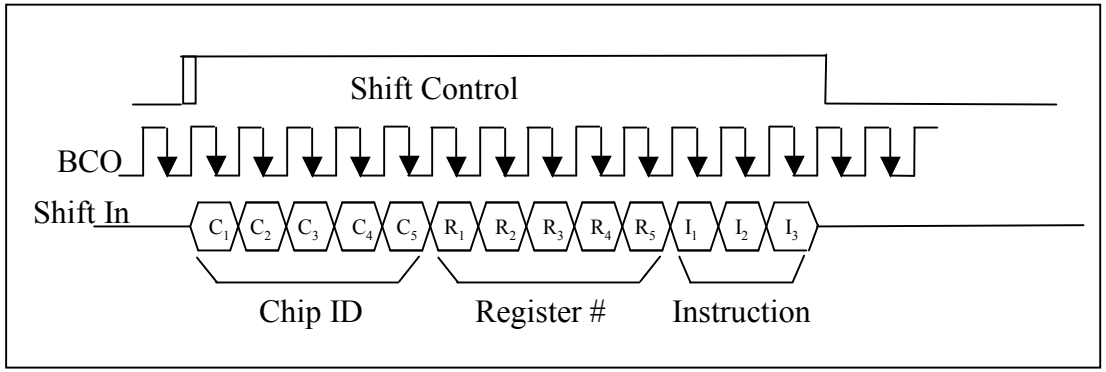
Two 70 MHz clocks, 90º out of phase.



Programming Interface

- Each FPIX2 has a chip id, which is set by wire bonds on internal bond pads.
- I/O is bussed on three pairs of lines: shift control, shift in, shift out.
- I/O is synchronous – clocked by the BCO clock.
- Commands can be addressed to a single chip, or broadcast to all chips on the bus.

Command Format



Programming Interface Instructions

- Write (followed by 2, 8, or 2816 bits of data)
- Set (all bits in register = 1)
- Read
- Reset (all bits in register = 0)
- Default (set register to default value)

Registers and DAC's

- 22 of 32 possible registers are used.
- 14 are 8 bit registers that control Digital to Analog Converters – used to set bias currents and voltages, and comparator thresholds.
- 2 are serpentine registers (kill and inject) running up and down the pixel columns, with 1 bit in each pixel.
- 6 control facets of chip operation (# of output pairs, BCO sync check, SendData, RejectHits, Core Reset, Programming Reset).

Conclusions

⇒ We successfully designed a full “quasi” final pixel readout chip for BTeV.

⇒ Design based on proven radiation-hard circuits. These circuits also proved to be very adequate as far as SEU is concerned.

⇒ Readout speed and features allow fast non-triggered operation.

⇒ Programmable features allow flexibility in optimizing the system for cost, simplicity or performance.

⇒ 3 different versions to evaluate during the next beam test.

⇒ Only feature(optional) to be added is an on-chip “pulse generator”.

More Information

- http://www-btev.fnal.gov/public/hep/detector/pixel/index.shtml
- “Radiation tolerance of prototype BTeV pixel detector readout chips” G. Chiodini, et al. FERMILAB-CONF-02-147-E (7/02).
- “Development of a readout technique for the high data rate BTeV pixel detector at Fermilab” B.K. Hall, et al. FERMILAB-CONF-01-335 (11/01).
- “Radiation tolerant circuits designed in two commercial 0.25µ CMOS processes” A. Mekkaoui, et al. FERMILAB-CONF-01-026-E (3/01).
- “FPIX2: A radiation-hard pixel readout chip for BTeV” D. Christian, et al. NIMA 473:152-156, 2001.
- “PreFPIX2: Core architecture and results” J. Hoff, et al. IEEE Trans.Nucl.Sci. 48:485-292, 2001.