A New Deep Submicron Readout IC for the Tevatron

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Collaboration

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SVX generations

	SVX	SVX2	SVX3	SVX4
Development	1986-89	1993-96	1995-98	2000-03
Foundry	UTMC	UTMC	Honeywell	TSMC
Feature size	3.0 µ	1.2µ	0.8µ	0.25µ
Channels	128	128	128	128
Beam Crossing	3 µsec	132/396 ns	132/396 ns	132/396 ns
Storage	None	32 cells	42 cells	42 cells
Signal output	Analog	8 bit	8 bit	8 bit
Programmable	No	Yes	Yes	Yes
Deadtimeless	No	No	Yes	Yes
Chip Size (mm)	6.3x4.6	6.3x8.9	6.3x11.9	6.3x9.0
Radiation	? Mrad	<10 Mrad	<10 Mrad	>20 Mrad
Experiment	CDF	DO	CDF	CDF&DO

Overview

- Motivation for SVX4
- A conceptual operational description
- Operational features and redesign summary by module
- Design flow for a “high-confidence” submission
- What was achieved—performance, functionality

Motivation for SVX4

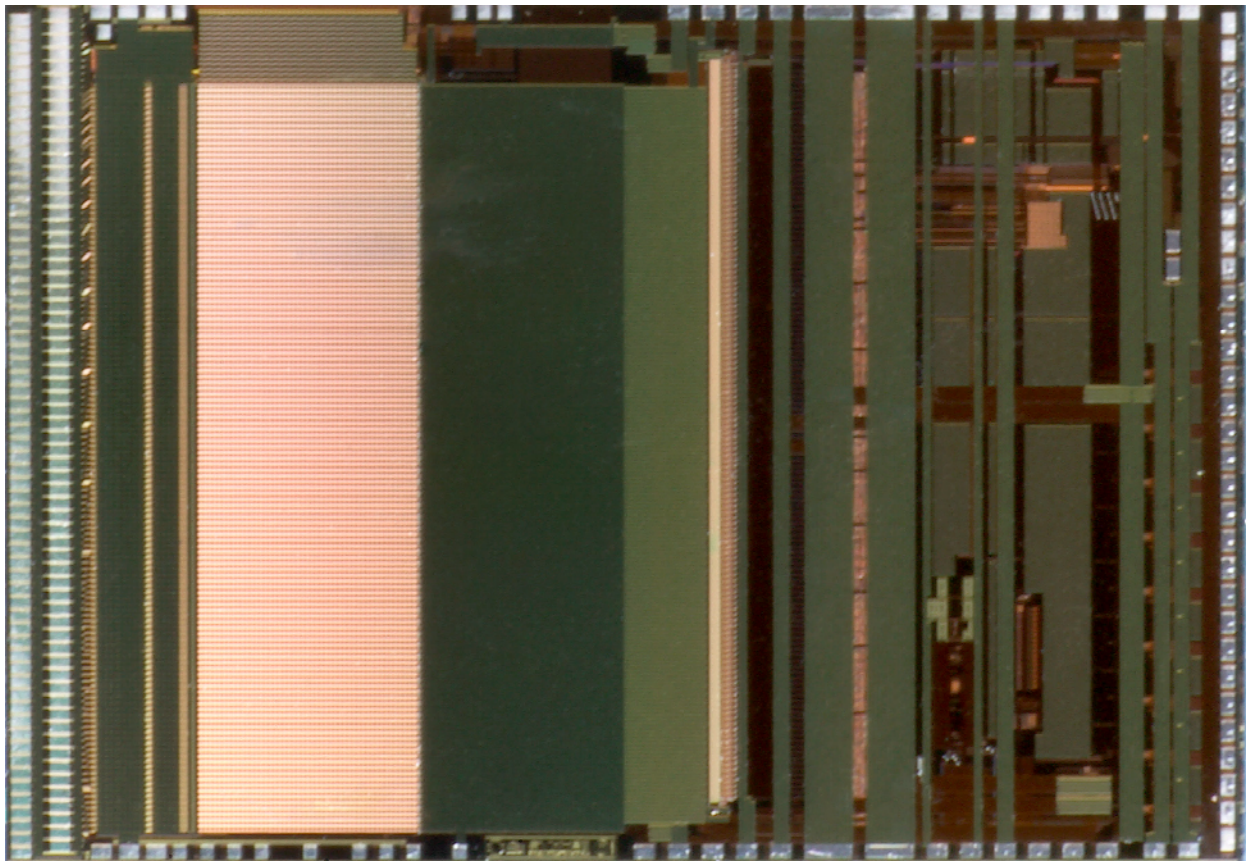
Requirements

- Higher total dose tolerance for Run IIb—use radiation tolerant-by-design methodology in TSMC 0.25um process
- Improve performance where possible, ***but***
- Fast turn-around for 0.8um – 0.25um conversion, ***and***
- Have functional devices on the prototype run

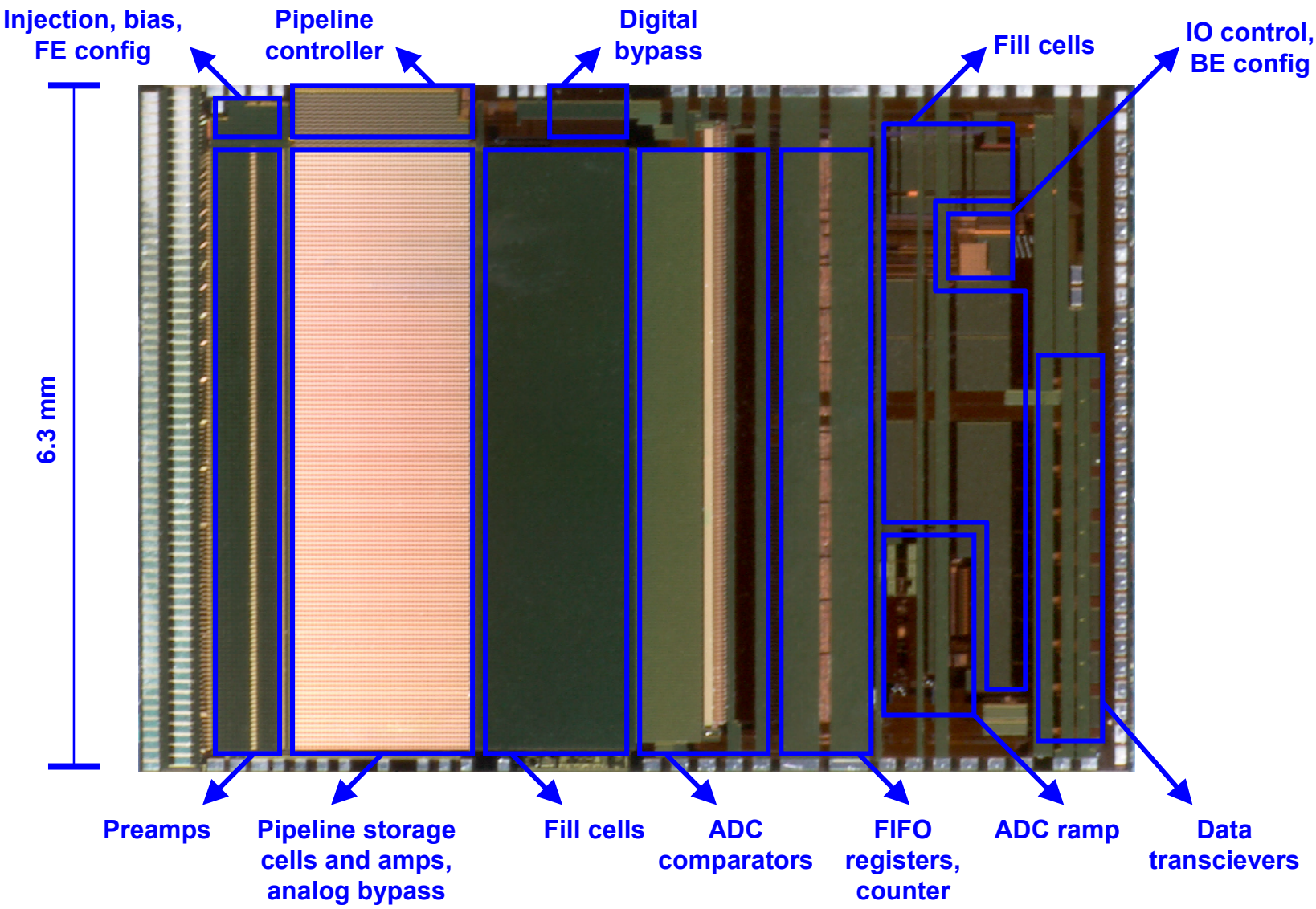
Approach

- Keep the existing floorplan
- Limit redesign
  - Where necessary for technology reasons
  - Where performance benefits are significant
  - Where reliability improvement is significant
- Integrate SVX2 (D0) and SVX3 (CDF) functionality into a single chip to reduce the design time
- Develop a comprehensive design verification procedure

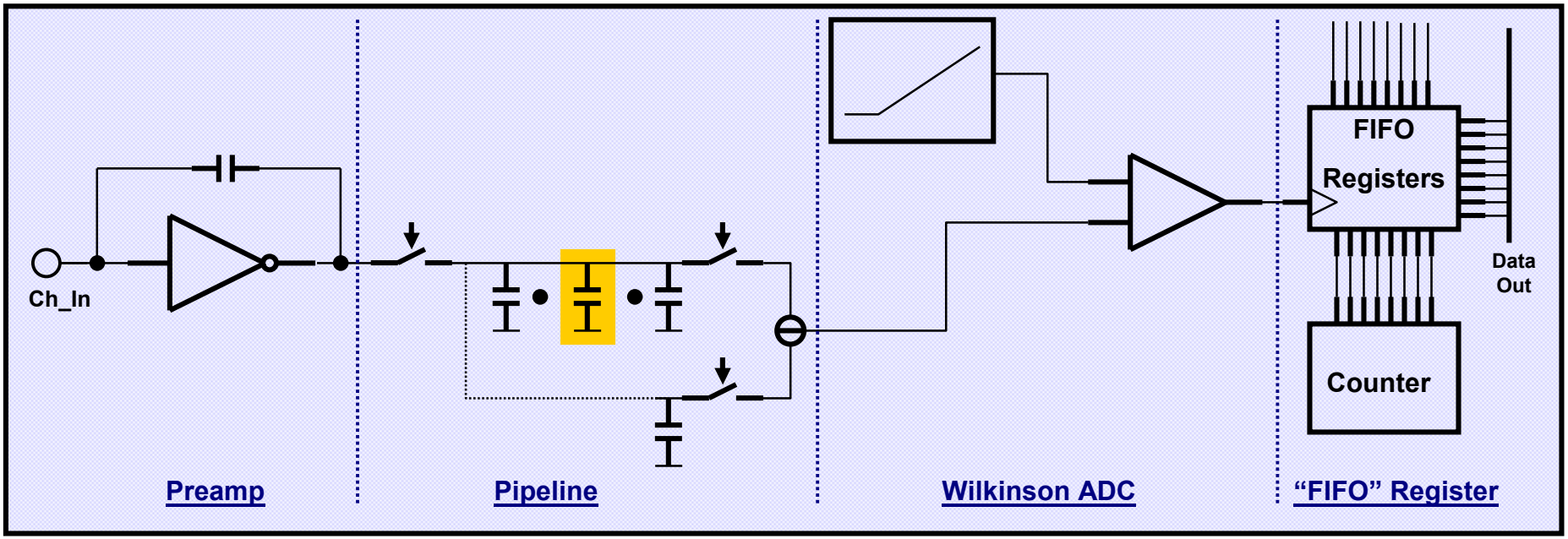
SVX4 die photo



SVX4 modules

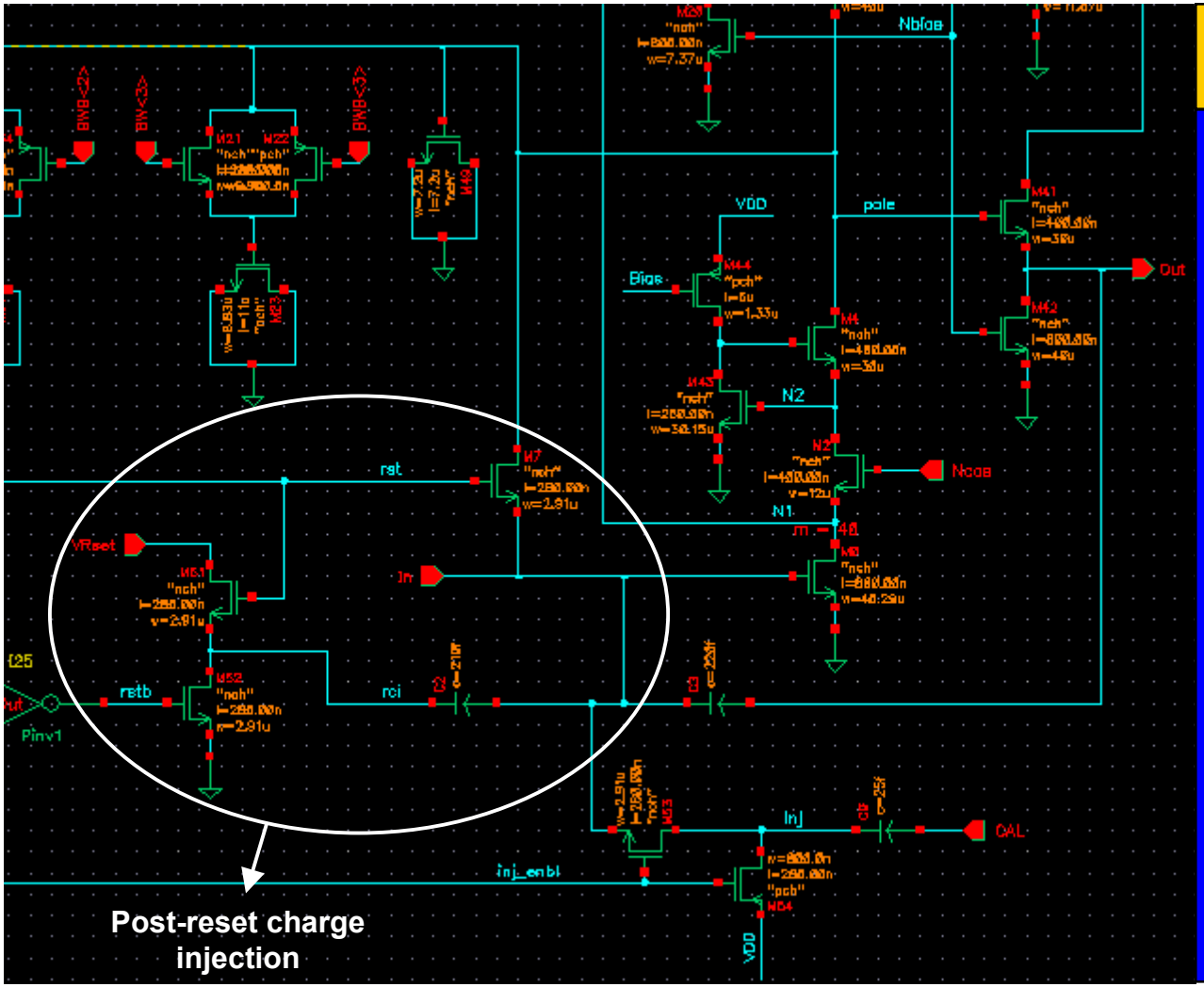


SVX4 conceptual operation



- For each channel, charge signals of up to 60 fC are stored in the 46-deep analog pipeline by sampling of the preamplifier output with a 132 ns period
- The pipeline operates as a ring of storage cells per channel, with the capability to remove up to 4 cells from the circular chain to accommodate the storage of up to 4 events before a digitize-readout sequence is required
- The value is digitized (minus a pedestal) by a Wilkinson ADC, latching the counter value when the ramp crosses the signal voltage
- The data value latched in the FIFO data register is readout as the signal magnitude; various levels of readout sparsification can be programmed
- The design features "dead-timeless" operation, meaning that pipeline data collection continues during digitize and readout modes

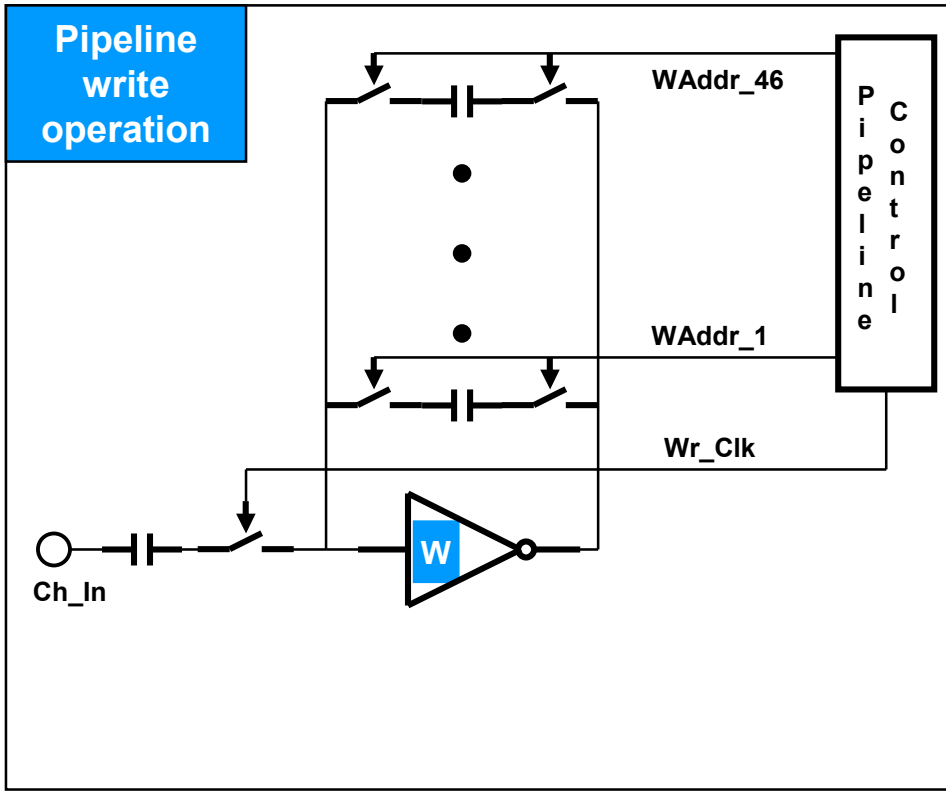
Preamp summary



Redesign for technology and enhanced performance

- **Quiescent level set by charge injection step after reset**
- **Reset method reduces reset time by allowing the capacitor to be reset through a buffered switch to the input, then the appropriate quiescent level can be set independently**
- **Better noise performance in 0.25um due to lower white noise of input transistor**
- **"Excess noise" of DSM process was evaluated vs. L of the input transistor in a prototype chip, optimum L for noise was chosen**

Pipeline summary

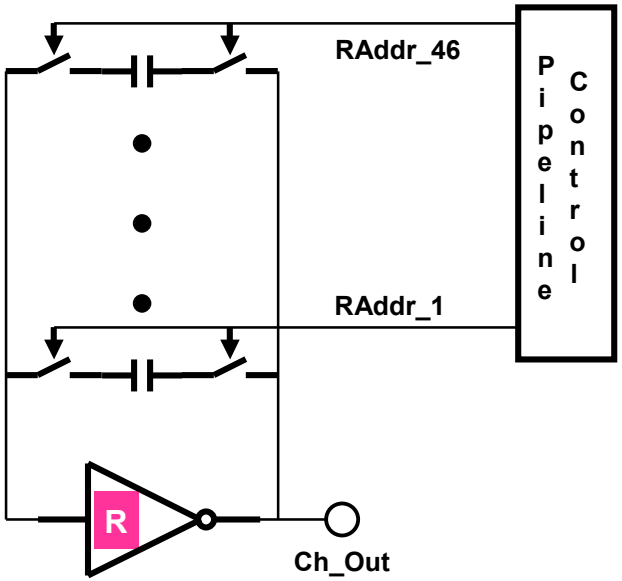


Redesign for technology and enhanced performance

- Pipeline controller redesigned to reduce space, fix bugs
- Pipeline storage cell and read/write amps redesigned to use MiM caps and optimize dynamic range at 2.5V Vdd
- CDS operation is accomplished by saving the previous preamp value across a common input cap
- 46-deep capacitor storage cells are successively written by an address pointer that is generated by a ring counter

Pipeline summary

Pipeline read operation



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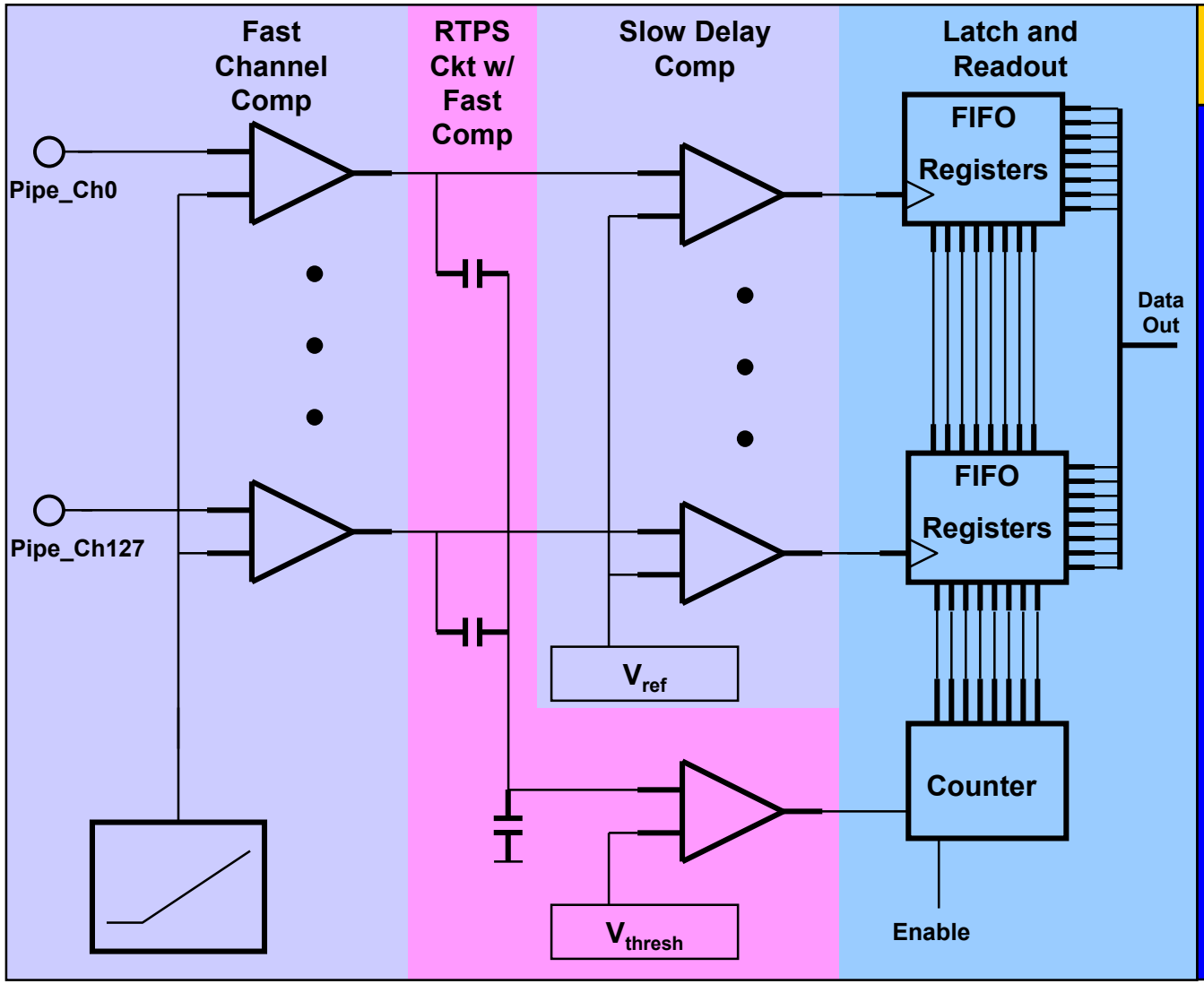
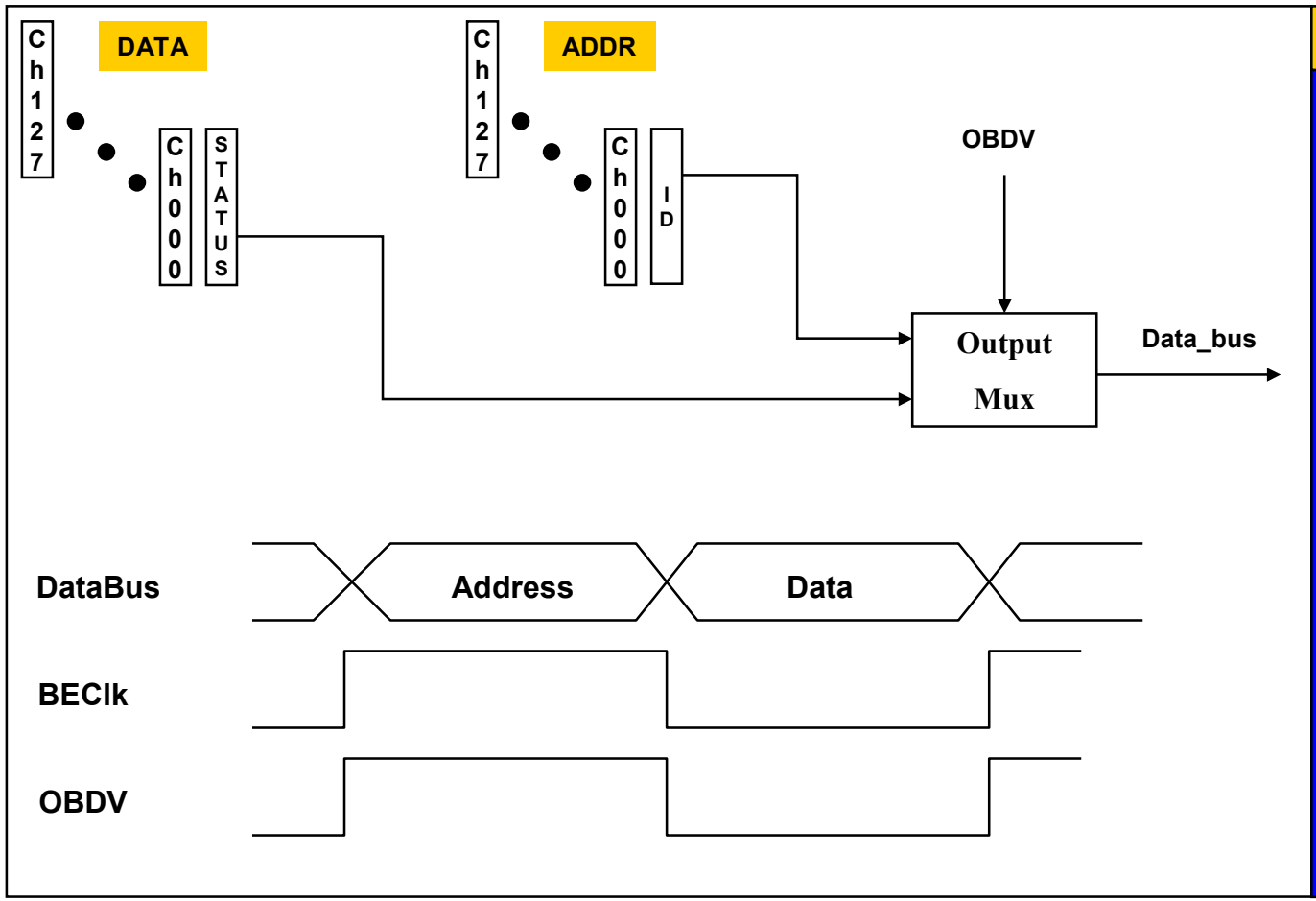
ADC summary



Redesign to meet performance spec

- A problem with spacial pedestal variation required redesign of the stage for optimum performance
- Non-RTPS mode gives an absolute pedestal determined by the two-comparator delay
- RTPS mode takes a fixed charge contribution from each channel firing 0-2.5V
- This total contribution is proportioned across a common capacitor
- The threshold voltage set on the RTPS comparator then determines the number of channels required to fire for the dynamic pedestal
- The counter is only then started, subtracting the dynamic pedestal

FIFO summary

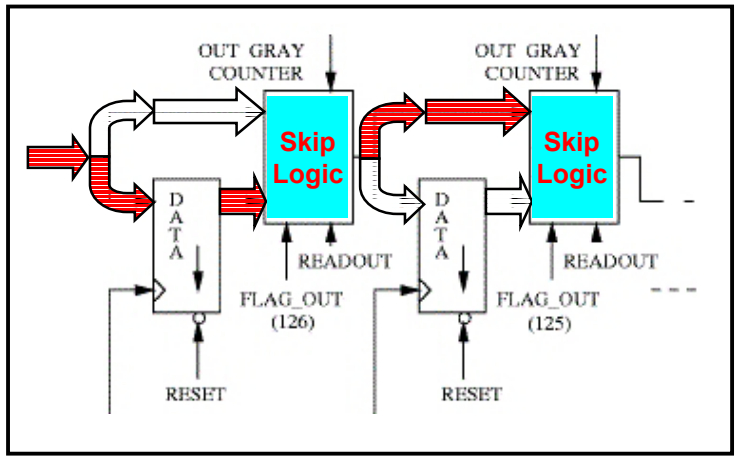


Redesign for technology

- Dynamic logic of previous design was custom for the technology
- "FIFO-collapse" sparsification method of SVX3D clever, but can't be synthesized in static logic using standard cell lib
- "FIFO-collapse" operation generates an undesirable power spike on DVDD
- New static design synthesized using ATLAS pixel cell library, autorouted with SE
- Config registers (unrelated) use ATLAS DICE cell

FIFO sparsification

- During DIGITIZE, the data dff arrays are accessed as 128 individual 8-bit registers with the gray counter as the input
- On READOUT↑, a channel is flagged for readout (FLAG_OUT=true) depending on its data value and the programmed sparsification level
- During READOUT, both the data and address arrays are accessed as shift registers, effectively "collapsed" in parallel by the "skip logic" cells



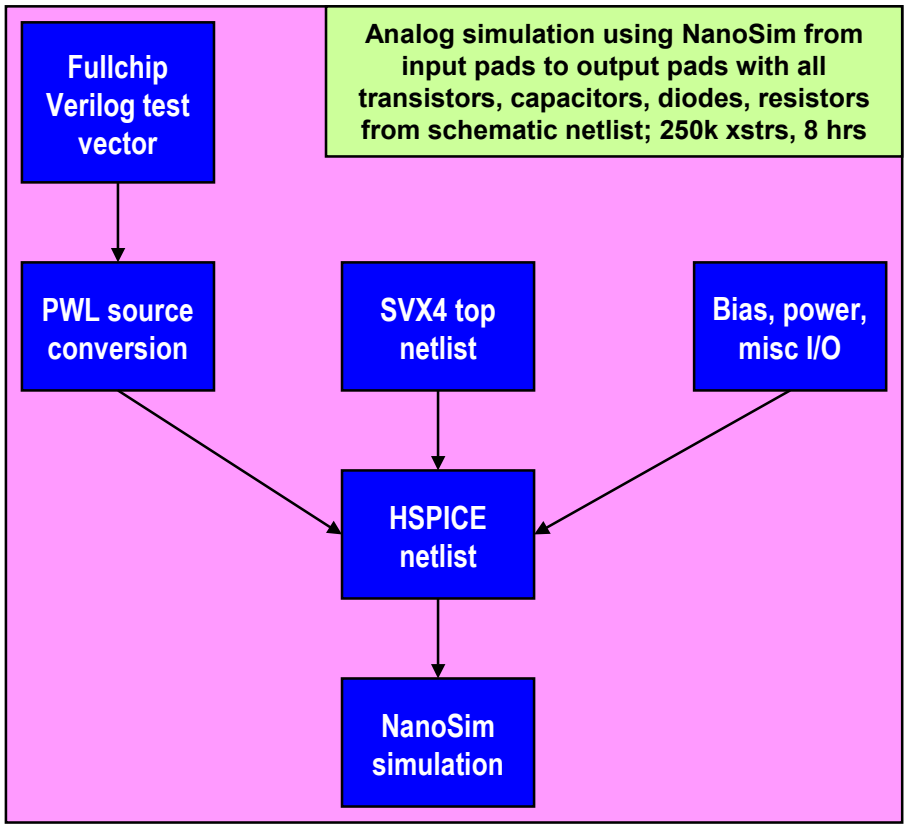
"FIFO" datapath

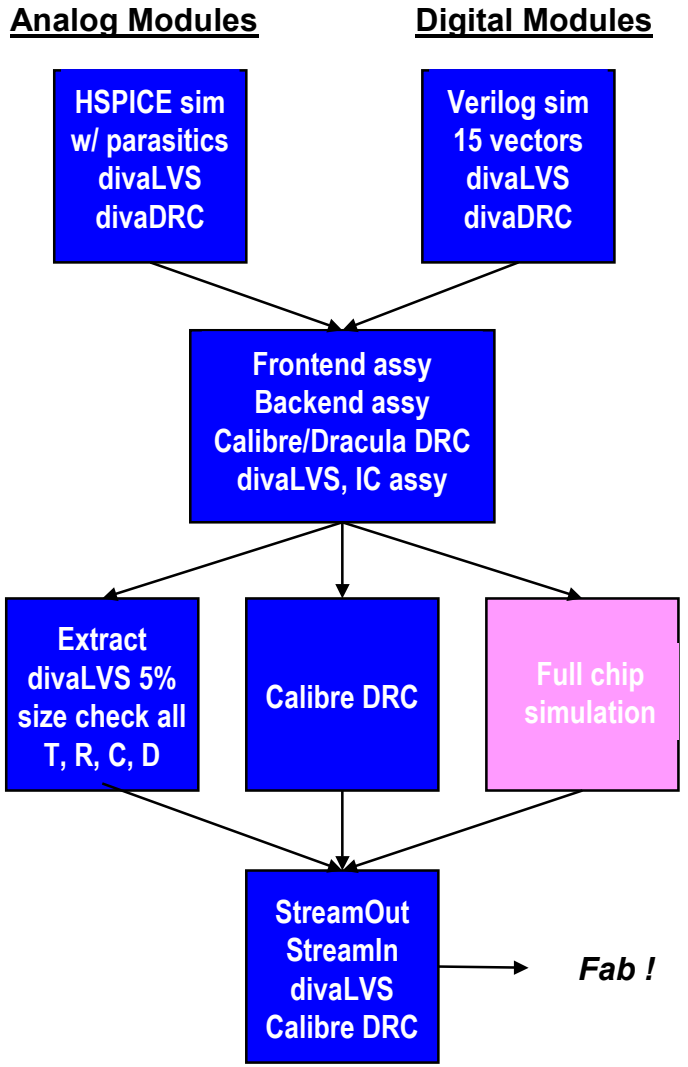
• Ch126 flagged for readout, ch125 is not

• Ch126 collapses to next flagged channel

• Readout speed is limited to (127*SkipCellDelay), worst-case in sparse mode

Design verification flow for SVX4





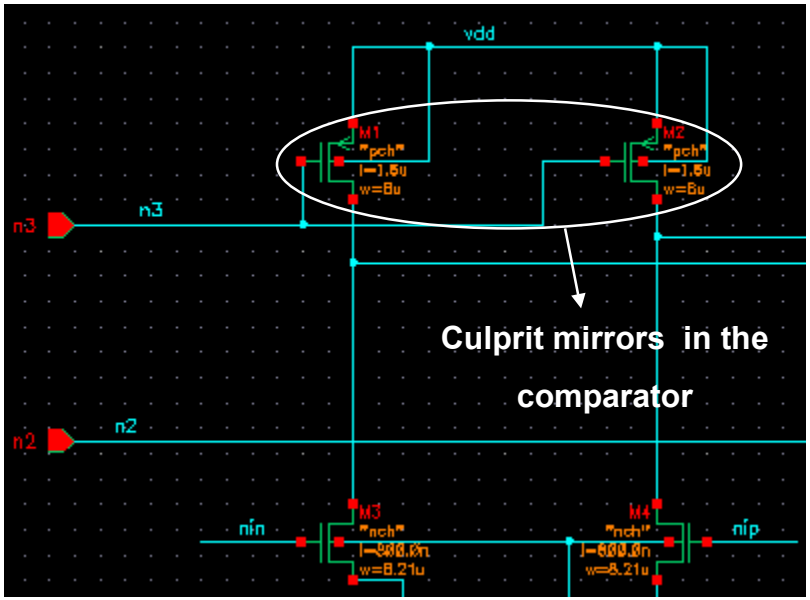
- **Eliminate interface discrepancies between modules**
- **Verify the correlation of digital control and analog events in the IC (especially important for A/D conversion)**
- **Functional *and* magnitude result of a sequence is available**

What was achieved?

- Prototype
  - Functional operation correct, with minor bugs
  - Performance meets spec with one principal concern
    - ADC pedestal variation 10 ADU pk-pk across chip
    - ADC absolute pedestal 60 ADU is too high

- Pre-production
  - Functional operation 100%
  - ADC fixed
    - Pedestal variation <1 ADU pk-pk
    - Pedestal absolute <20 ADU

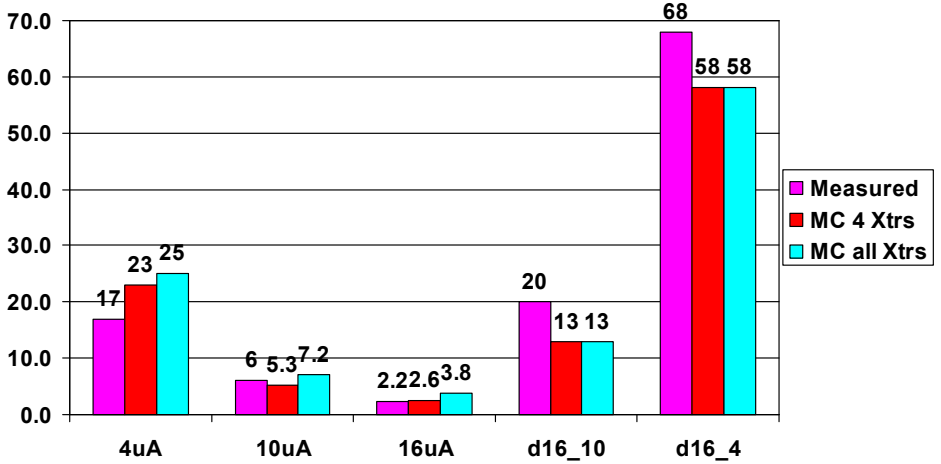
ADC pedestal analysis



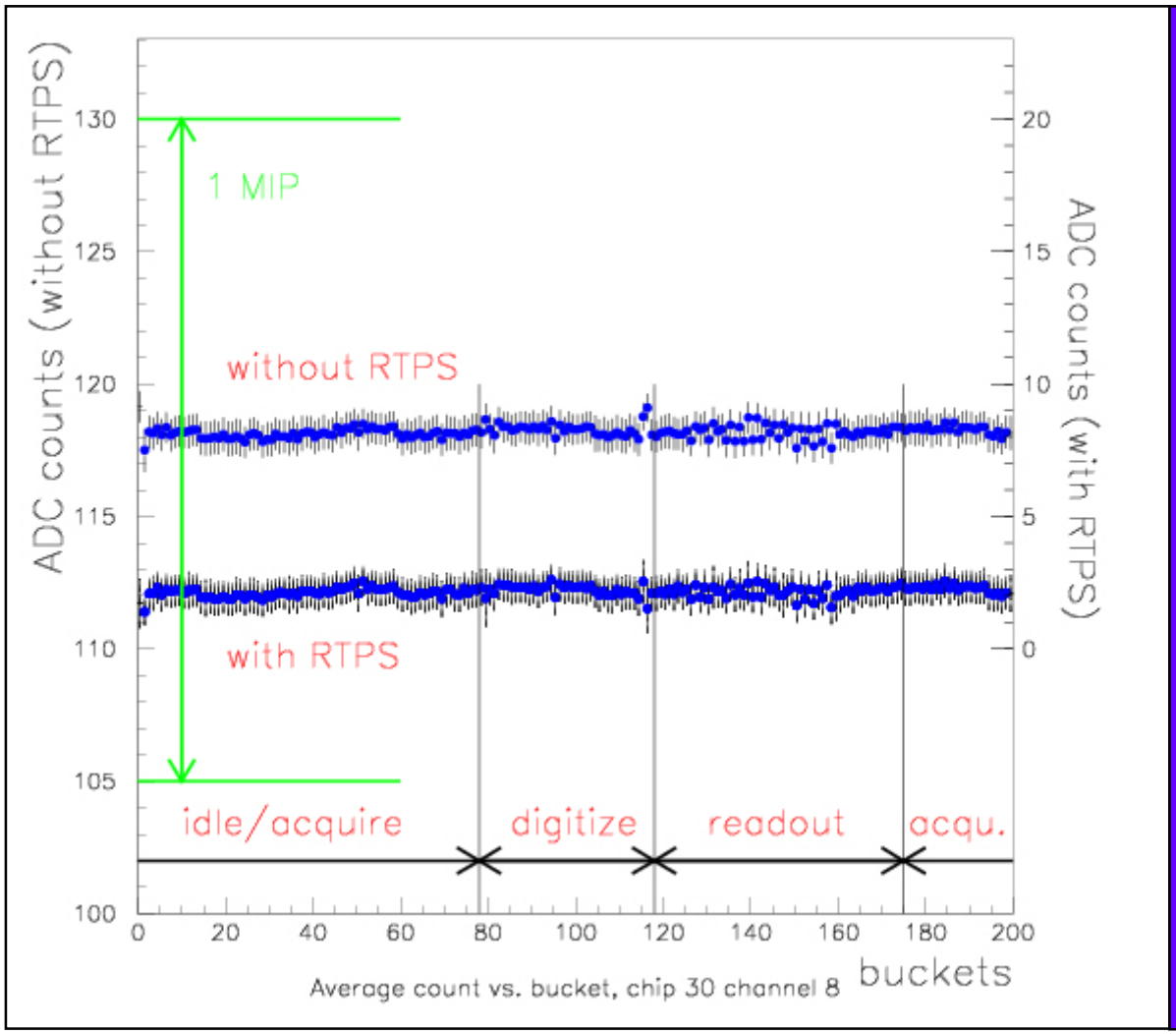
- The pedestal variation was traced to the comparators in the ADC by measurement and simulation of the problem at different bias currents
- Variation of the Vth over the process range revealed current sources which were operating at low (Vgs-Vth), and therefore sensitive to spacial process variation in Vth

- The magnitude of the problem predicted in simulation using monte-carlo analysis matched the measured results
- The new design could therefore be verified using the same tool
- The performance of the new design is as simulated:
  - 2 ADU pk-pk for version 2a
  - 1 ADU pk-pk for version 2b

Ramp-up Pedestal Variation: Measured vs. Monte-Carlo Simulation of Vth Using TSMC Process Data



Dead-timeless operation



- An excellent mixed-signal test
- Depicts the pedestal value for a single channel during various modes of operation
- Horizontal axis is the pipeline cell number, which is overwritten modulo 46
- Blue dots are the average of 200 events in a single pipeline cell during a specific mode, error bar is the RMS
- This is the chip only, no inputs bonded
- The ability of the chip to operate within a couple of counts pedestal variation w/o Real Time Pedestal Subtraction provides a desirable basis for correcting system effects
- Effectiveness for RTPS to operate at a fraction of a count demonstrates its utility

Summary of SVX3 and SVX4

	SVX4	SVX3D
Die size	6.3 x 9 mm	6.3 x 12.3 mm.
Power supply voltage	2.5	5 V
Average power	2 mW/ch	2 mW/ch
Preamp gain	5 mV/fC	5 mV/fC
Dynamic range	60 fC	80 fC
Overall gain (nominal)	0.15 fC/bit	0.15 fC/bit
Digitize speed	> 212 MHz	106 MHz
Readout speed	53 MHz	53 MHz
Acquisition period	132 ns.	132 ns.
ADC INL/DNL/Noise	< 1 LSB	< 1 LSB
Total dose tolerance	> 20 MRad	4 MRad
SEU register tolerance	$< 6 \times 10^{-17}$ cm^2	$< 6\text{x } 10^{-16}$ cm^2
ENC, 30 pF, 4 MRad	1600 e-	2800 e-
Backside ground	< 10 mΩ	< 10 mΩ

Onward and upward—a CDF hybrid …