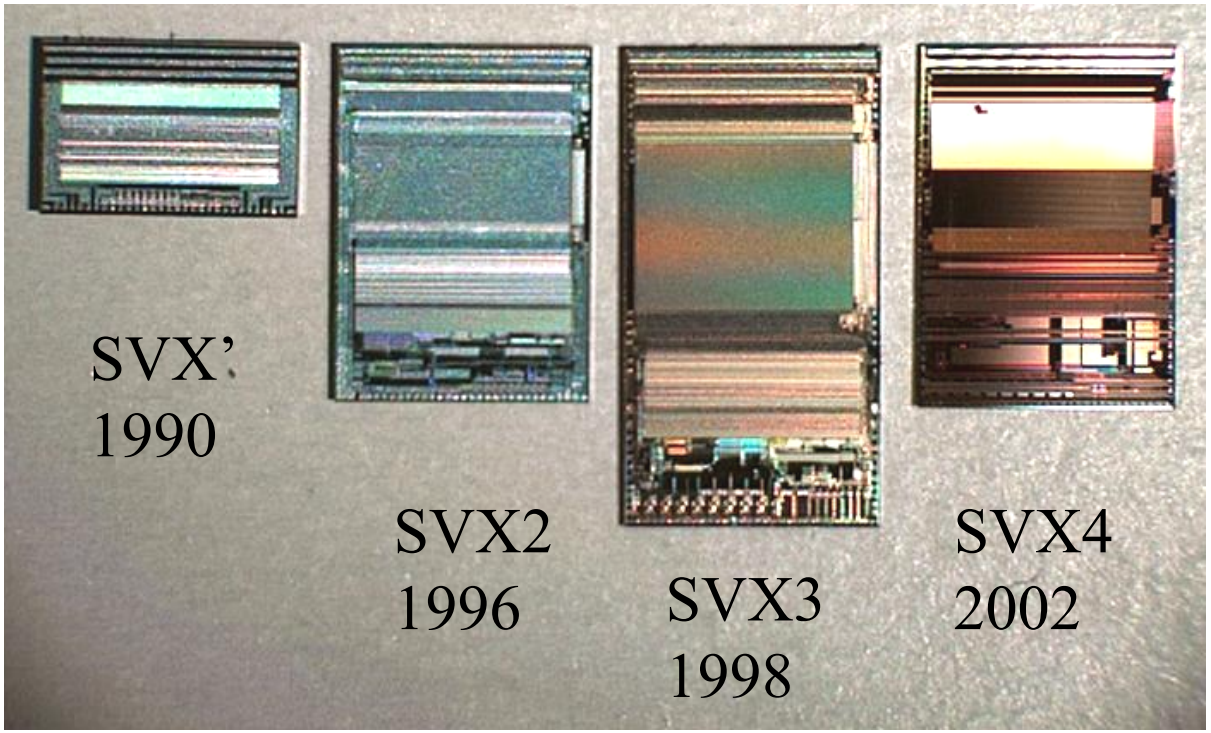
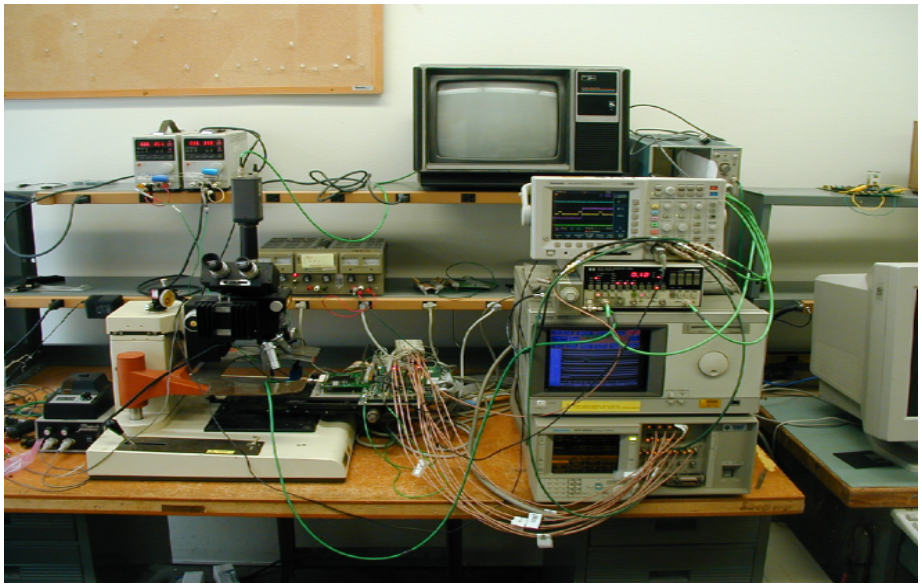
Test Results from the SVX4

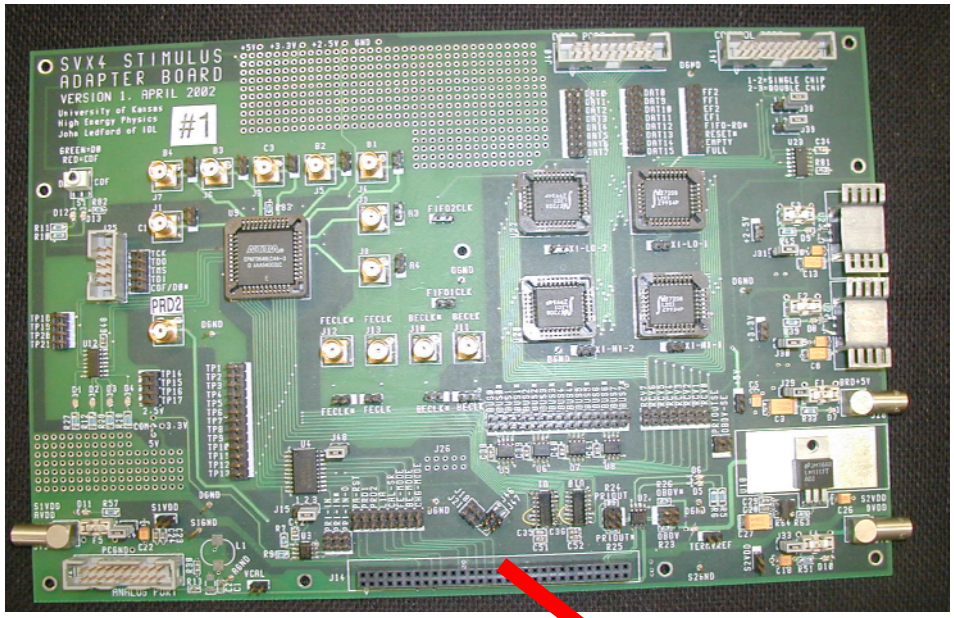


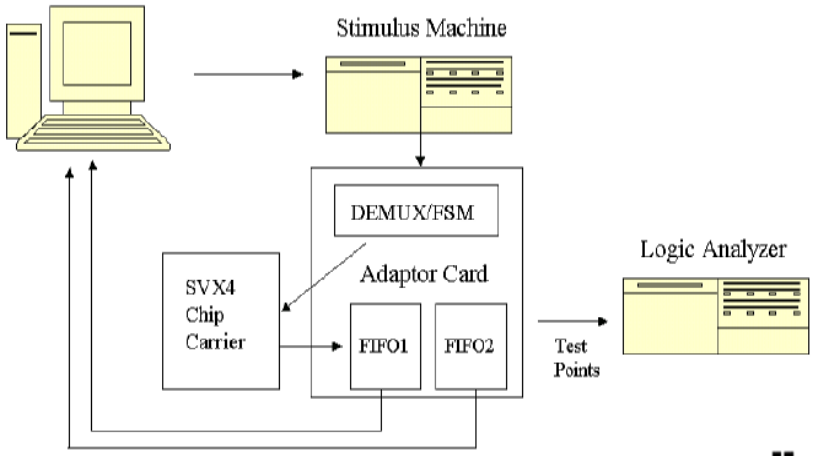
Len Christofek

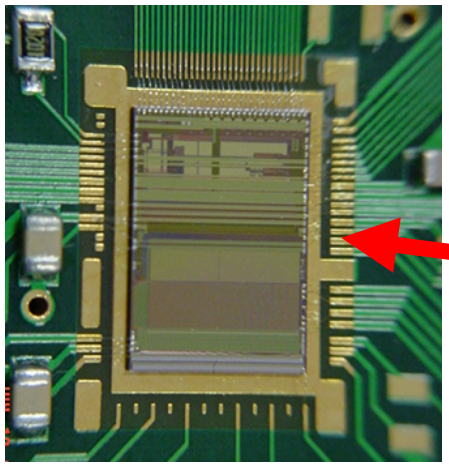
University of Kansas

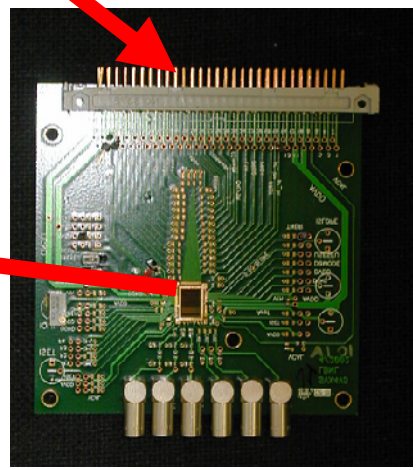
The Stimulus Test Stand





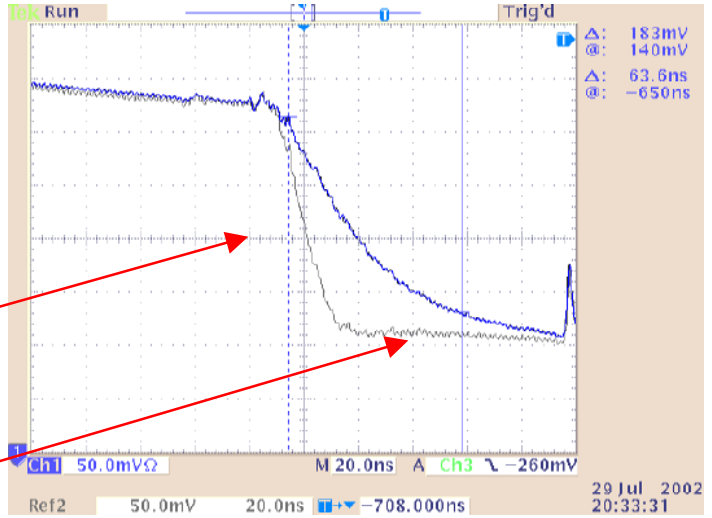




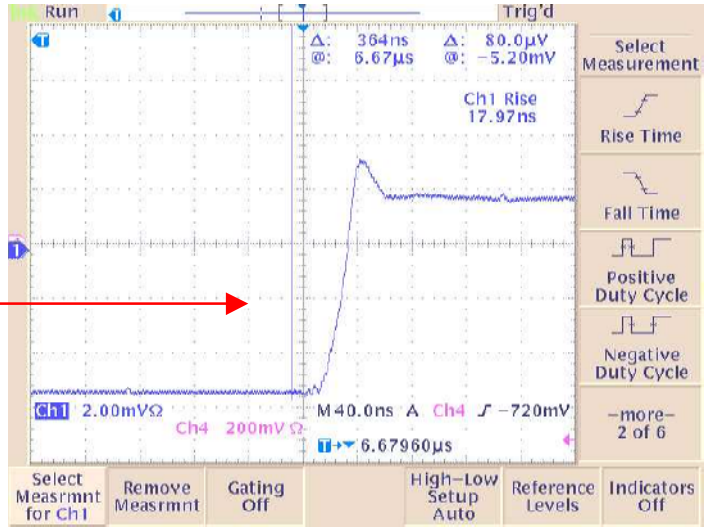


Preamplifier Measurements

- Risetime 0-90%
  - Adjustable in 60-100ns for any load
  - 4 bits allow 15 settings
  - E.g. C = 10 pF
    - 0001 20 ns
    - 0011 32 ns
    - 0111 46 ns
    - 1111 64 ns

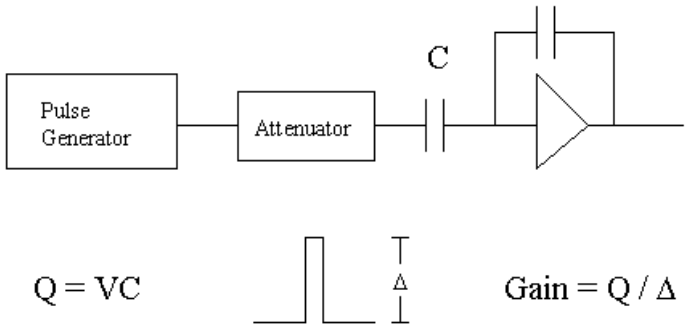


- Reset and Settling Time
  - < 100 ns any condition
  - We measured 20 ns
- Calibration Injection Cap
  - C = 25 fF

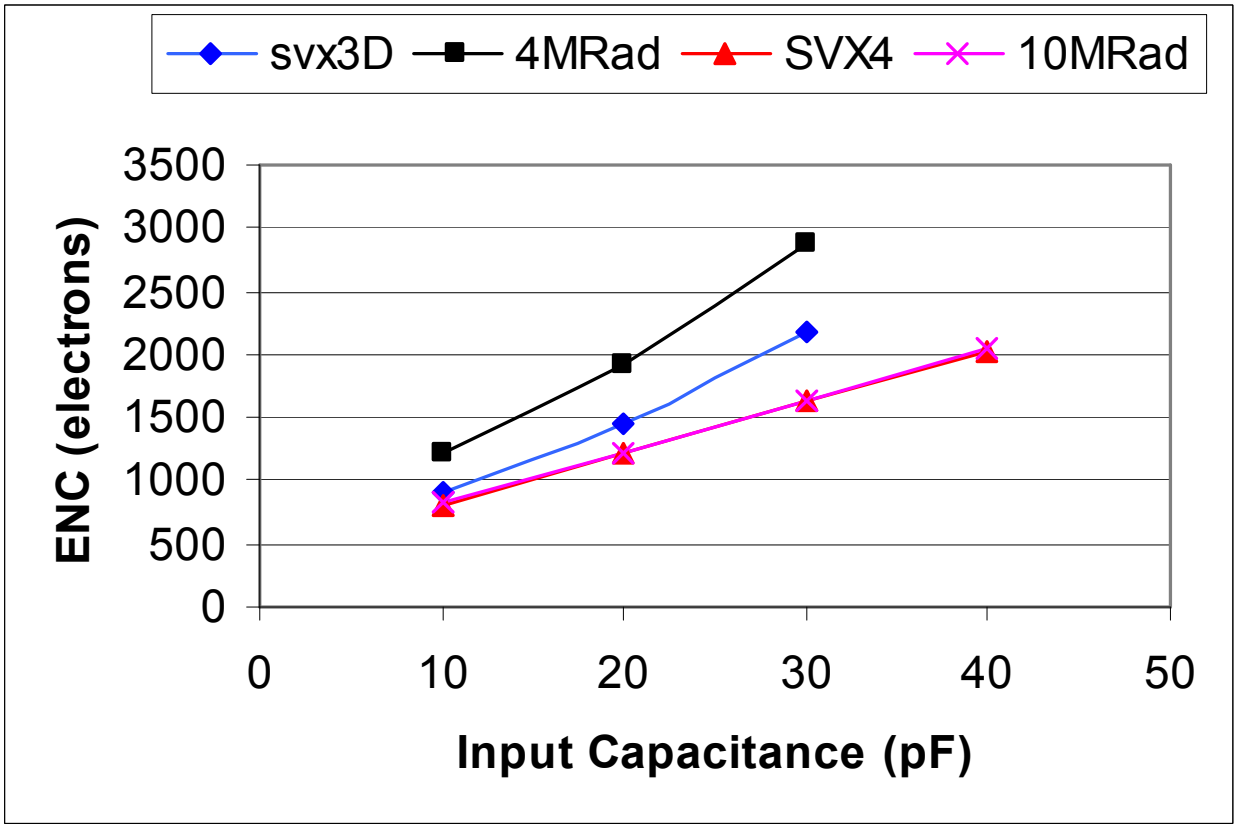


Preamplifier Measurements (cont.)

- Gain
  - 4.4 mV/fC [3.3 mV/fC]
  - Uniformity of < 1%
  - Operates with 10-50 pF load
- Equivalent Noise Charge (ENC)
  - For fixed rise time τ = 69 ns with C=40 pF
    - 2025 e [<2000 e]
    - ENC 🕓 300 + 41 ◈ C [pF]
- Linearity
  - Linear for pulses up 20 fC
- Dynamic Range
  - > 200 fC



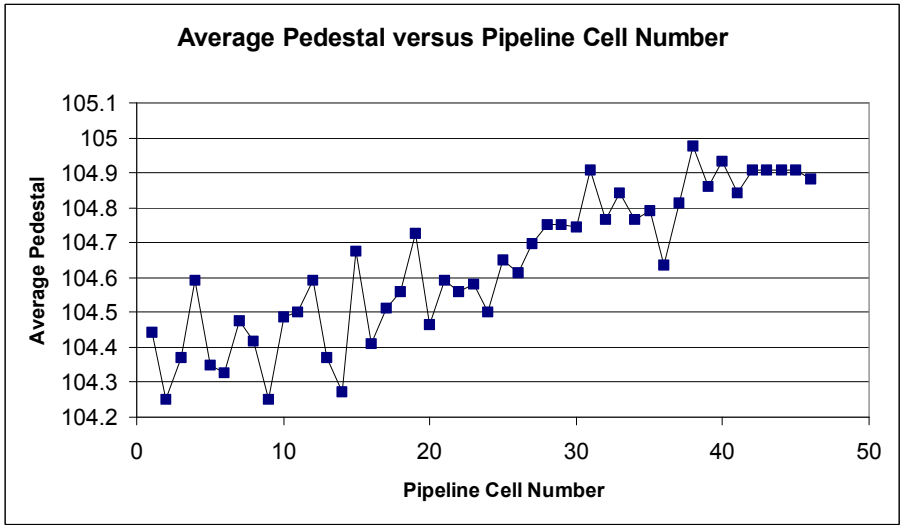
Preamplifier Measurements (cont.)



- 70 ns rise time (0-90%)
- 100 ns integration time (accelerator upgrades for 132 ns collisions, but will probably operate at 396ns)

Pipeline Measurements

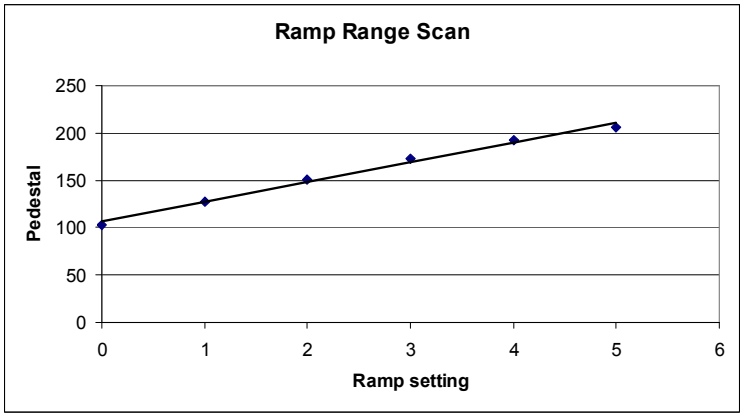
- Gain
  - G = 3.4 [3-5]
  - Uniformity of < 1% channel-channel
- Rise time
  - τ = 10 - 40ns using 0-90%
- ENC
  - < 500 e
- Linearity
  - Linear for pulses up to 20 fC
- Dynamic Range
  - > 40 fC
- Reset time
  - < 20 ns for any condition

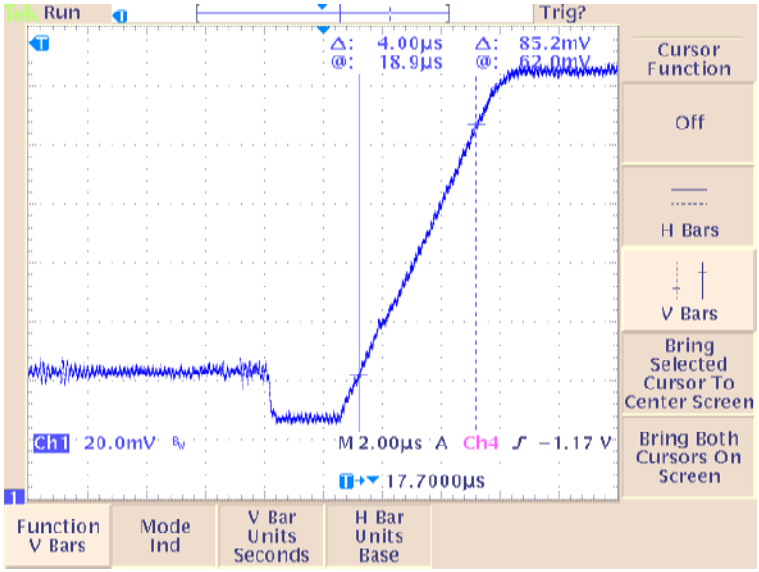


- Pedestal uniformity
  - < 500 e channel-channel
  - < 1000 e cell-cell No!

ADC Measurements

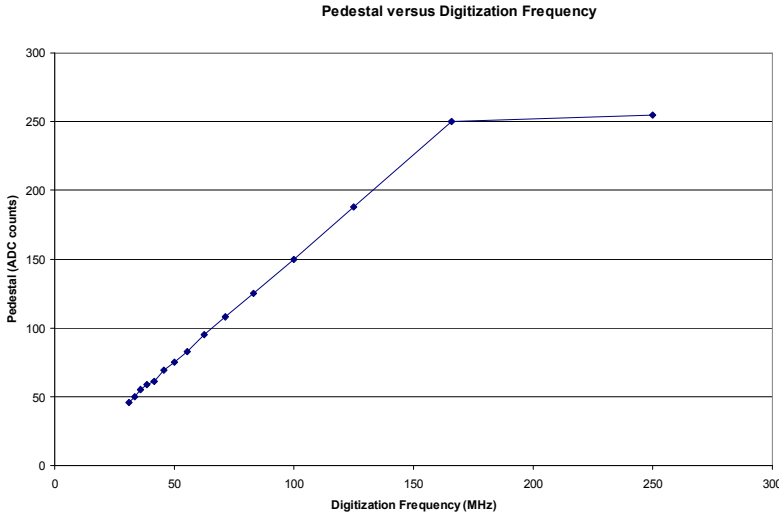
- Ramp Setting
  - 4 bits
  - Uniformity of < 5% channel-channel
- Linearity
  - 0.25% for rates between 0.1-1.0 V/µs
- Digital Counter
  - 255 counts full scale
  - 8 bit Gray code

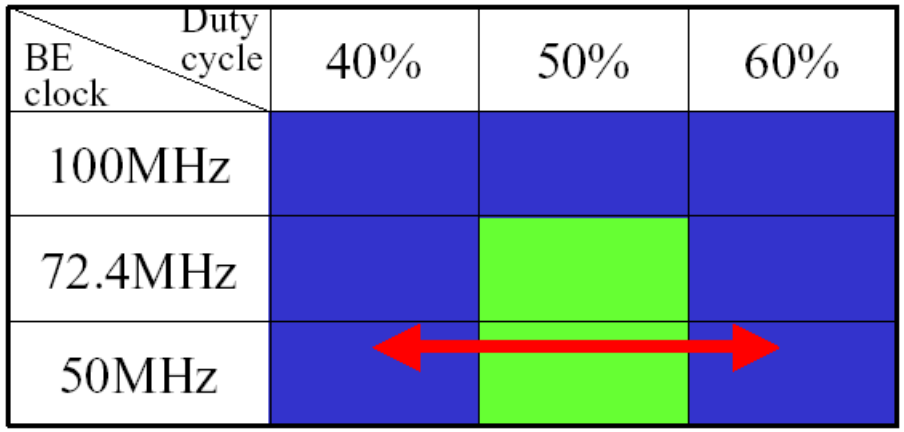




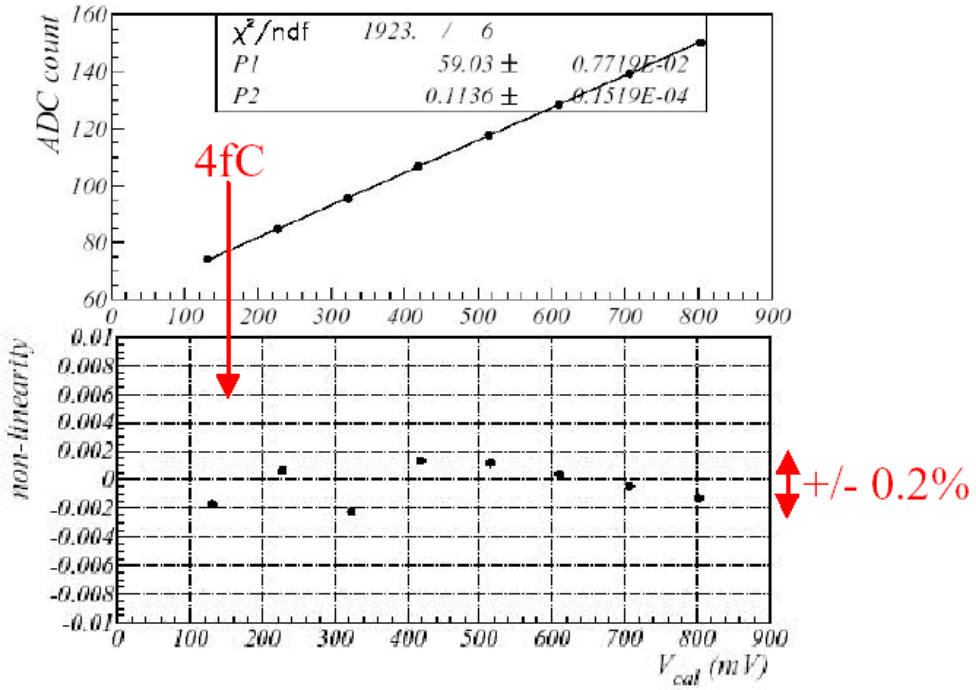
ADC Measurements (cont.)

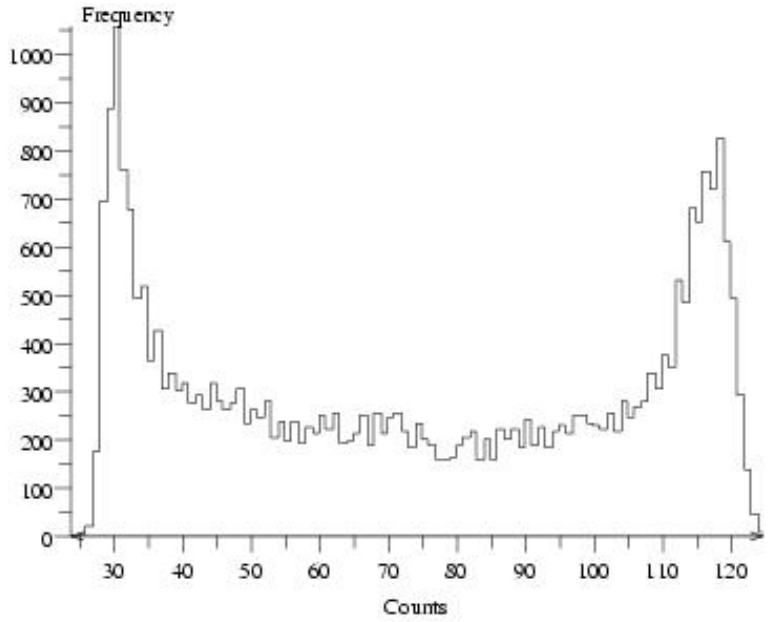
- Digitization
  - Simultaneous for all channels.
  - Clock frequency 53.5 MHz with digitization on both edges, so effectively 107 MHz.
- Data Readout
  - Not related to ADC, but here is the best place discuss it.
  - Clock frequency 26.5 MHz with readout occurring on both clock edges, so effectively 53 MHz.
- Frequency Margins
  - Design 40/60 duty cycle, 20% frequency margin for experiments.
  - Never failed!





ADC Measurements (cont.)





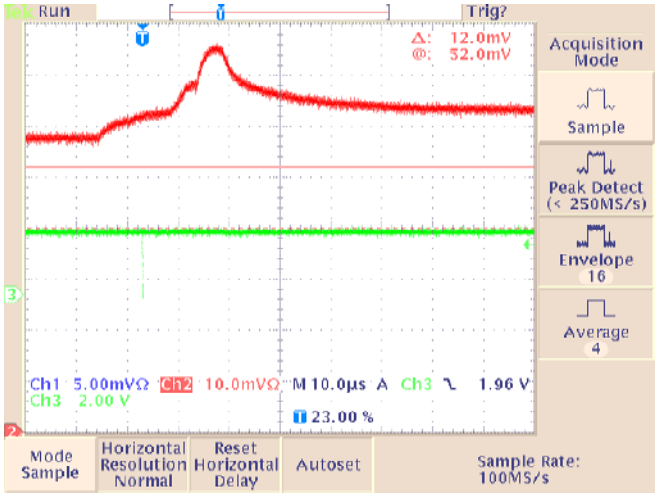
- Integral Linearity
  - Up to 2.5 V * 25 fF
  - < 0.2% deviation
- Differential Nonlinearity
  - Even-odd effect
  - ~ 5% [0.5 LSB]
  - Used sine wave (f=1 kHz)

Other Measurements

- Current consumption
  - I_{max} = 126 mA (1 event cycle)
- Data Output Drivers
  - Rise time 2ns < ♦ < 4ns
  - Bidirectional or Single Ended

Bit	Measured	Design
001	5.6 mA	5.6 mA
010	9.4 mA	9.2 mA
100	13.2 mA	13.4 mA

- ESD tolerant
  - Preamplifier input (5000V)
  - Control and data lines (6000V)



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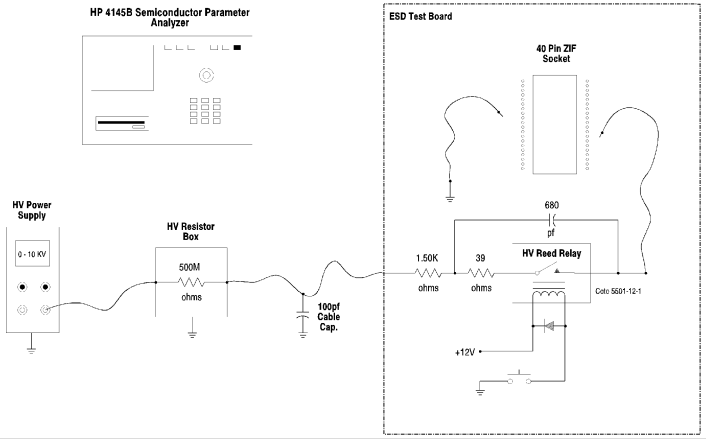
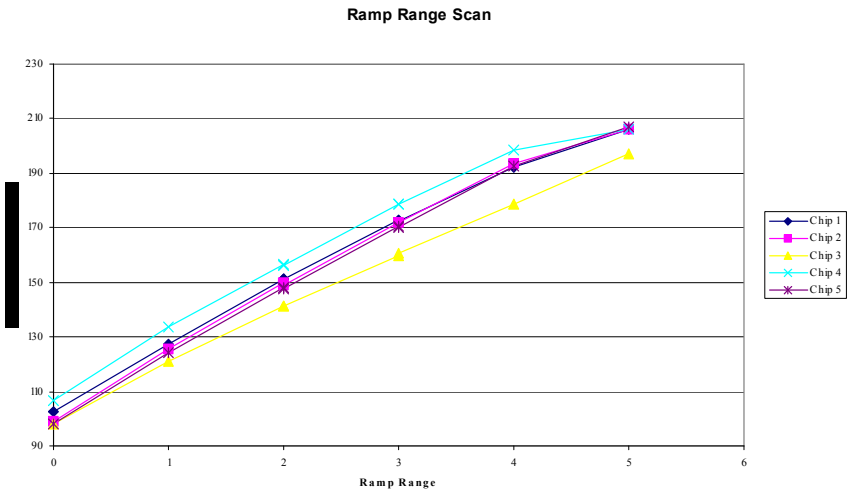
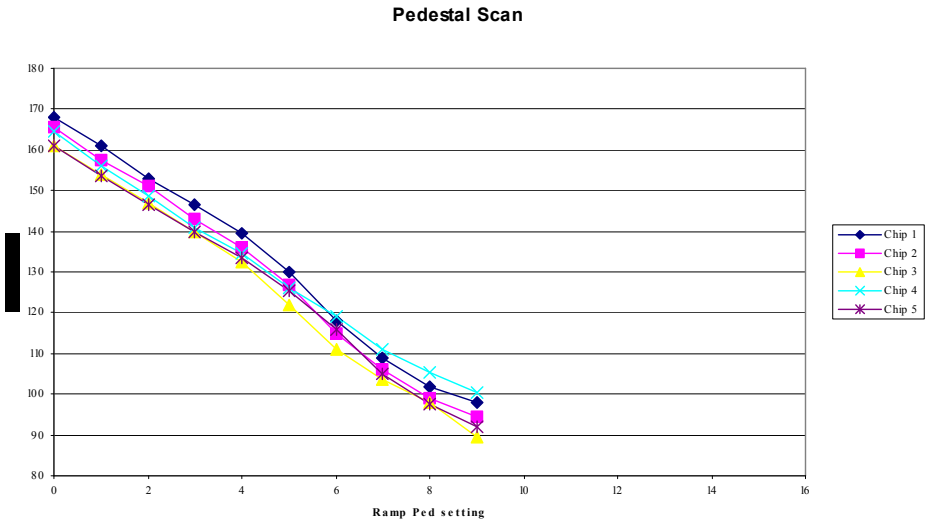
ESD Test Setup Schematic



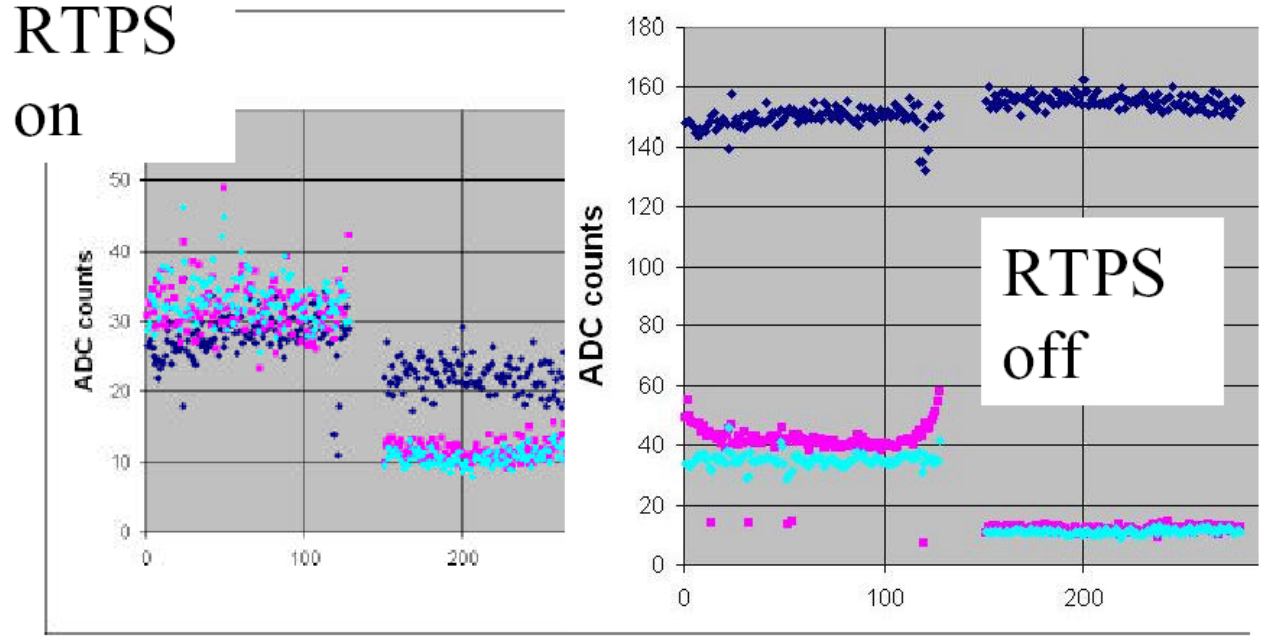
Chip to Chip Variations

- We looked at several different chips in order to measure the variations.
- We used the ramp and pedestal settings from chip to chip to give us an idea of the variation.
- We observed a 7.5% difference from chip to chip in ramp settings and a 11% difference in pedestal settings (some of this variation is coming from the pedestal nonuniformity – see slide 14).





Dynamical Pedestal Subtraction

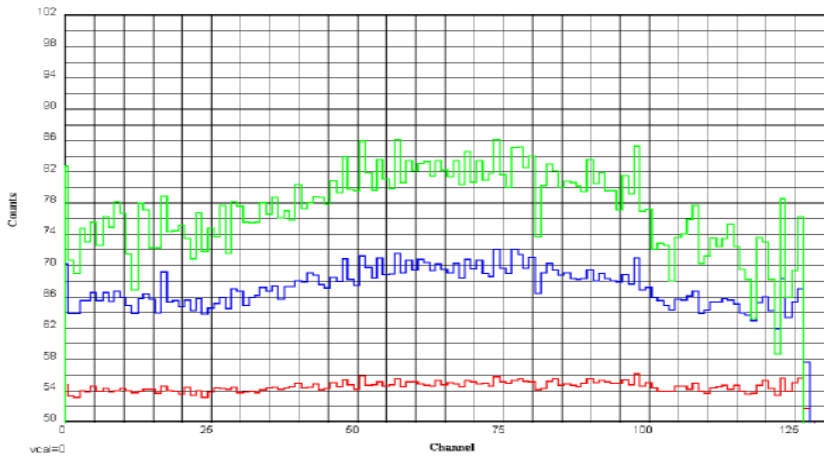


- Dynamical Pedestal Subtraction (DPS) or Real Time Pedestal Subtraction (RTPS): long names for on chip common mode subtraction algorithm.
- A democratic vote from all channels when to begin the counter
- Data above from a 2-chip D hybrid (only first chip wirebonded to sensor)
  - **Dark Blue – pedestals**
  - **Pink – raw noise 10**
  - **Light Blue – common mode subtracted noise 10**

SEU and Radiation Hardness

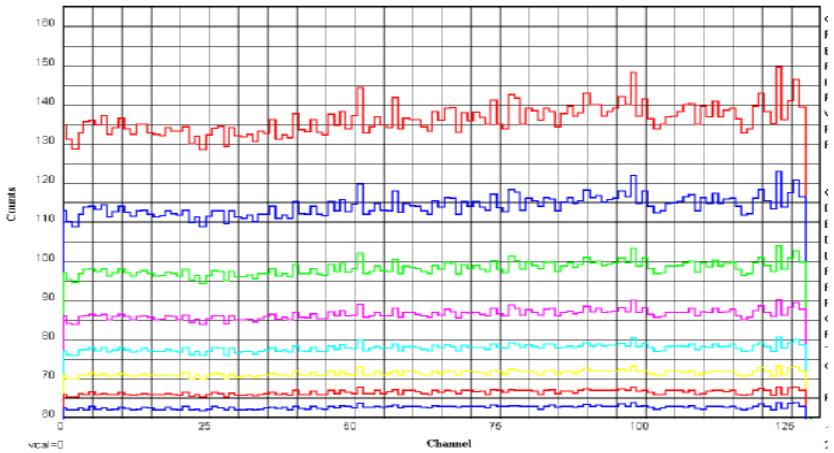
- New design of registers that hold operating information for chip
  - How did we detect an SEU?
    - Establish a pedestal above counter modulo.
    - Read the chip out continually until data readout does not equal counter modulo
    - One of the bits flipped in this field
    - Same procedure with chip id: set the chip id to 128, if at any time it changes in the readout a SEU has occurred.
- SEU test with 63 MeV protons. Total fluences = 14E14
  - SEU cross section 2.2E-17 to 1.6E-16 cm^2 @95%CL
  - Integrated dose of 19 Mrad, no change in performance.
- Co-60 irradiation of CDF
  - Survived 16-18 Mrad, no change in analog performance.
- D hybrid irradiation at KSU by 16 MeV protons
  - Survived 25 Mrad, no change is performance.

Performance Issues



Less bias

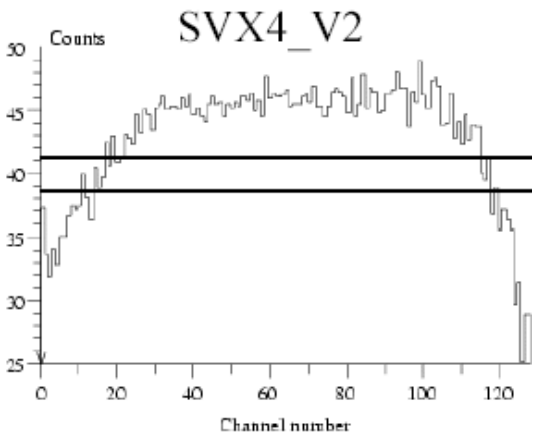
More bias

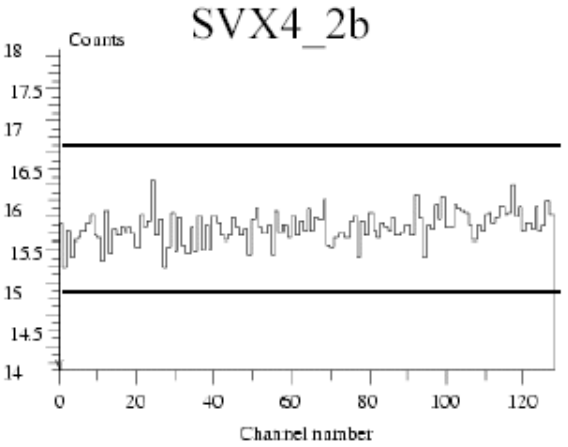


- Certain operating conditions give a nonuniformity in the pedestal distribution
  - Long comparator delays (slew times) with small variations at the transistor level from channel to channel produces this result
  - This has been verified “on the bench” by extending the time between the comparators become active and when digitization begins and also in simulation

Pre-production Chips

- Since all effects were reproduced by the designers in simulation, a 2 version approach was taken in the preproduction submission
  - Version A: Fall back solution (increase the biasing inside chip with out altering anything).
  - Version B: Aggressively redesign the ADC to improve the biasing scheme and to speed up the comparators making it less sensitive to slight variations between transistors.
- Lastest submission a success and preproduction chips are production quality.





Conclusions

- The SVX4 is a success with excellent performance.
- The SVX4 has a low SEU cross section and is rad hard. It will survive the Run IIb Tevatron luminosities.
- DPS or common mode subtraction algorithm works well.
- Latest results from recent preproduction run show no nonuniformity in the pedestals and smaller channel to channel scatter.
- Production should begin at the beginning of this fall.