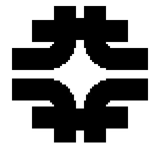


SEU Tolerance of Different Register Architectures in a 0.25μm CMOS Process

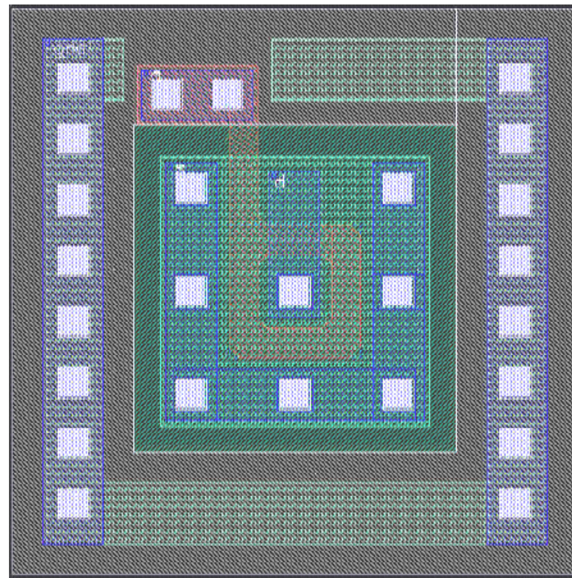
Jim Hoff[(a)], William Wester[(a)], Brad Hall[(a)], Paul Rubinov[(a)], Suen Hou[(b)], P.K. Treng[(b)]

(a) Fermilab, P.O. Box 500, Batavia, IL
(b) Institute of Physics, Academia Sinica, Taipei, Taiwan

Fermilab

Focus – head-to-head comparisons

- Commercial 0.25um process (TSMC)
- Only Total Dose Tolerant designs
  - Enclosed Geometry FETs

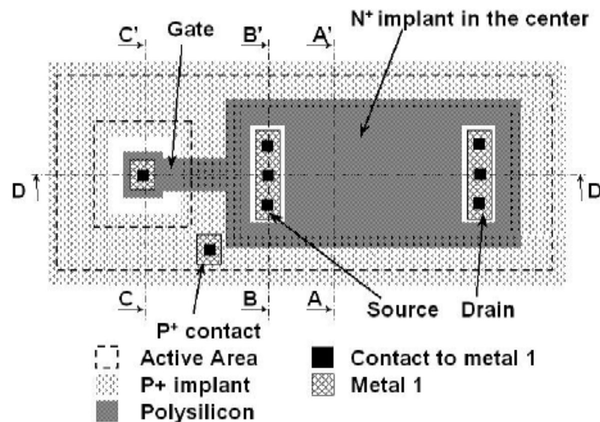


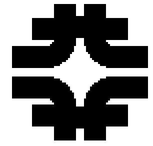
- Limited transistor W/L ratios
- Minimum W/L ratio
- "Weak" transistors difficult to make

Fermilab

Focus – head-to-head comparisons

- Commercial 0.25um process (TSMC)
- Only Total Dose Tolerant designs
  - –Enclosed Geometry FETs
  - –Unsuccessful use of MoRT Transistors (IEEE Trans. Nucl Sci, Vol 49, No 4, p. 1829 (2002))





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  - Unsuccessful use of MoRT Transistors (IEEE Trans. Nucl Sci, Vol 49, No 4, p. 1829 (2002))
  - Excludes Liu Cell (IEEE Trans. Nucl Sci, Vol 39, No 6, p. 1670 (1992))
  - Introduces a new Fermilab-developed, SEU-tolerant cell

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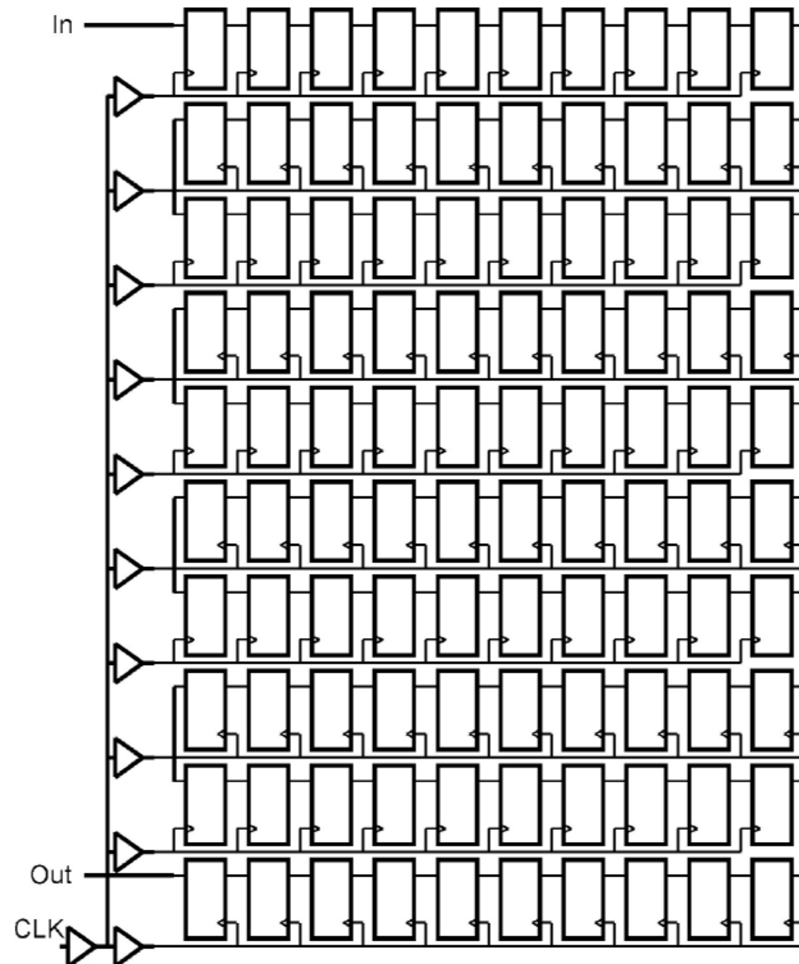
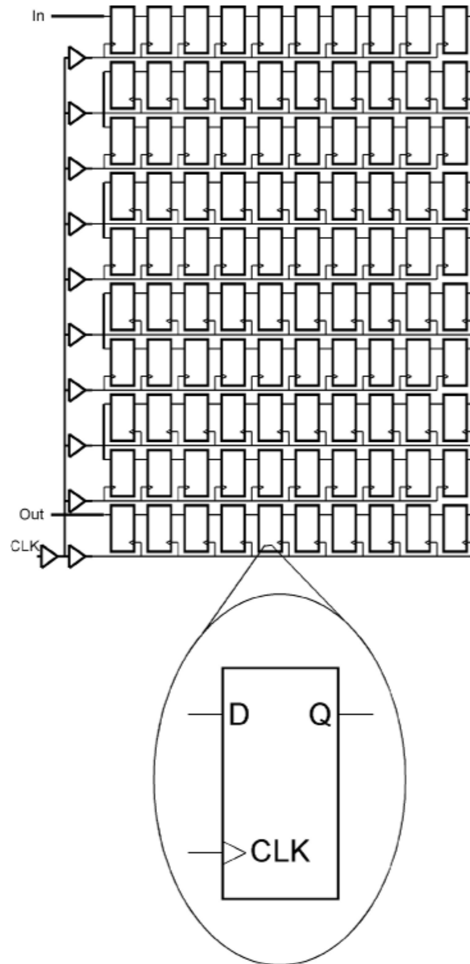
Consistency



- Each register type is arranged into a 1x100 shift register

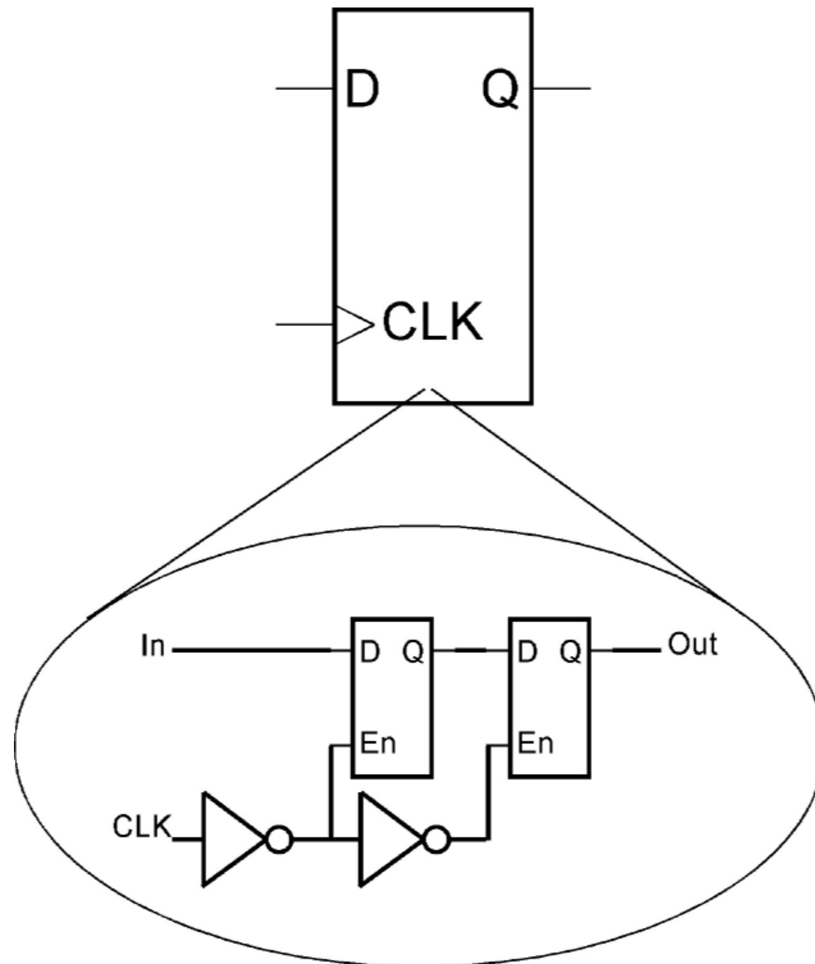
Fermilab

Consistency



- Each register type is arranged into a 1x100 shift register
- Each register is a positive-edge-triggered D-ff

Consistency



- Each register type is arranged into a 1x100 shift register
- Each register is a positive-edge-triggered D-ff
- Each D-ff consists of master and slave latches enabled by Clk signals generated internally.

Fermilab

Registers Tested

- A Normal flip-flop
- The Hit Cell by Velazco, Bessot, et al
- The Dice Cell by Calin, Nicolaidis, et al
- The Seuss Cell developed at Fermilab
  - Laid out in two different ways
- The TRed Cell, a triply-redundant extrapolation of the Seuss Cell

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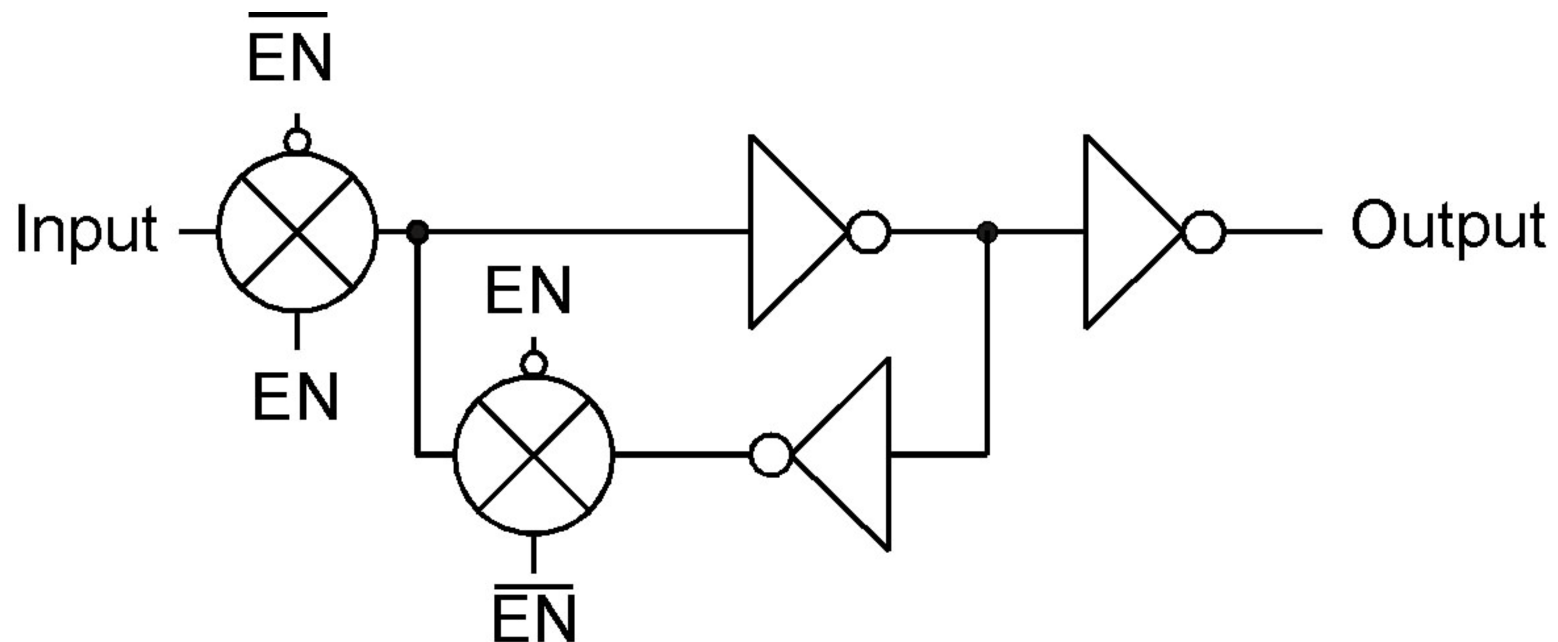
The “Normal” Register



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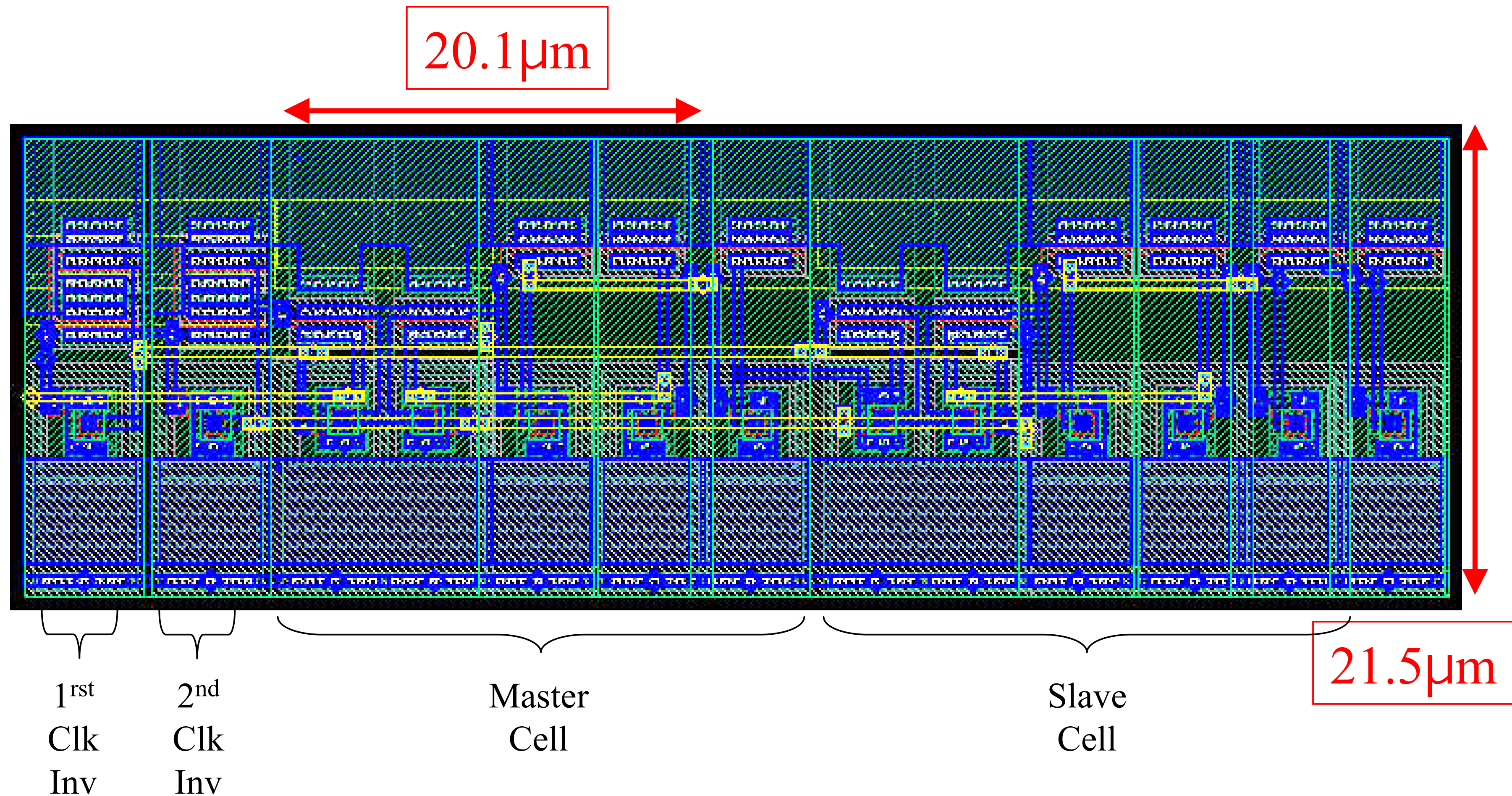
The "Normal" Register



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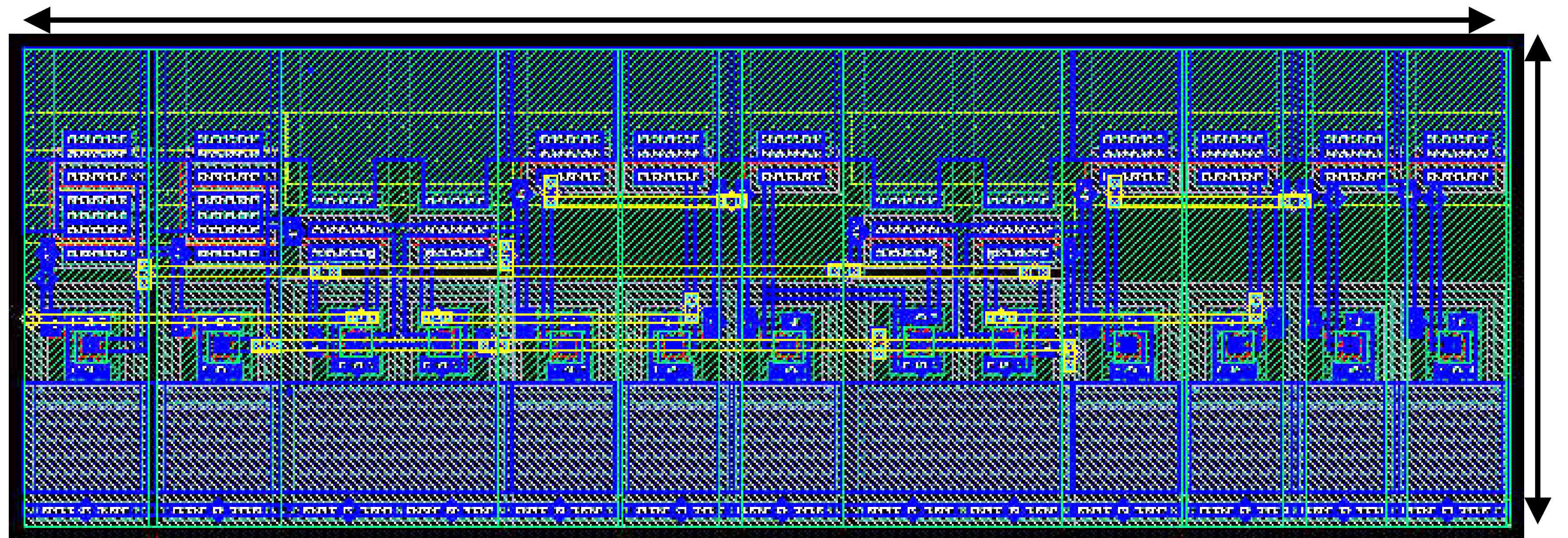
The "Normal" Register



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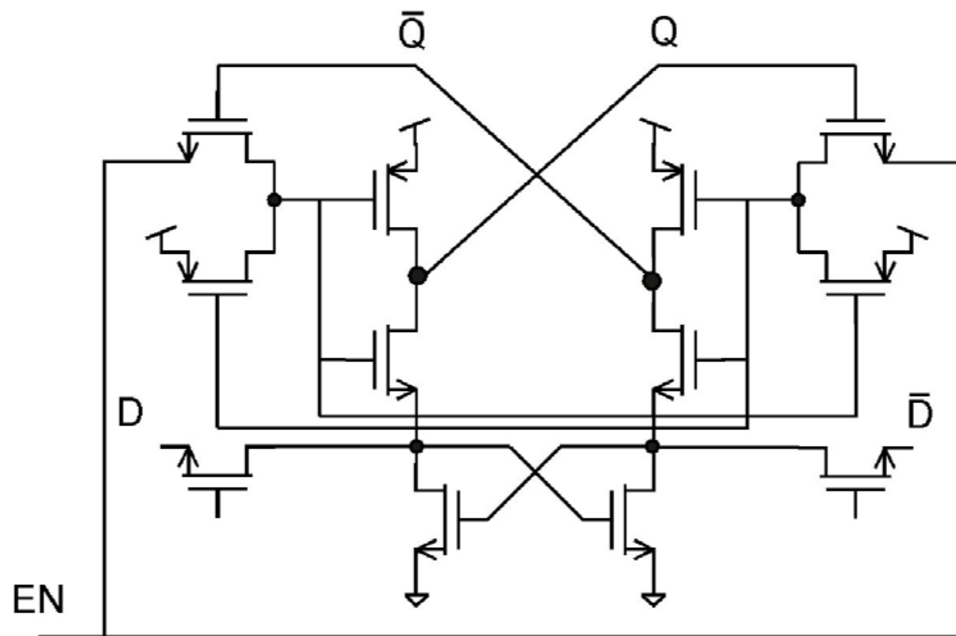
The Hit Cell

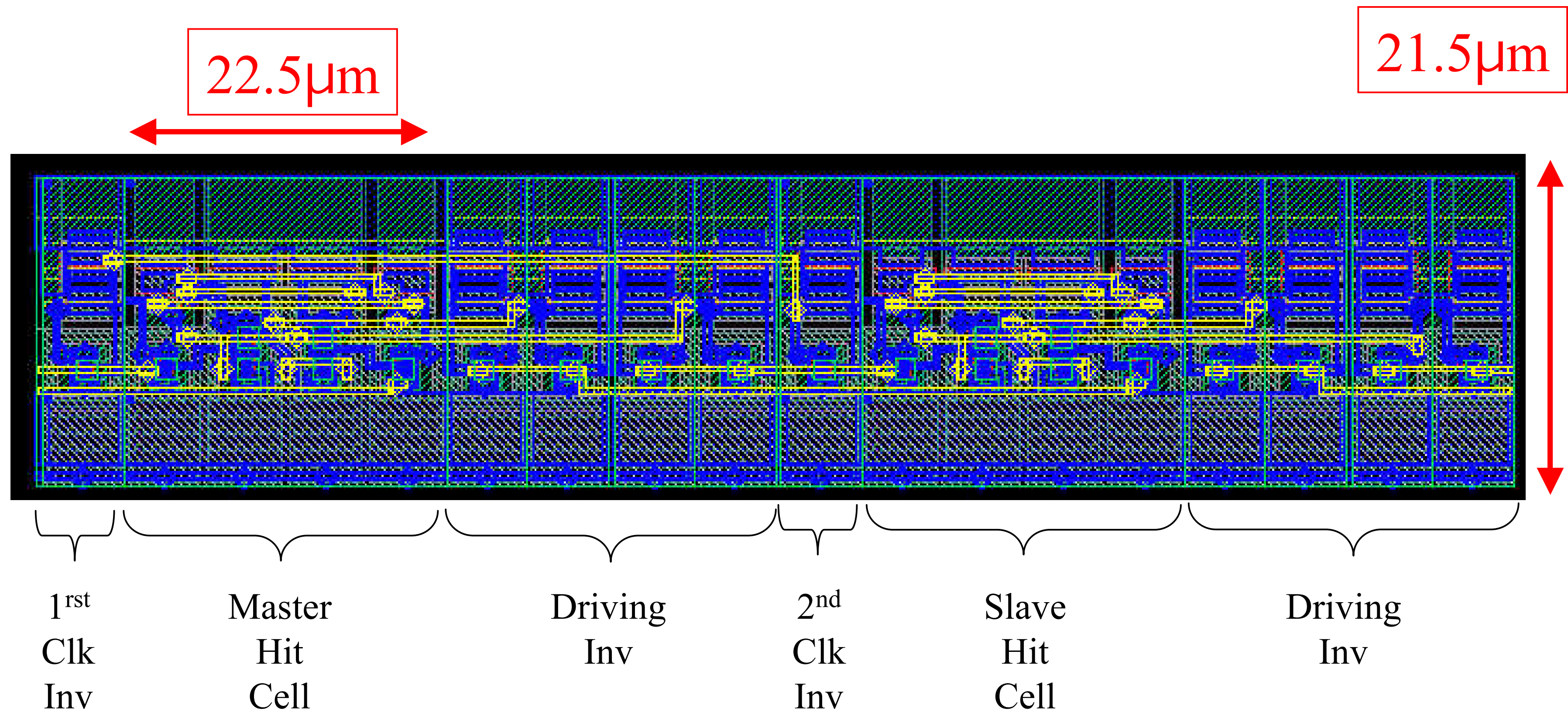


•Hit or "Heavy Ion Tolerant" Cell

•D. Bessot, R. Velazco, "Design of SEU-Hardened CMOS Memory Cell", RADECS '93, p. 563, 1993 INSPEC 4744705

•R. Velazco, *et al.*, "Two CMOS Memory ells Suitable for the Design of SEU-Tolerant VLSI Circuits", IEEE Trans. Nucl. Sci. Vol. 41, No. 6, p. 2229, 1994

The Hit Cell



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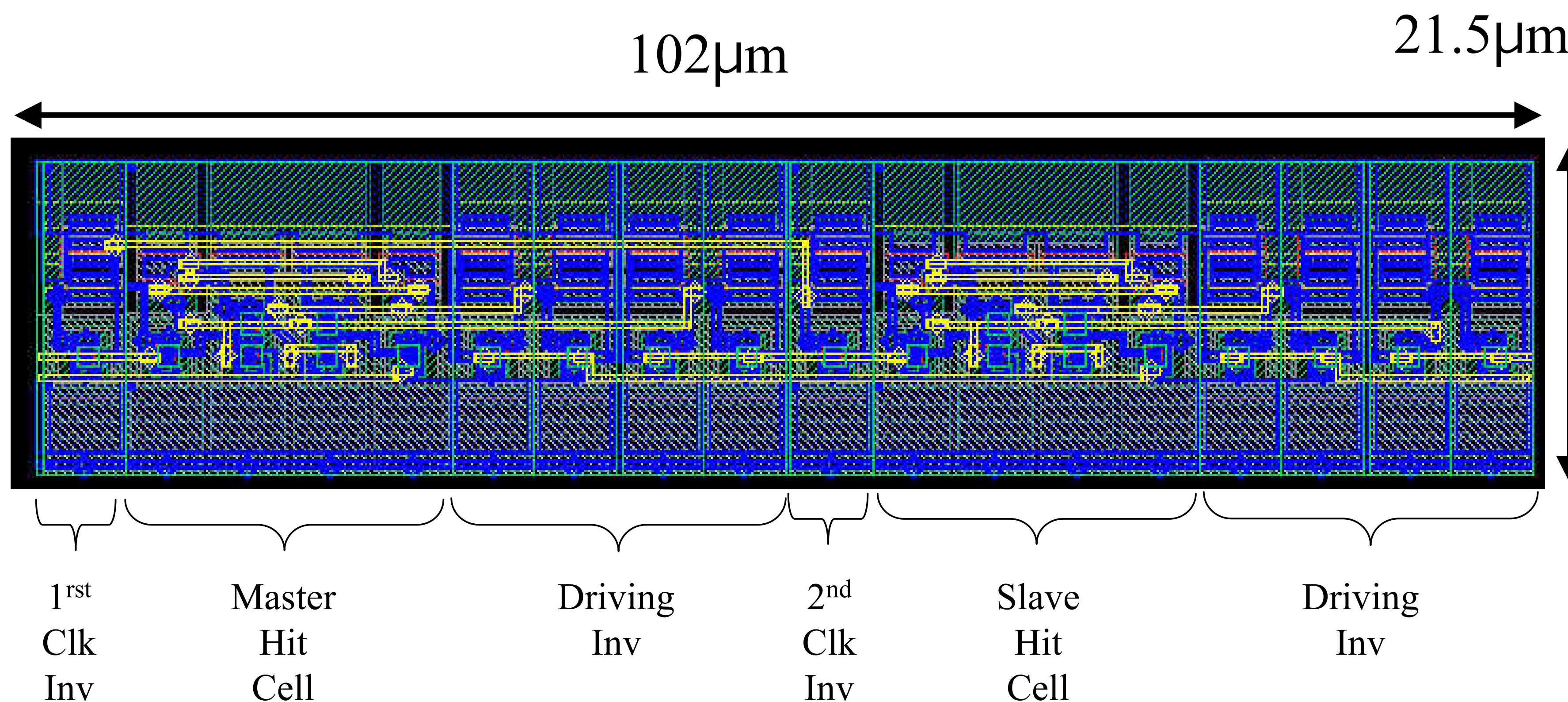
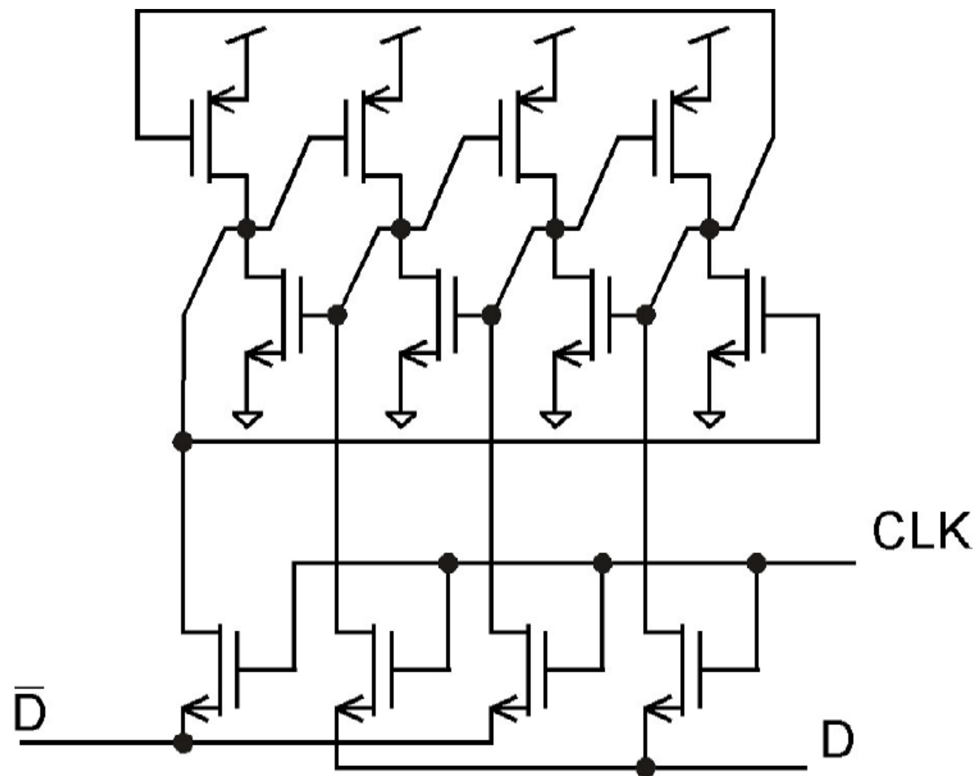
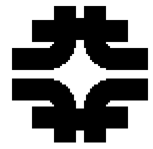
The Hit Cell



The DICE Cell



- DICE or Dual Interlocked Storage Cell
- T. Calin, M. Nicolaidis, R. Velazco, IEEE Tran. Nucl. Sci. Vol 43, No. 6, p. 2874 (1996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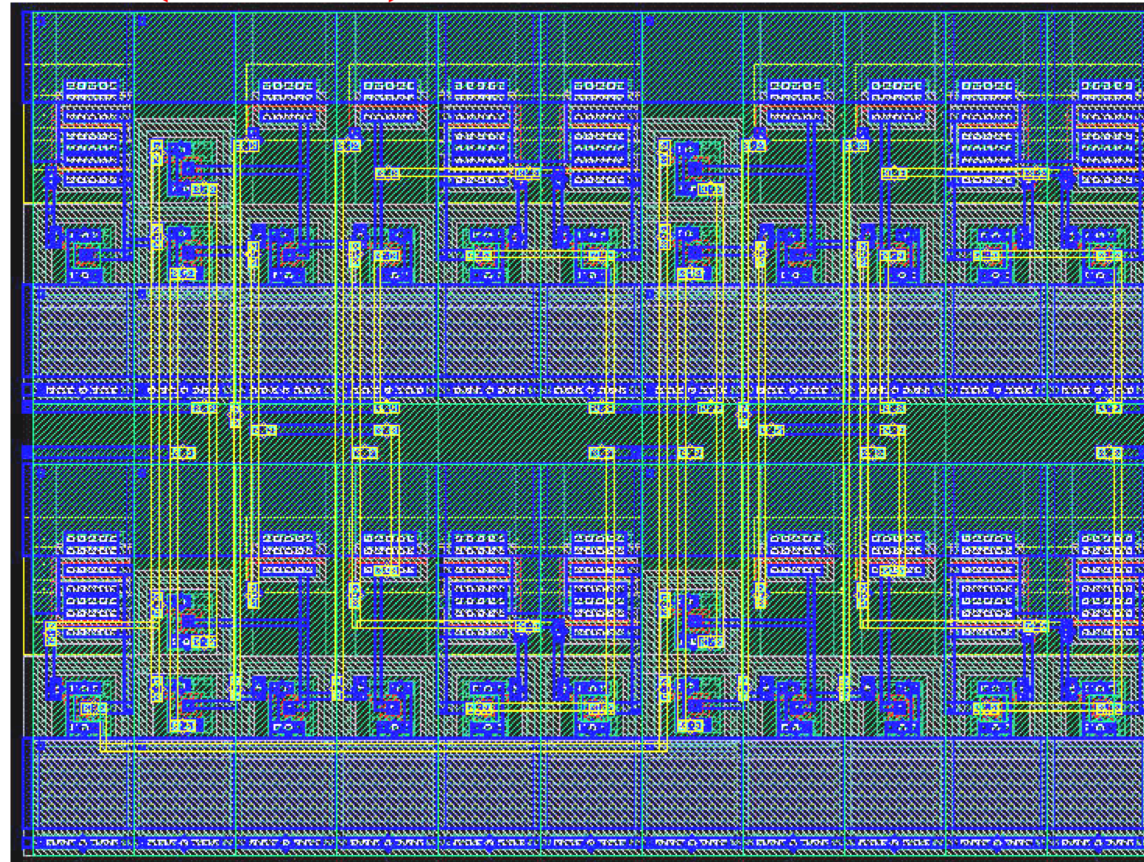
The DICE Cell



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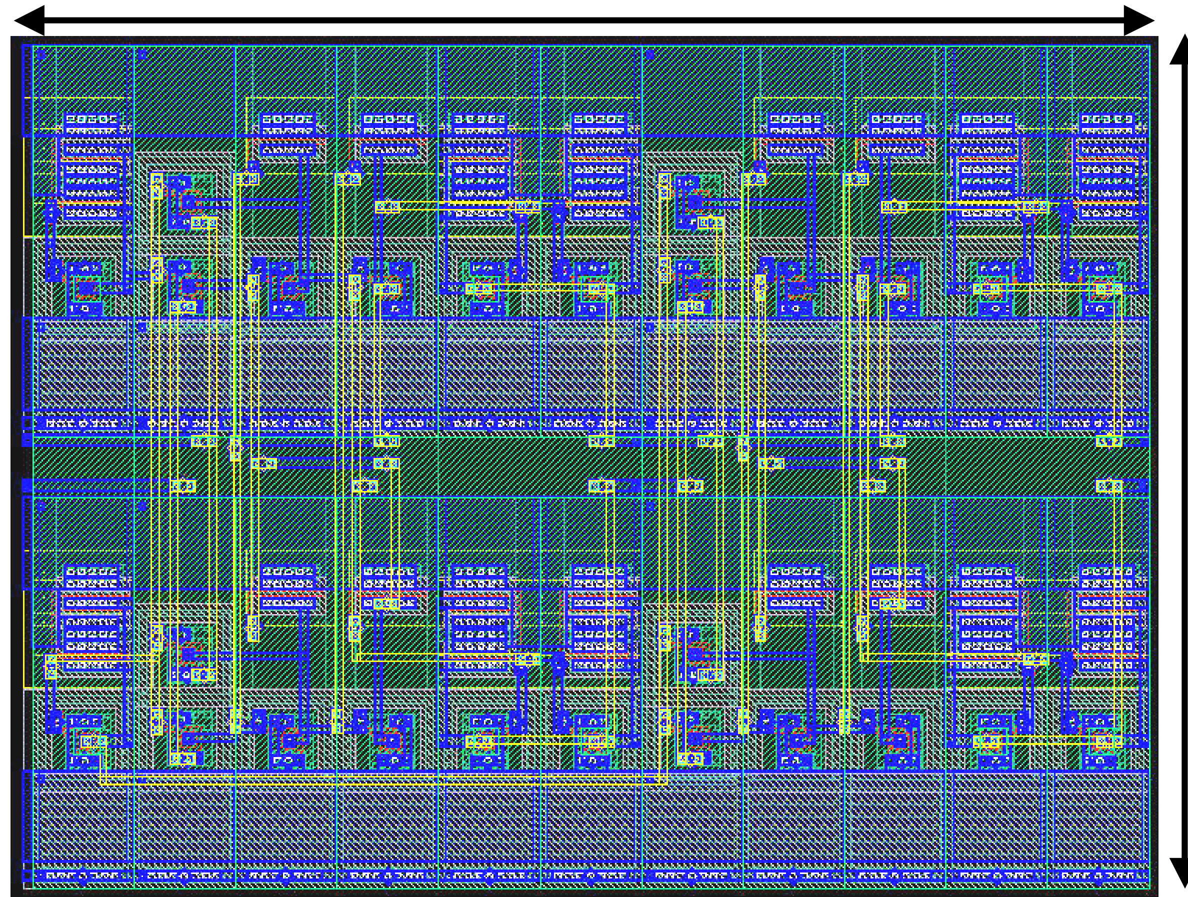
The DICE Cell

61.5μm



46.5μm

1rst Clk Inv

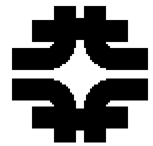
2nd Clk Inv

Master DICE Cell

Driving Inv

Slave DICE Cell

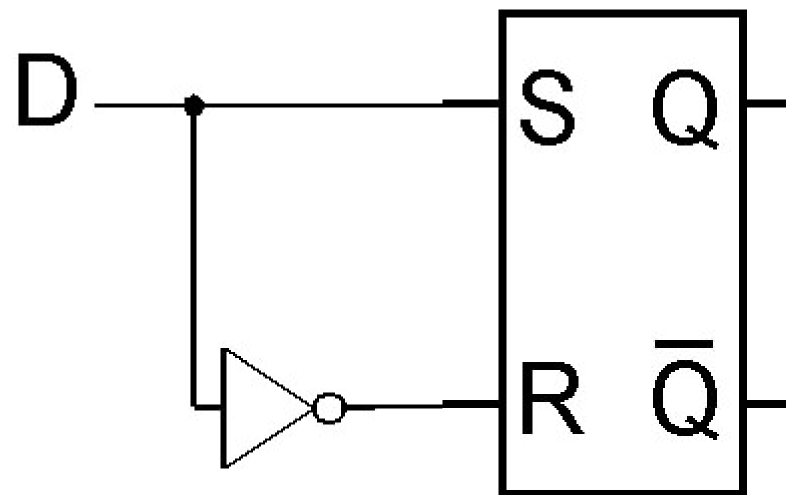
Driving Inv



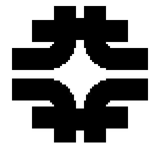
The Seuss Cell

- Reduce power consumption
- Have inputs drive gates not sources and drains.
  - Eliminate need for “weak” transistors
  - Eliminate “back-drive”
- Increase design flexibility without compromising SEU tolerance
- Use minimum size transistors; Eliminate the need to scale and redesign every time we change processes
- End Result – An SEU tolerant SR-flip-flop

Seuss Benefits - Flexibility



- The S-R flip-flop is the fundamental Building block of sequential logic.
- You can build anything with it.



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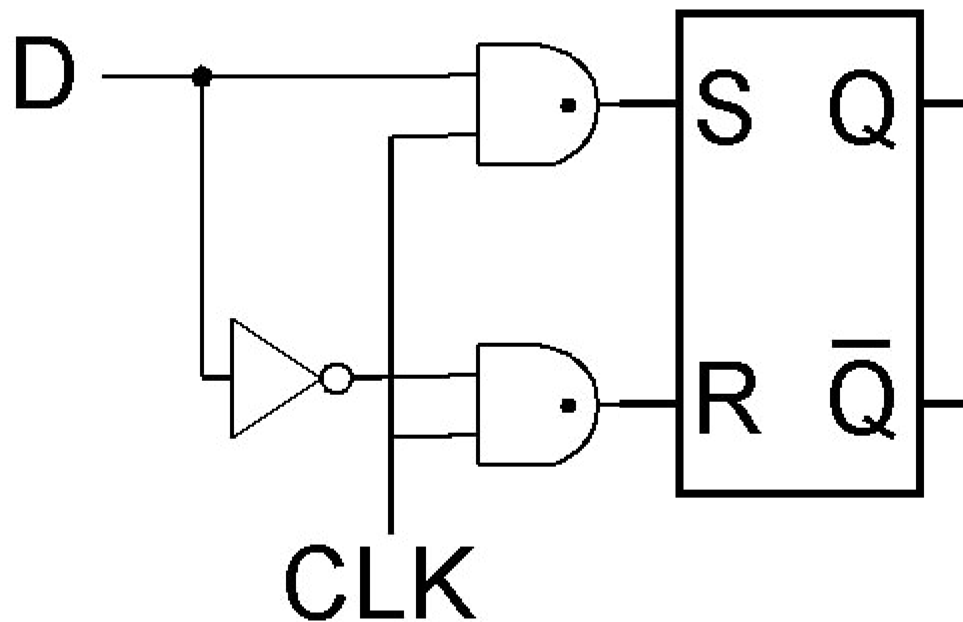

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Fermilab

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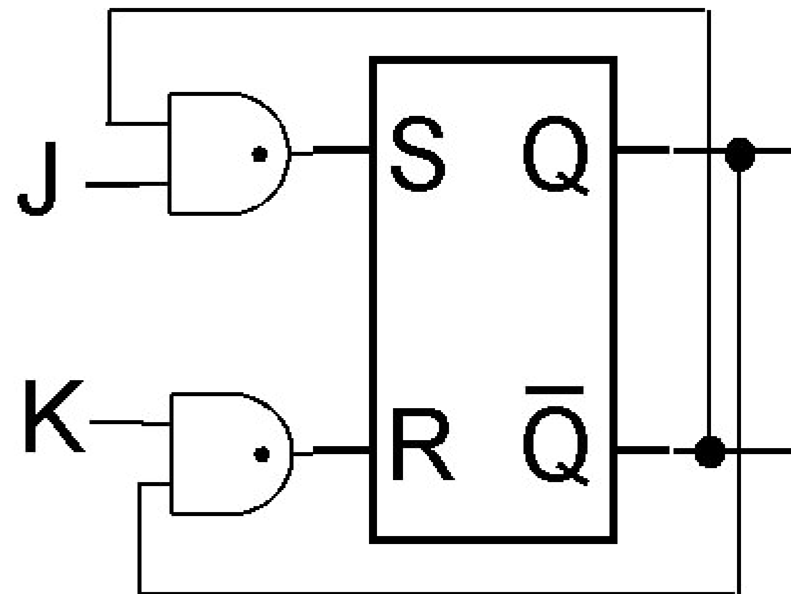

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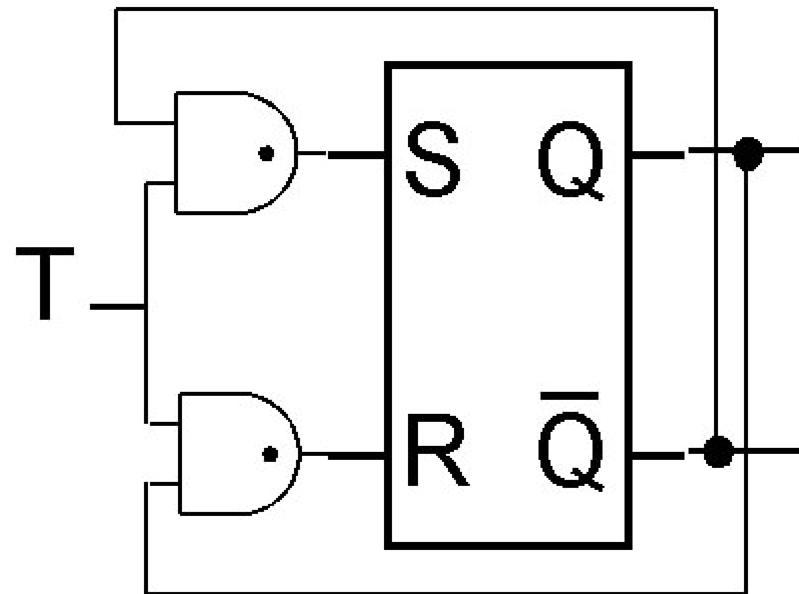

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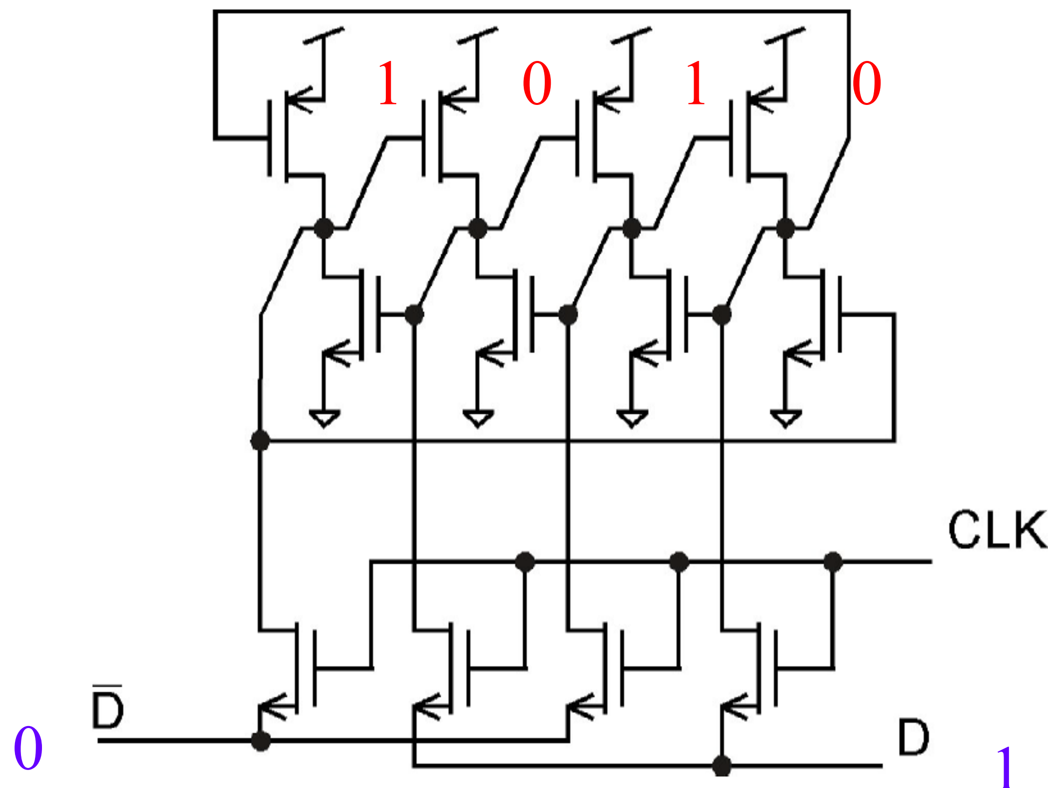
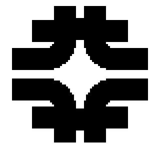
Seuss Benefits – Dynamic Power



- Does the input have enough drive capacity to change the state?
- How much power will be consumed while the cell is changing state?
- Transistor sizing compromises

Seuss Benefits – Dynamic Power

•Regardless of the direction of state change, and regardless of the size of the input drivers and regardless of the size of the SEUSS transistors, the state change is guaranteed.



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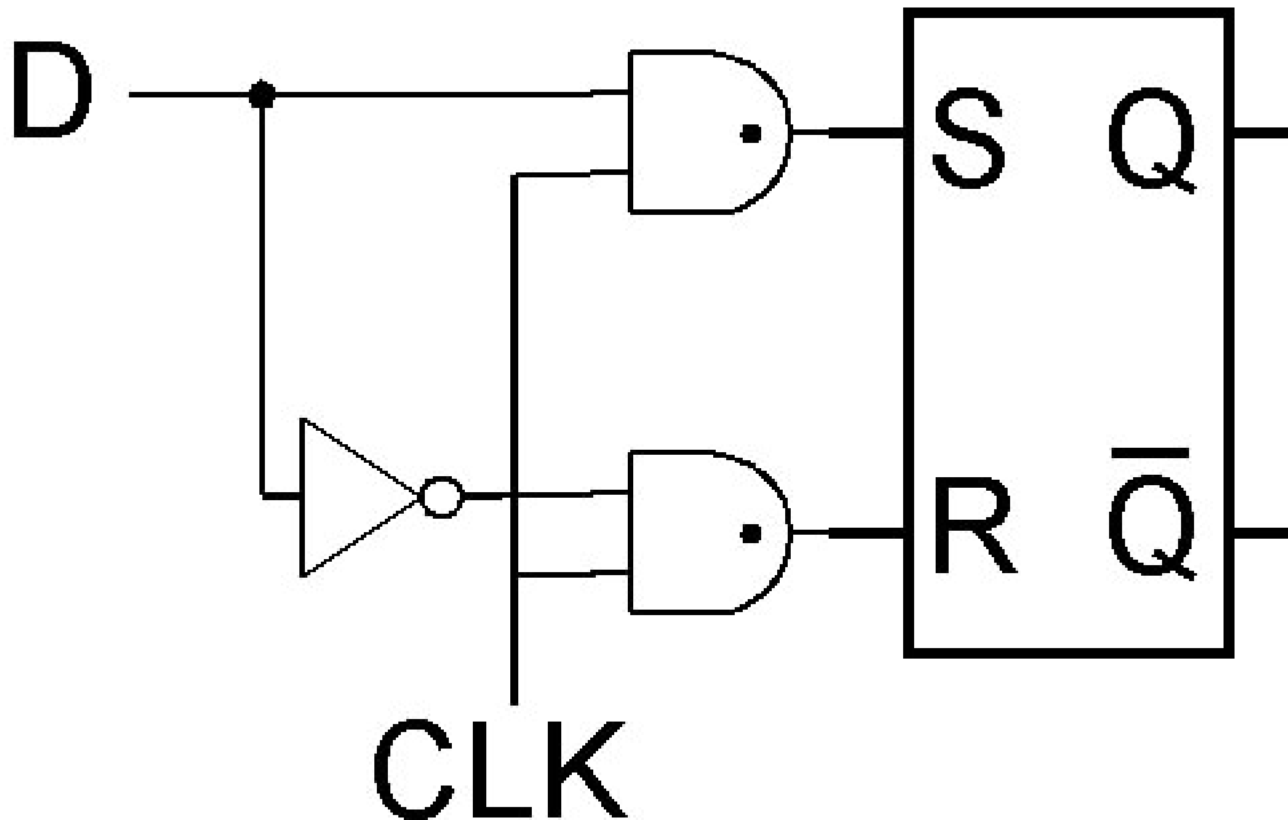
Seuss in the Rad Test Chip



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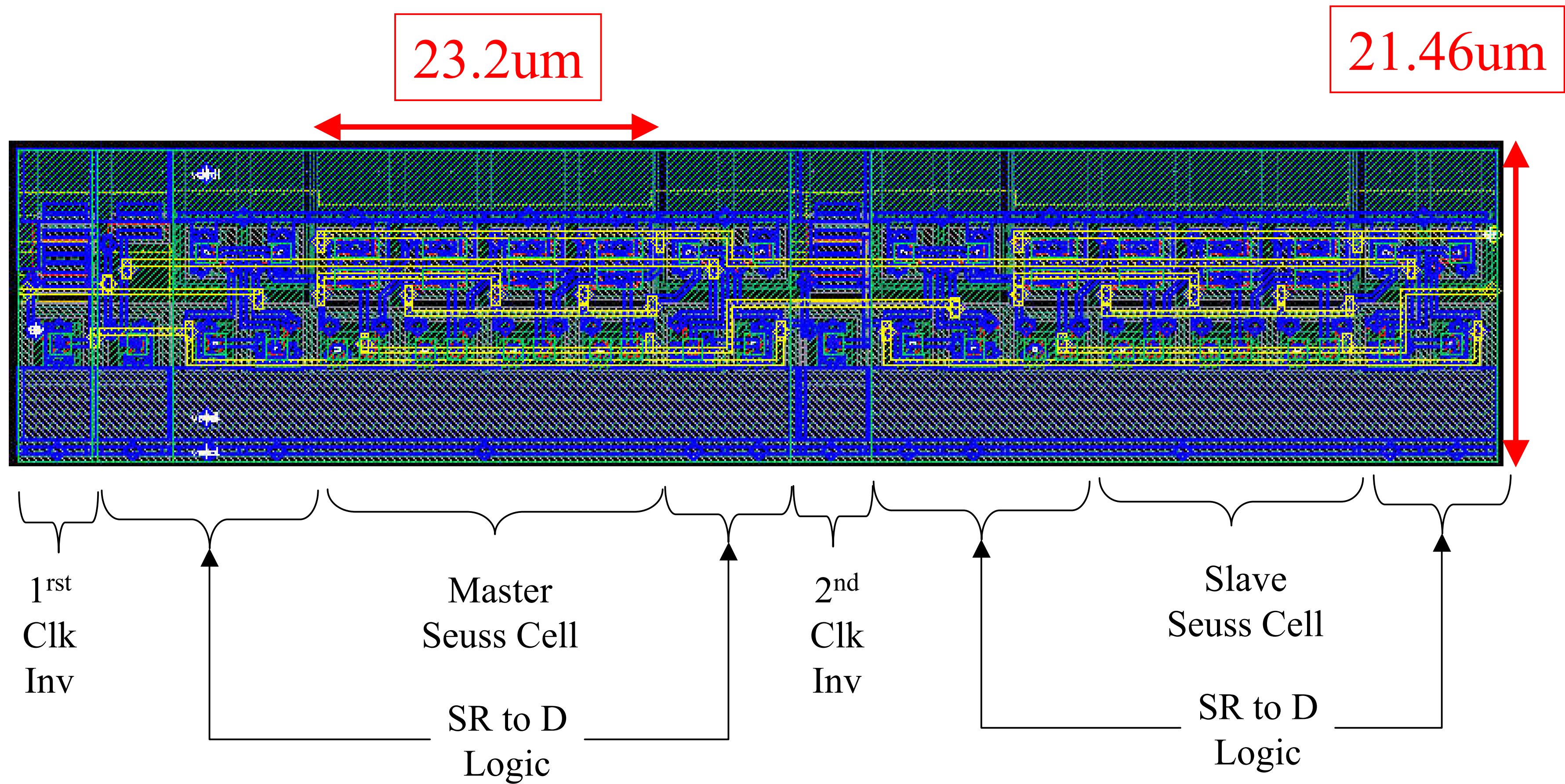

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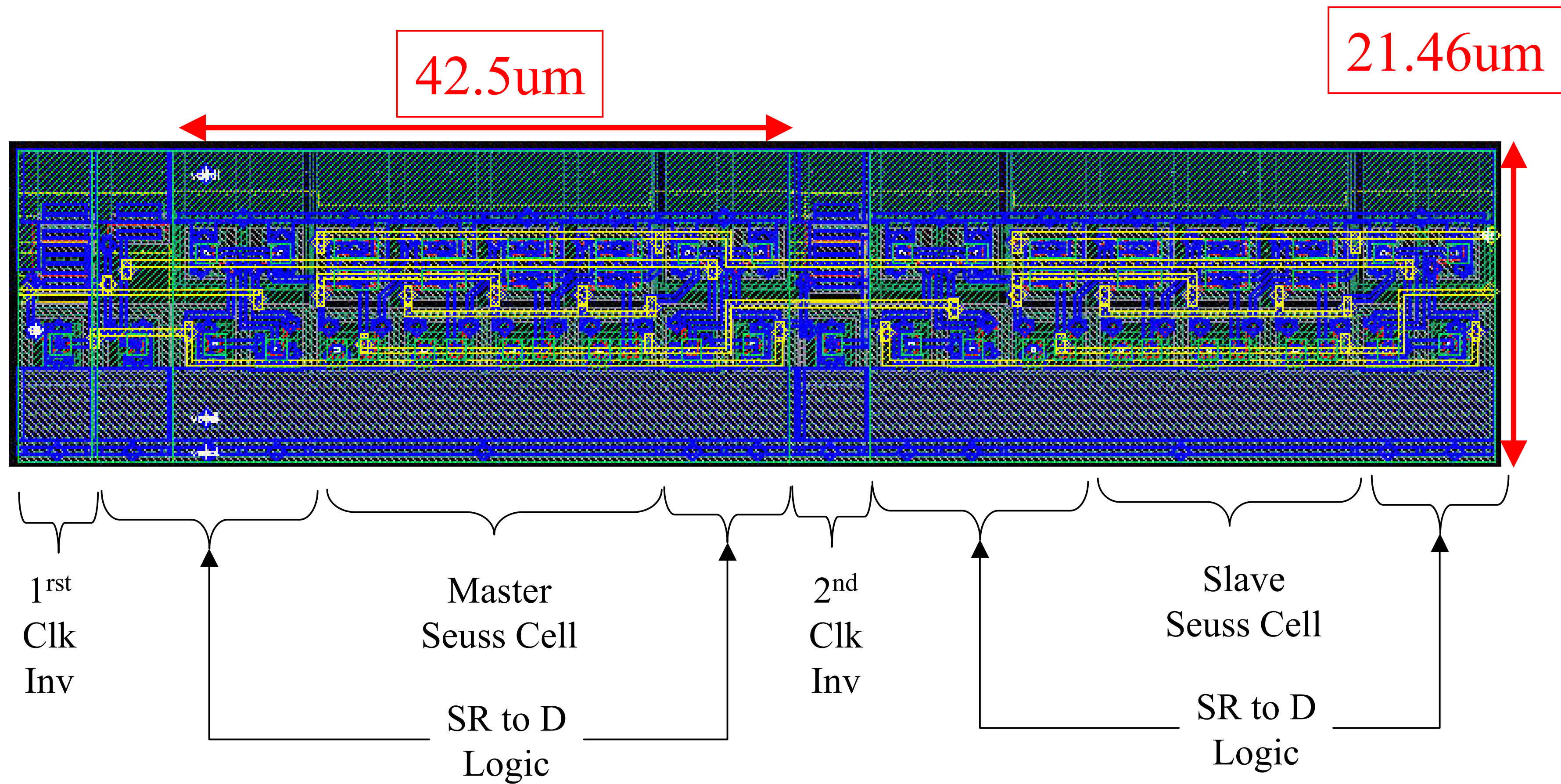

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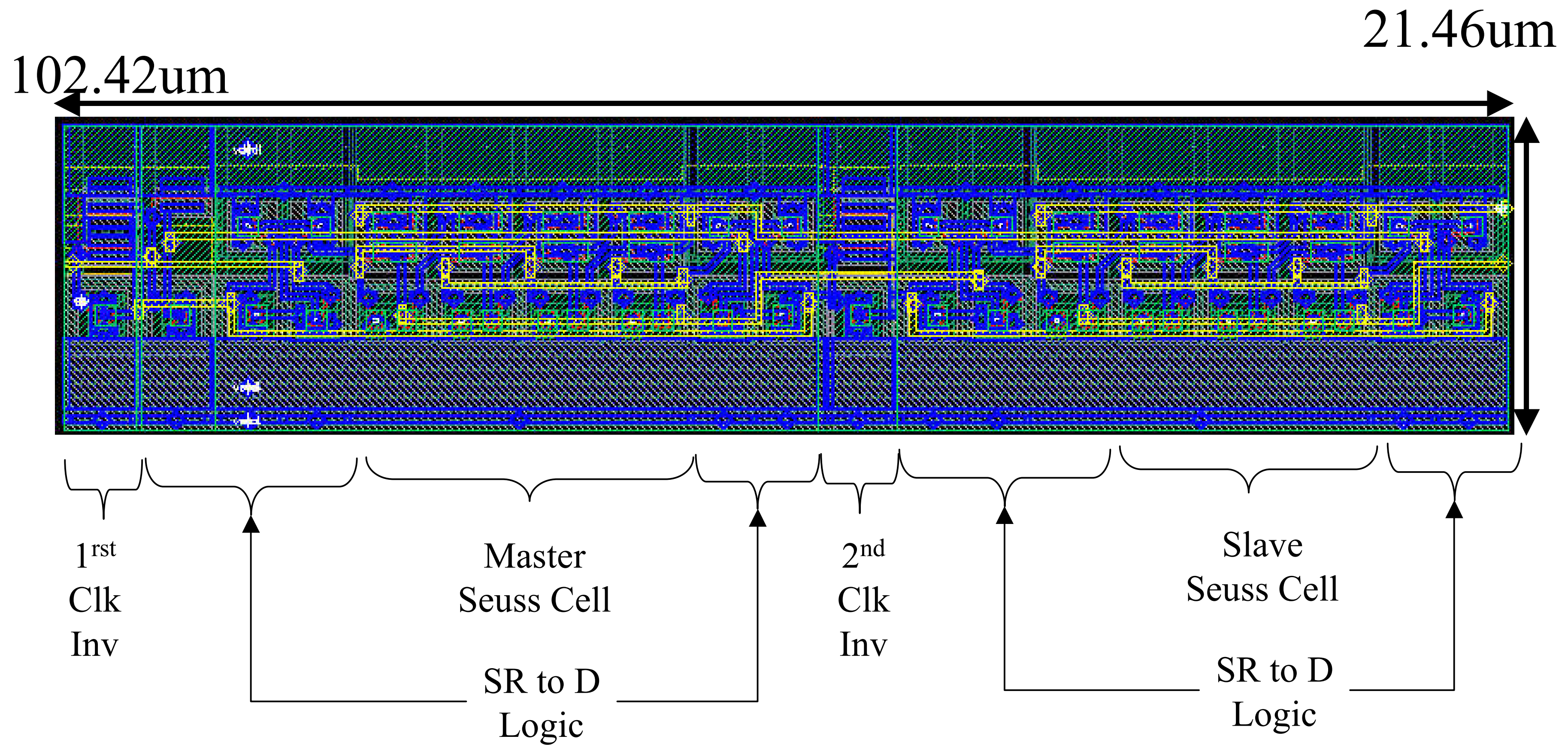

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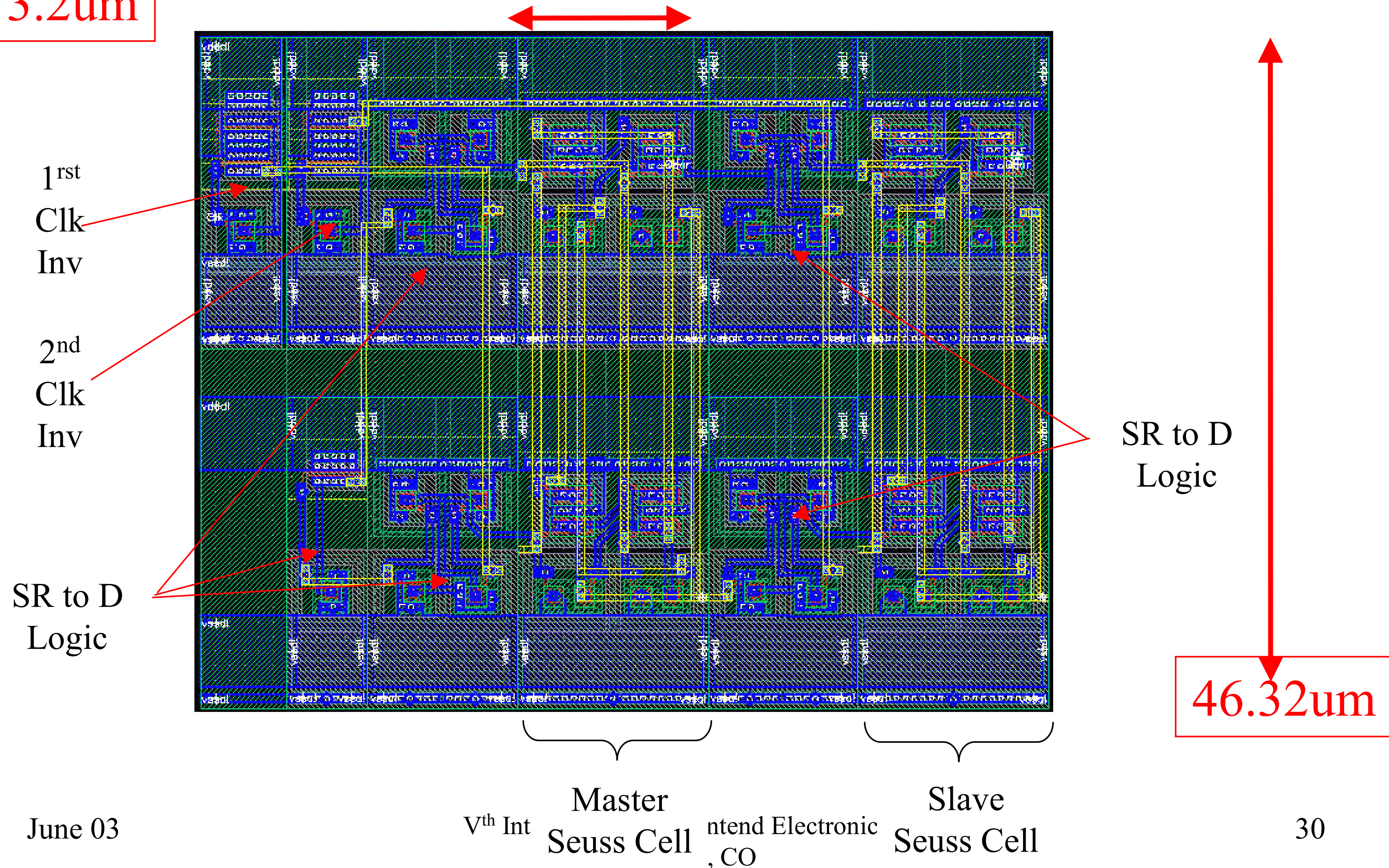

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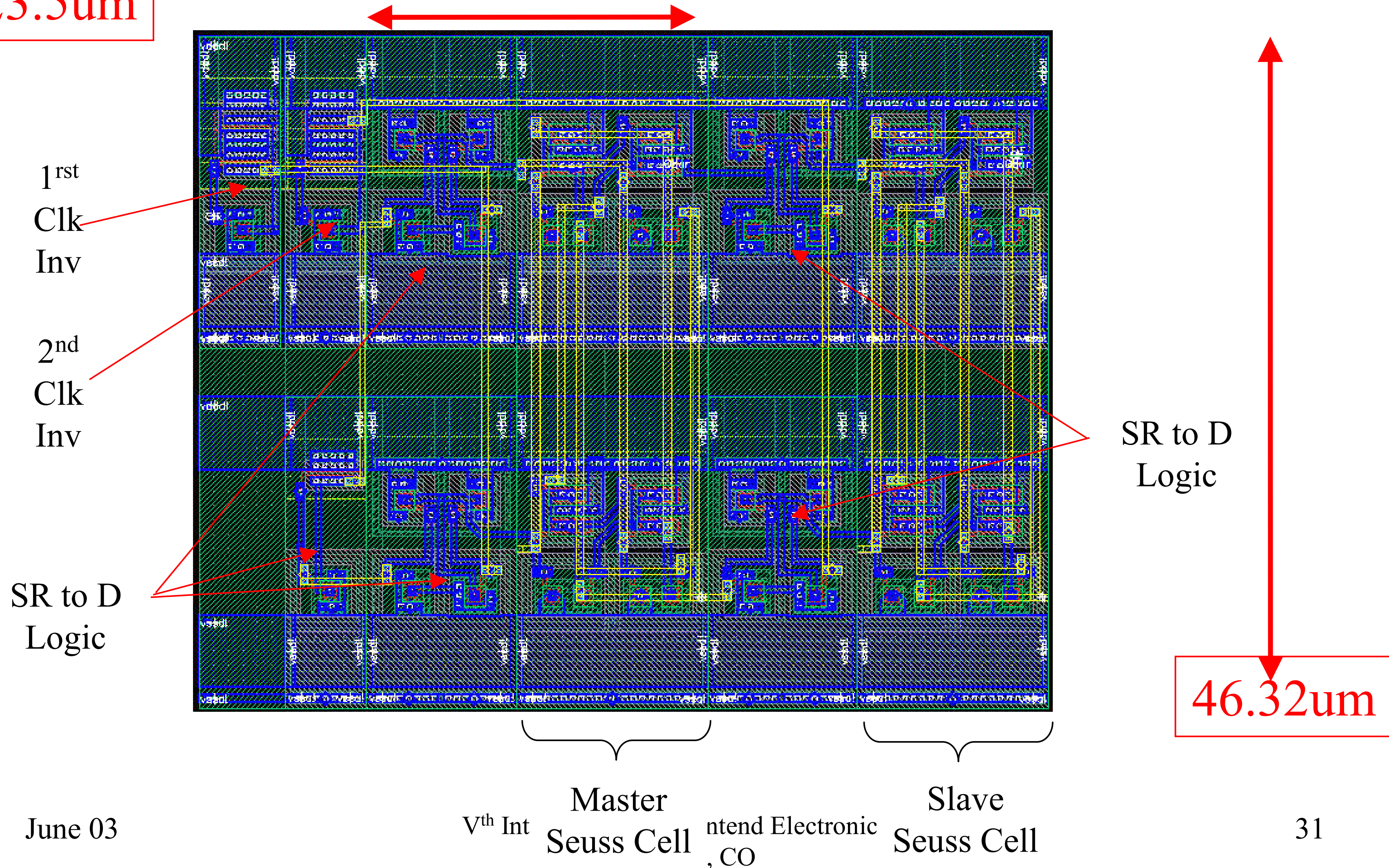

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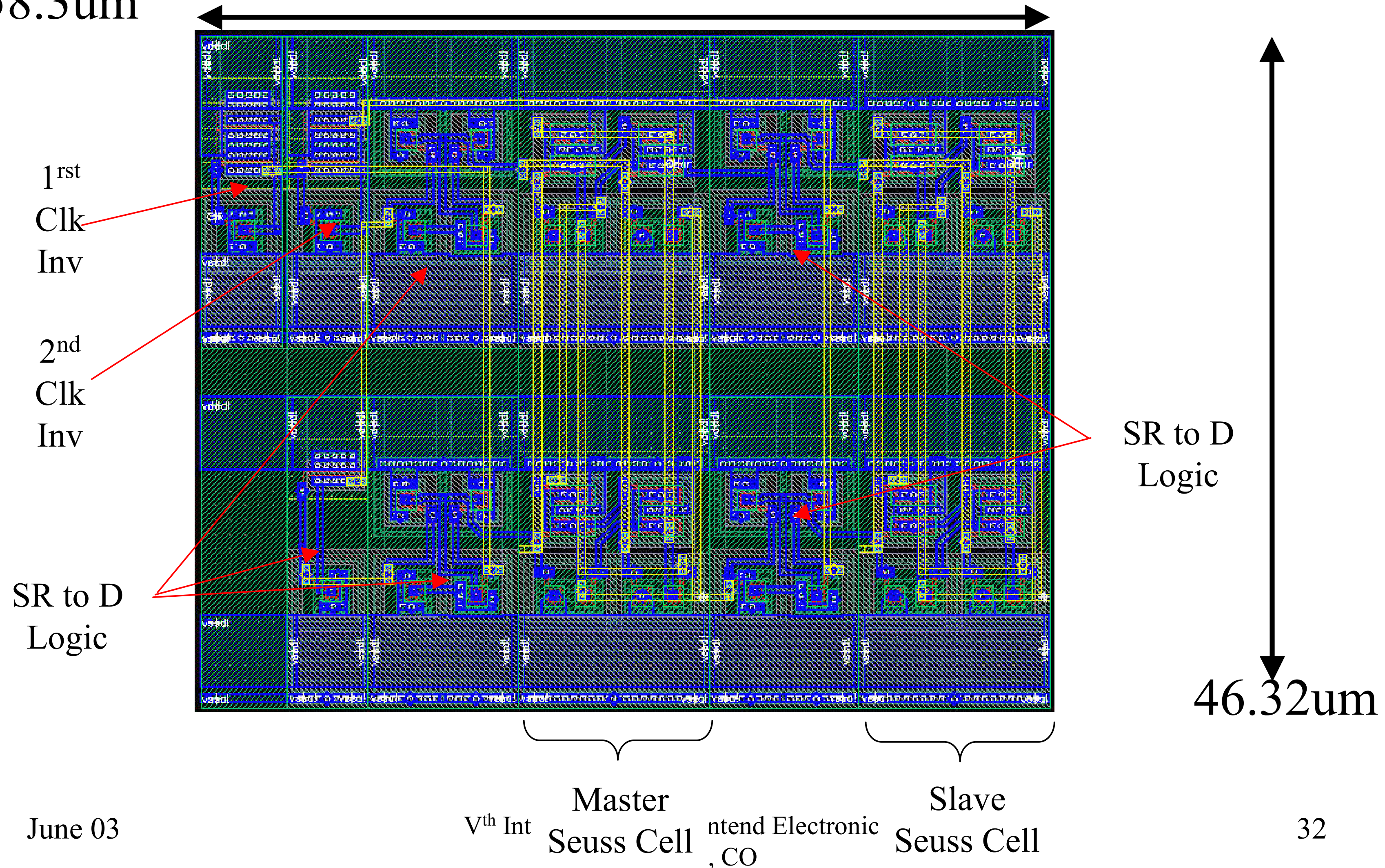

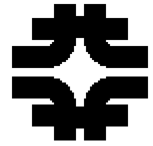

The TRed Cell

- A simple demonstration of Seuss flexibility.
- A triple-redundant implementation with self correction using registers that are already SEU tolerant.
- Box Torture Redundancy.

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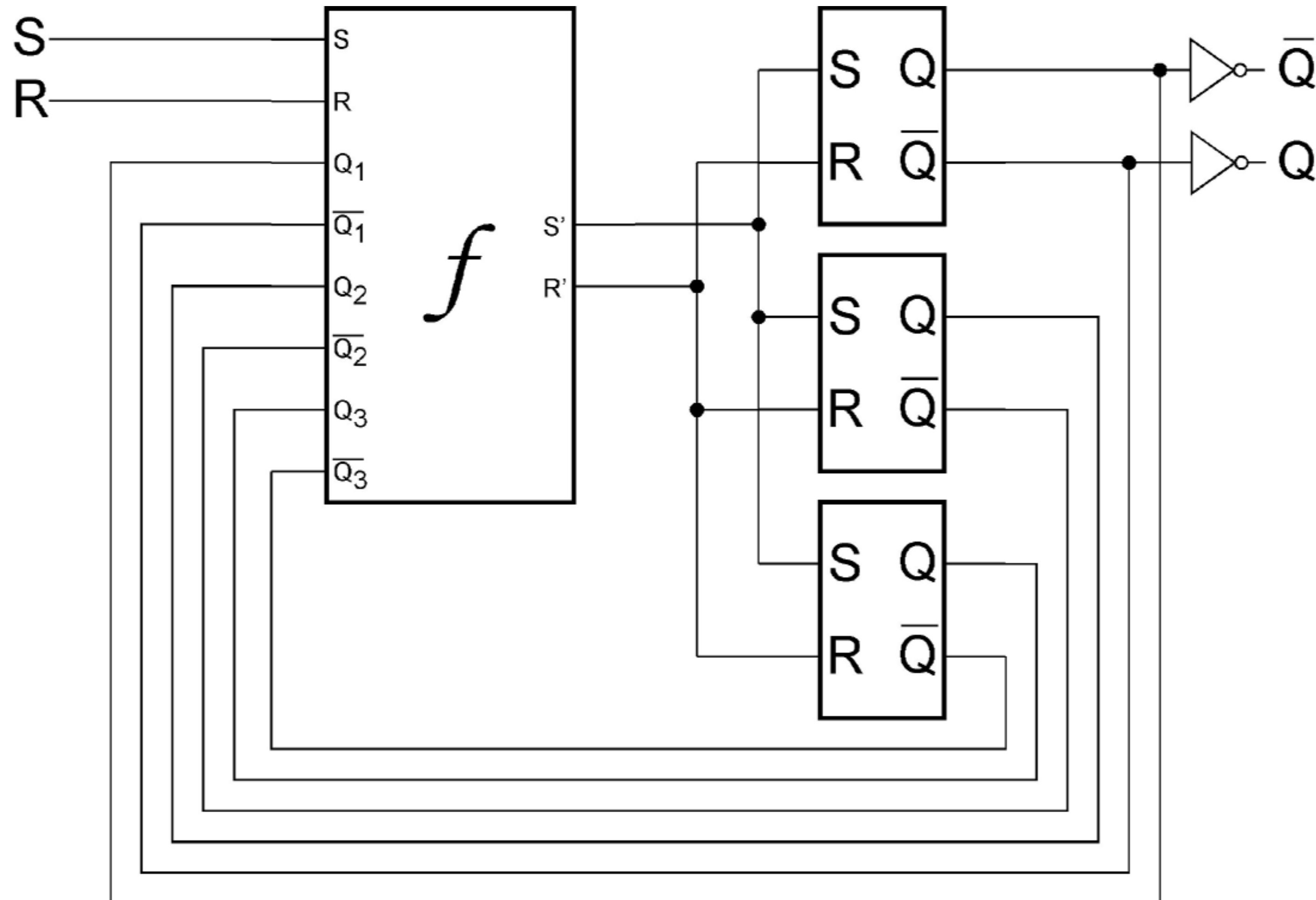
The TRed Cell



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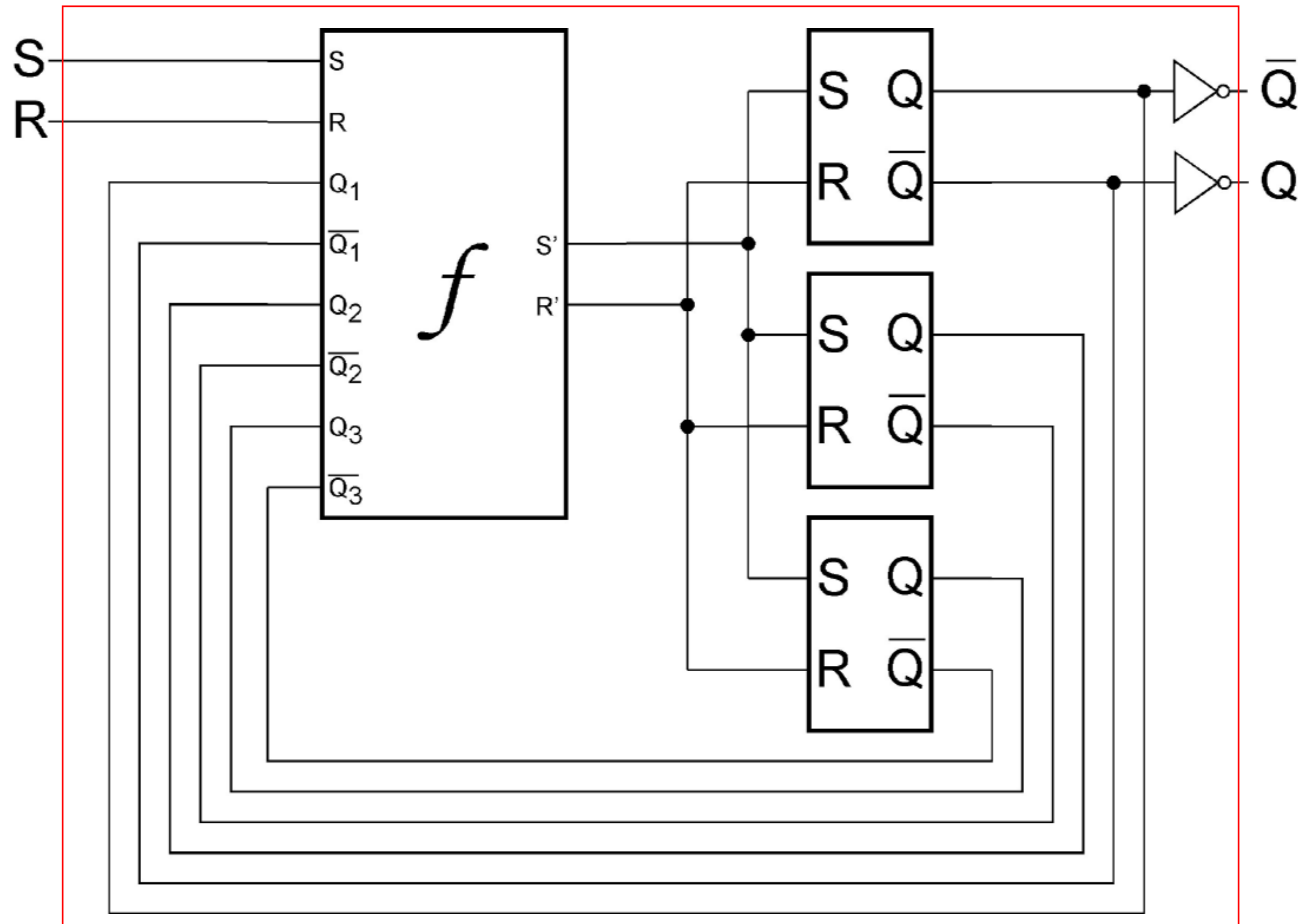
The TRed Cell



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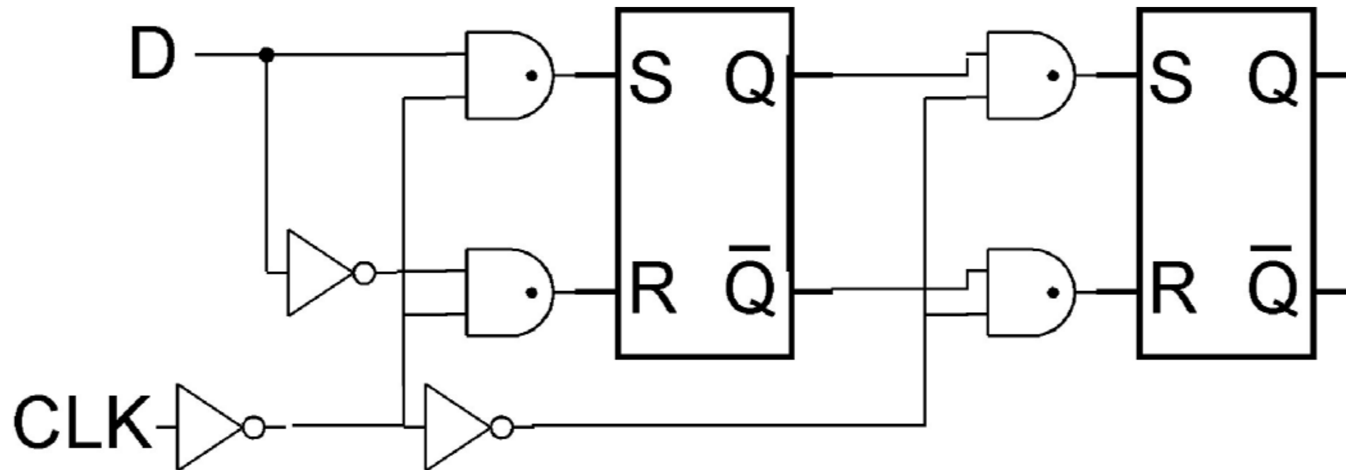

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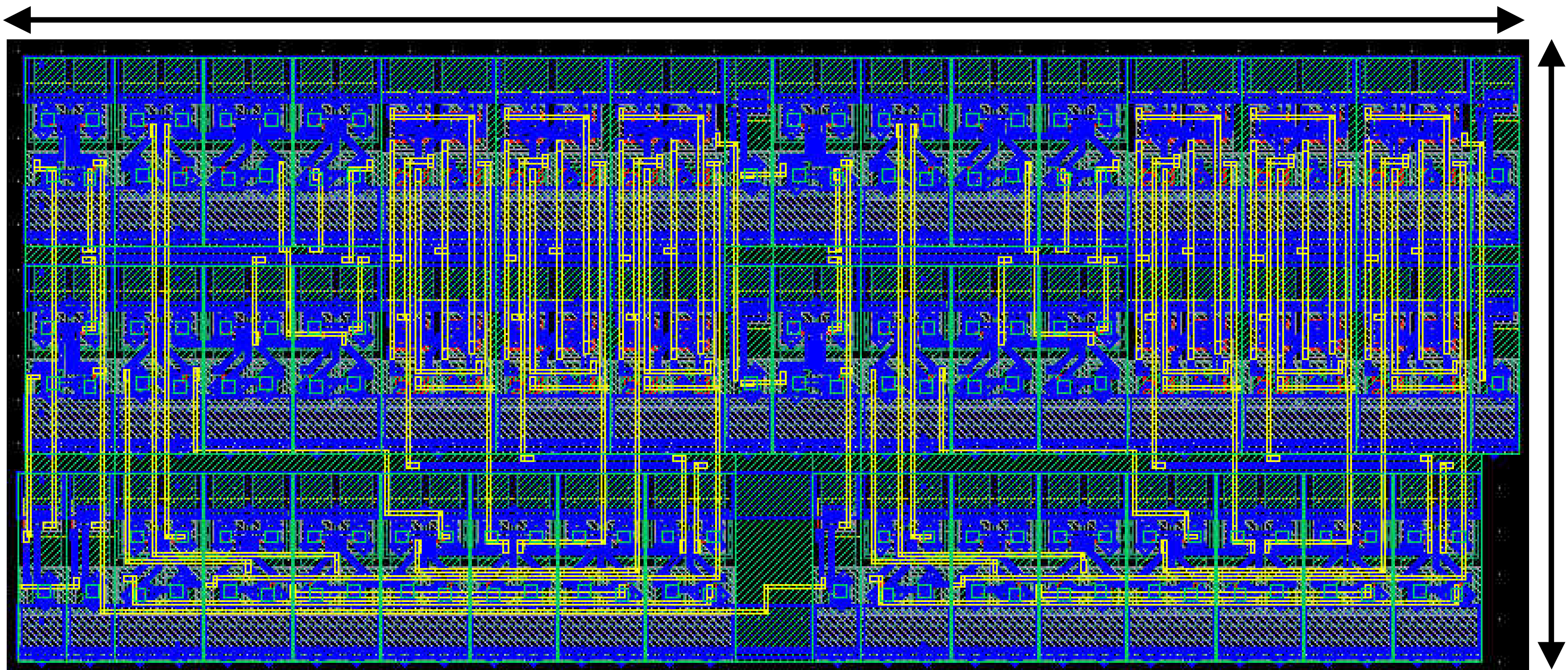
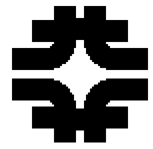
The TRed Cell

172.34um



69.1um



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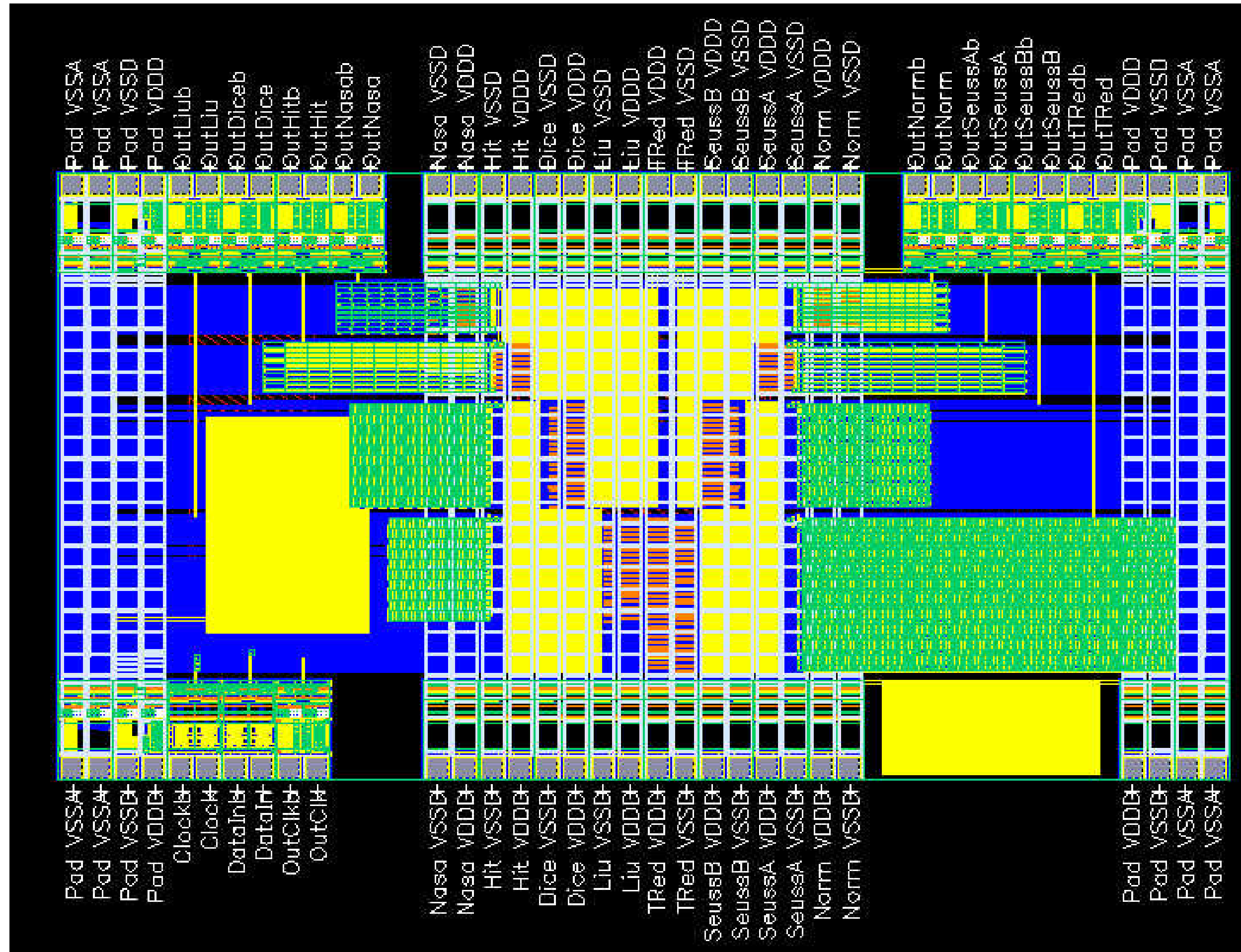
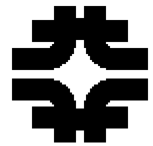
The Full Chip

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Experiment

- To test for possible total dose correlation to SEU, one board was irradiated to 20MRad (Co^{60}) at INER in Taiwan.
- SEU tests performed at the Indiana University Cyclotron Facility in Bloomington, IN. (200MeV protons).
  - Total fluence = $1.3e^{15} \cong$ 75 Mrads.
  - Total exposure time = 10 hours.

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Gamma-ray test at INER

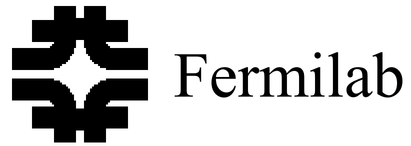
Register Board at Steel drawer.

Thickness : 2mm

Power cable.

Does rate: 6KGray/h

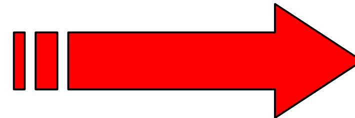
Ready for Irradiation.

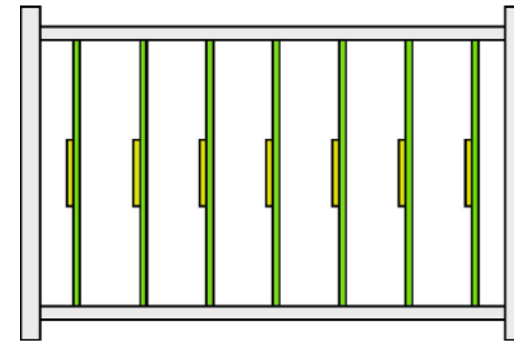


SEU Tests

- 7 boards
- 1 chip per board
- 100x1 Shift Register of each type on each board

Test Monitor



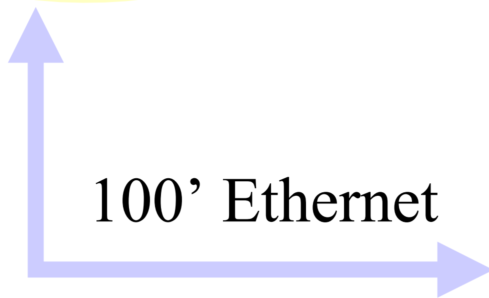


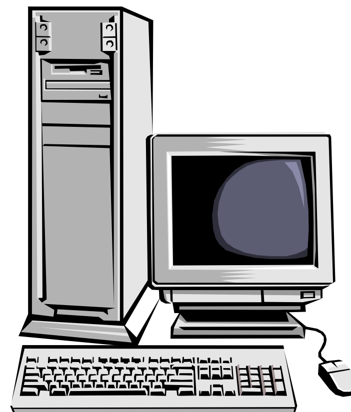
Test Control

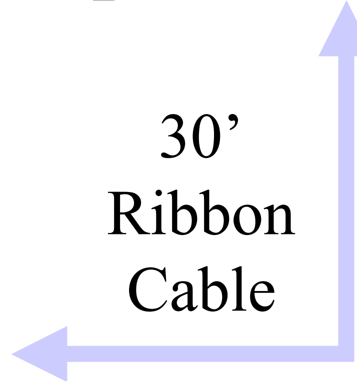
Devices Under Test

30' Ribbon Cable

100' Ethernet







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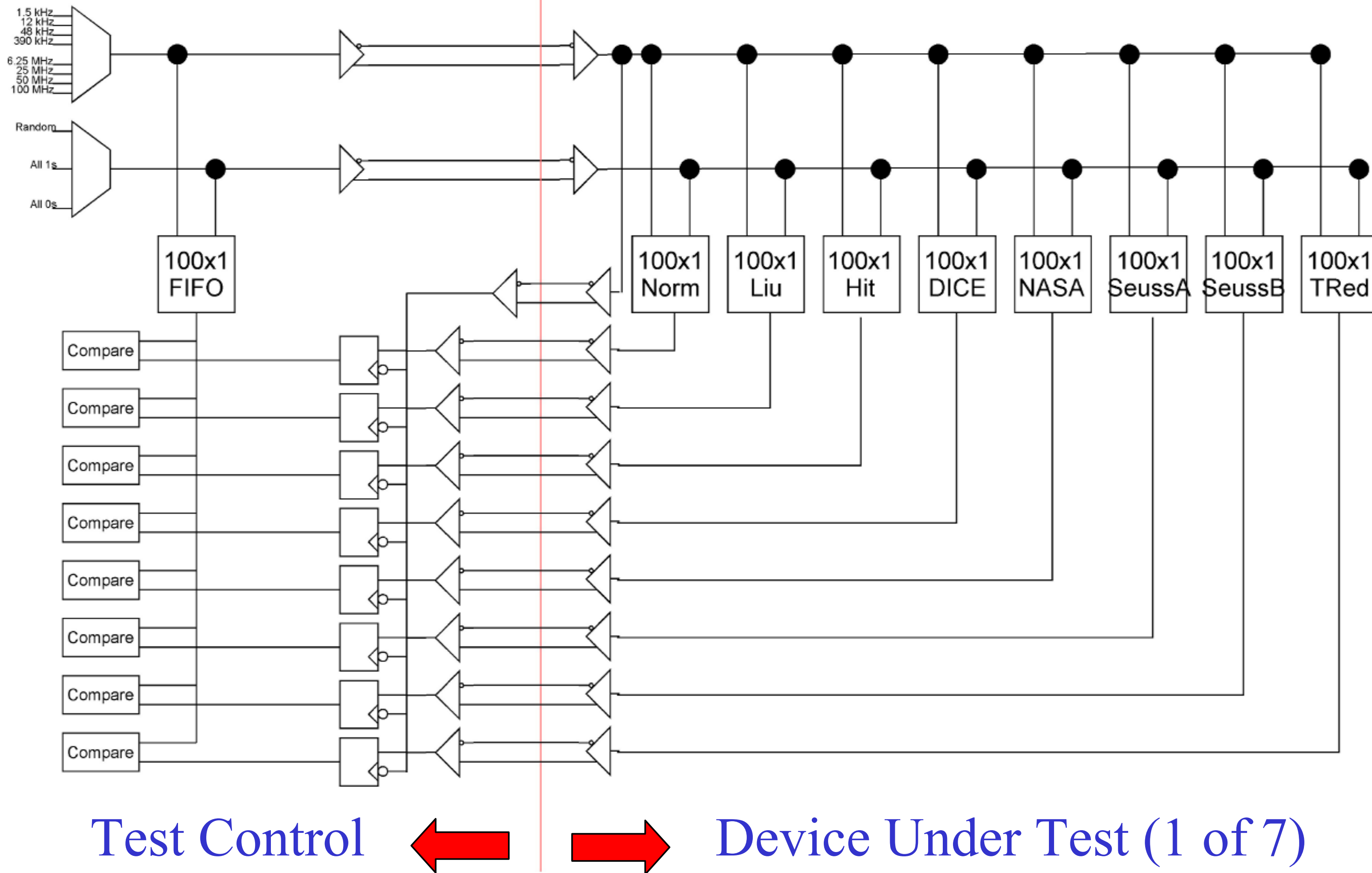
SEU Tests



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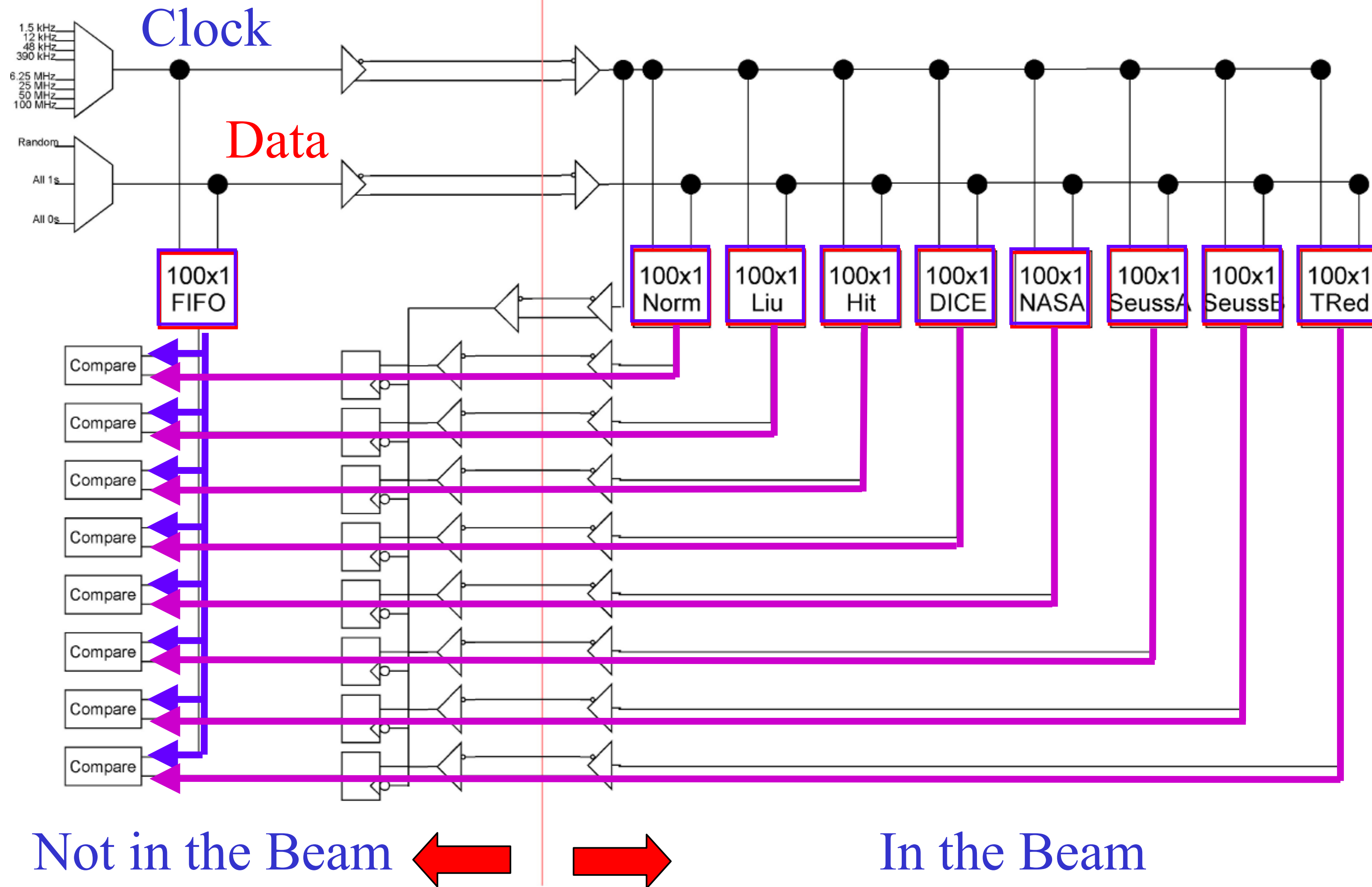
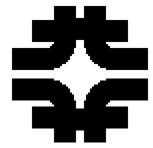
SEU Tests



SEU Exposures

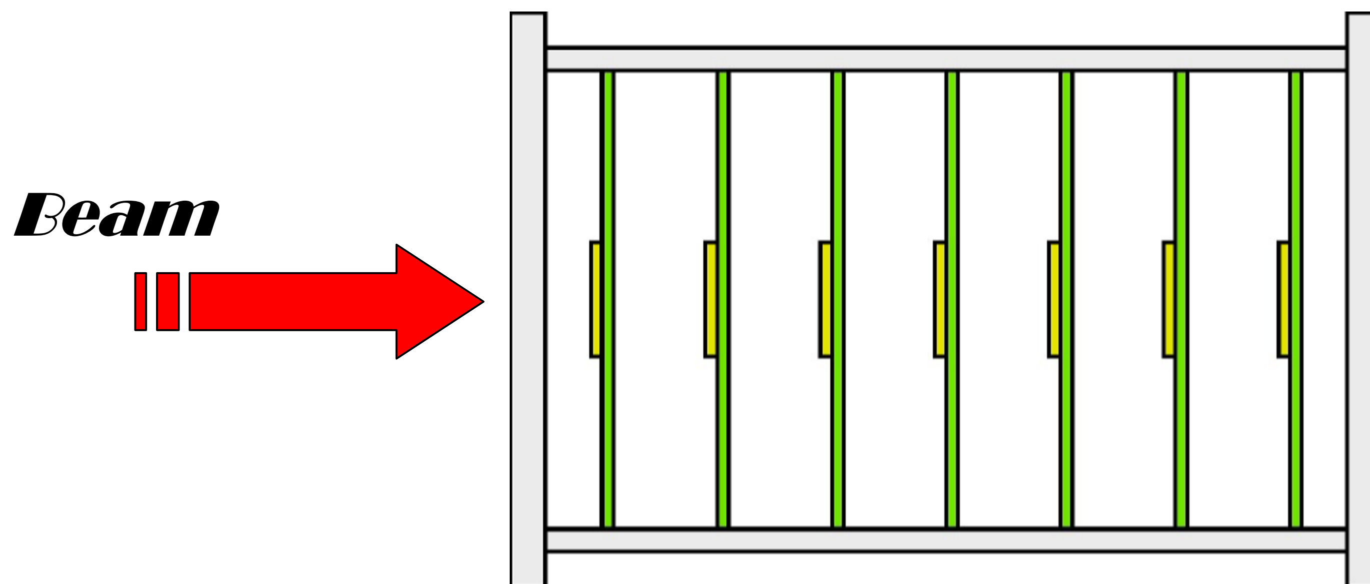
Run	Fluence	Exposure Time	Clock Frequency
A	1.0×10^{13}	30 min	25 MHz
B	5.0×10^{13}	30 min	12 kHz
C	2.4×10^{14}	2 hours	50 MHz
D	4.9×10^{14}	4 hours	50 MHz
E	5.1×10^{14}	4 hours	50 MHz



Raw Results

Type \ Run	A	B	C	D	E
Normal	2	7	78	157	146
Hit	0	0	0	2	1
Dice	0	0	0	8	1
SeussA	1	0	5	20	10
SeussB	0	0	1	10	1
TRed	0	0	0	3	2

Beam Penetration?



Error Count in Normal Registers							
	Board 1	Board 2	Board 3	Board 4	Board 5	Board 6	Board 7
D	23	13	21	20	26	33	21
E	19	19	19	17	28	19	25

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SEU Analysis

$$ERR = \frac{1}{\sqrt{U}}$$

The statistical error margin of a measurement.

- **U** is the number of upsets

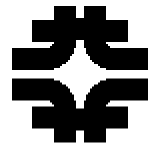
$$\sigma = \frac{U}{NF\cos\vartheta}$$

The SEU cross section.

- **U** is the number of upsets
- **N** is the number of registers of a particular type in the beam (in this case, 700)
- F is the Fluence of the beam (in this case, $1.24e^{15}$)
- θ is the angle of incidence (90°, therefore cos θ = 1)

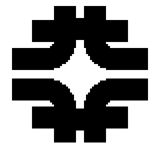
SEU Results (50 MHz)

Register	Area Cell	Area Reg	Upsets (U)	ERR	σ $\left(10^{-18}\ \frac{\text{cm}^2}{\text{bit}}\right)$
Normal	1	1	382	.05	440 ±22
SeussA	2.11/1.15	1.53	35	.17	40.3 ±6.9
SeussB	2.5/1.42	1.88	12	.29	13.8 ±4.0
DICE	1.8	2	8	.35	9.2 ±3.2
TRed	N/A	8.3	5	.45	5.8 ±2.6
HIT	1.12	1.52	4	.50	4.6 ±2.3



Discussion and Conclusions

- Circuit design may be a science,
  but layout is an art.
- Layout (especially size) has a dramatic effect on SEU tolerance.
  - Somewhat less significant, but still important, is the effect of clock edge control.
- Each technique improved SEU tolerance by at least a factor of 10 and all of them survived 75 to 100 Mrads of total dose without failing.

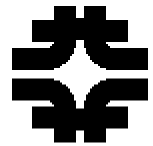


Discussion and Conclusions

- For pure SEU tolerance and area efficiency, the HIT Cell wins.
  - Back drive is significant.
- For design flexibility with SEU tolerance, consider using the Seuss Cells.

Future Work

- MoRT Transistors in TSMC
- Low frequency tests
- SEU consequences of asynchronous resets
- Repeat for 0.13um? Repeat for another process?



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