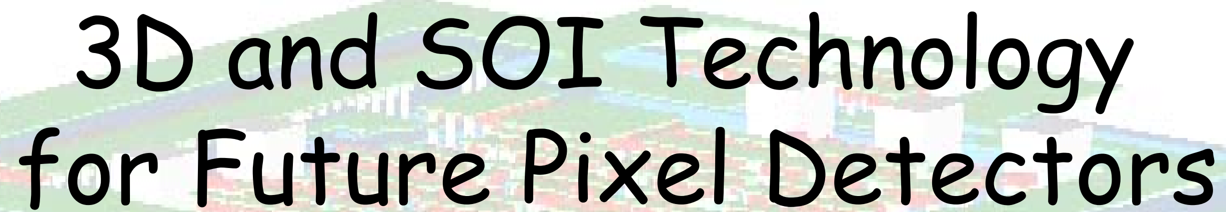


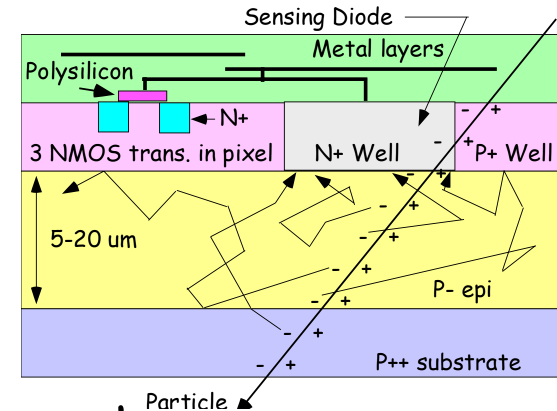
3D and SOI Technology for Future Pixel Detectors

Ray Yarema
Fermilab

Common ATLAS CMS Electronics Workshop
At CERN
March 19-21, 2007

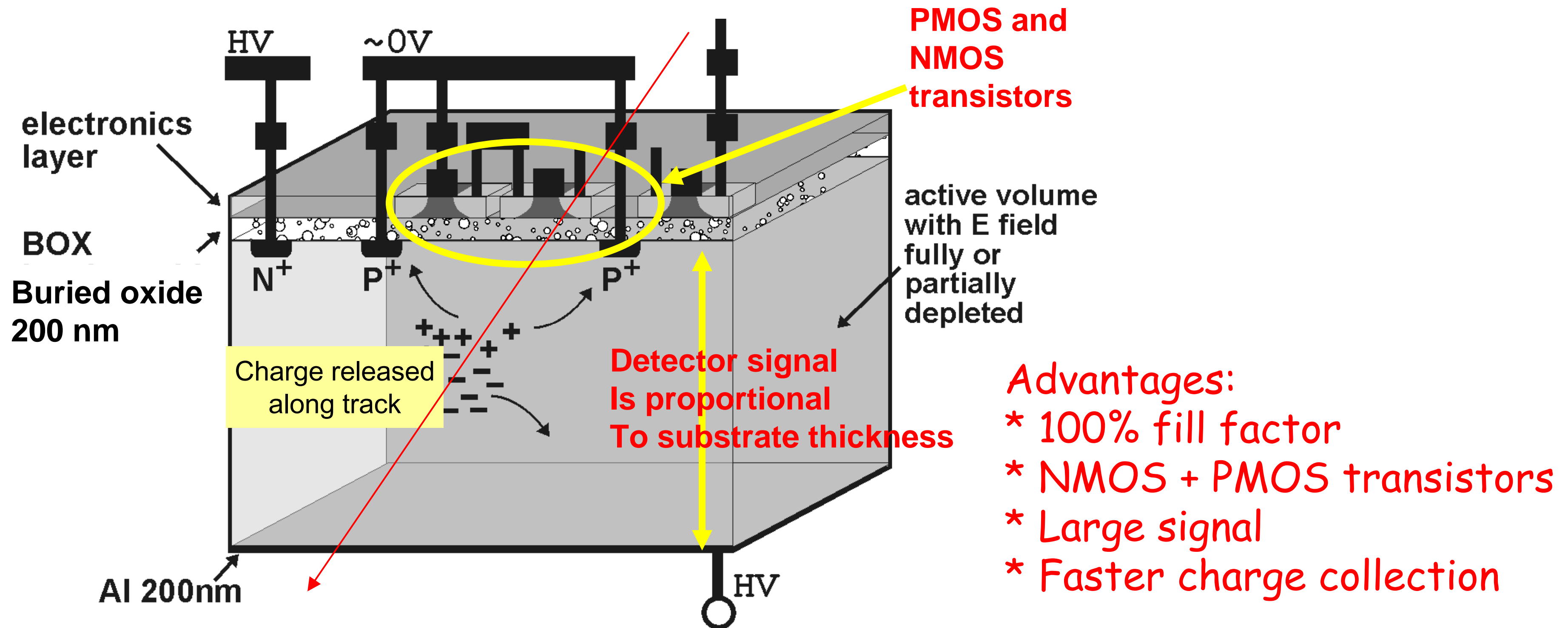
Introduction

- Requirements for HEP pixel electronics and detectors continue to push the limits for lower mass and power, and higher resolution.
- Significant progress has been made to address these issues by integrating sensors and front end electronics within the pixel cell.
  - Monolithic Active Pixel Sensors (MAPS)
    - Much has been accomplished but there are fundamental limitations to this approach
      - Small signal dependent on epi thickness
      - Most designs are limited to NMOS transistors (limited functionality)
      - Slow rise time set by diffusion



  - There are other choices under development
    - SOI (Silicon on Insulator) Pixel Sensors
      - Offers improvements over MAPS
    - 3D integrated circuits
      - Offers improved performance over SOI pixel sensors.

Active Pixel Sensor in SOI



Advantages:
* 100% fill factor
* NMOS + PMOS transistors
* Large signal
* Faster charge collection

Thin top layer has silicon islands in which PMOS and NMOS transistors are built.
A buried oxide layer (BOX) separates the top layer from the substrate.
The high resistivity substrate forms the detector volume.
The diode implants are formed beneath the BOX and connected by vias.
The raw SOI wafers are procured from commercial vendors such as SOITEC in France.

Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at two different foundries :OKI in Japan, and American Semiconductor Inc. (ASI) in US . The two processes have different characteristics as seen below

Process	**0.15μm Fully-Depleted SOI CMOS process,** **1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).**
SOI wafer	**Wafer Diameter: 150 mmϕ,** **Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick** **Buried Oxide: 200 nm thick** **Handle wafer: Cz、 >1k Ω-cm (*No type assignment*), 650 μm thick (SOITEC)**
Backside	**Thinned to 350 μm, no contact processing, plated with Al (200 nm).**

OKI Process

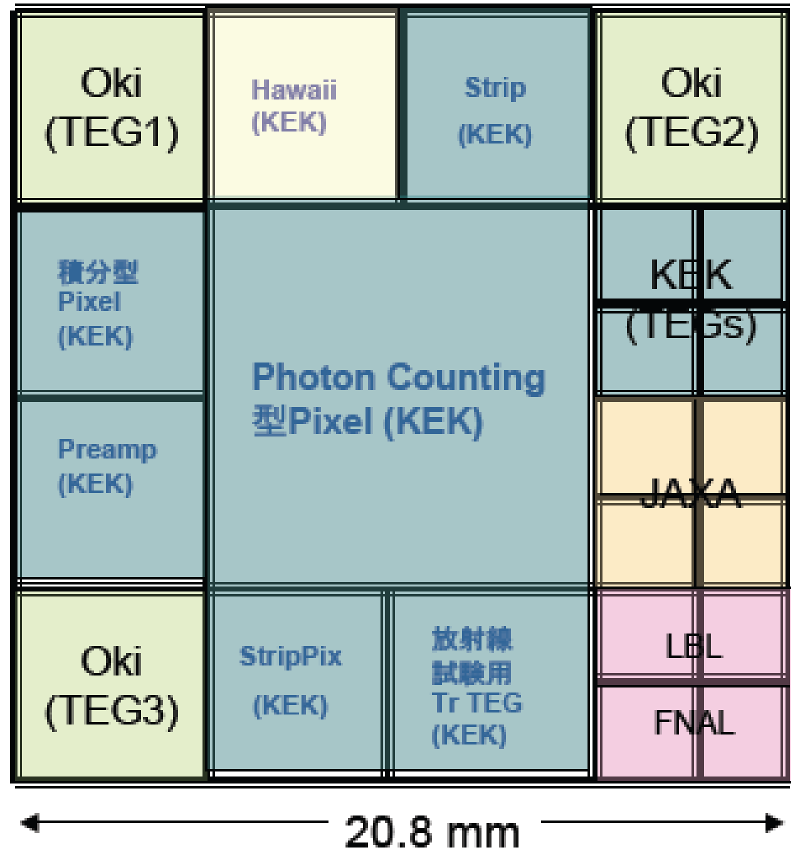
Process	**0.18μm partially-Depleted dual gate SOI CMOS process,** **Dual gate transistor (Flexfet),** **No poly, 5 metal (American Semiconductor / Cypress Semiconductor.)**
SOI wafer	**Wafer Diameter: 200 mmϕ,** **Handle wafer: FZ>1k Ω-cm (*n type*)**
Backside	**Thinned to 50-100 μm, polished, laser annealed and plated with Al.**

ASI Process

OKI Process

- KEK has organized two multi-project wafer (MPW) runs at the OKI foundry. [1]
  - Second MPW run has 17 designs from 7 different organizations.
    - Chips due back in March
  - A 3rd run is planned for later this year
- First SOI Detector Workshop took place March 6, 2007 at KEK.

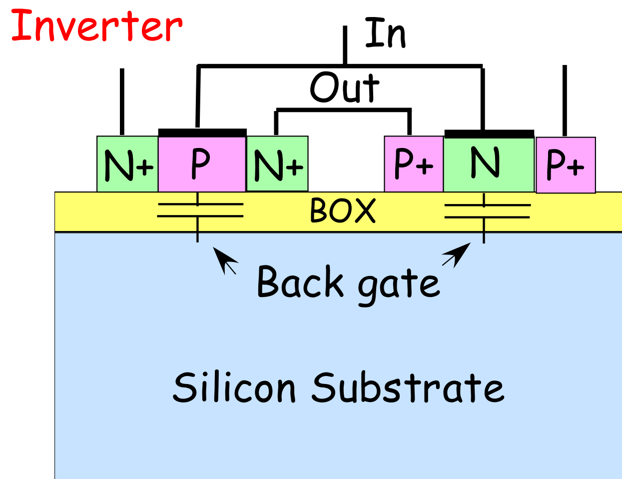
Reticule for 2nd OKI MPW run



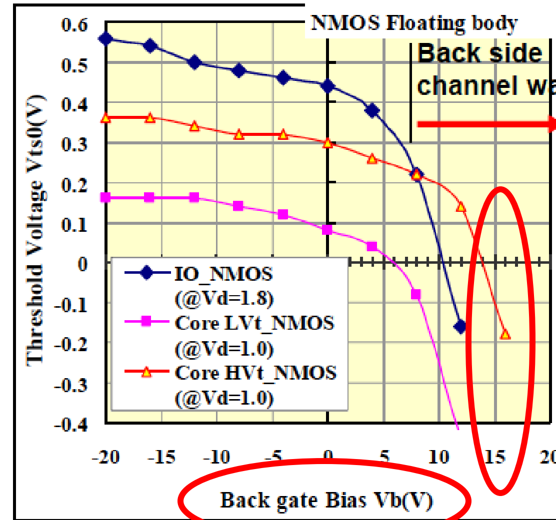
Fermilab Pixel Design in OKI Process

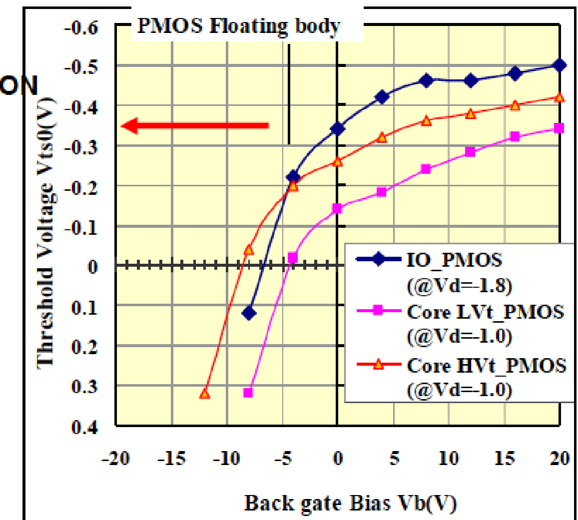
- A chip has been designed in the OKI 0.15 micron process to understand the advantages and problems of SOI detector design. [2]
  - The chip is a wide dynamic range counting pixel detector chip that is sensitive to 100-400 KeV electrons, high energy X-rays, and minimum ionizing particles.
- Issues uncovered
  - Trapped charge in the BOX due to radiation can be a problem in high radiation applications.
    - The radiation induced threshold shift can be corrected by changing the voltage on the substrate.[3]
  - The back gate effect, which appears in detector applications, is an important design consideration in the OKI process.

Back gate Effect in OKI Process[1]

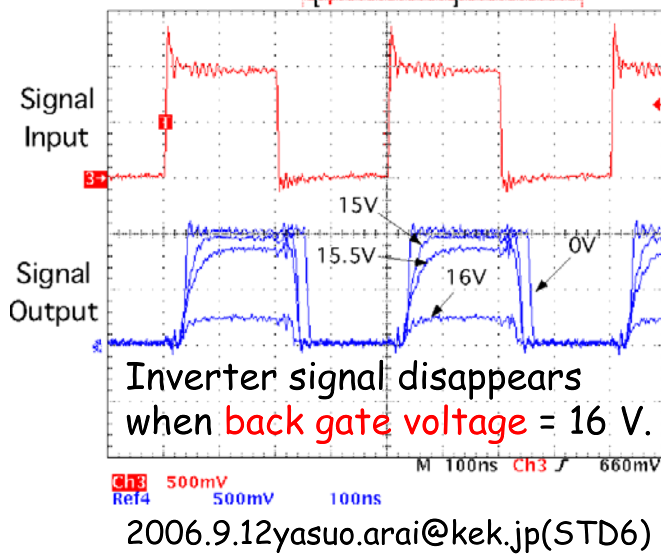


Substrate voltage acts as a back gate bias and changes transistor threshold





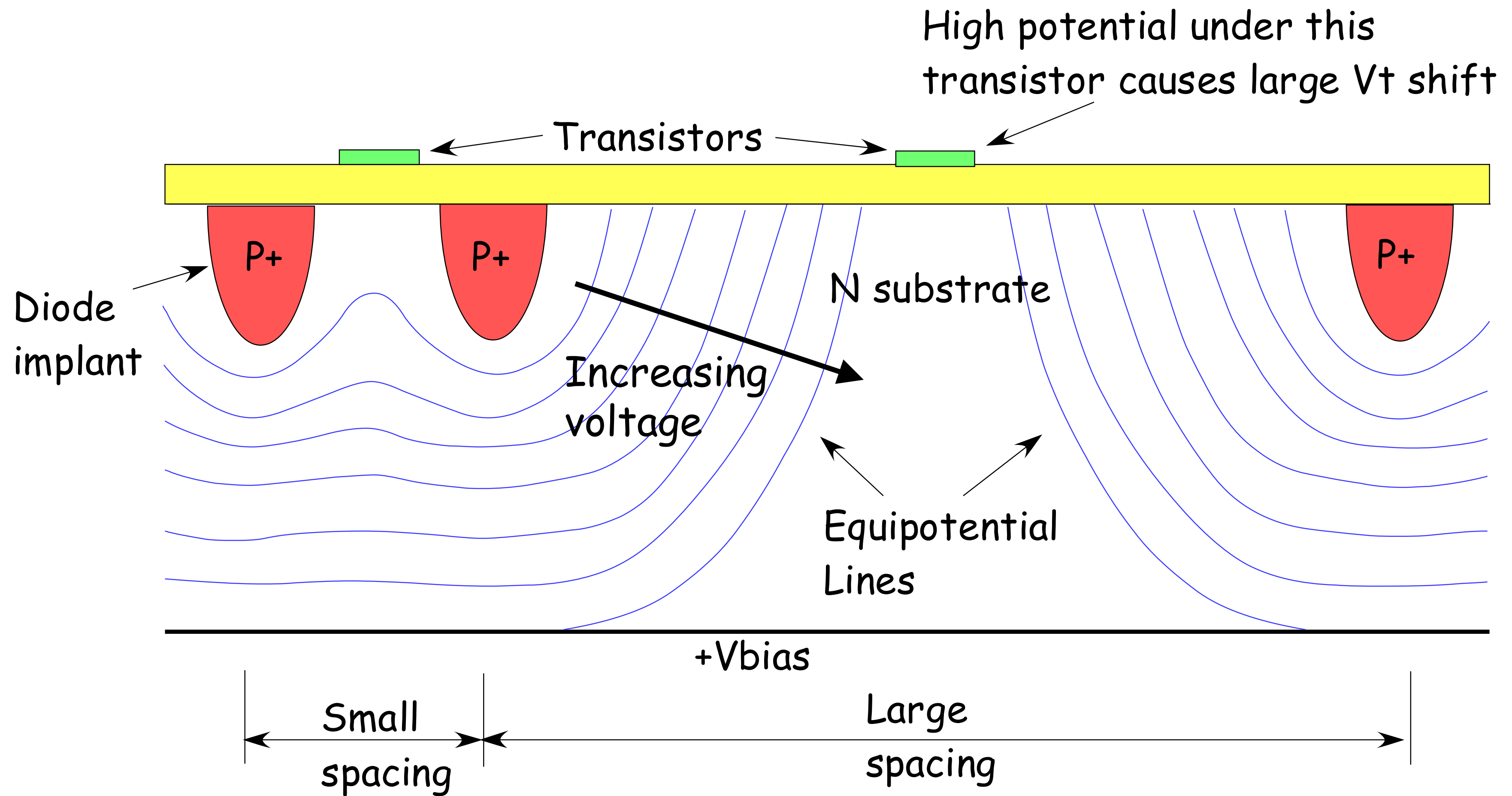
Inverter response to back gate



2006.9.12yasuo.arai@kek.jp(STD6)

The threshold shift problem exists for SOI transistors in processes like OKI which have a floating body. <u>The ASI process has a discrete back gate which shields the transistor from the substrate and thus eliminates the problem</u>.

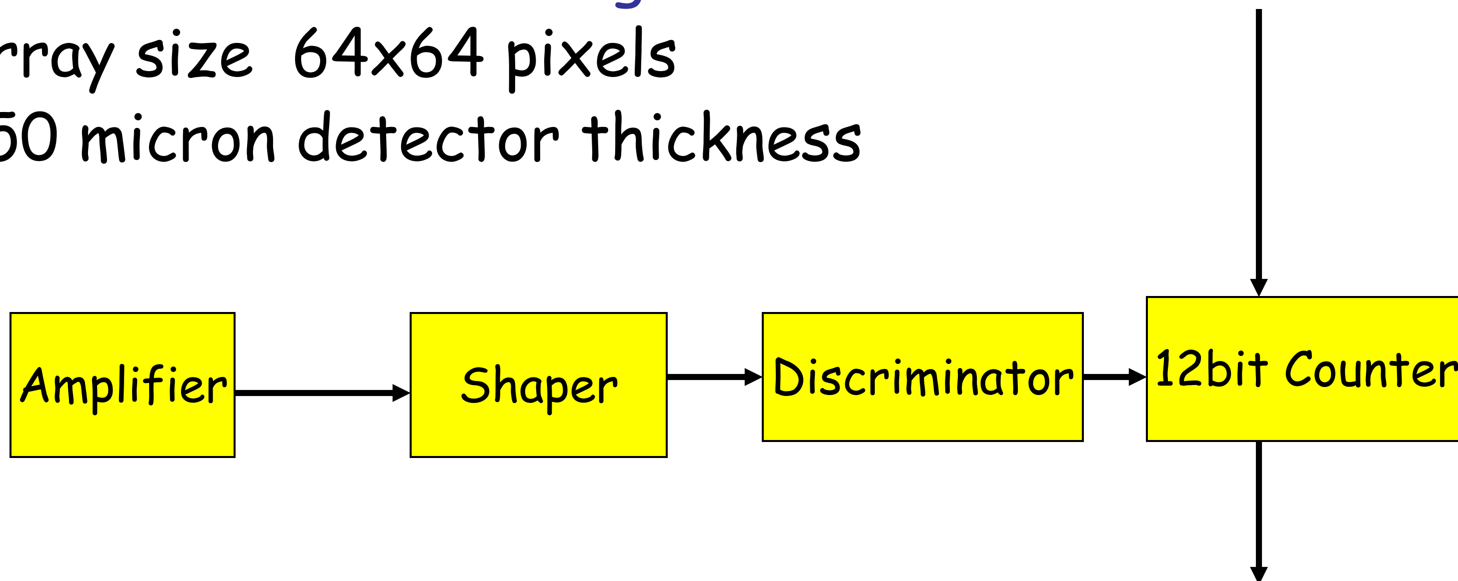
Back Gate Voltage Control



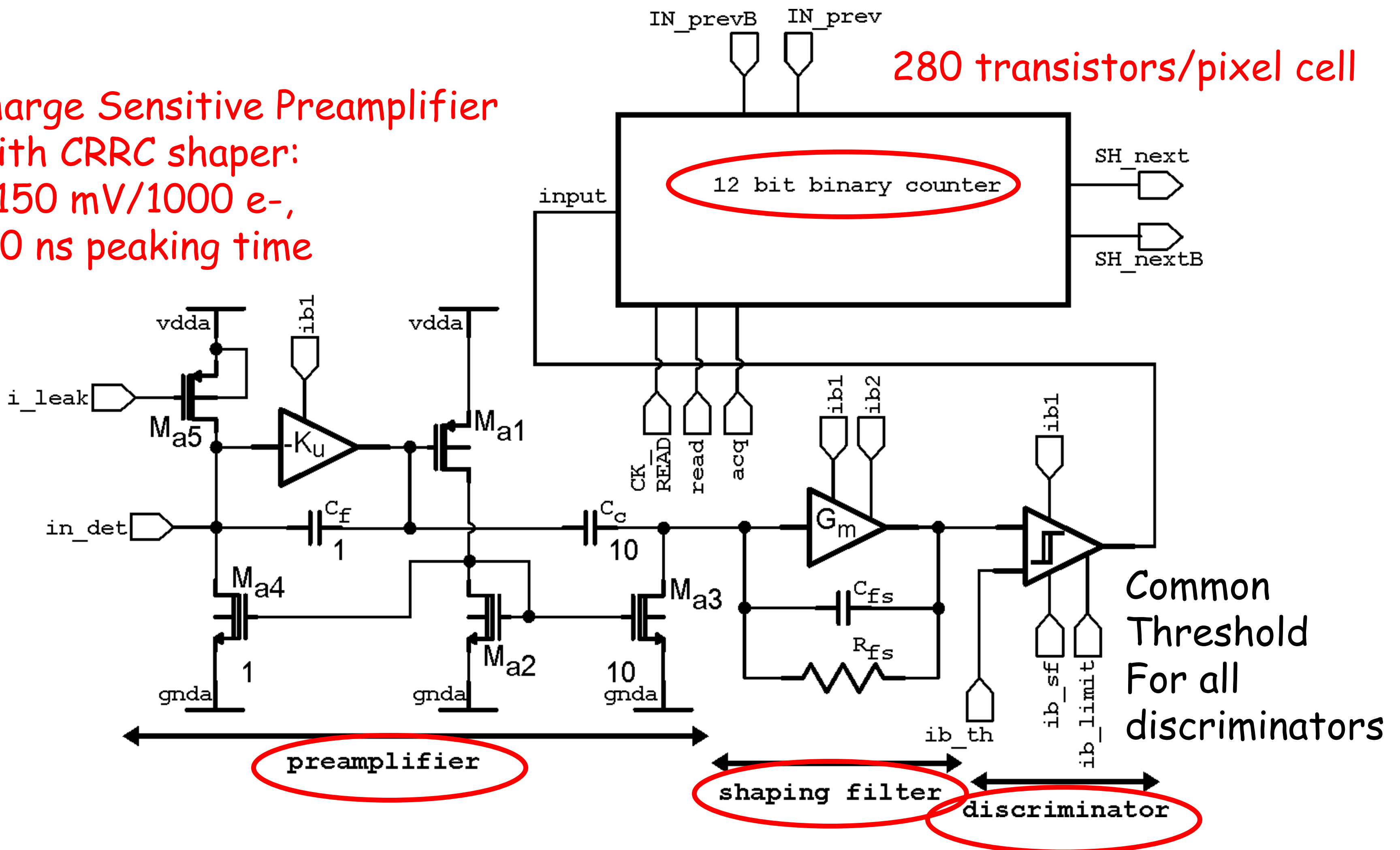
To reduce voltage under the transistors, keep P+ implants close together.

Fermilab MPW Pixel Design for OKI

- Counting pixel detector plus readout circuit
  - Maximum counting rate ~ 1 MHz/pixel.
- Simplified architecture due to design time constraint
  - Reconfigurable counter/shift register
    - 12 bit dynamic range
  - Limited peripheral circuitry
    - Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness



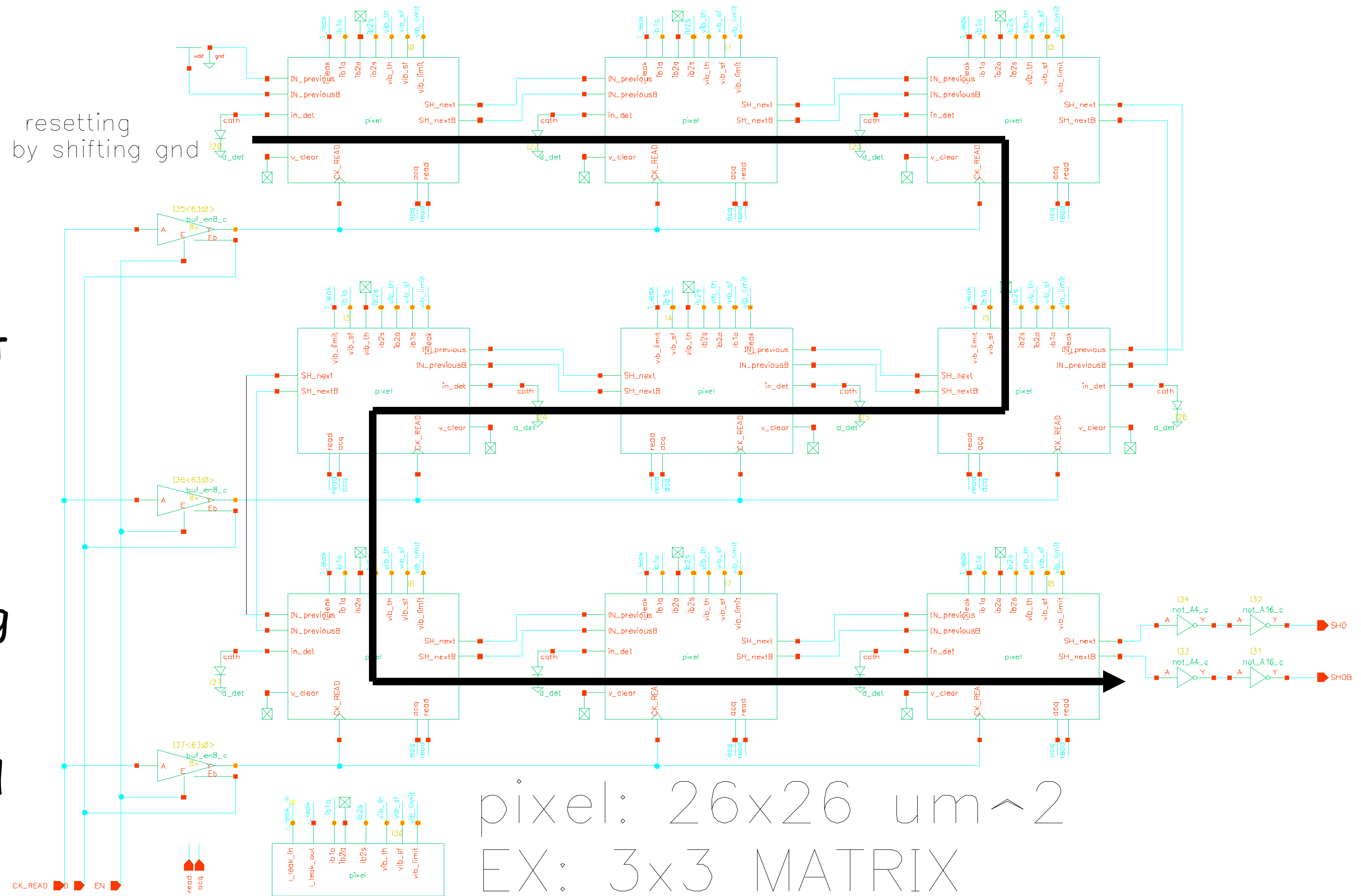
Pixel Design in OKI Process



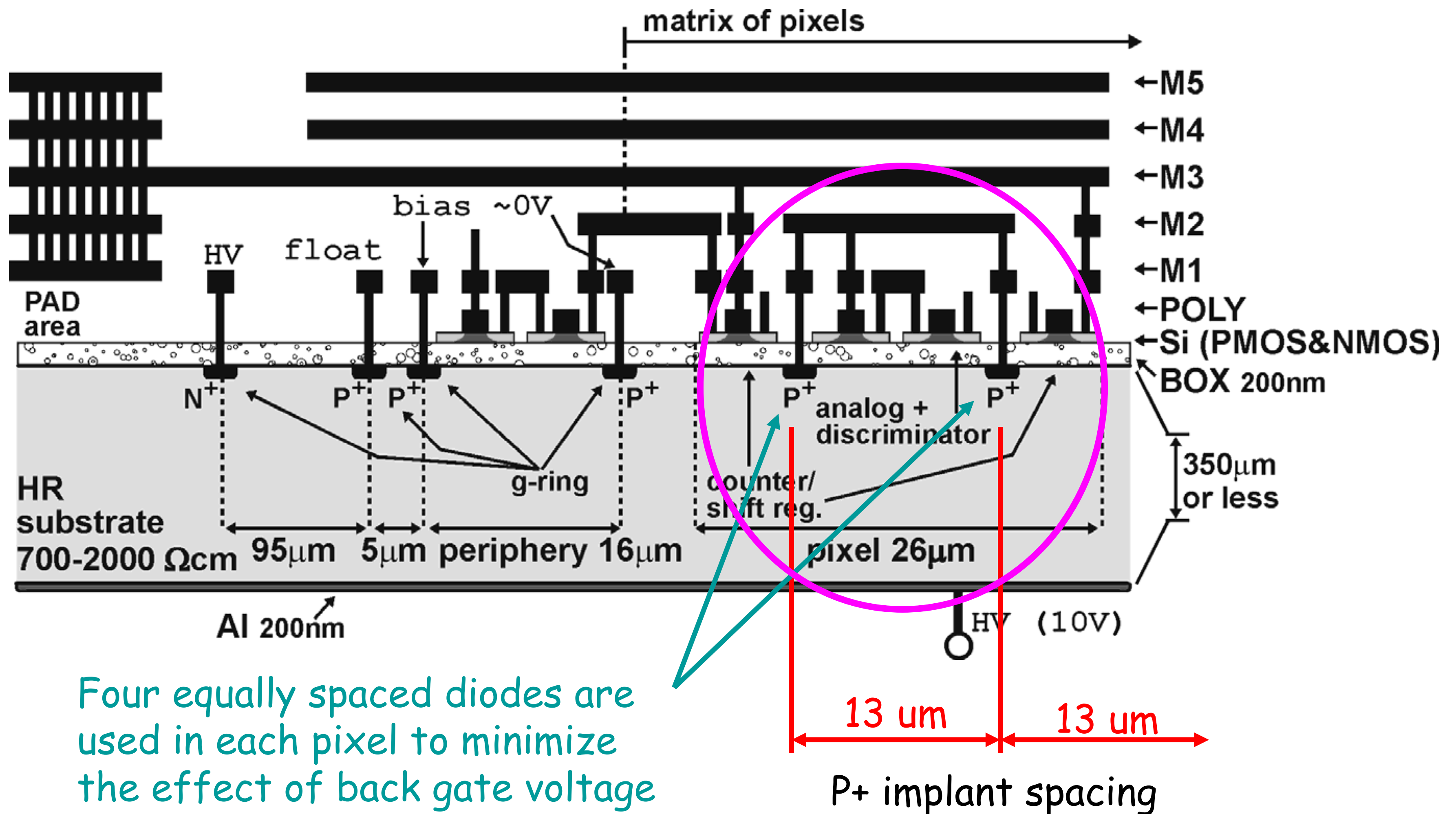
Simplified 3 x 3 Pixel Matrix

Operates in two modes:
Acquire/Read out

12 bit counter is reset by changing counter to a shift register configuration and shifting in zeros during read out.



OKI Pixel Detector Cross Section



Four equally spaced diodes are used in each pixel to minimize the effect of back gate voltage by keeping the implant spacing small (13 microns).

Pixel Cell Layout

One of four detector diodes

One of twelve D flip-flops arranged around perimeter of pixel cell

All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

26 microns

4K Pixel Design in OKI Process

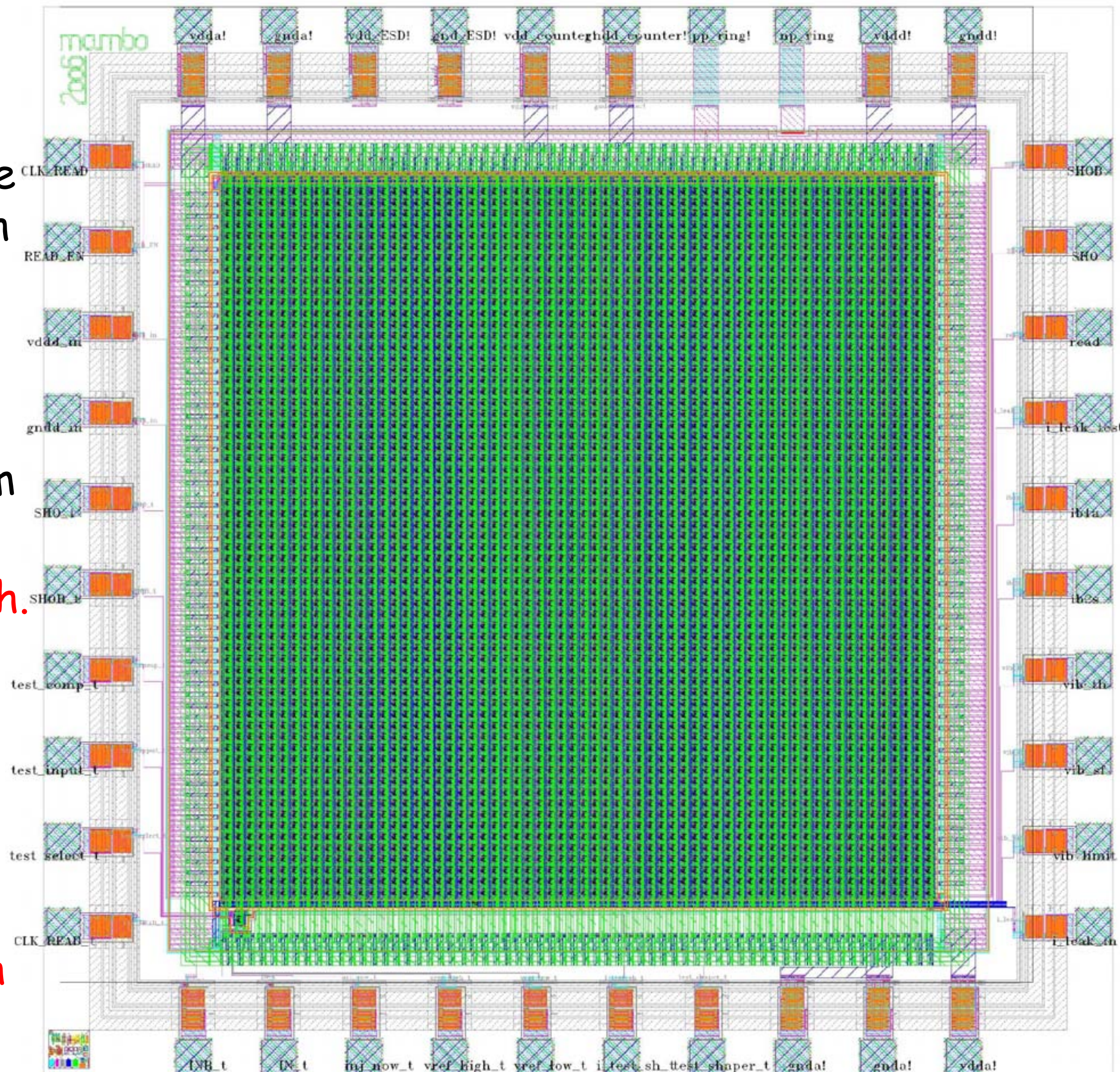
Chip name is MAMBO:

Monolithic Active pixel Matrix with Binary cOunters

Chip size:
64 x 64 array
2.5 mm x 2.5 mm

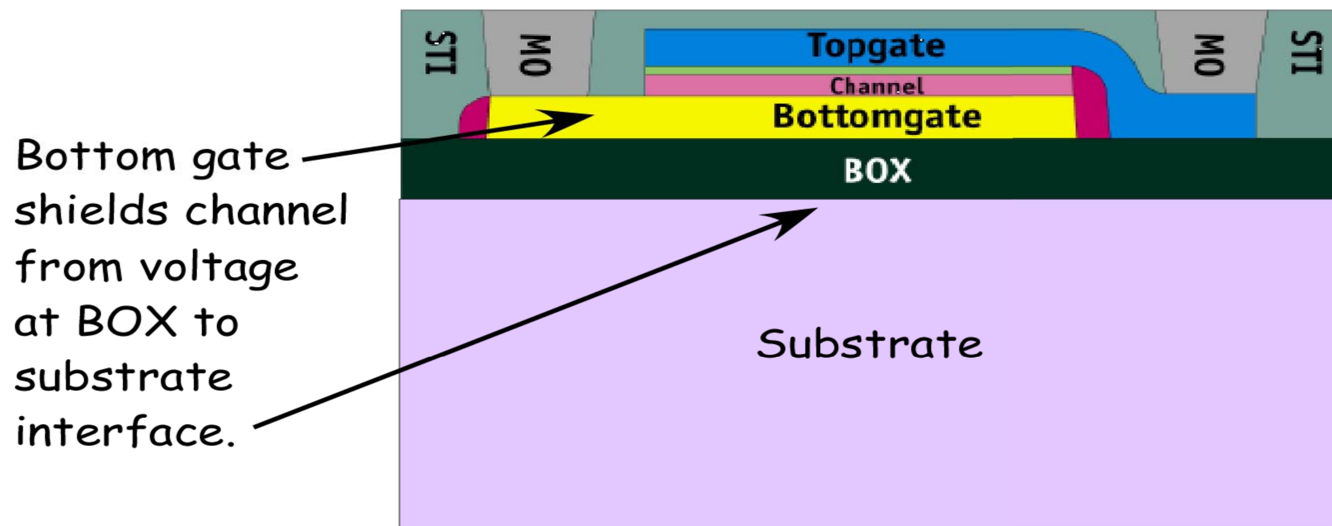
Chip due in March. Will examine crosstalk issues and check rad tolerance.

Designed by Gregory Deptuch



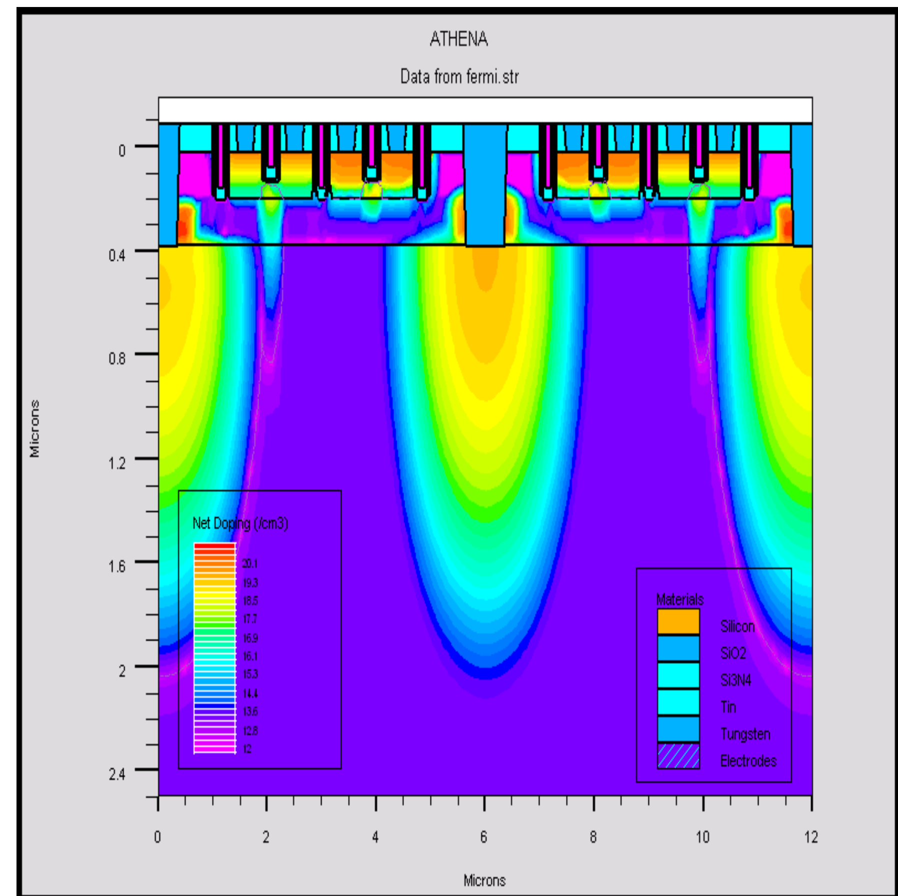
ASI Process

- ASI process based on dual gate transistor called a Flexfet.[4]
  - Flexfet has a top and bottom gate.
  - Bottom gate shields the transistor channel from charge build up in the BOX caused by radiation.
  - Bottom gate also shields the transistor channel from voltage on the substrate and thus removes the back gate voltage problem.



Design in ASI Process

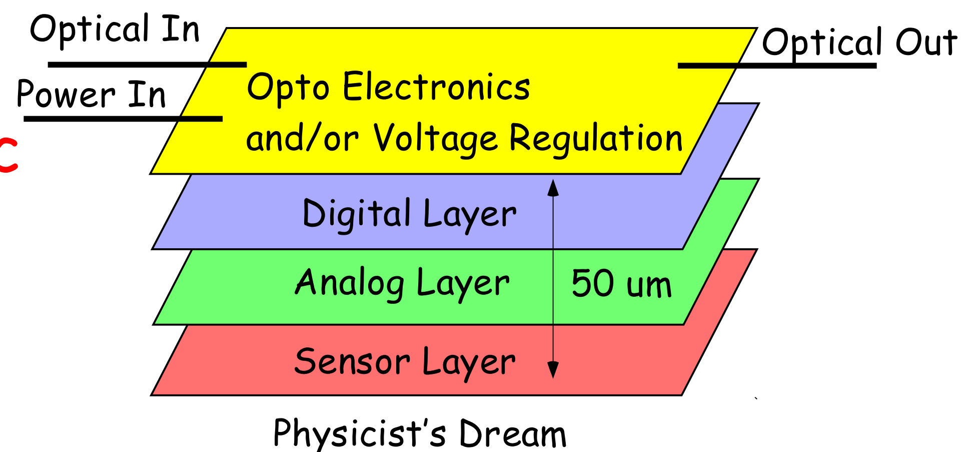
- US Department of Energy Small Business Innovation Research (SBIR) phase 1 funding
- Modeling and process simulation of a thinned, fully depleted sensor/readout device.
- Studies of backside thinning, implantation, and laser annealing.
- Circuit design for ILC vertex detector in progress.



Diode simulation in Flexfet process

Vertical Scale Integration (3D)

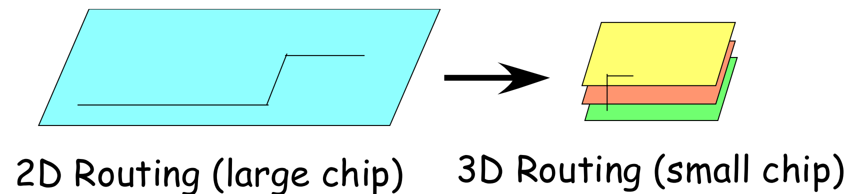
- SOI detector technology offers several advantages over MAPS.
- 3D offers advantages over SOI detectors
  - Increased circuit density due to multiple tiers of electronics
  - Independent control of substrate materials for each of the tiers.
  - Ability to mate various technologies in a monolithic assembly
    - DEPFET + CMOS or SOI
    - CCD + CMOS or SOI
    - MAPS + CMOS or SOI



Physicist's Dream

3D Integrated Circuits

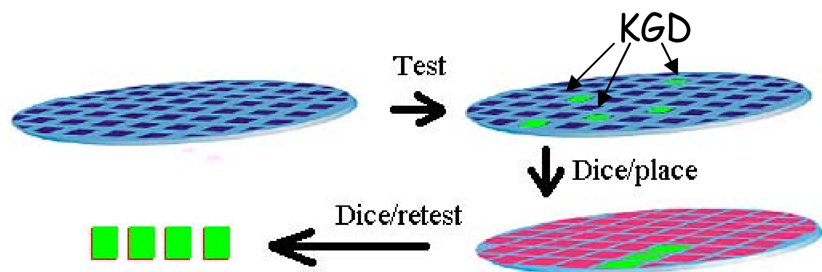
- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance. (Performance limited by interconnect)
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



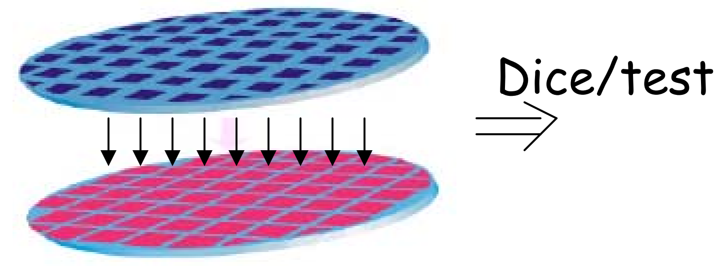
- HEP should watch industry and take advantage of the technology when applicable.
- Numerous examples of industry produced devices.[5,6,7] (See backup slides)

Two Different 3D Approaches for HEP

- Die to Wafer bonding
  - Permits use of different size wafers
  - Lends itself to using KGD (Known Good Die) for higher yields
- Wafer to Wafer bonding
  - Must have same size wafers
  - Less material handling but lower overall yield



Die to wafer bonding



Wafer to wafer bonding

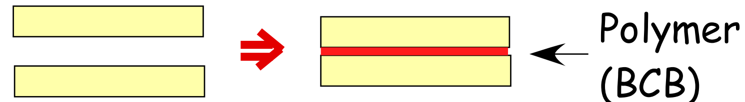
Key Technologies for 3D

- There are 4 key technologies
  - Bonding between layers
  - Wafer thinning
  - Through wafer via formation and metalization
  - High precision alignment
- Many of these technologies are also used in the development of SOI detectors

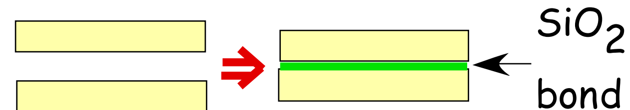
Key Technologies

1) Bonding between Die/Wafers

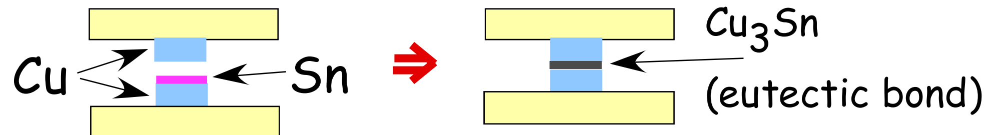
a) Adhesive bond



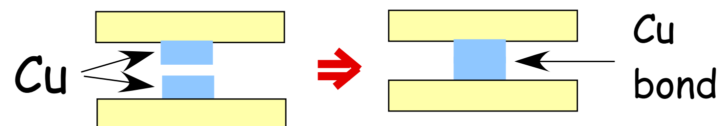
b) Oxide bond (SiO2 to SiO2)



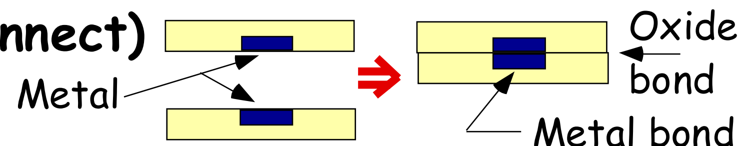
c) CuSn Eutectic



d) Cu thermocompression



e) DBI (Direct Bond Interconnect)

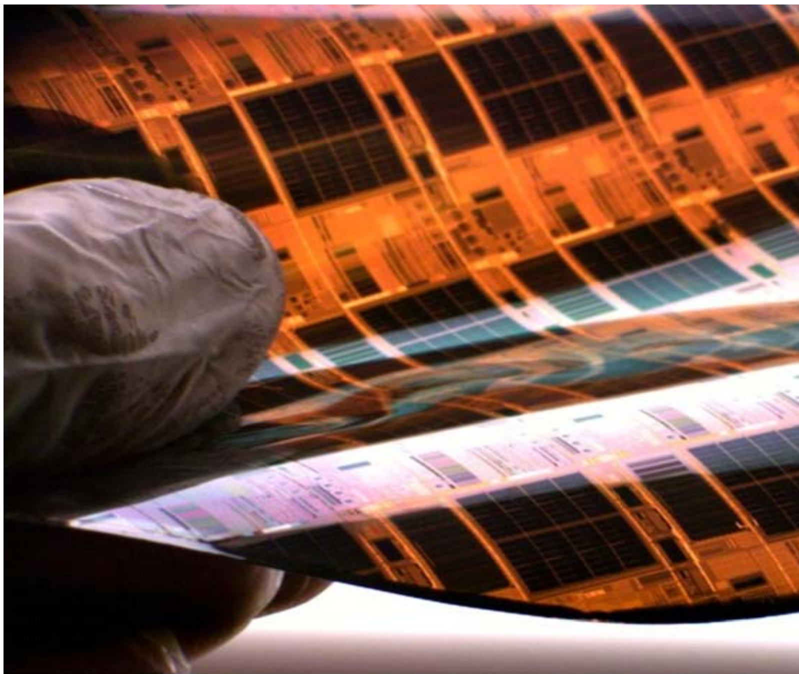


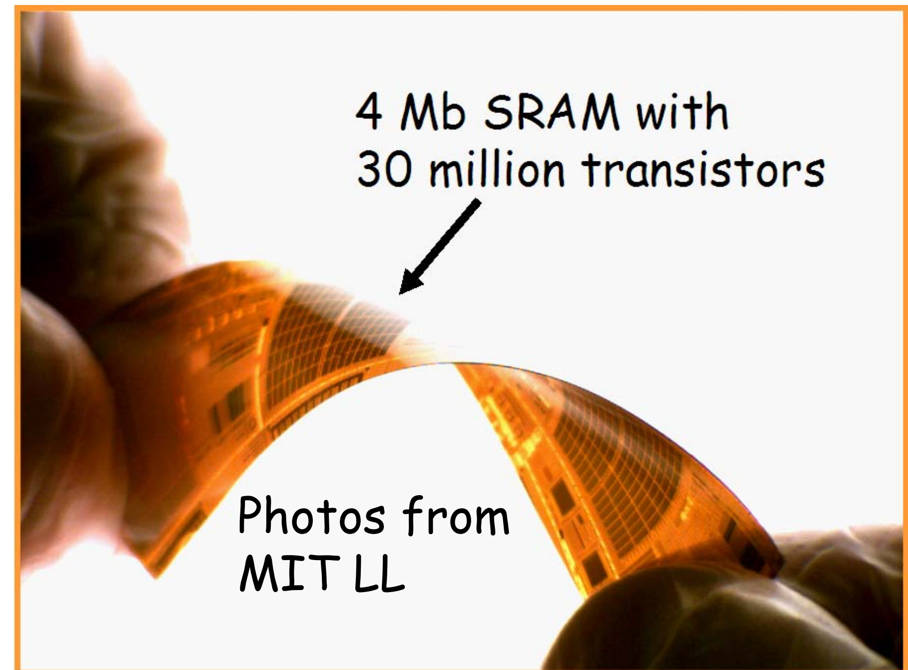
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

Key Technologies

2) Wafer thinning

Through wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area associated with the via as small as possible, the wafers should be thinned as much as possible. Thinning is typically done by a combination of grinding, lapping, and chemical or plasma etching.





Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

Key Technologies

3) Via formation and metalization

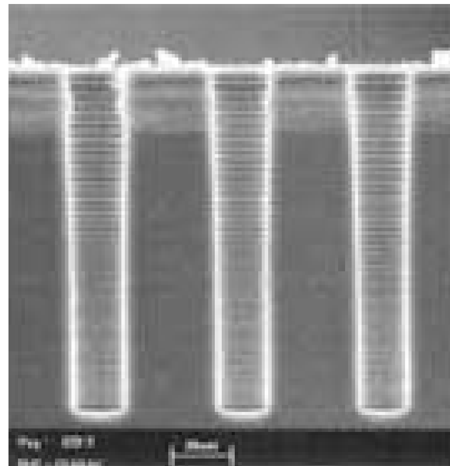
Two different proceedures are generally used:

Via First - vias holes and via metalization take place on a wafer before wafer bonding.

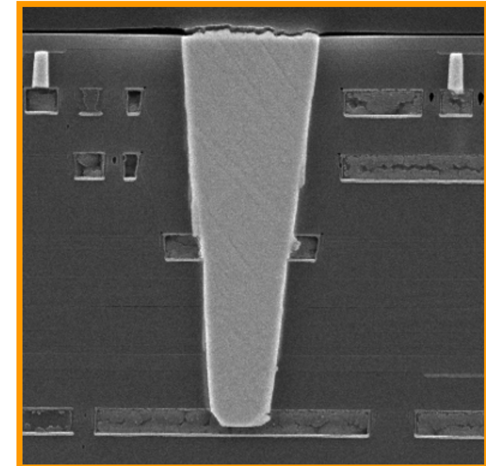
Via Last - vias holes and via metalization take place on a wafer after wafer bonding.

Vias in CMOS are formed using the Bosch process and must be passivated before filling with metal while Vias in SOI are formed using an oxide etch are filled without passivation.

SEM of 3 vias using Bosch process[8]



Via using oxide etch process (Lincoln Labs)



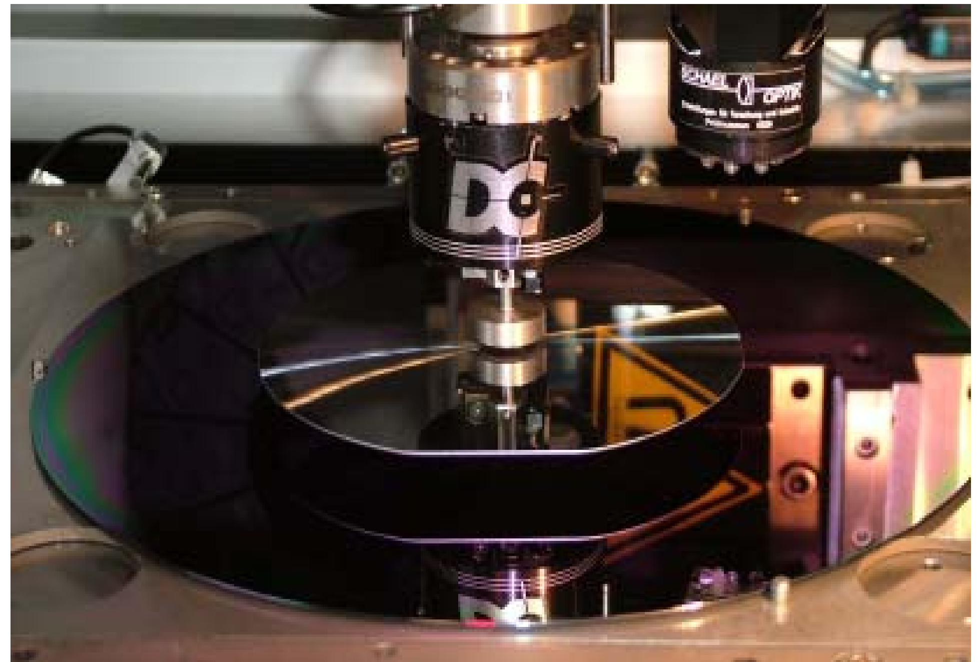
Typical diameters are 1-2 microns

Key Technologies

4) High Precision Alignment

Alignment for both die to wafer and wafer to wafer bonding is typically better than one micron. (Photos by Ziptronix.)

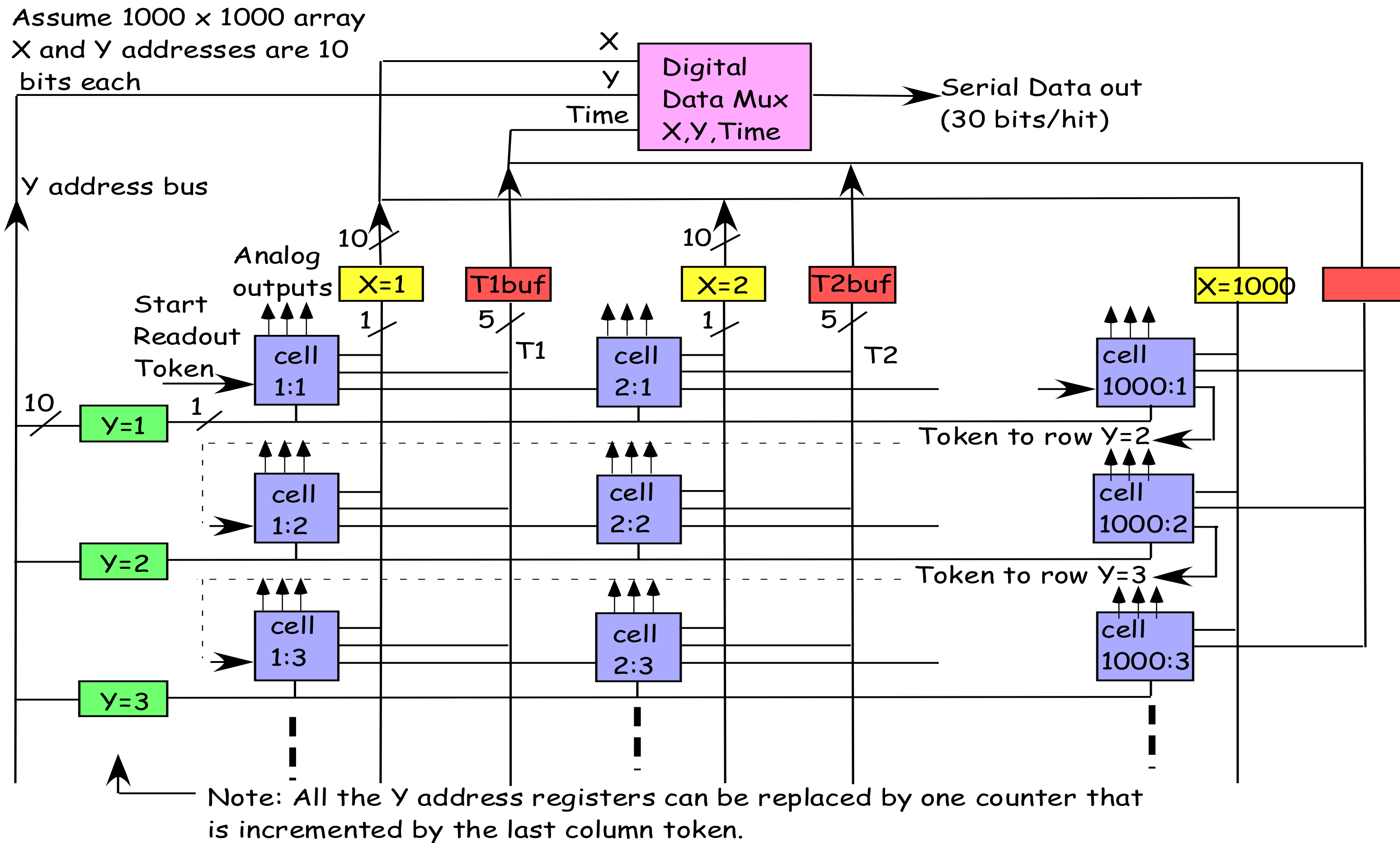
Die to Wafer alignment and placement



Wafer to Wafer alignment and placement

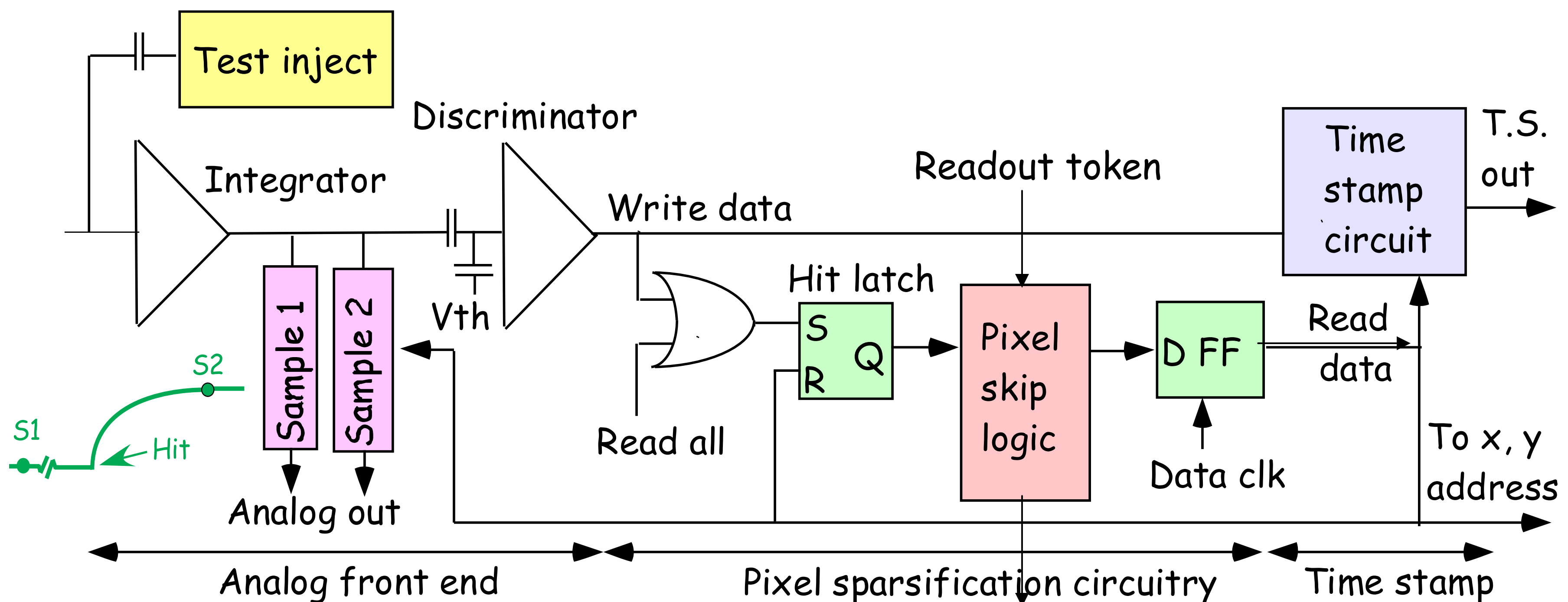
3D Pixel Design for ILC Vertex[9]

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
  - Key features: Analog pulse height, sparse readout, high resolution time stamps.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- 64 x 64 pixel demonstrator version of 1k x 1K array.
- Submitted to 3 tier multi project run. Sensor to be added later.



Simplified Pixel Cell Block Diagram

- When a Hit occurs, the Hit pixel stores Sample 1 & 2 and the Time Stamp, and sets the Hit Latch in sparse readout circuit.
- During readout, when the read out token arrives, the time stamp and analog values are read out, and pixel points to hit address found on perimeter of chip.
- While outputting data from one pixel, the readout token is passed ahead looking for next pixel that has been hit.

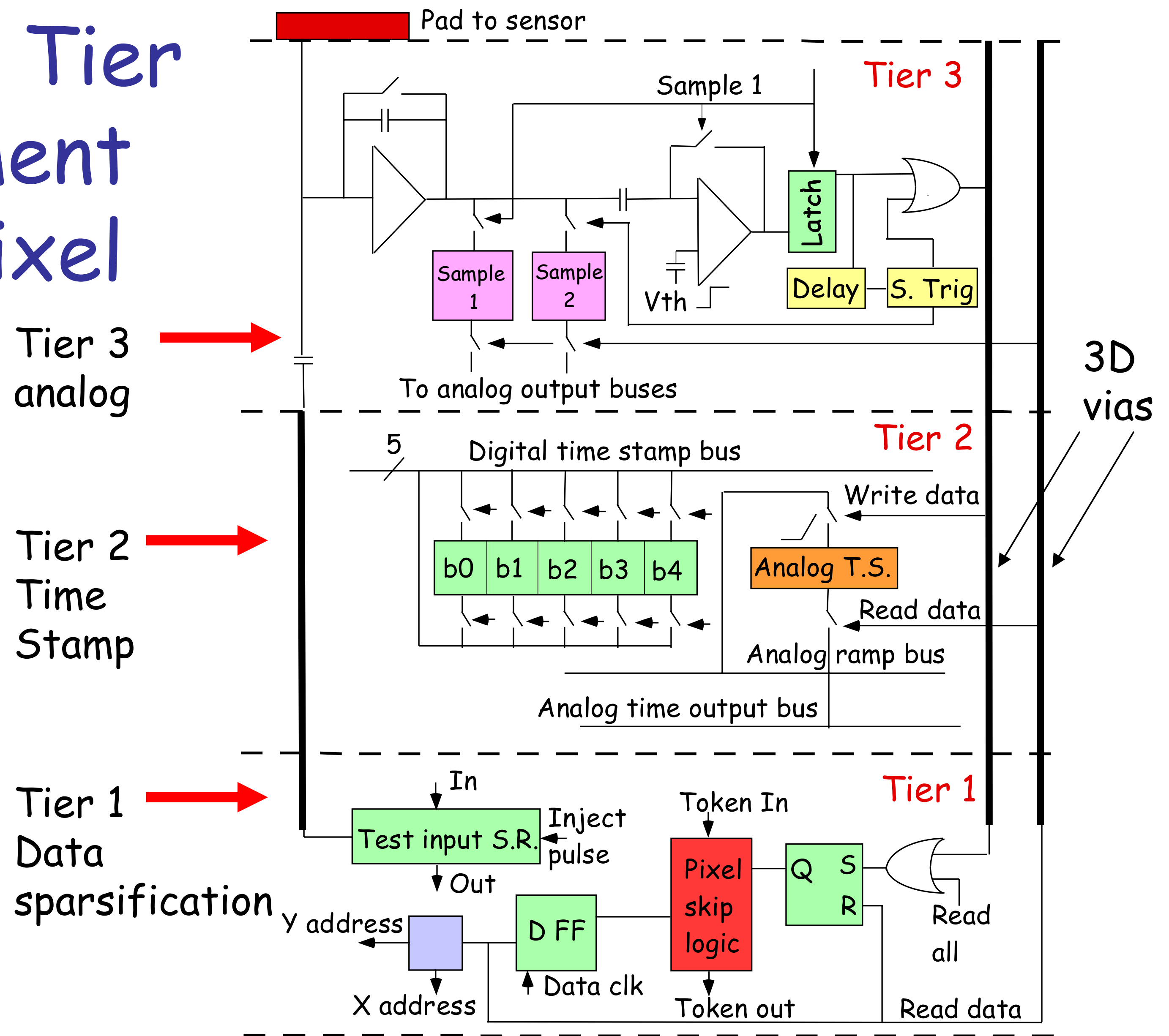


3D Three Tier Arrangement for ILC Pixel

Tier 3 analog

Tier 2 Time Stamp

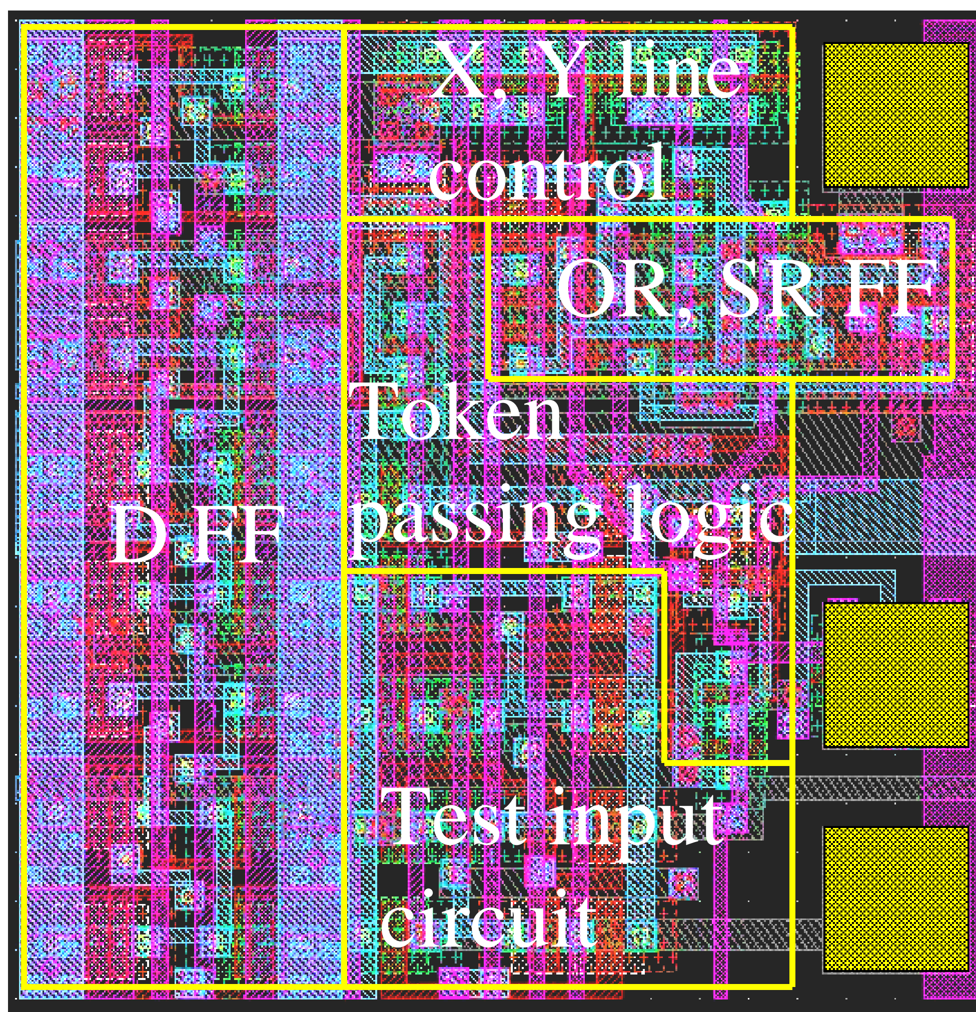
Tier 1 Data sparsification



Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff

Tier 1 - Sparsification

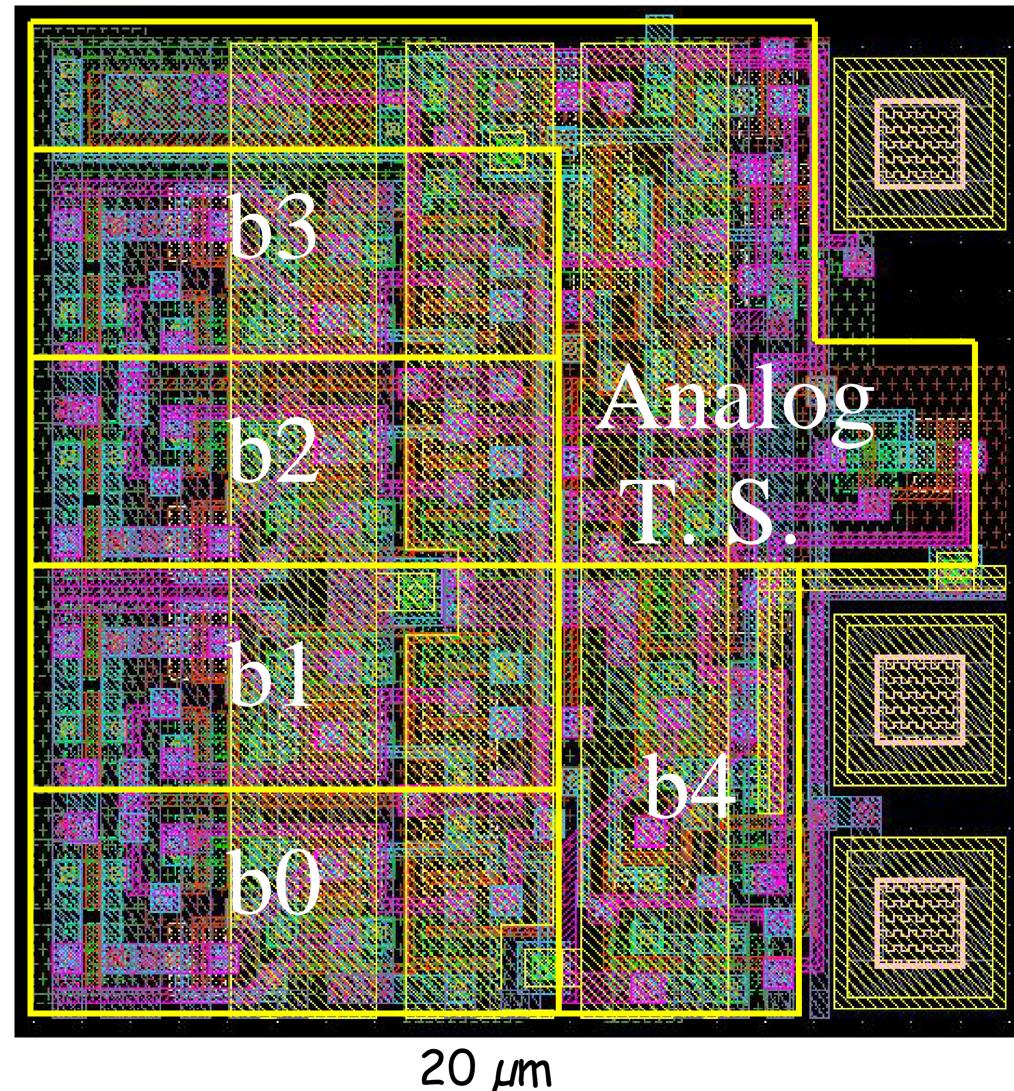
- OR for READ ALL cells
- Hit latch (SR FF)
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



20 μm

Tier 2 - Time Stamp

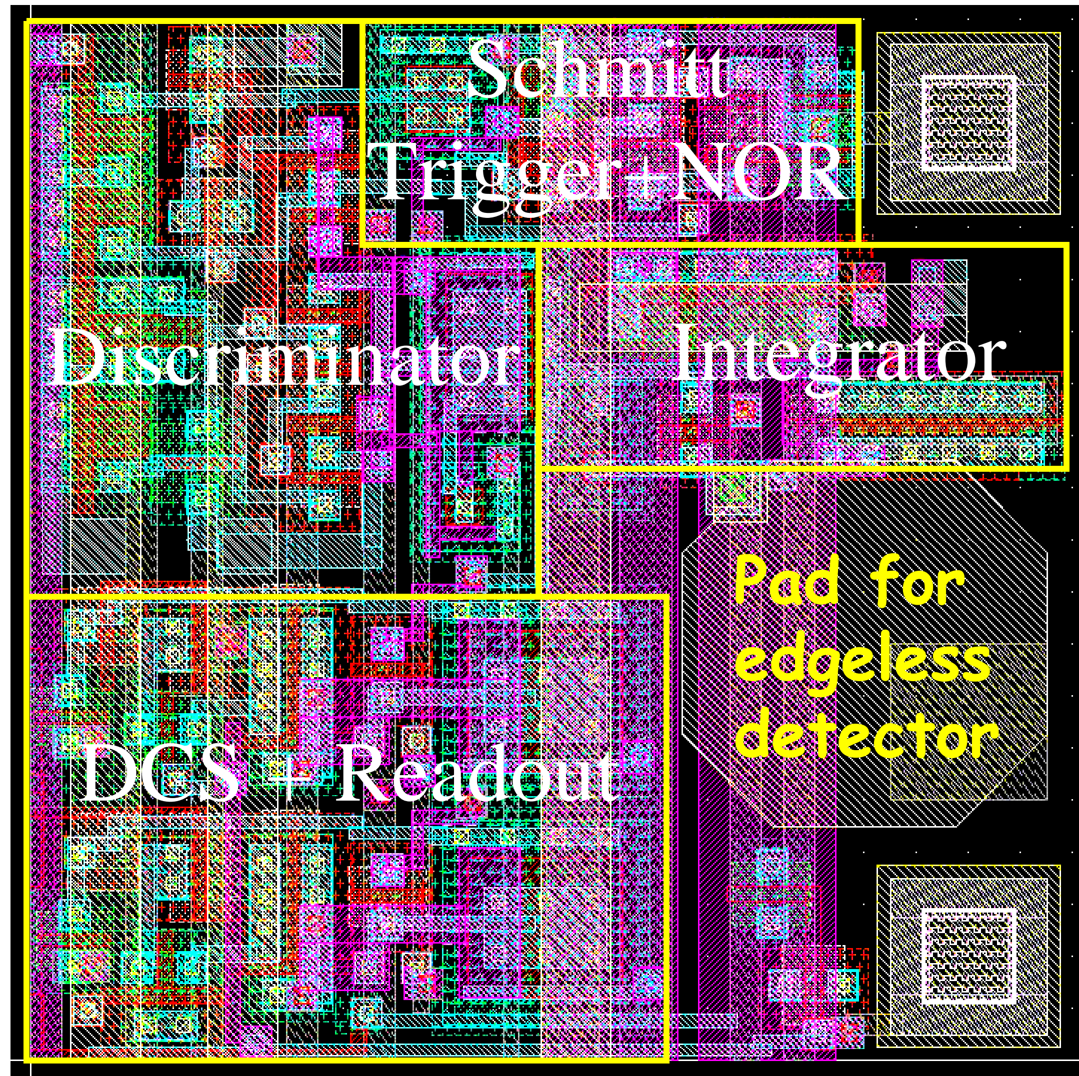
- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Gray code counter on periphery
- 72 transistors
- 3 vias



20 μm

Tier 3 - Analog

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input
- 38 transistors
- 2 vias

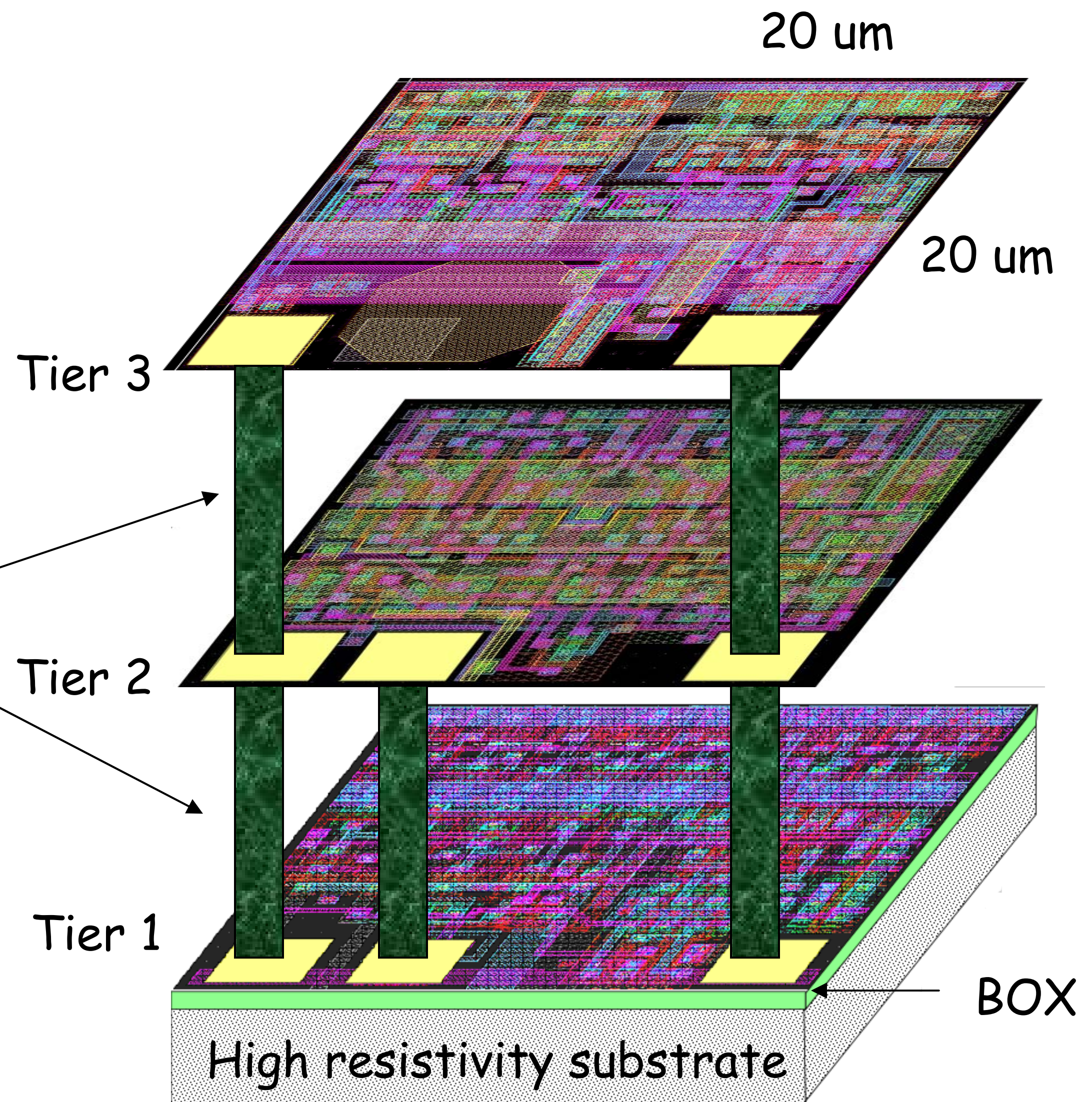


3D Stack with Vias

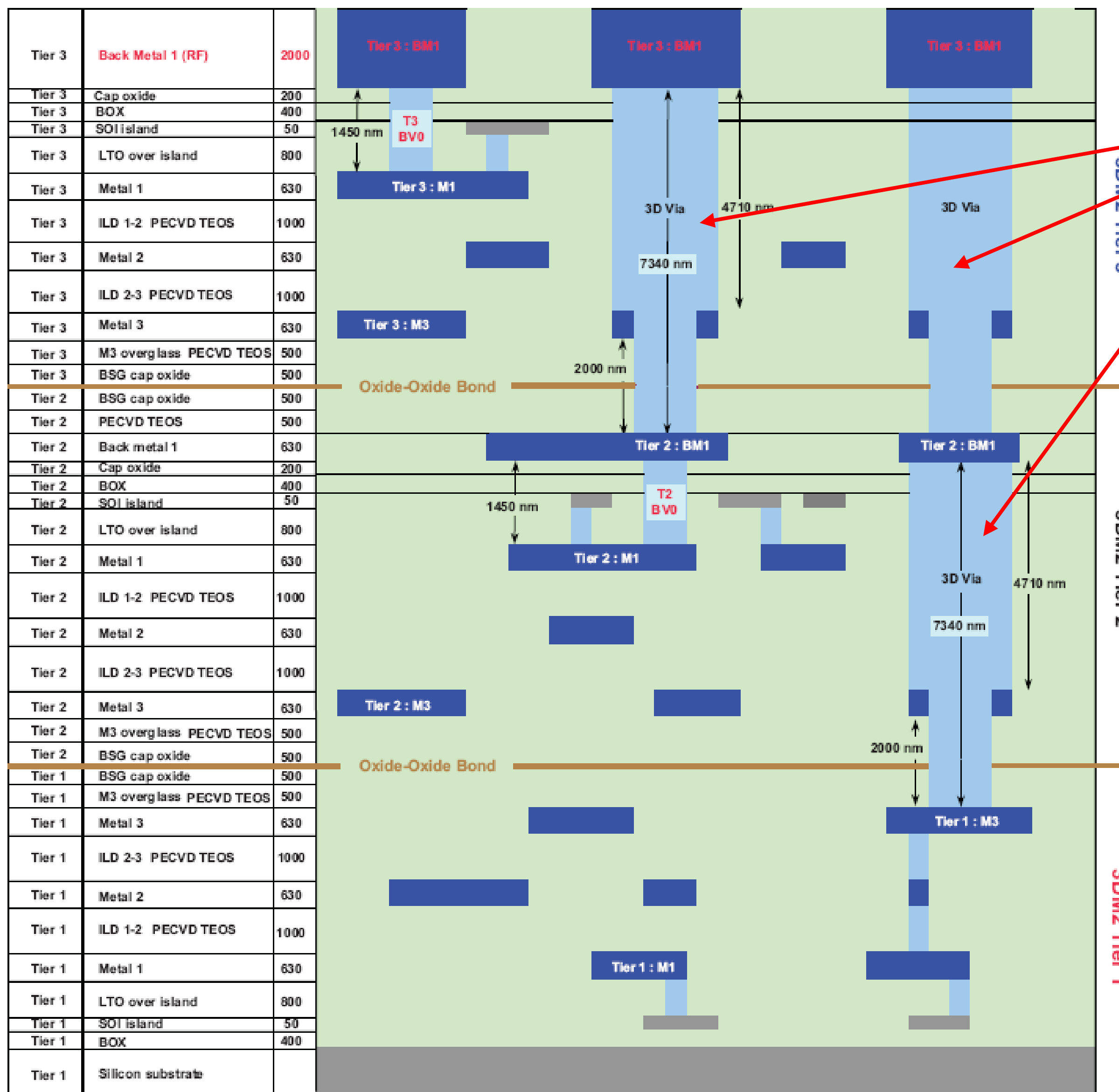
Pixel cell:
*175 transistors in 20 μm pixel.
*Unlimited use of PMOS and NMOS.
*Allows 100 % diode fill factor.

Vias: 1.5 um dia by 7.3 um long

Chip is due back in August. Issues to be studied include analog performance, yield, and radiation tolerance.



MIT LL 3D Multiproject Run Chip Cross Section



3D vias

8.2 µm

7.8 µm

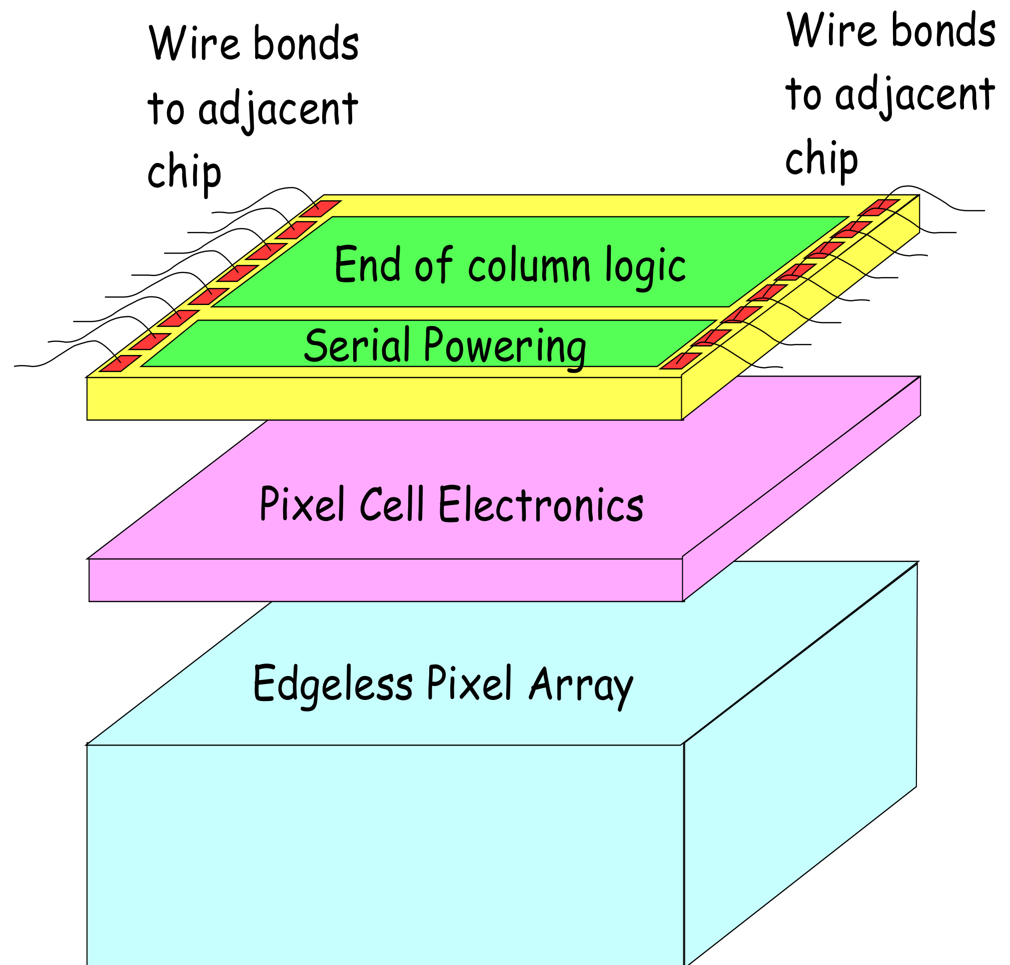
6.0 µm

Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

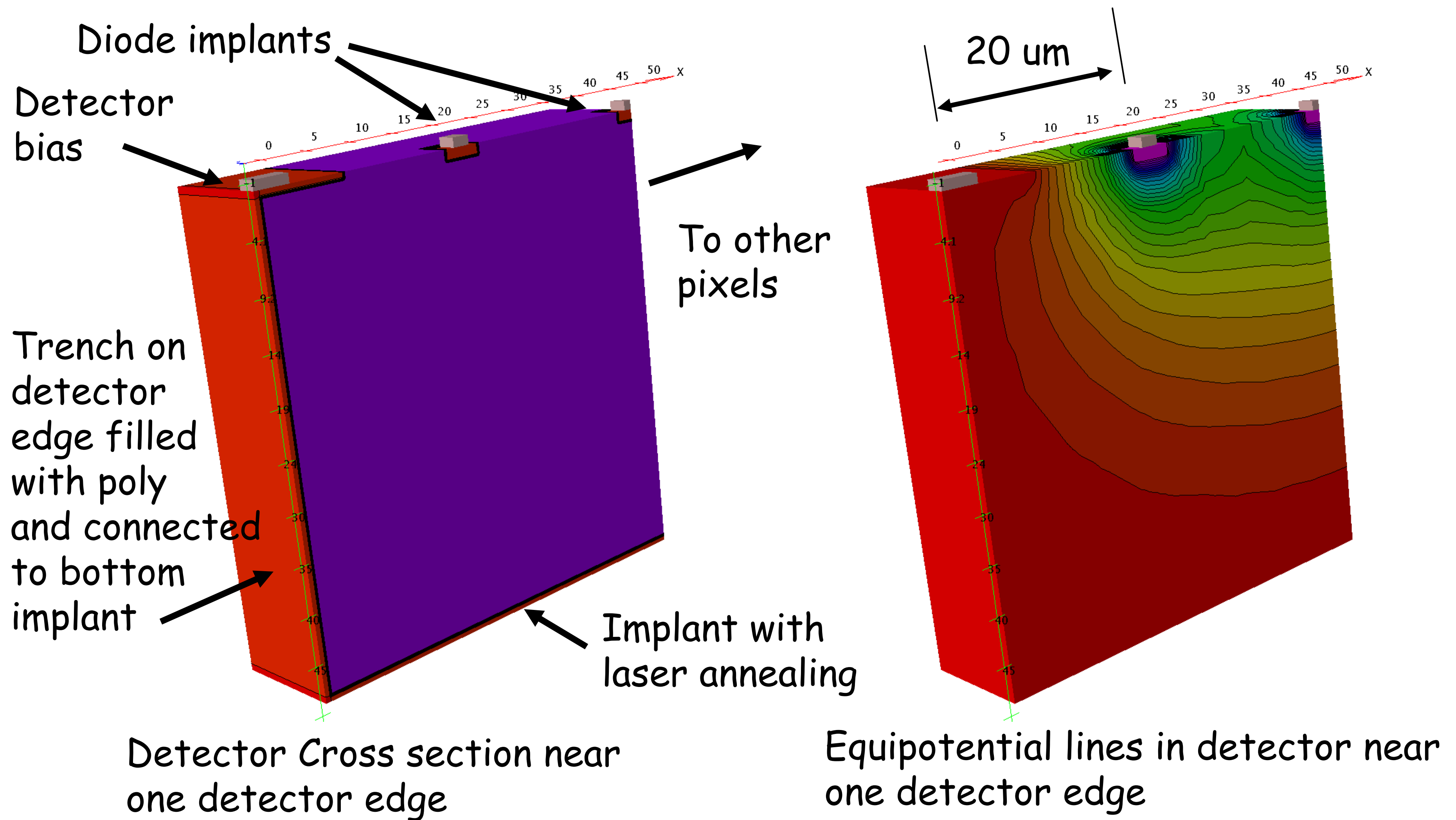
The MIT LL process description is given in a backup slide.

Possible Application to SLHC Pixels

- Future pixel upgrades will look for
  - Less mass
    - Thinner sensors (lower V)
    - Less copper
  - More complexity
    - Higher readout speed
    - More functionality
  - May want smaller pixels for reduced noise to go along with smaller detector signal.
- Use serial powering for pixel Read Out chip.
- 3D allows for creative solutions, e.g.
  - Accommodates serial powering
  - Higher functionality/area
  - Thinner assemblies
  - Allows use of edgeless detectors



Edgeless Detector Concept



Summary

- Progress is being made to integrate sensors and readout electronics in a monolithic structure for pixels.
- Commercial foundries are starting to develop SOI detectors and ROICs.
  - OKI, ASI, and perhaps Hammamtsu
  - May have limited radiation tolerance but sufficient for most applications.
- 3D is being pursued by many commercial organizations[9]
  - HEP groups are beginning to look at 3D technologies
    - MPG in Munich is starting an activity to bond pixel sensors to ROICs and is looking for interested partners.[10]
    - Group at Strasbourg is starting to look at wafer bonding techniques.[11]
  - Expensive but offers a great deal of design flexibility.
  - Use of CMOS provides very rad hard parts.
  - Can be used with a variety of current approaches for vertex detectors, MAPS, DEPFET, etc.
- These new technologies offer new opportunities for difficult applications that can't be satisfied with older approaches.

Acknowledgements

- I want to thank the designers of the Fermilab chips mentioned in this talk
  - Grzegorz Deptuch
  - Jim Hoff
  - Tom Zimmerman
- And also thank members of the ILC pixel design group at Fermilab for their helpful comments in preparing this talk.

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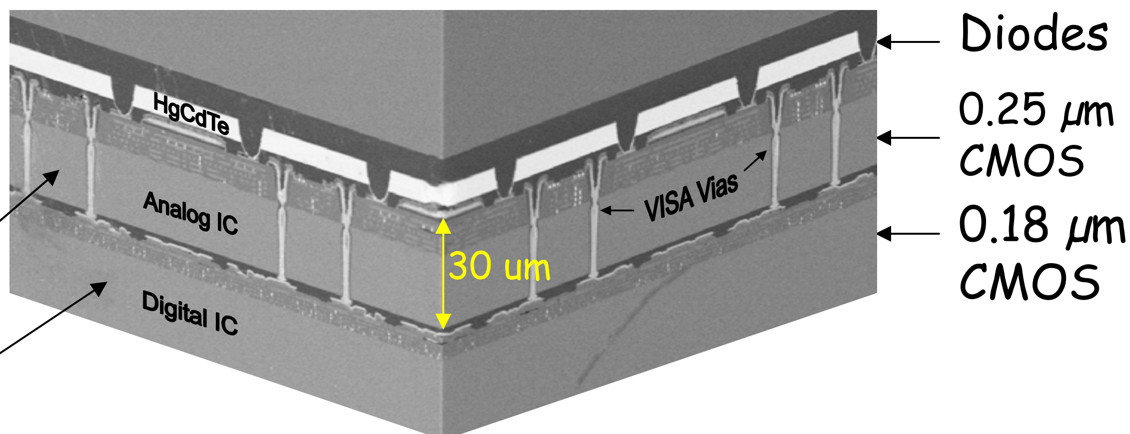
- 9) "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", R. Yarema, ILC Vertex Workshop, Ringberg Castle, Tegernsee, Germany, May 29-31, 2006.
- 10) "R&D on thin pixel sensors and a novel interconnection technology for 3D integration of sensors and electronics", R. Nisius and Hans-Gunther Moser, Max Planck Gesellschaft, January 19, 2007.
- 11) Private communication with Wojtek Dulinski, March 6, 2007.

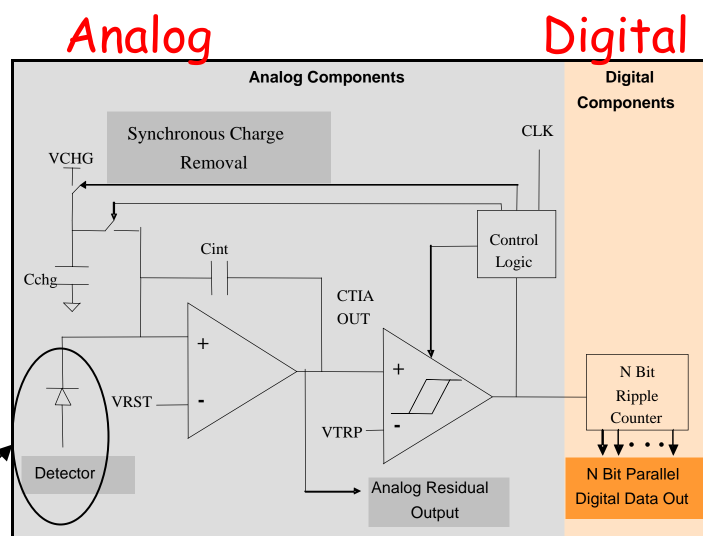
Back Up Slides

RTI 3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor

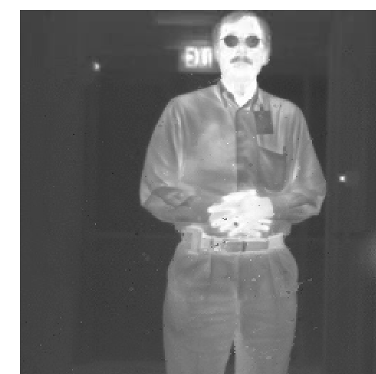


Array cross section



Diode

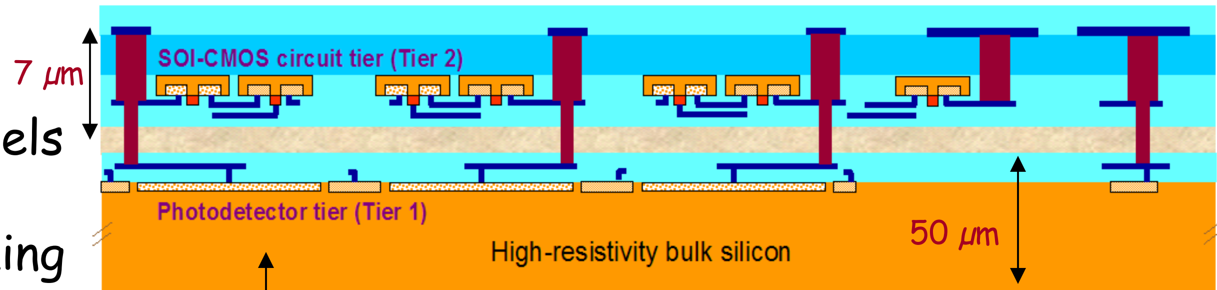
3 Tier circuit diagram

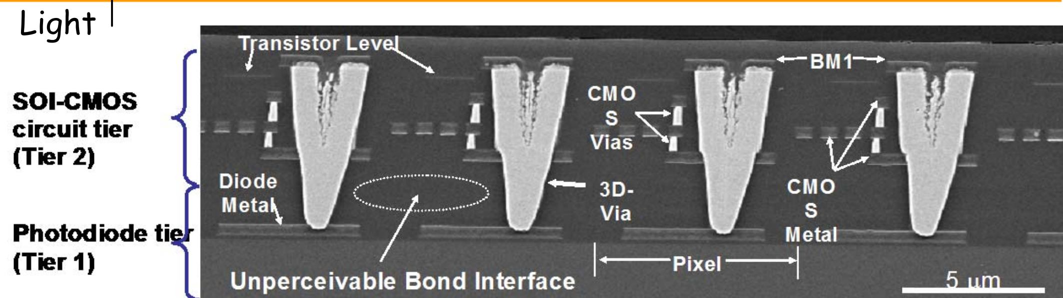


Infrared image

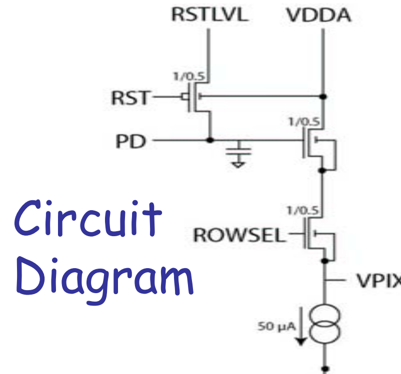
MIT LL3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section



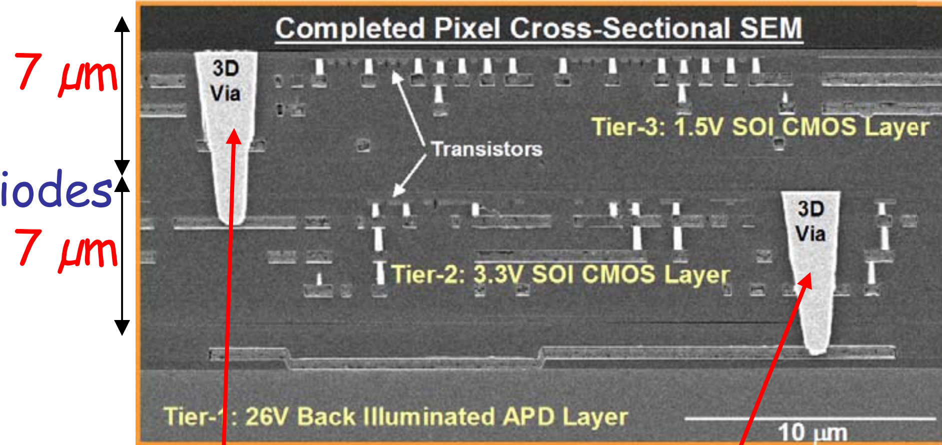
Circuit Diagram

Image

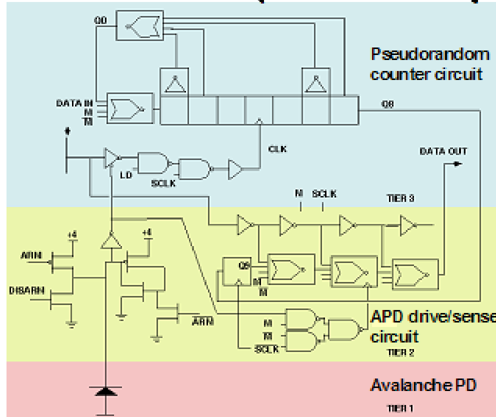
MIT LL 3D Laser Radar Imager

64 x 64 array, 30 μm pixels
3 tiers
- 0.18μm SOI
- 0.35 μm SOI
- High resistivity substrate diodes

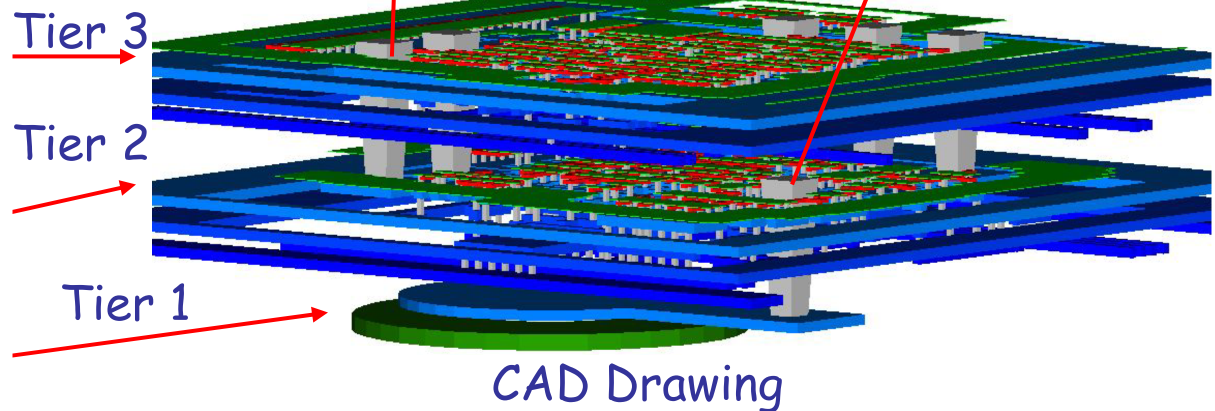
Oxide to oxide wafer bonding
1.5 μm vias, dry etch
Six 3D vias per pixel



SEM Cross section



Schematic

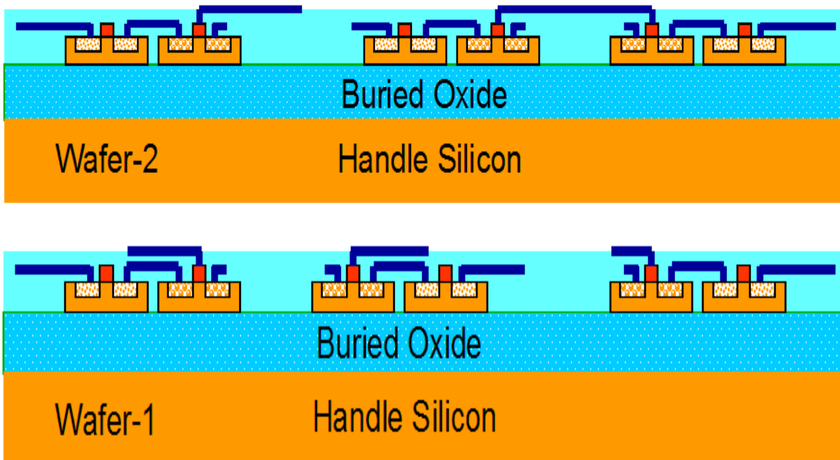


CAD Drawing

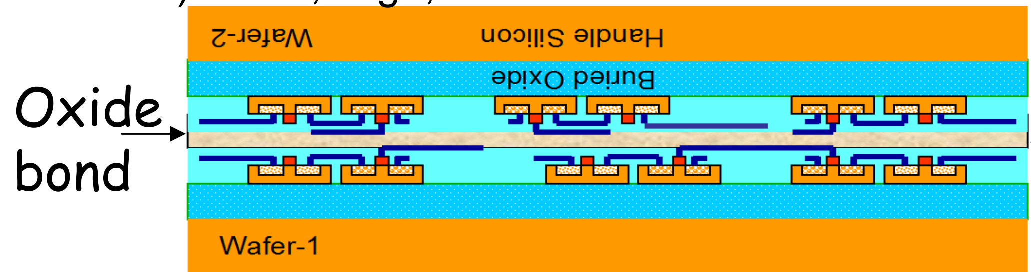
Process Flow for MIT LL 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

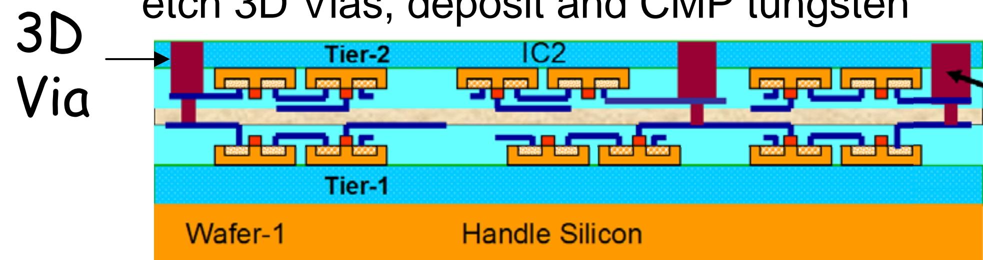
1) Fabricate individual tiers



2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3