Challenges in Front-end Electronics for Future HEP Experiments

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Fermilab

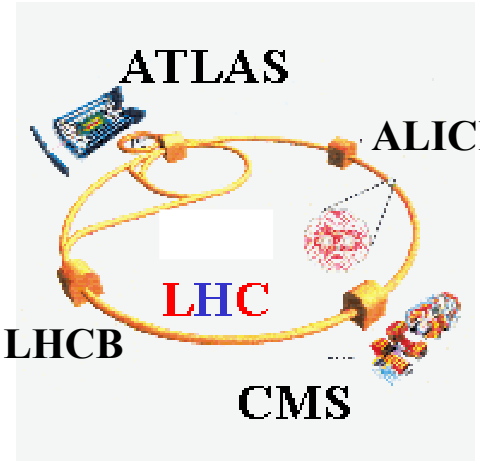
Batavia, Illinois

14th International Workshop on Vertex Detectors

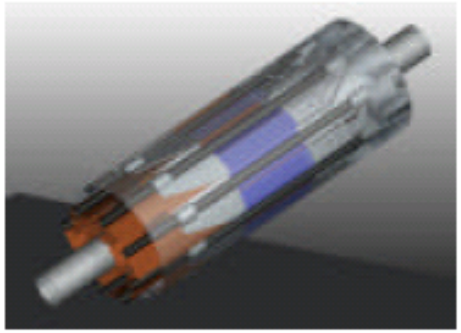
Nikko, Japan, November 2005

Where is the Future?

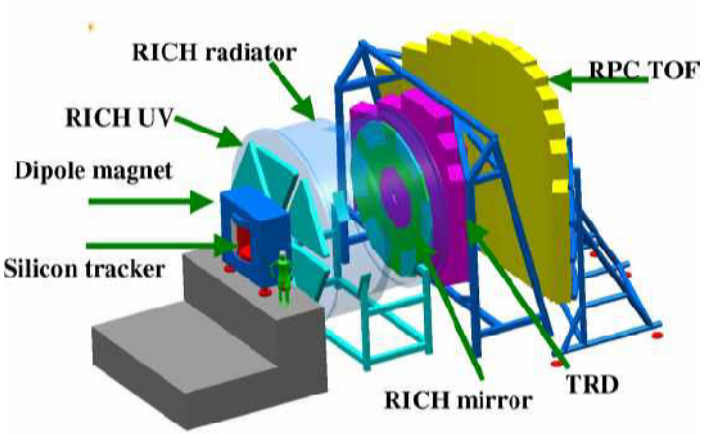
T2K/NOvA, Japan/USA, 2009



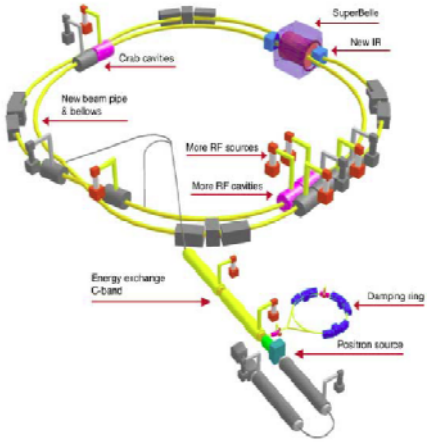
SLHC, CERN, 2015



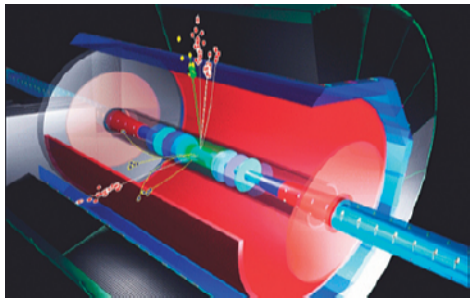
STAR/Phenix upgrade, BNL, 2011



CBM, Darmstadt, 2015



SuperBELLE, KEK, 2012



DESY, Hamberg

ILC, ?, 2015

What are the Challenges?

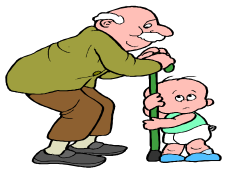
- The "Big Four" technical challenges
  - *Lower power*

  - *Less Mass (high density)*

  - *Higher Radiation tolerance*

  - *Higher speed/performance*

- The practical challenges
  - *Process obsolescence*
  - *Cost and complexity of new processes*



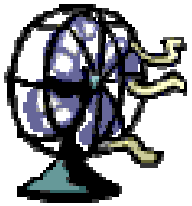
- Any one of these could be a talk by itself
- Can only discuss a few thoughts for each

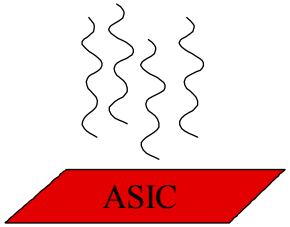
Lower Power

- Front end electronics channel count continues to increase.

  e.g. SLHC, ILC, Super Belle

  – Higher channel counts increases power which increases cooling needs
  – Added cooling means more mass

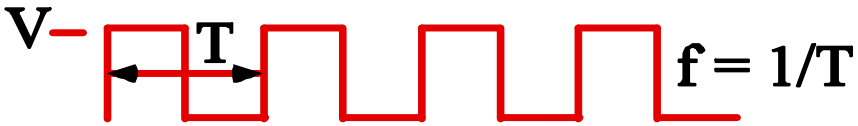




- Approaches to consider for reducing analog and digital power
  – Reduce power supply voltage
  – Power down
  – Change design approach
  – Serial powering (to be discussed in section on mass)

Digital Power Reduction

- Digital Power can be reduced by going to lower voltage (smaller feature size processes)
- CMOS logic power is proportional to CV^2f (neglecting the transconductance power and leakage current power)



  - Going from 0.25 μ to 0.13 μ reduces the power supply voltage from 2.5 to 1.5 V which reduces power by $(2.5/1.5)^2 = 2.77$ at fixed frequency
  - In a very tightly packed digital circuit where trace length (capacitance) is small compared to gate capacitance, C goes down. (Although the gate capacitance per unit area goes up, the gate area goes down resulting in a net decrease in C of about 1.73 for a given complexity)
  - Thus ideally, power could be reduced by 2.77 x 1.73 = 4.8 by going from 0.25μ to 0.13 μ.
  - Unfortunately, frequency is often increased in DSM designs, limiting the power savings.
- Since the transistor leakage current is usually low, there is no significant advantage in reducing the power supply voltage during periods of non-digital activity.

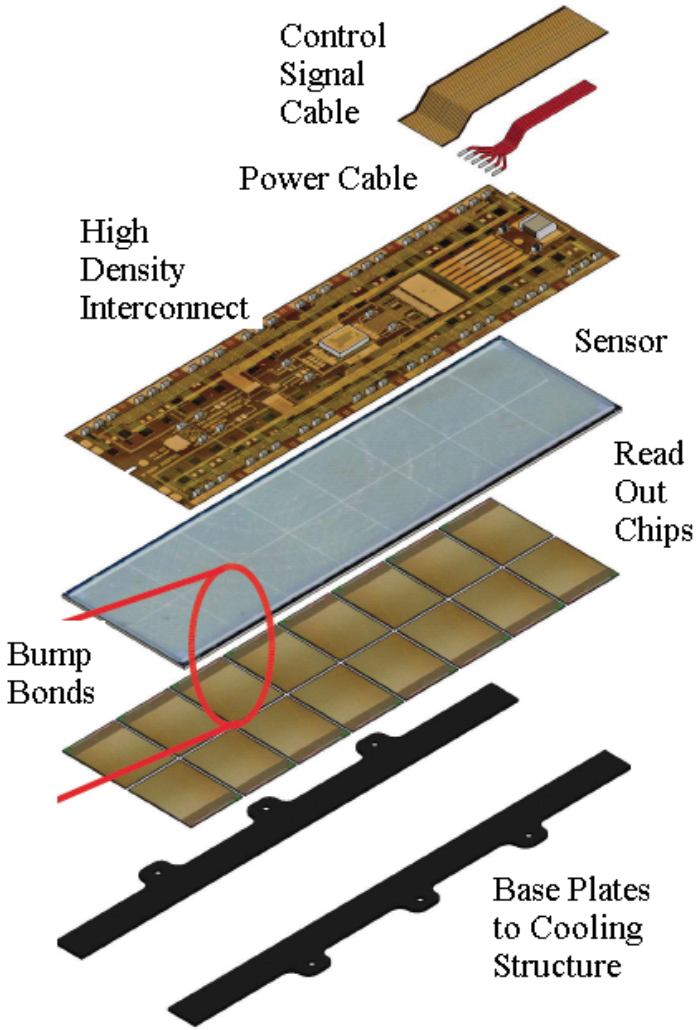
Analog Power Reduction

- Analog power can also be reduced by going to lower voltage (smaller feature size processes).
- Power in analog sections is I_{rms} x V
  - Going from 0.25 μ to 0.13 μ reduces the power supply voltage from 2.5 to 1.5 V which ideally reduces power by (2.5/1.5) = 1.66, assuming constant current.
  - In practice, the current in the analog section may actually be increased to compensate for lower dynamic range. Thus the power savings in the analog section is not as dramatic as in the digital section.
- Since analog circuits draw current even when quiescent, significant power savings can be achieved by ramping the analog voltage off during periods of inactivity. Power reduction = 1/duty cycle.
  - This approach has been used in Babar and is being considered for the ILC.
  - ***Challenge is to insure that circuits are stable and ramped currents do not interfere with system operation.***

- Another approach is to eliminate as many analog circuits as possible – go digital as soon as possible.
  - ***Challenge is to live without analog signal information for as many systems as possible.***

Less Mass

- Scattering from vertex and track detectors poses a serious problem for future HEP experiments
  - Currently the best hybrid pixel and silicon strip front ends have about 1% - 2% X_0
    - Includes silicon
    - Cabling, HDI, cooling, and support
  - Goal for some future experiments is a factor of 10 improvement or 0.1% X_0 (100 microns of silicon)
    - One approach is to reduce power so less mass is need to extract heat from the detector – this option already discussed
    - Some other approaches to reducing mass
      - Series powering of modules
      - Thin silicon (detectors, ROC)
      - Monolithic Active Pixels
      - 3D circuits



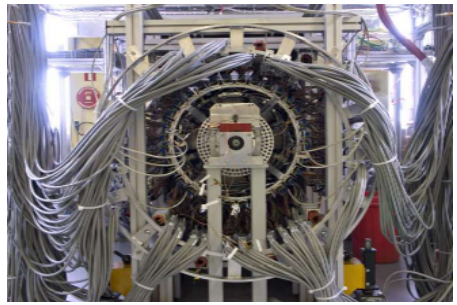
CMS Barrel Pixel Module

C. Hoermann, PSI

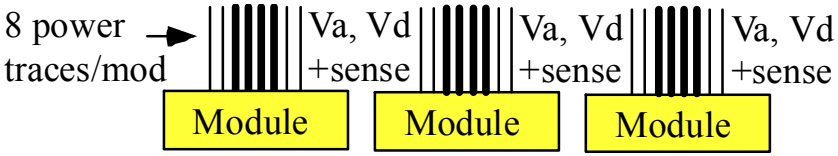
Serial vs Parallel Powering of High Density Detectors

Cables represent a significant portion of the mass in a high density detector (silicon or pixel).
Use the ATLAS pixel detector as an example

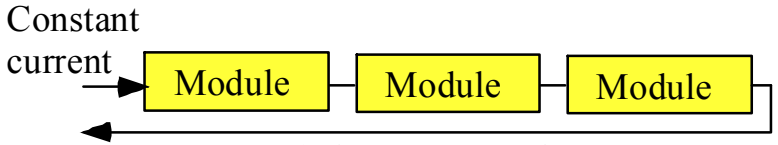
Cables in the active region = 0.073%X_0
In addition, power in cables to a 13 module ladder is 281% of power in the modules.


ATLAS SCT

For upgrades to present systems or new lower mass systems, the problem requires a new ideas – Serial Powering.



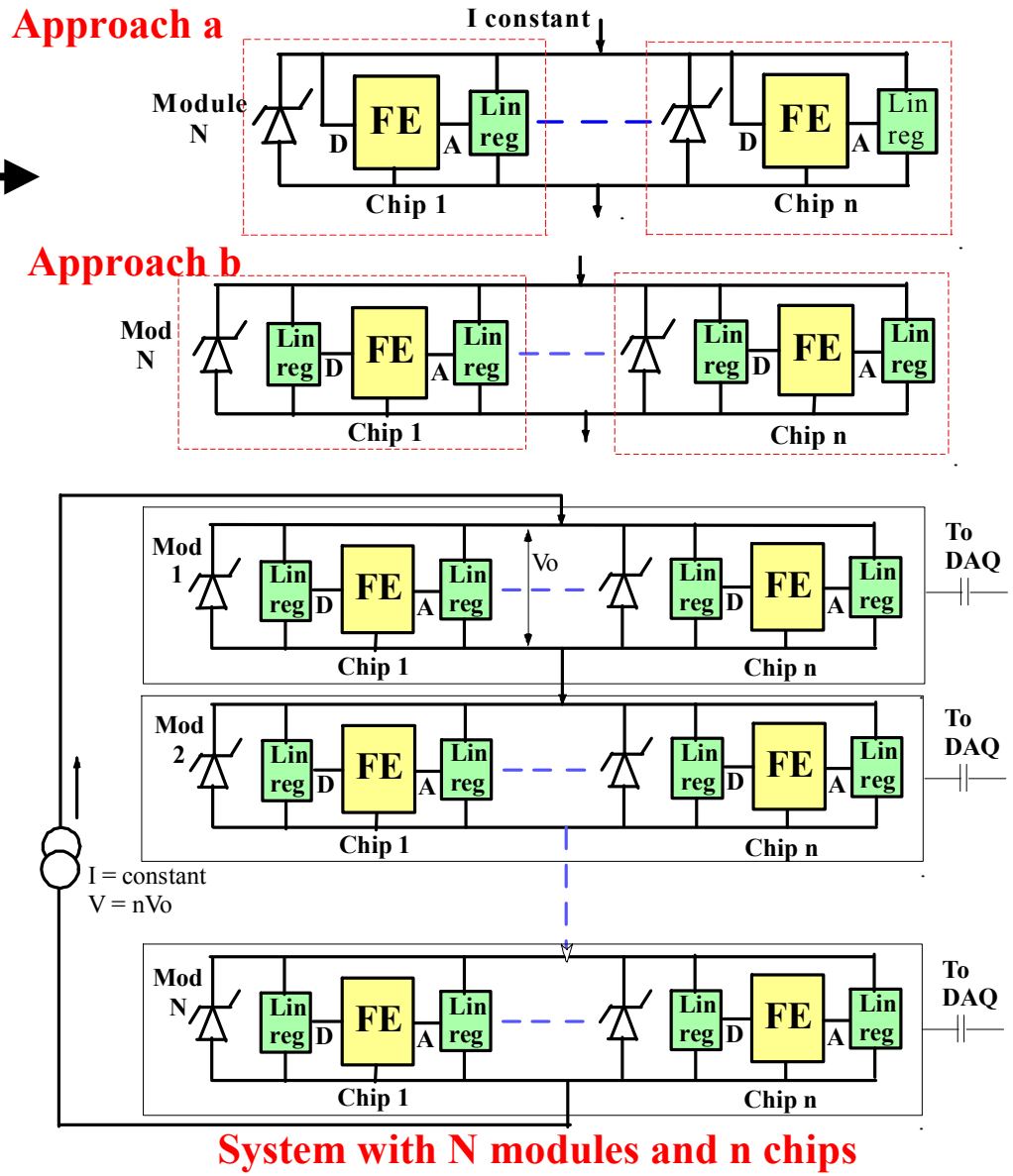
Parallel Power Scheme



Serial Power Scheme

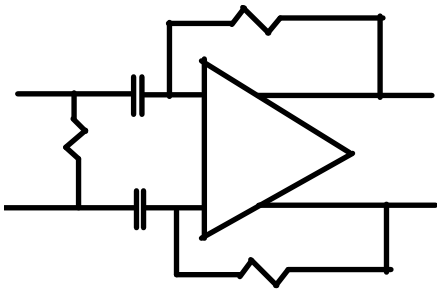
Serial Power

- Serial voltage regulators
  - Several approaches have been examined using shunt and linear regulators. Here are two.
- Consider advantages to ATLAS pixels
  - Number of power cables reduced by factor of 50 (lower mass, cost)
  - Radiation length/layer due to cables is reduced by factor of 6.5
  - Power dissipated in cables reduced by factor of 10 (Reduced heat pickup in other detector systems)
  - Voltage regulation done locally gives better dynamic performance
  - Lower power supply cost

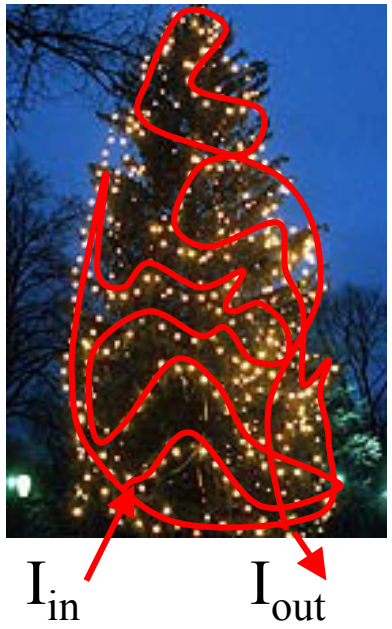


Serial Power

- Disadvantages
  - Slightly higher dissipation in chip
  - AC coupled output needed to/from module
    - Added buffer and components on module
- *Challenges*
  - *Keep module to module noise pickup low*
    - *Shown to be low in test system*
  - *Examine all possible failure modes and develop protection schemes*
    - *Chip failure (shunt reg, overcurrent, etc)*
    - *Bond pad failure*
  - *Integrate into future FE chips*

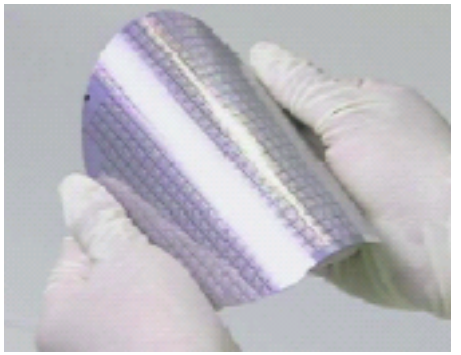


AC interface to/from pixel module



Wafer Thinning

- Detectors and readout chips make a significant contribution to multiple scattering
  - Every 100 μ of silicon is 0.1% X_0
  - Hybrid pixels have 2 layers of silicon, each greater than 100 μ thick
- Take advantage of work being done in industry by major companies (IBM, INTEL, Toshiba, etc.) to reduce wafer thickness
- Thinning
  - Thinning to 50 microns is in production
  - State of the art – CMOS wafers thinned to 10-15 microns by lapping/grinding followed by wet or plasma etch and CMP. Thinner for SOI.
- Challenges
  - ***Handling/breakage***
  - ***Thickness uniformity on large wafers***
  - ***Circuit performance changes due to thinning***
    - ***No change in Vt for 25u wafer (Fraunhofer, IZM)***
    - ***No change in Idsat for 25 u wafers (IZM)***
    - ***More tests needed***

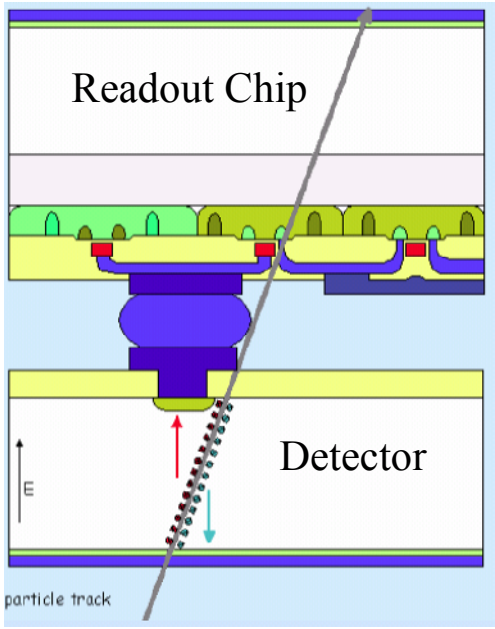


Thinned IC wafer (J. Joly, LETI)

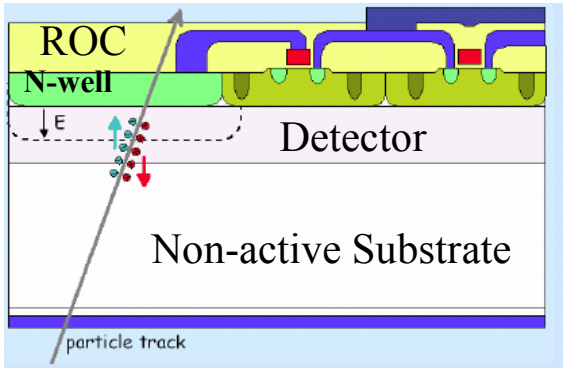
Thinned 200 mm wafer transferred on to glass handle wafer (A.Young, IBM)

Monolithic Active Pixel Sensors (MAPS)

- Hybrid Pixel sensors have achieved a level of maturity in HEP. Continuing future problems are cost, mass, and cooling of detectors under high radiation.
- CCDS can be thin but need separate support chips. They are not covered in this talk.
- Much work is being done on MAPS to reduce mass.
- A MAPS is a silicon structure where the detector and the primary readout electronics are processed on the same substrate.
  - Note, only the top few microns of an IC contain active circuitry.
  - The rest is merely a support structure.
- MAPS can be divided into two classifications:
  - Those using standard CMOS processes.
  - Those using specialized processes



Hybrid Pixel Principle

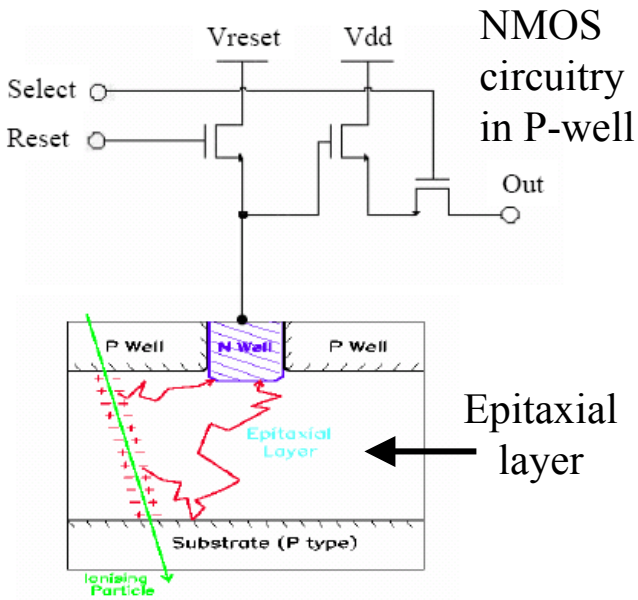


MAPS Principle

Kucewicz, Krakow

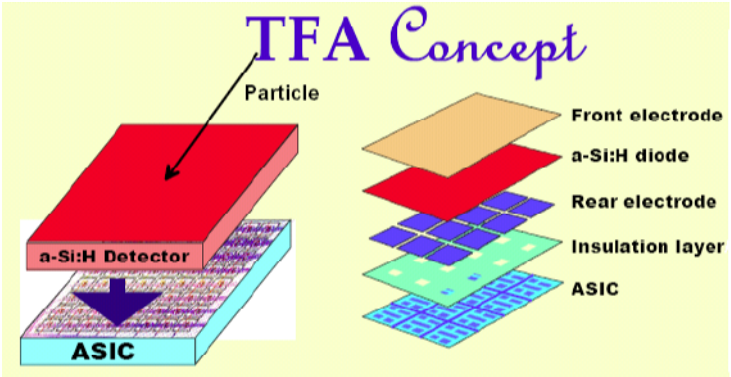
Standard CMOS Processes

- MAPS with epi layer
  - Many groups studying concept – RAL, IReS, Hawaii, INFN, etc.
  - Most collect charge by diffusion from epi layer (5-15 um) & some charge from substrate
  - Challenges
    - ***Transistor options are limited***
    - ***Many newer processes have thinner or no epi, resulting in very small signals***
- TFA – Thin Film Active Pixel Sensor
  - Activity centered at CERN
  - Radiation hard sensors, fast collection time
  - Challenges
    - ***Low noise readout to handle small signals***
    - ***Development of non-commercial process***
- **Biggest advantage to CMOS MAPS is the long term existence of the basic processes.**



CMOS Monolithic Active Pixel Sensor

J. Velthuis, Liverpool



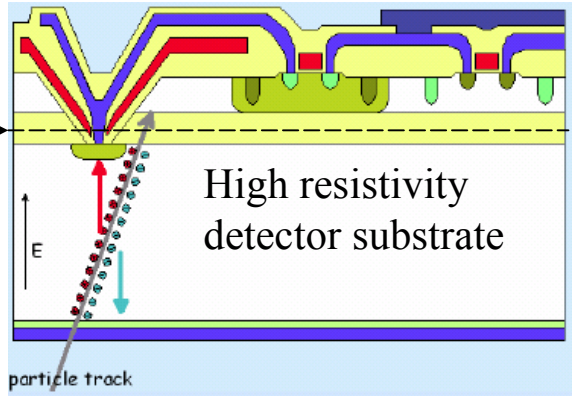
Thin Film Active Pixel Sensor

P. Jarron, CERN

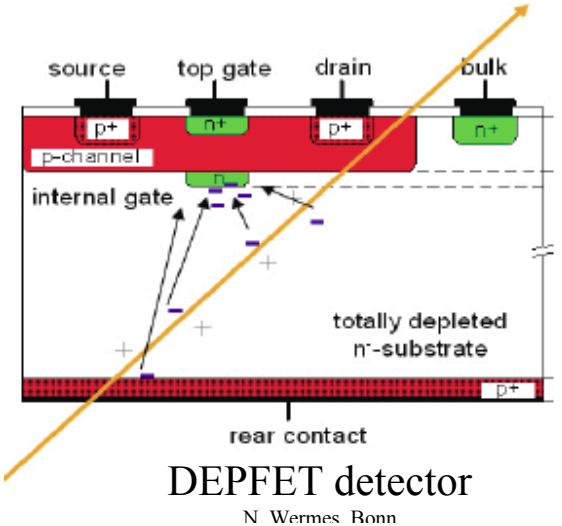
Non-standard Processes

- Silicon on Insulator Detector
  - Work progressing at Poland, Italy
  - Should be rad hard, can have NMOS + PMOS
  - Challenges
    - ***Fabrication of circuits at both sides of BOX***
- DEPFET
  - Work centered Bonn, Mannheim, MPI
  - Uses high resistivity substrate for sensor, provides large signal with low input capacitance
  - Challenges
    - ***Needs additional readout chips => more mass***
- 3-D sensor
  - Work lead by Parker: provides high speed signals
  - No working model with readout chip at this time

- **The biggest concern with all non-standard processes is whether the process will mature and sill be available 10 years from now.**
  Remember DMILL!!



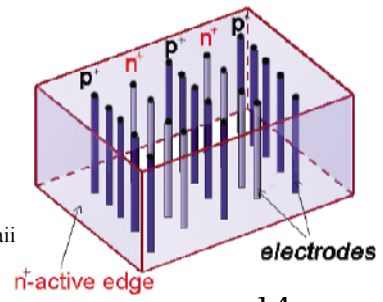
Silicon on Insulator Detector



DEPFET detector

N. Wermes, Bonn

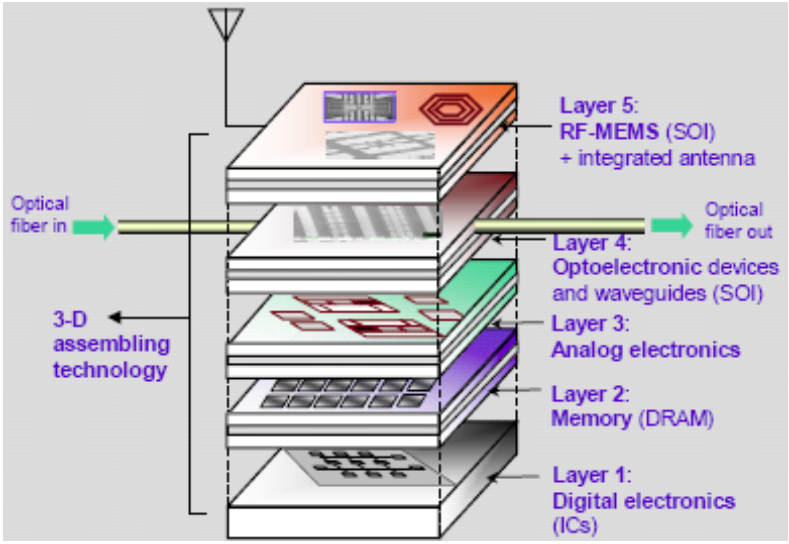
3-D sensor



S. Parker, Hawaii

3D Circuits

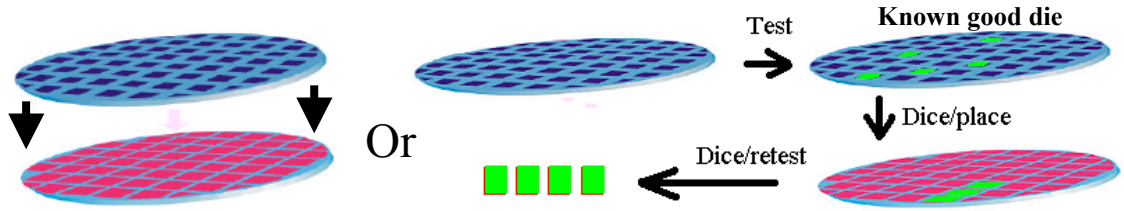
- Movement building within industry to develop 3D chips to meet ITRS (International Technology Road map for Semiconductors) requirements for increased speed and density.
- What is a 3D chip?
  - A 3D chip is comprised of 2 or more layers (N) of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit.
  - Frequently the layers are comprised of devices made in different technologies.
- Reasons for 3D in industry
  - Reduce interconnect length (R, L, C)
    - Improve speed ($N^{1.5}$)
    - Reduce interconnect power ($1/N^{0.5}$)
    - Reduce crosstalk
  - Reduce chip footprint size
  - Process optimization for each layer
- Can HEP take advantage of this technology?



The industry dream

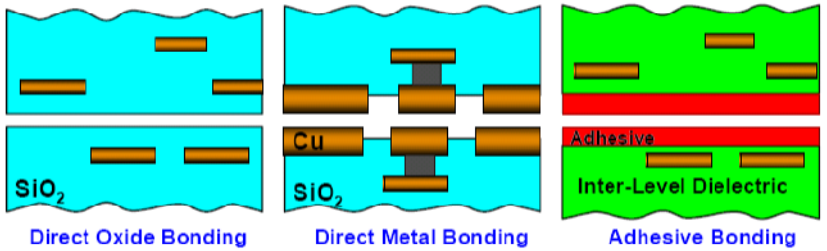
3D Options

- Wafer to wafer or die to wafer



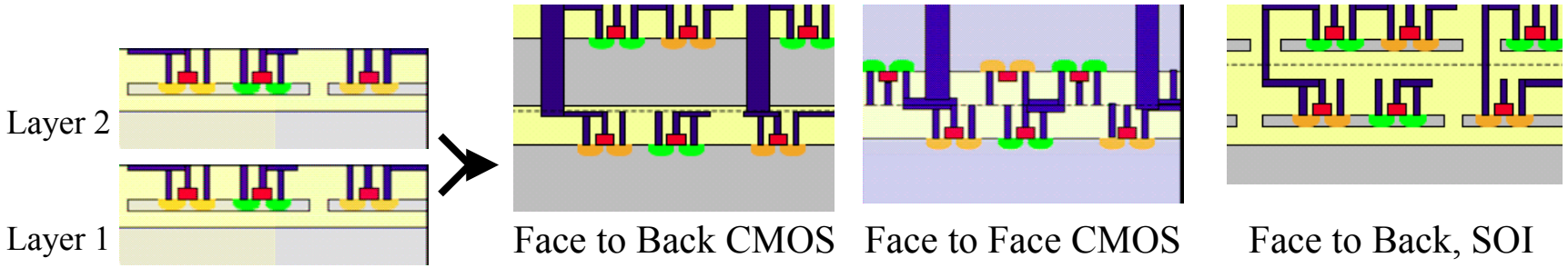
Wafer to wafer Die to wafer

- Bonding chemistry



J, Lu, RPI

- Thinning - before or after bonding
- Face to face, or face to back

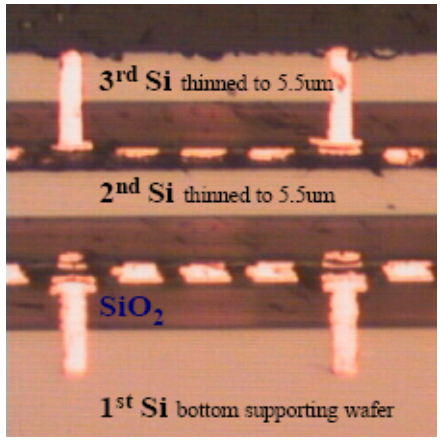


Face to Back CMOS Face to Face CMOS Face to Back, SOI (Similar to MAPS SOI)

- Vias – Deep, Short, None → Deep (25 μ) Deep, none Short (1-10 μ)

State of 3D

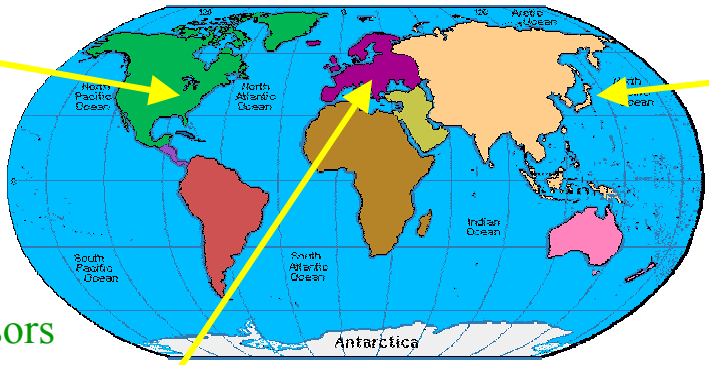
- State of the art
  - Numerous option combinations are being studied
  - Three and four layer stacks
- A few commercial products announced
- International effort is underway



3 layer cross section

(Tezzaron)

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT,RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix

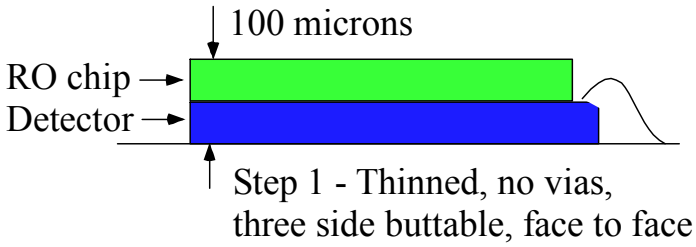


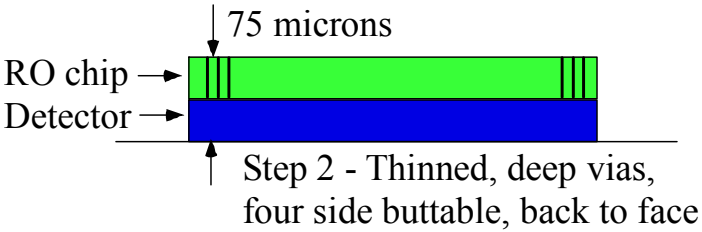
Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

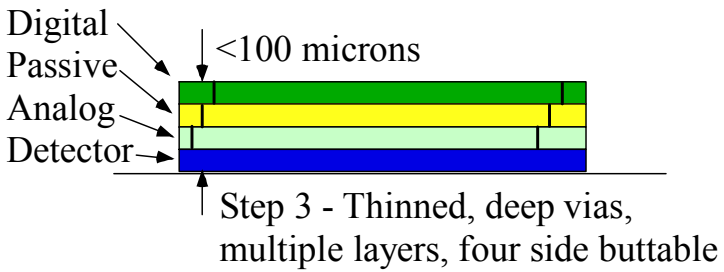
Europe: Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

3D Circuits in HEP

- Use in high density applications for experiments starting in 2010 or later
- Options
  - For detector applications use wafer to die bonding to provide optimal yield
  - Although SOI processes are easier to thin, use CMOS since CMOS processes are more readily available
- Advantages
  - Offers best detector and readout technologies
  - Can increase circuit density without going to smaller feature size process
  - Can use standard CMOS processes
- Disadvantage
  - Relatively early development stage
- Challenges
  - ***Build multilayer chips that are 100 microns thick or less.***
  - ***Handling thin circuits***
  - ***Finding an industry or university partner***



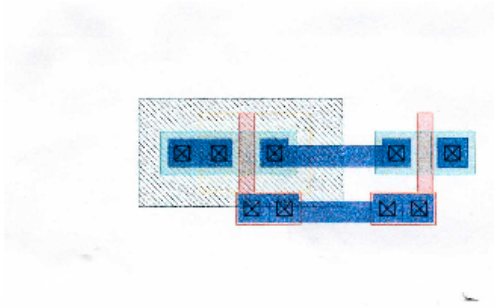




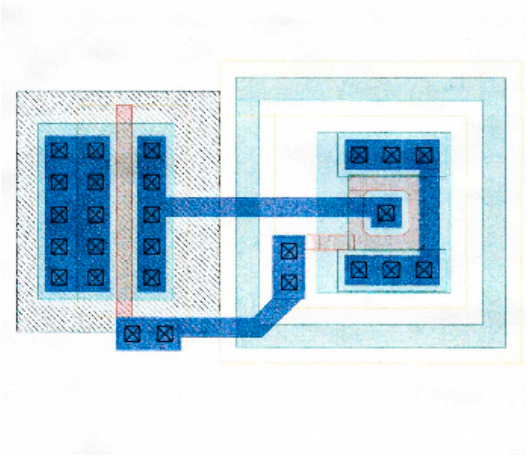
Possible dream pixel detector for HEP

Higher Radiation Tolerance

- In last few years, HEP has moved away from specialized rad hard processes.
- Has been shown that commercial DSM processes can be used for HEP radiation hard designs.
  - To overcome design problems due to threshold shift
  - To overcome transistor leakage current problems
- In commercial DSM processes
  - As gate oxides get thinner and thinner, threshold shifts with radiation due to trapped interface states and trapped charge become insignificant. (0.25 u CMOS)
  - Leakage current in field oxide still a problem in standard 0.25 u NMOS devices
    - Use special ELT (enclosed layout transistor) layout rules (However, there is a design and size penalty)
  - How does radiation tolerance change at even smaller feature size processes (0.13 u and below)
    - Can special layout rules be waived?
    - Can tolerances > 100 Mrads be achieved?



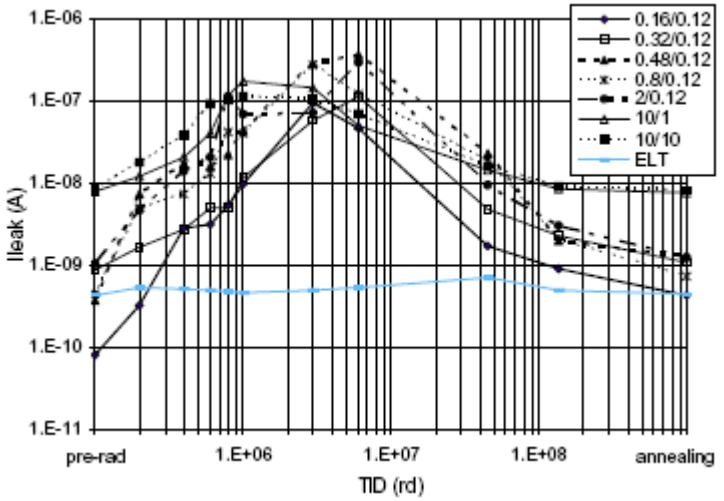
Standard Transistor Inverter

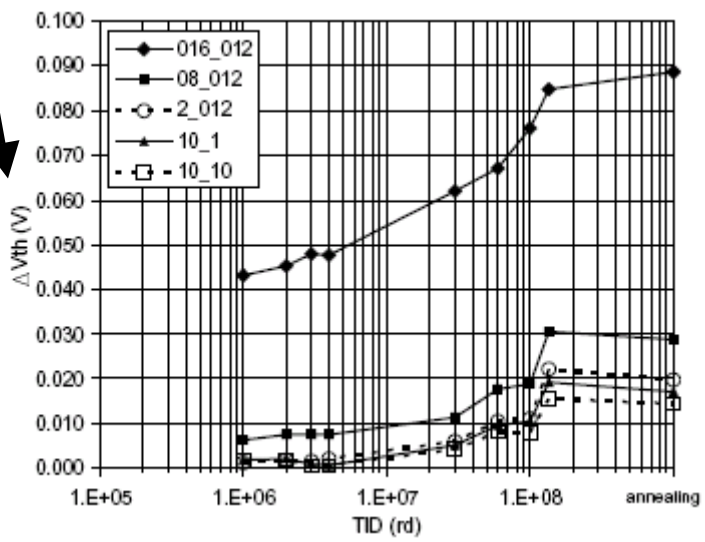


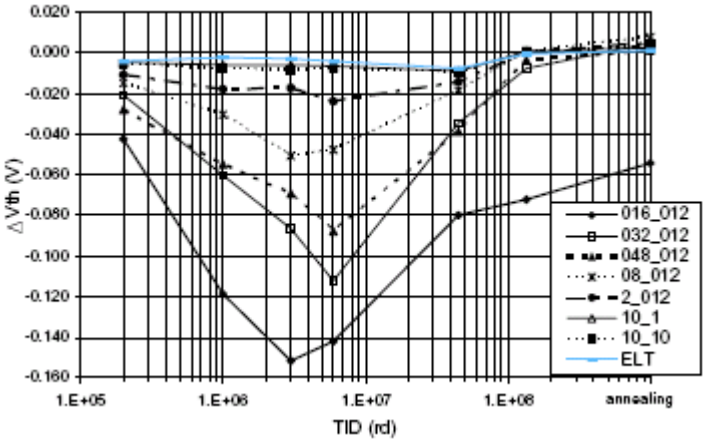
Enclosed Transistor Inverter

Preliminary Radiation Results at 0.13u

- For ELT, no change in NMOS Vt or leakage current observed up to 140 Mrads
- Core NMOS linear device performance
  - Leakage changes for all size devices
  - Vt changes for small devices
  - Changes due to Radiation Induced Narrow Channel Effect (RINCE) –see F. Faccio.
- Core PMOS (linear) device performance
  - No change in leakage for all device sizes
  - Apparent Vt shift for narrow device sizes







F. Faccio, CERN

0.13 micron (cont.)

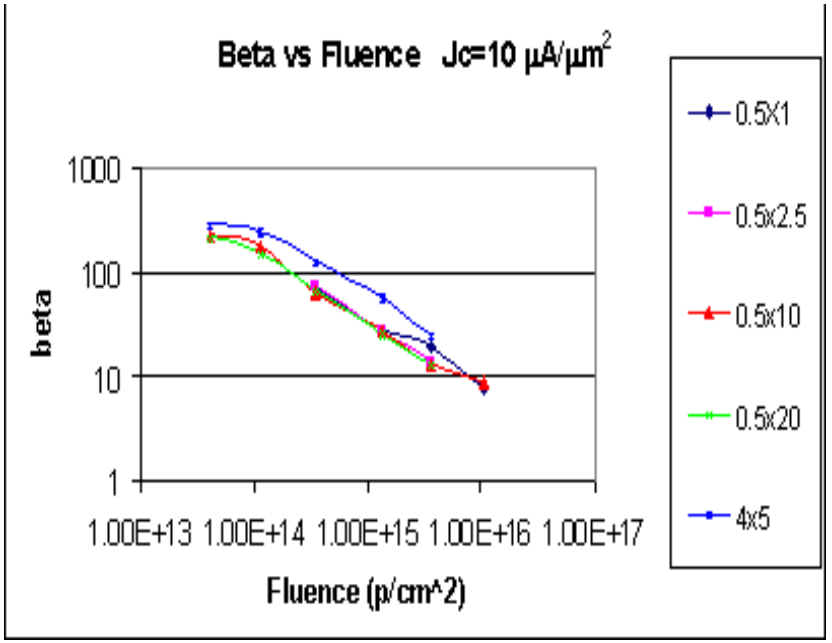
- Effects observed in 0.13 μ were found to be dependent on dose rate and temperature
- The Total Ionizing Dose tolerance of the 0.13 μ appears to be better than a 0.25 μ process.
- Challenges
  - *How to design a circuit that takes advantages of the 0.13 μ process and at the same time minimizes the size of the circuit without using ELTs.*
    - *Should circuits be pre-irradiated?*
    - *Can standard cell libraries be used?*
    - *Is overall circuit performance limited by I/O structures that have thicker gate oxides?*
    - *Will eventual process changes affect radiation performance?*
    - *Are there any other problems that might be found at 0.13 μ and how might these change for deeper sub micron processes?*
  - *Investigate 0.13 μ processes from other foundries*

High Speed/Performance

- Bipolar front end circuits have been used with higher capacitance detectors where fast shaping, low noise and low power are required.
  - ATLAS SCT, Zeus LPS, etc.
  - Separate CMOS readout used
- High speed BiCMOS processes now available using SiGe (strained silicon).
  - Some current foundries: IBM, STM, AMS, IHP (Germany)
- Characteristics of SiGe BiCMOS process
  - Very high quality, high speed bipolars (200 GHz)
  - Deep submicron CMOS for low power operation.
- Features of SiGe bipolar devices
  - Significant broadband and 1/f noise improvement over standard BJTs
  - SiGe BJT are inherently more radiation hard than standard BJTs
  - Noise does not change with radiation
  - Some unusual cryogenic features
    - As temperature goes down for BJTs, beta, speed, and noise get **worse**
    - As temperature goes down for SiGe, beta, speed and noise get **better**.

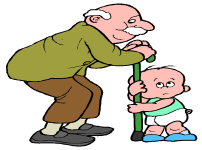
Some SiGe applications for HEP

- SiGe CMOS technology proposed for ILC and SLHC
  - ILC (J. Genat)
    - Front end circuitry for Silicon tracker: 50 pF detector and noise < 1000e @ 3usec shaping
  - SLHC (E. Spenser)
    - At 20 cm, readout for short strips with Cdet = 5 pf with fluence of 10^{15} n/cm^2
    - At 60 cm, readout for strips with Cdet = 15 pF and fluence of 3 x 10^{14} p/cm^2
    - Good radiation performance of SiGe transistors is critical
  - ATLAS replacement for ABCDS/FE using IHP SG25H1 SCT-FE
    - Power saving for 25 pF detector: 1.5 mW/ch => .36 mW/ch
- Other applications: High speed communication, low noise cold electronics, detectors.
- ***Challenges: Cost, availability, consistency, and yield from different vendors need to studied by HEP community.***

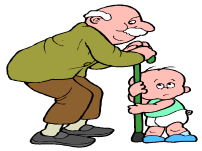


Radiation performance appears to be acceptable for SLHC

E. N. Spencer, SCIPP-UCSC

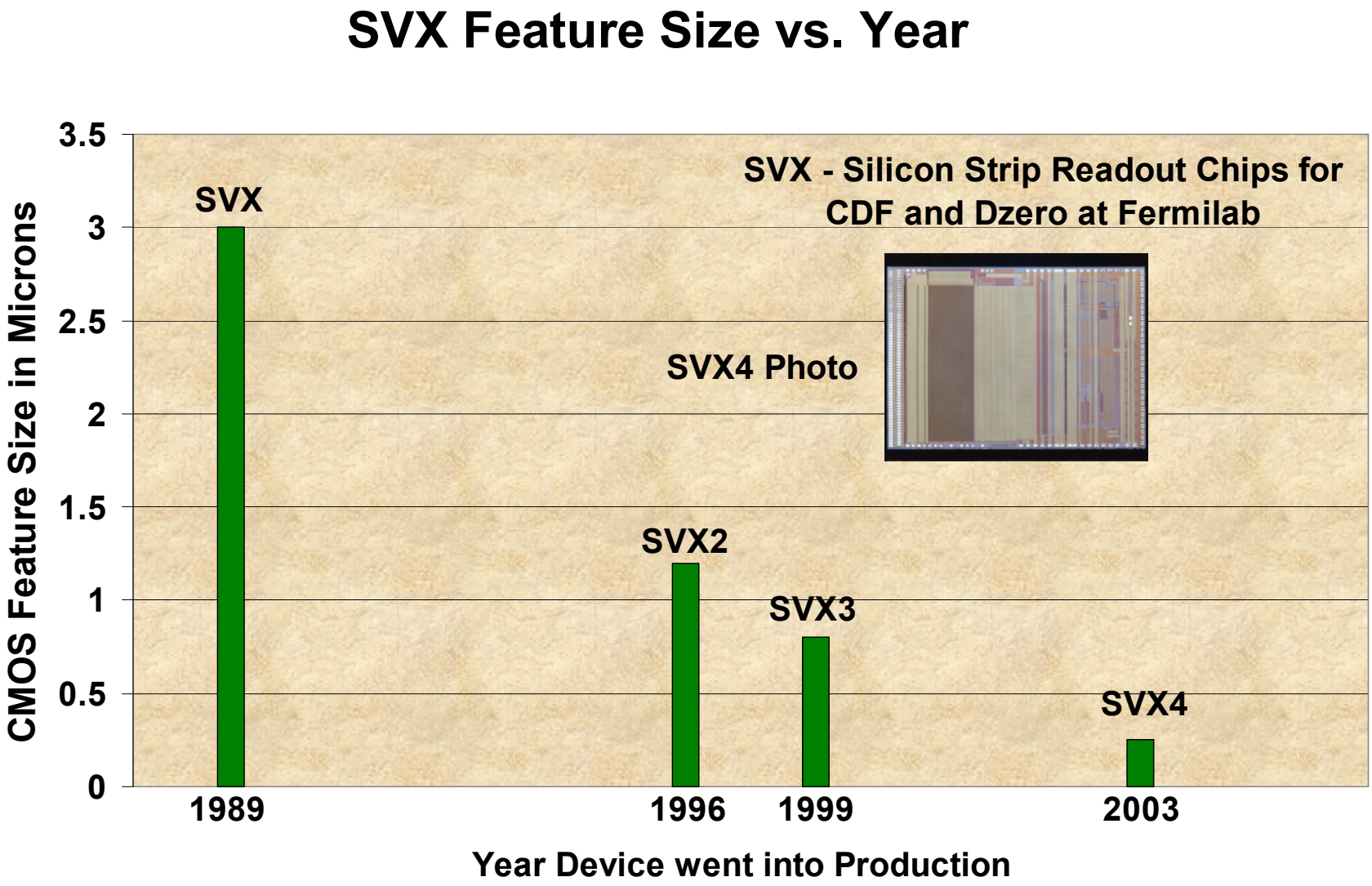


Process Obsolesce



- Long term projects (and even some short term projects) must face the challenge of process obsolescence or foundry management changes
  - Causes rushed designs
  - Must buy large quantities of spares to cover loss of process.
  - Obsolete processes – UTMC, DMILL, to name a couple
  - Largest CMOS feature size currently readily available through MOSIS, CMP, Europractice is 0.7 microns. Look at trend for SVX chips.
- Challenge
  - ***Plan ahead***
  - ***Live with ever changing market***

CMOS Feature Size Decrease



Selected Portions of ITRS

(International Technology roadmap for Semiconductors)

Table 81 a

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Number of metal levels	9	10	11	11	11	12	12
Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4
Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	579	688	907	1002	1117	1401	1559
FITs/m length/$cm^2 \times 10^{-3}$ excluding global levels [2]	8.6	7.3	5.5	5.0	4.5	3.6	3.3
Jmax (A/cm^2) – intermediate wire (at 105°C)	3.7E05	5.0E05	6.8E05	7.8E05	1.0E06	1.4E06	2.5E06
Metal 1 wiring pitch (nm) *	240	214	190	170	152	134	120

Table 81 b

2010	*2012*	*2013*	*2015*	*2016*	*2018*
hp45		*hp32*		*hp22*	
45	*35*	*32*	*25*	*22*	*18*
54	*42*	*38*	*30*	*27*	*21*
25	*20*	*18*	*14*	*13*	*10*
18	*14*	*13*	*10*	*9*	*7*
12	12	12	13	14	14
4	4	4	4	4	4
1784	2214	2544	3544	4208	5035
2.8	2.3	2.0	1.4	1.2	1.0
3.0E06	3.7E06	4.3E06	5.1E06	5.8E06	6.9E06
108	84	76	60	54	42

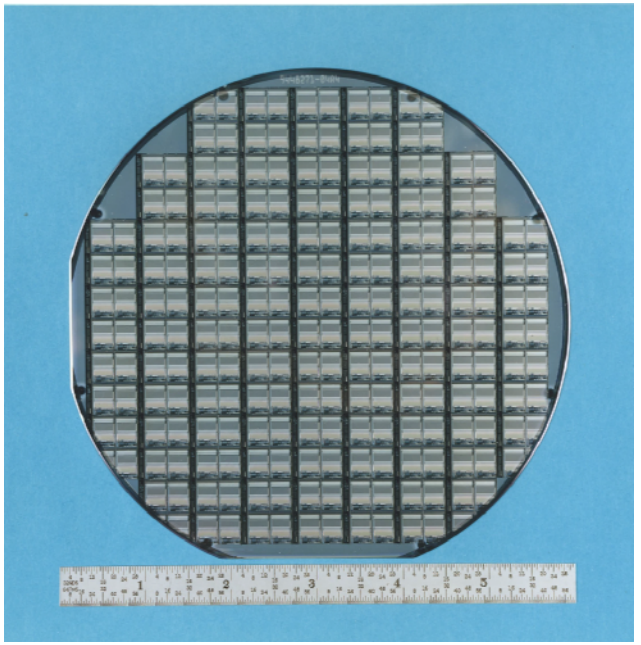
Many technological problems, the next simplest approach could be reducing trace length by going 3D.

Solutions are known

Solutions are not known

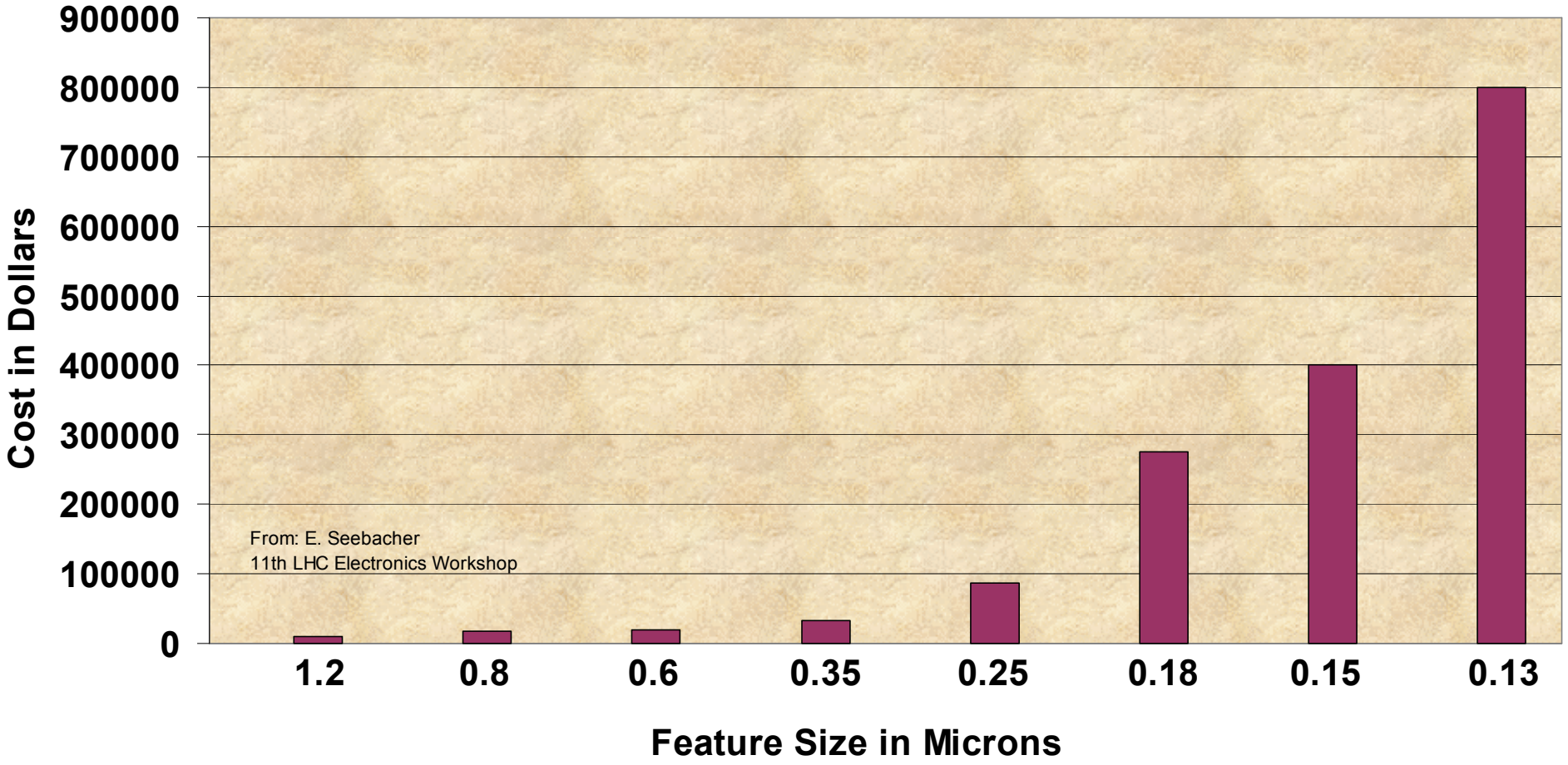
IC Fabrication Cost

- Can HEP afford 0.13 u and below DSM for lower power, less mass, higher radiation, higher speed?
- Cost considerations
  - Design cost appears in several different ways
    - Minimize number of design iterations
      - Use experienced designers when possible
    - Cost of tools - must upgrade with processes
      - FNAL tools
        - » Cadence (DIVA, ASSURA, ~~Dracula~~, Virtuoso)
        - » Mentor (ELDO, Calibre, Mixed signal simulation, Verilog)
        - » Synopsys (Nanosim)
      - Maintenance ($325K/yr)
  - Wafer processing cost is not the major issue
  - Mask cost is a major issue
  - Challenge
    - ***Maintain current IC designer experience for HEP***
    - ***Share mask costs whenever possible***



200 mm SVX wafer

Mask Cost for CMOS Processes



Challenges and the Future

- Technology tradeoffs must be made depending on the application.
- As a general rule good tools and experienced designers will reduce the number of design iterations saving development time and overall cost.
- A few questions to think about
  - What is the proper balance between on chip regulation (higher power dissipation) with the potential reduction in cabling mass and power?
  - Will special design rules still be necessary at smaller CMOS features sizes, or at what level will the special design rules be necessary
  - Will wafer thinning and 3D circuits become practical for HEP
  - Can power ramping be made to work in future very large systems
    - Readout stability
    - Thermal cycling
    - Pickup
  - Can analog information be given up to reduce system complexity and reduce power dissipation?
  - Can designs be tested in larger feature sizes to save development money
    - Similar thing was done before with rad soft to rad hard design process.
- Many questions – lots of work to be done
- Start thinking now - the future is just around the corner

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