Testing Experience with TSMC 0.25 µm

FNAL ASIC Testing Lab

TSMC 0.25 µm devices

Testing Results

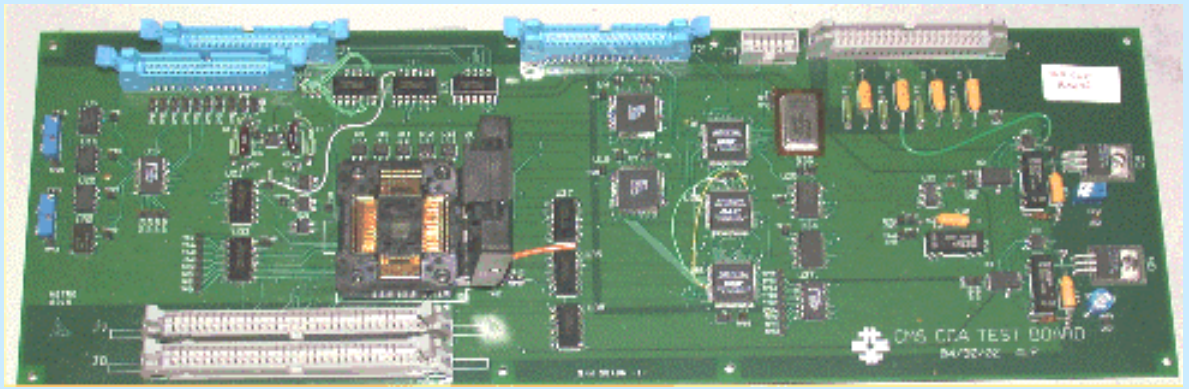
Conclusions

ASIC Testing Lab

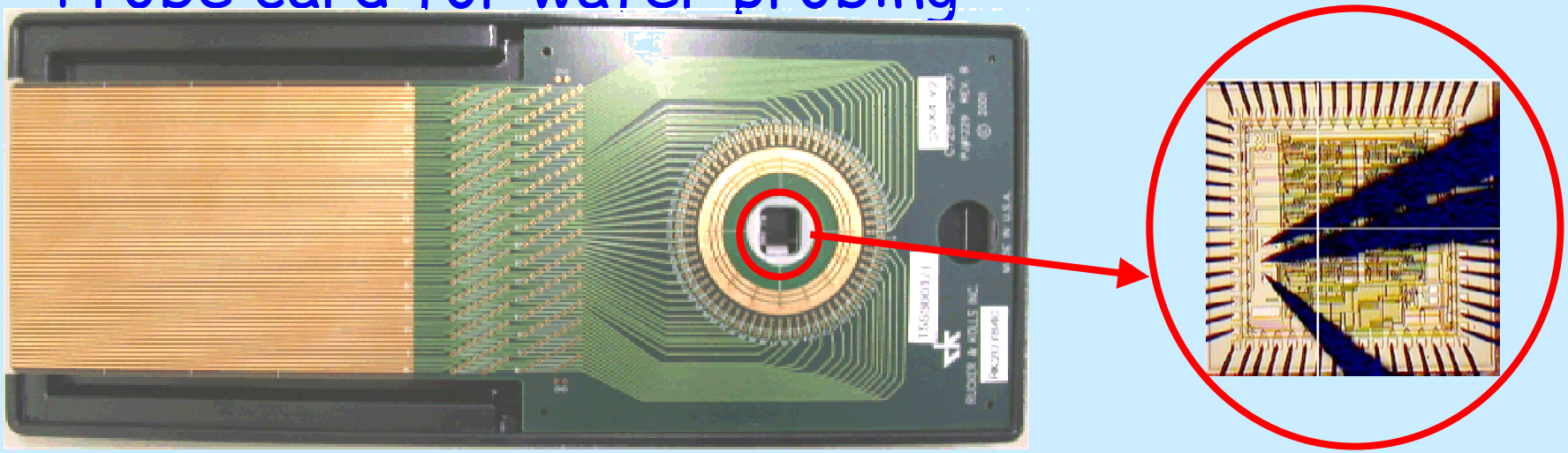
- Probe station
  - 8" wafer guarded thermal chuck
  - environmental chamber
- Tester box
  - Analog and digital
  - Micro-P controlled
  - Programmable with software (visual BASIC)
- Linux based DAQ and other possibilities

ASIC Testing Lab

- Interface printed circuit board

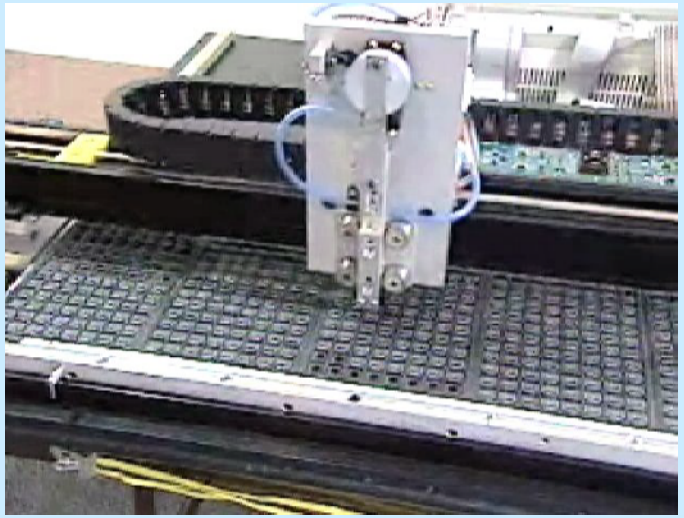


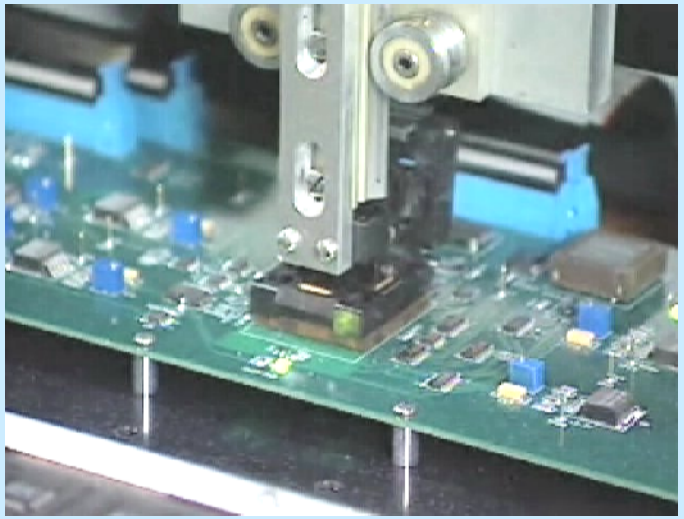
- Probe card for wafer probing



New Robotic Tester

Robot is now in use testing CMS QIE devices

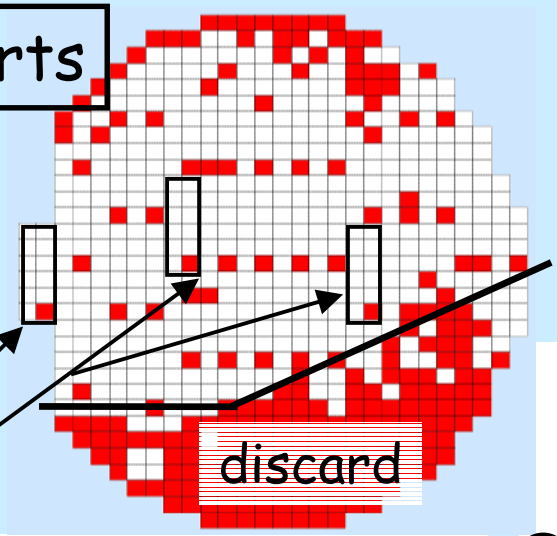




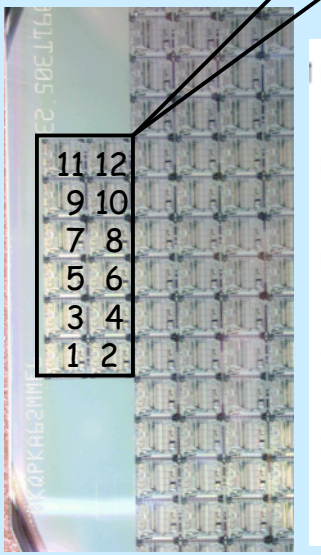
Example results MINOS QIE

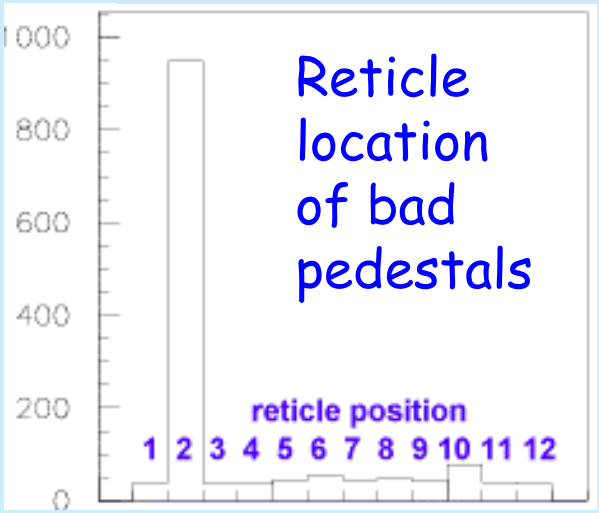
Reject bad parts

Discard bad regions on a wafer

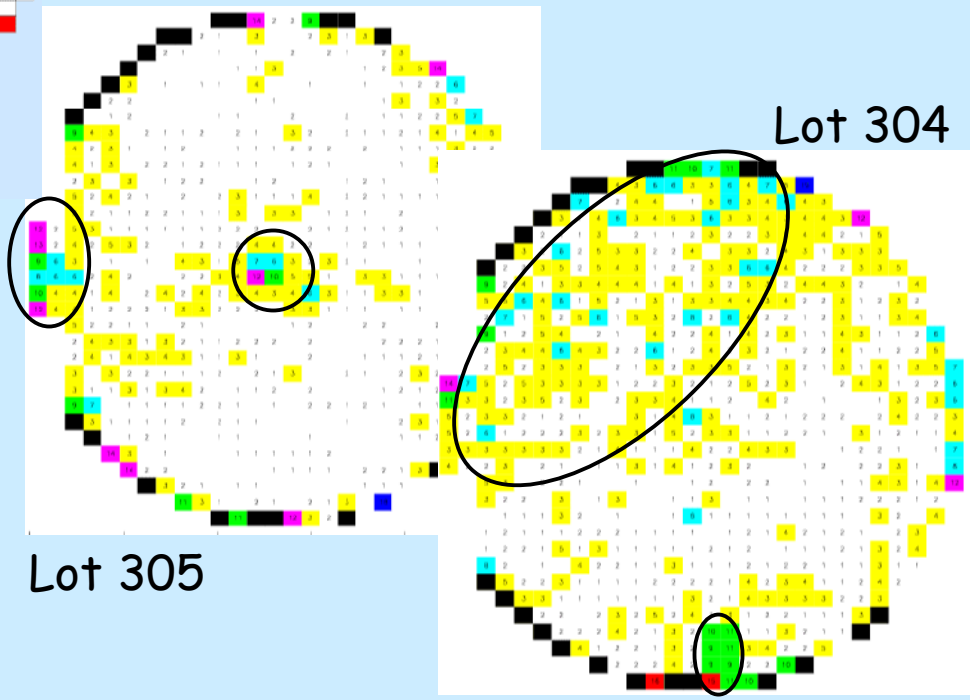


Variations in process, wafer level, and lot level can be studied





Reticle location of bad pedestals

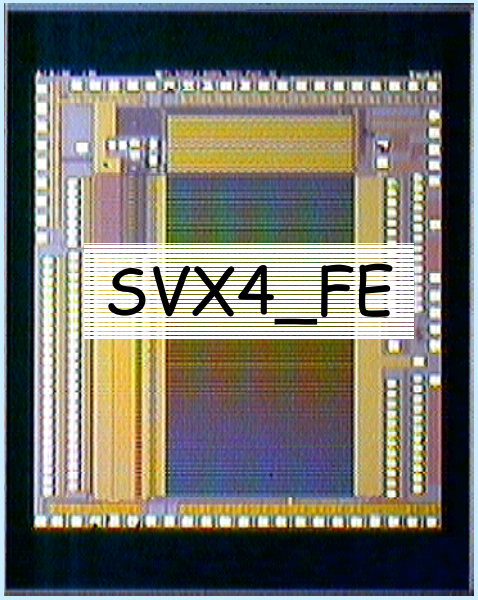


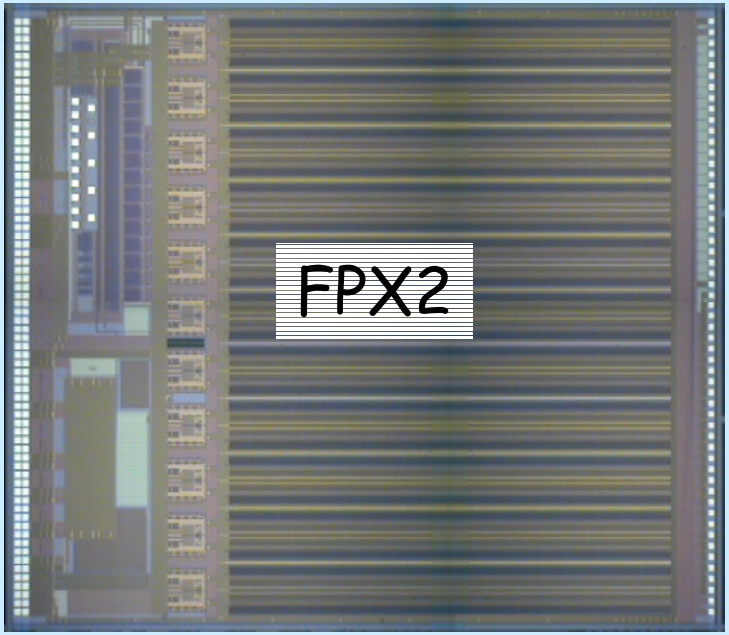
TSMC 0.25 µm devices

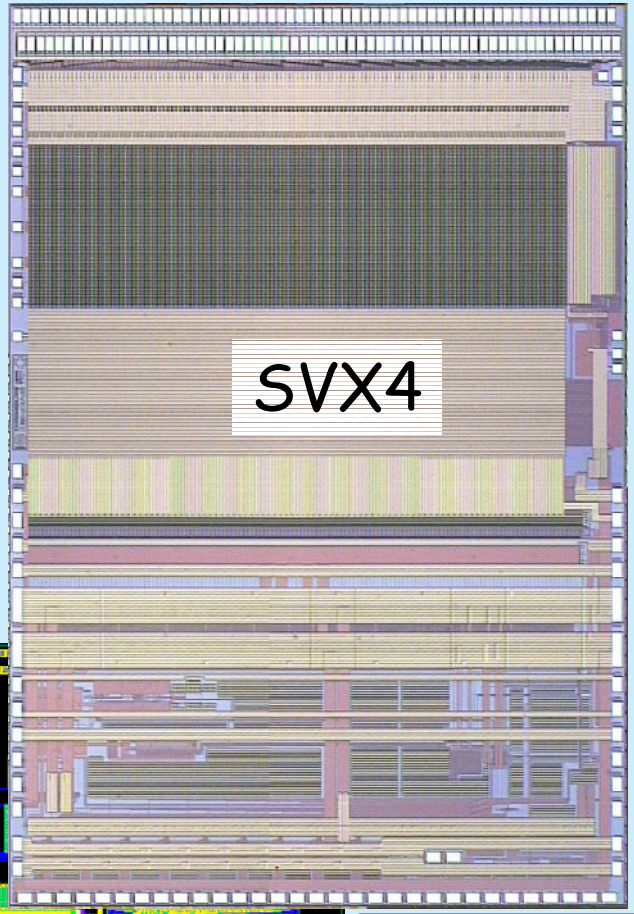
- Test and R&D chips
  - Rad test structures
  - Serial register (J. Hoff talk)
- BTeV chips
  - Pre-FPIX2t (A. Mekkaoui talk)
  - Pre-FPIX2tb
  - FPIX2 A,B,C
- CDF/D0 chips
  - SVX4-FE
  - TRX25
  - TriP (P. Rubinov talk)
  - SVX4_V1, _V2 (various talks)
  - SVX4_2a, _2b
- BTeV Si strip chip
  (in design) FSSR

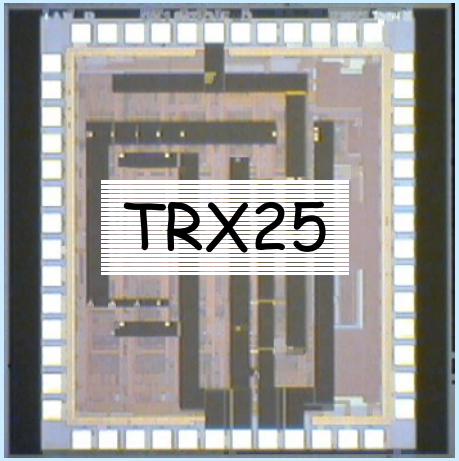
All in TSMC 0.25 µm
Multiple wafers indicated

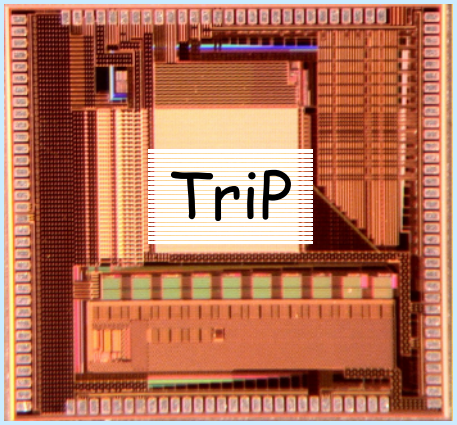
Devices, devices, devices

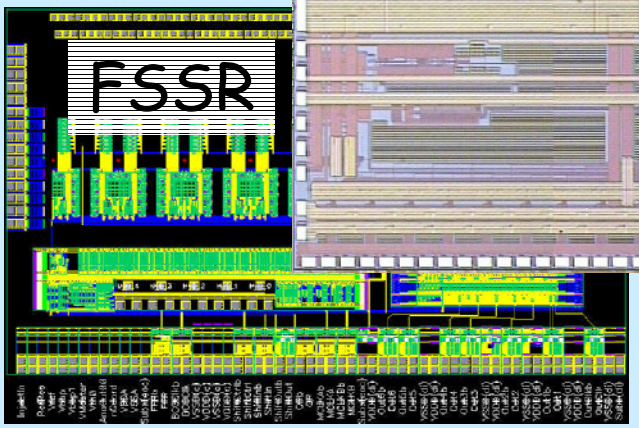










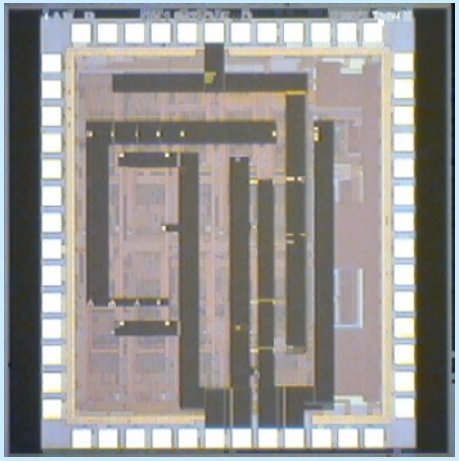


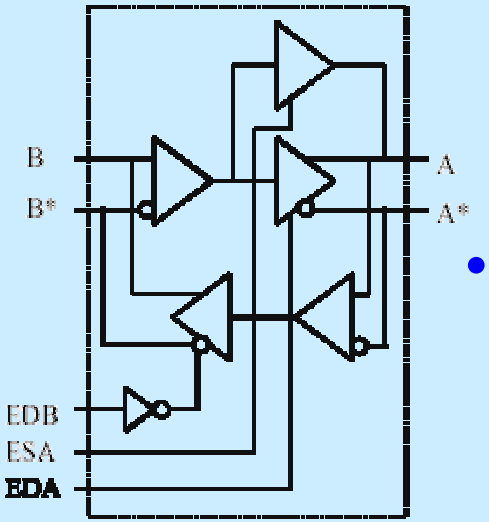
+several test chips

TSMC Wafer Yield

- Previous assumption is 0% yield on 20% of the wafers ordered
- May 2002: 12/12 SVX4_V1/2 + TriP
- Dec 2002: 22/24 FPIX_A/B/C+ TRX25
- May 2003: 24/25 SVX4_2a/b
  - Lost wafer was dropped at the foundry
- Realized wafer yield: 58/61 = 95%
- New recommendation is 10% bad wafers

TRX25 Testing



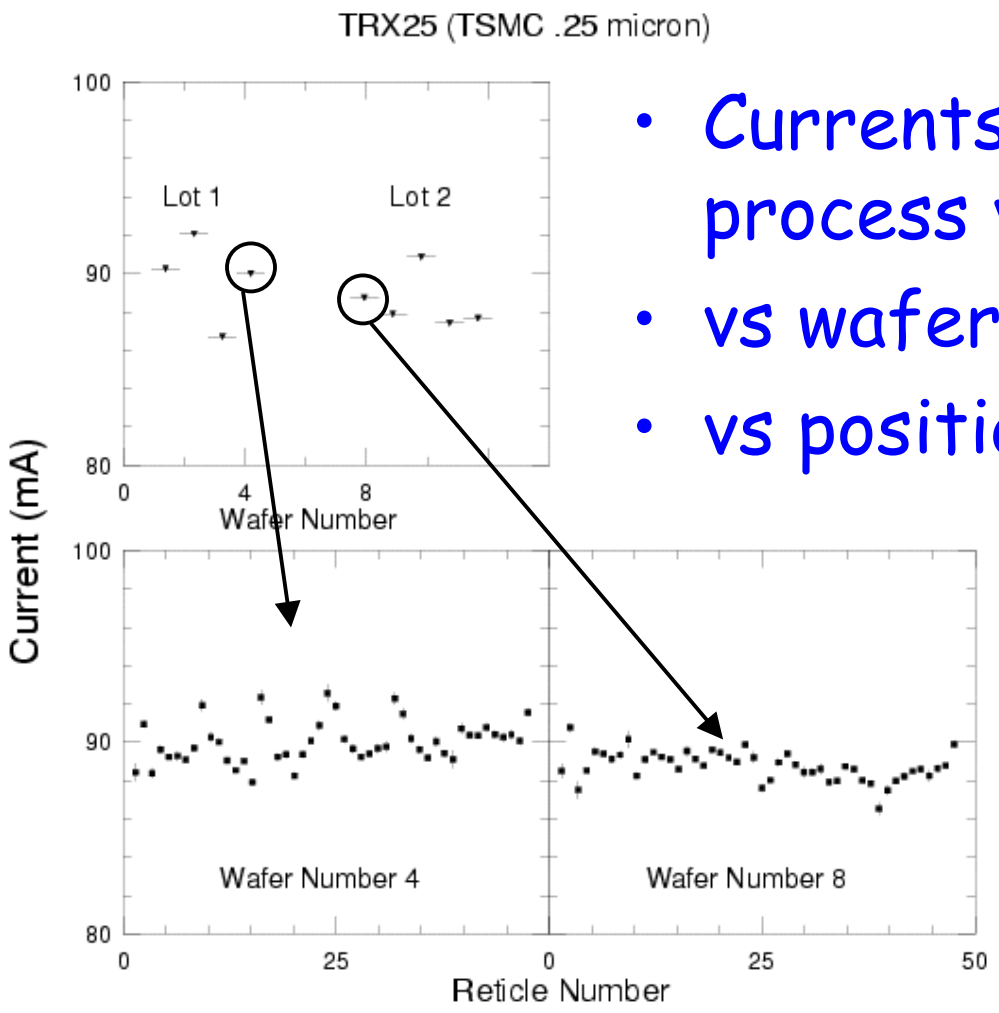


- 10 channel LVDS bi-directional transceiver with adjustable output current (4-16 mA).
- 22 wafers x 48 reticles x 12 chips = 12672 parts (CDF requires only 1500 chips – spare wafers for BTeV bump bonding).
- Shared with FPIX_A/B/C so cost to CDF was $50K (marginal cost for 12 more wafers).

TRX25 Testing

- Fairly simple chip, fairly simple tests
  - Digital pattern on all 10 channels for all modes
  - Select and measure output current on 1 chan.
  - Measure and record current draw, bias, etc.
- Results from 9 wafers (5,184 devices)
  - 43 devices fail over all modes (99% functional)
  - 158 devices fail analog measurements (>5σ)
  - Process variation at 10% level
- Yield: 96.1%

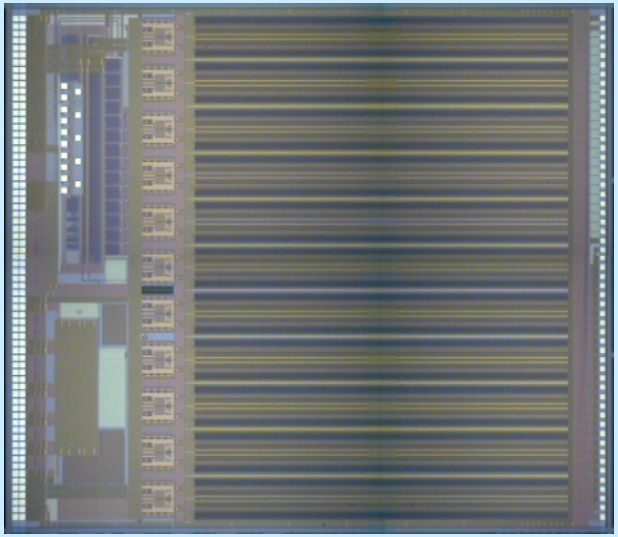
TRX25 Testing



- Currents to study process variations
- vs wafer number
- vs position on wafer

All good die are within ~10% of the mean. Some differences between wafers and versus wafer position.

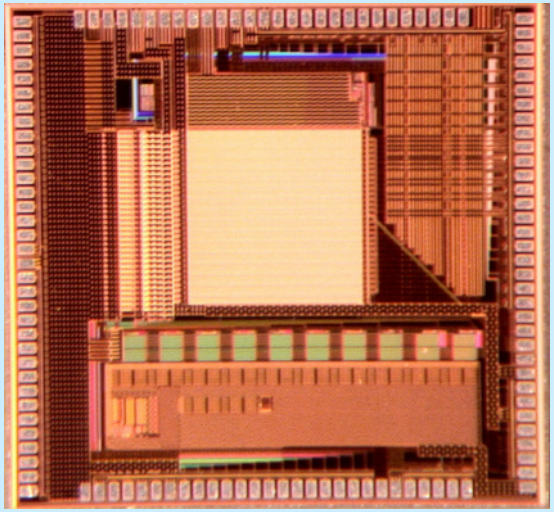
FPIX2 Testing



No custom interface PCB. The DAQ system is quite flexible.

- Minimal testing for first look and to screen devices for prototypes
- Measure currents and look for functionality of program interface.
- 98.6% pass this test on one wafer.
- No yields are quoted.

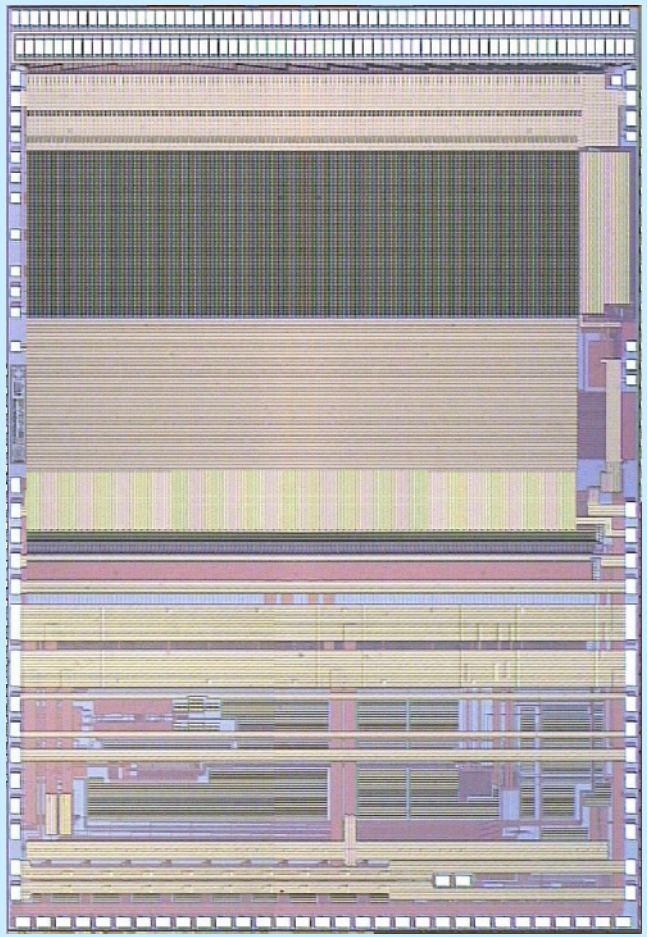
TriP Testing



Robot tester used with actual module PCB using conductive mat (no clam shell).

- Trigger-pipeline chip for D0 fiber tracker
  - Analog + trigger output with SVX4 pipeline -> fast 132 ns beam timing
- Production quantity made with SVX4_V1/V2 (no prototype!)
  - 12 wafers x 52 reticles x 11 chips = 6864 produced (3168 needed).
- Plan is to use packaged parts - limited testing on 132 parts. 9 have high currents and 2 have bad registers. 121/132 = 92%

SVX4 Testing



- V1: full-size prototype
- V2: on-board bypass caps
  - 12 wafers x 52 reticles = 624 of each (prototypes).
- 2a: improved ADC (backup)
- 2b: re-designed ADC
  - 24 wafers with 76 "a" and 378 "b". Over 9K "b" chips.
  - "b" could be production chip

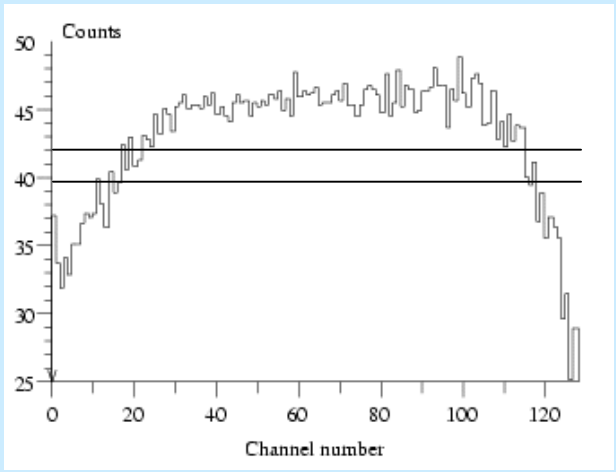
SVX4_V1/V2 Testing

- 12 wafers total, 9 with probing results
  - (2 diced before tests, 1 with some suspect results)
- 9 wafers probed for currents
  - 18/936 chips fail with bad current draw on either AVDD or DVDD (i.e. shorts) (1.9%)
- ~7 wafers probed for basic functionality
  - 37/762 chips have a small problem (bad channel(s), fail sparsification, etc.) (4.3%)
- 3 V2 wafers tested fully (all pipeline cells etc.)
  - 4/156 chips have a very small problem (more than one bad pipeline cell, noisy, etc.) (2.6%)
- Overall yield: 91.2% pass all, (98% functional)

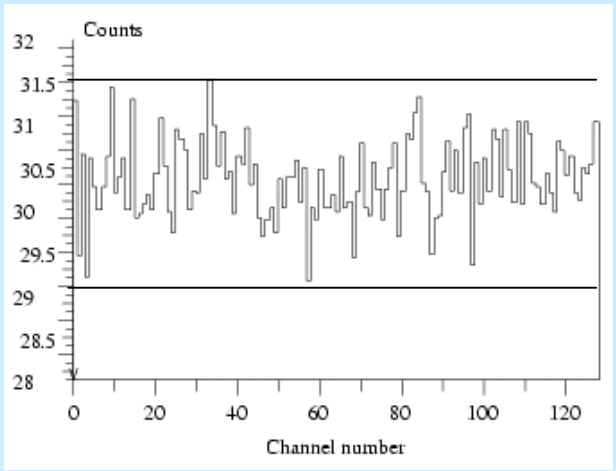
SVX4_2a/2b Testing

- First testing results have been to check changes compared with V1/V2 devices.

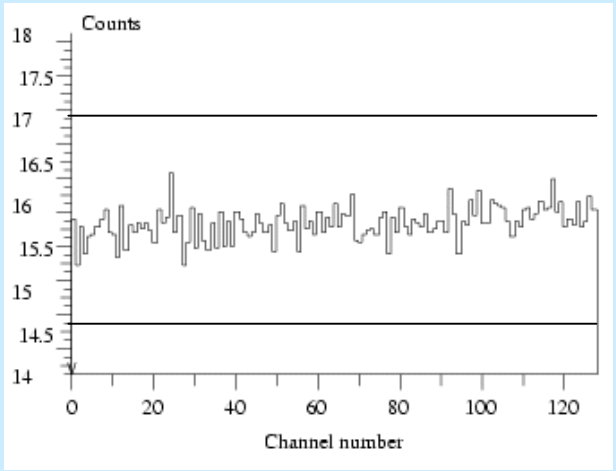
SVX4_V2



SVX4_2a



SVX4_2b



Extreme settings result in pedestal vs channel "bow." This is fixed.

SVX4_2a/2b Wafer Testing

- Two wafers probed so far (852 devices)
- Full suite of tests (3 min/chip, 1 wafer/day)
  - Serial Line
  - Pedestals/Noise/Gain for every pipeline cell
  - Advanced measurements
    - Pipeline cell pointer
    - ADC latches
    - Preamp risetime
    - Dynamic Common Mode Suppression
    - Sparsification

Full analysis is in progress

SVX4_2a/2b Wafer Testing

- Of the 852 devices, all but 29 are functional. (96.6%).
- Look for bad channels or pipeline cells
  - 66/109K channels bad
  - 23/5M pipeline cells bad
- Rejecting chips with even a single bad cell – 84 chips rejected
- Preliminary yield: 90.1%

(includes die out to the edge of the wafer)

Conclusions

- TSMC "wafer yield" measured to be 95%
- Six fundamentally different chip designs show ~95% of the chips are functional and have a preliminary yields of ~90%.
- Internally sharing wafer area in dedicated projects has many benefits.
  - Costs of masks shared
  - Can obtain small number production quantities
  - Easy to integrate test structures/prototypes