TriP Chip

Paul Rubinov, Fermilab

- TriP is the front end preamplifier, trigger and pipeline chip for the VLPC based detectors at Dzero (central fiber tracker and central and forward preshowers)
  - This is an upgrade for an existing system
  - Flaw* in custom chip in original design
- Two main requirements:
  - DO IT FAST
  - DO IT CHEAP
  - Also should work as well as original FE
- Chip design, system design and testing from the experimenters point of view

*Ask me later

The Project

- **People:**

  from Dzero: M.Johnson, F.Borcherding,A.Bross, B.Hoeneisen, J.Estrada, C.Garcia, J.Anderson, P.Rubinov…

  from EED: R.Yarema, A.Mekkaoui, T.Zimmerman, J.Hoff, W.Wester, A.Baumbaugh, K.Knikerbocker, P.Rubinov…

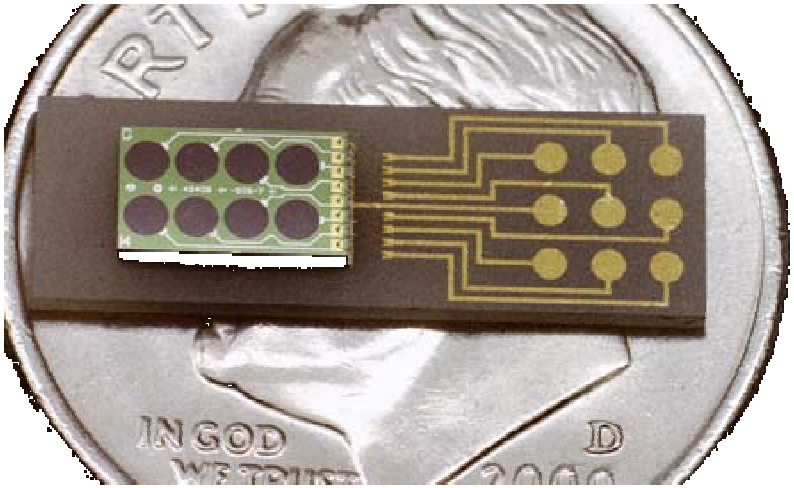
- **The job:**

  Readout signals from the fiber tracker and preshower detectors using VLPCs every 132ns Detect hits and send the discriminator bits to trigger system every xing. Store analog info for read out on demand.

The Sensor

- **V**isible**L**ight**P**hoton**C**ounters
  - 100k ch at Dzero
  - 40K gain, 90%QE, 7V bias
  - work at 9K (LHe)

  Two detectors:
  - fiber tracker- 5 to 10 pe
  - preshower- up to 450pe



8ch VLPC hybrid sitting on a dime

Comments

fairly dense

6fC/photon typical

cryostat, long cables

enormous dynamic range: from 5 to 5000fC

TriP Chip Specs

For Fiber Tracker and Preshower MIP layer (high gain):

- max before saturation = 300 fC
- threshold: 4 to 20 fC
- 99% of channels within +-4 fC
- rms noise < 1.0 fC

Same chip!

For Preshower Detector shower layer (low gain):

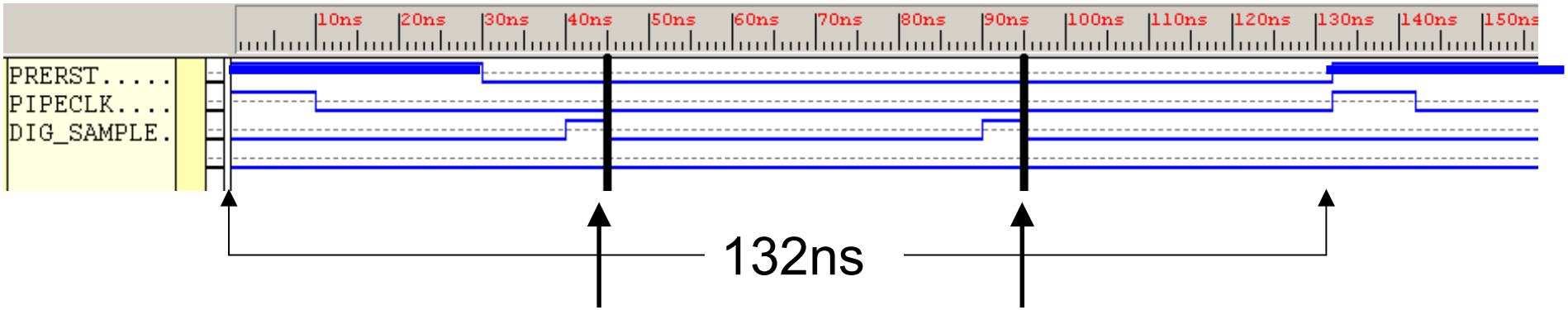
- max before saturation = 5000 fC
- typ: 450 photoelectrons = 1890 fC
- threshold desired: 100 to 750 fC

Analog outputs:

- channel uniformity should be within +-3%,
- rms noise (high gain)< 1 fC referred to the input

The Problem

- **Requirements (cont):**
  - Bunch crossing rate = **132 ns**
  - Window for charge collection:
    … **50 ns** …



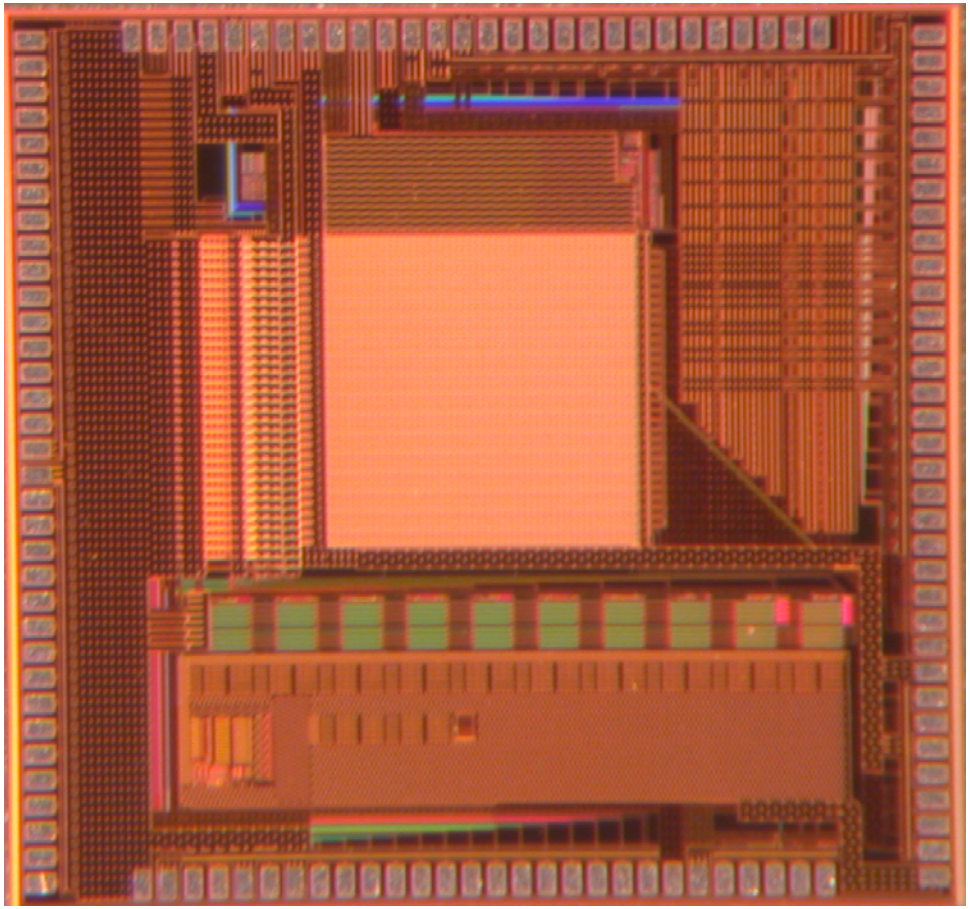
Must be able to trig here:
i.e. have settled to 1%

Must still be able to collect charge if it comes here

Chip must be FAST

TriP Chip

- The chip (finally)



Designed by
Abder Mekkaoui
(J Hoff and T Zimmerman)

1st (and only!) submission

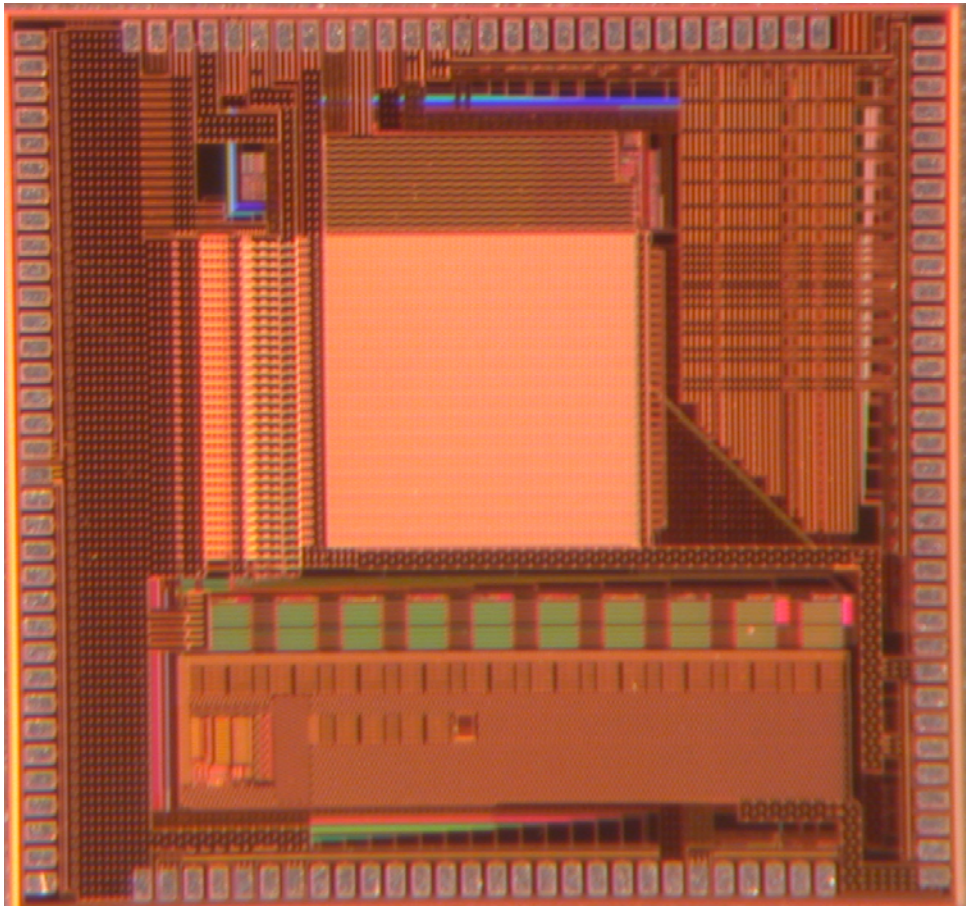
0.25um 2.5V CMOS (TSMC)

4.55mm x 4.80mm

32ch per chip

TriP Chip

- The chip (finally)



Joint submission with SVX4 prototype run (same reticle)

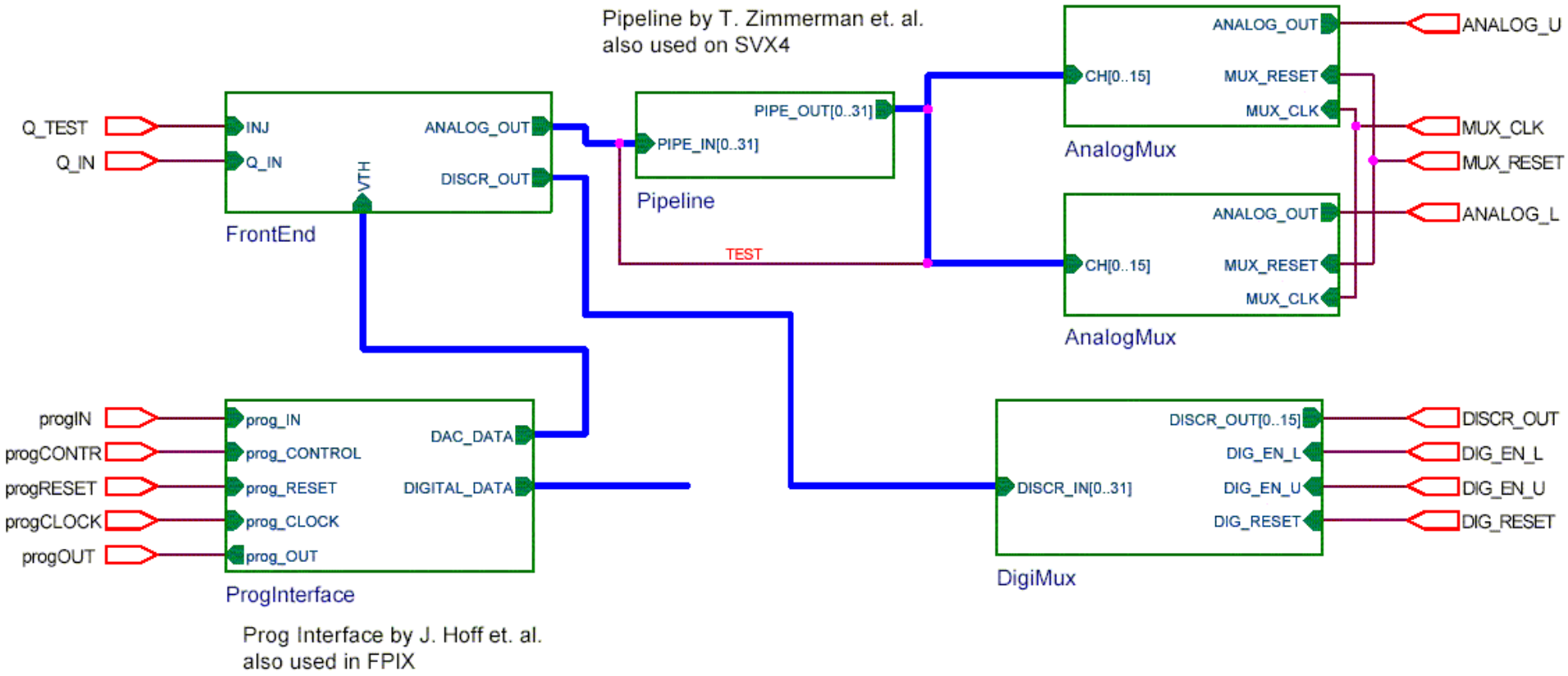
~6800 made

(need ~ 3500 w/spares)

Exactly 1yr from 1st meeting (Jun 2001) with Ray and Abder to chip in hand

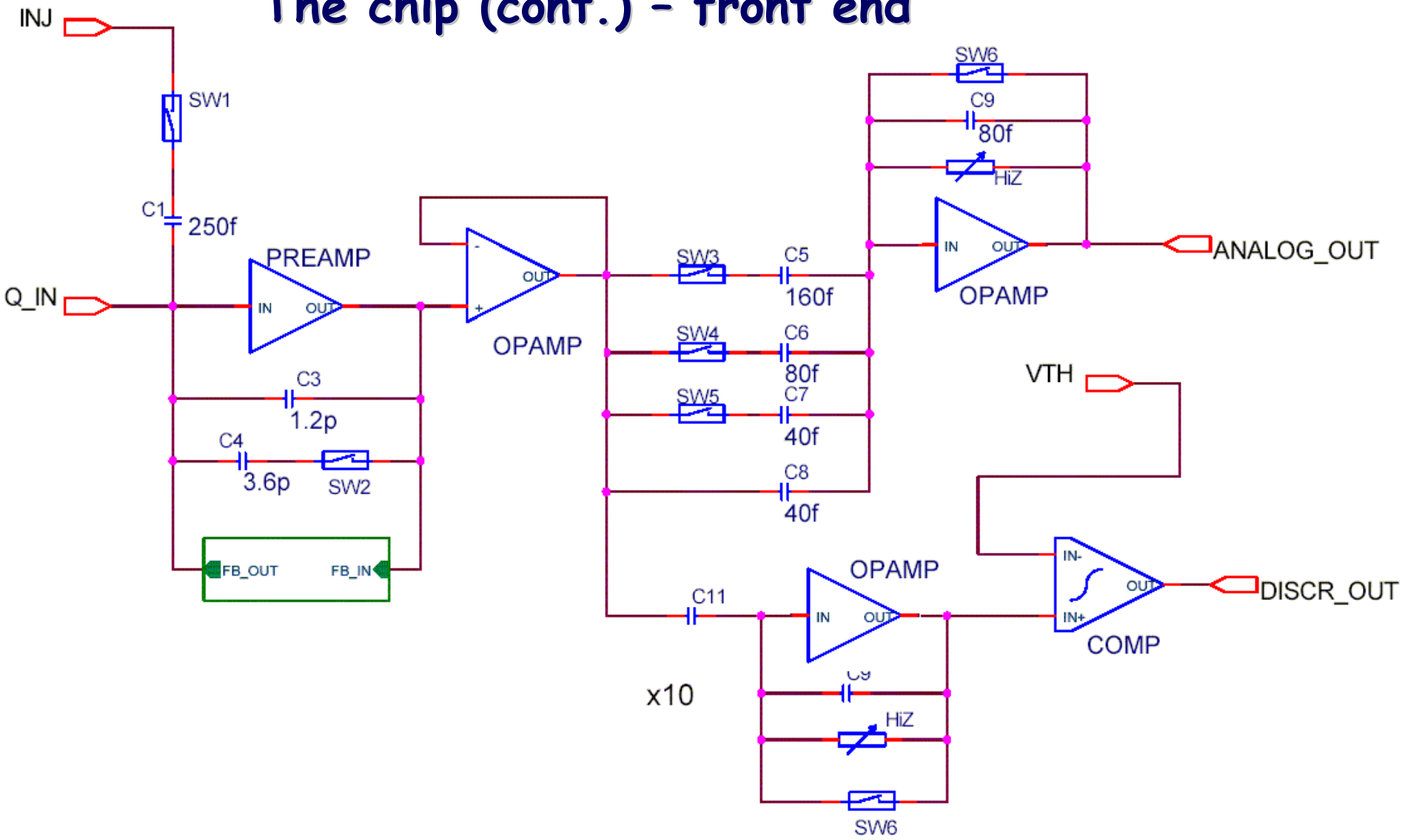
TriP Chip

Simplified schematic



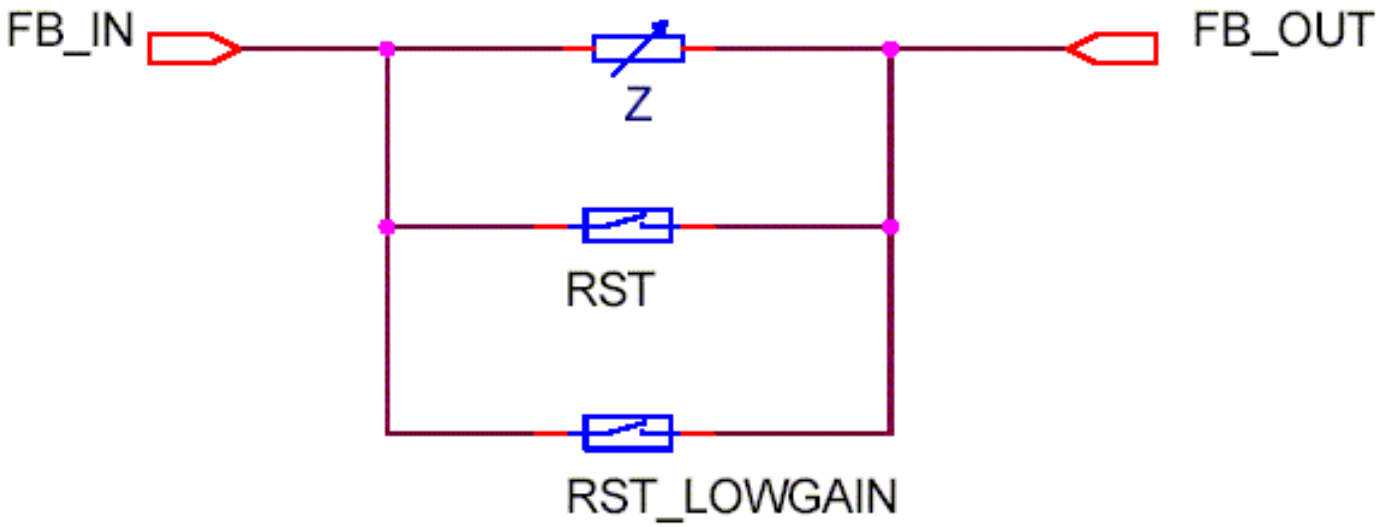
TriP Chip

The chip (cont.) – front end



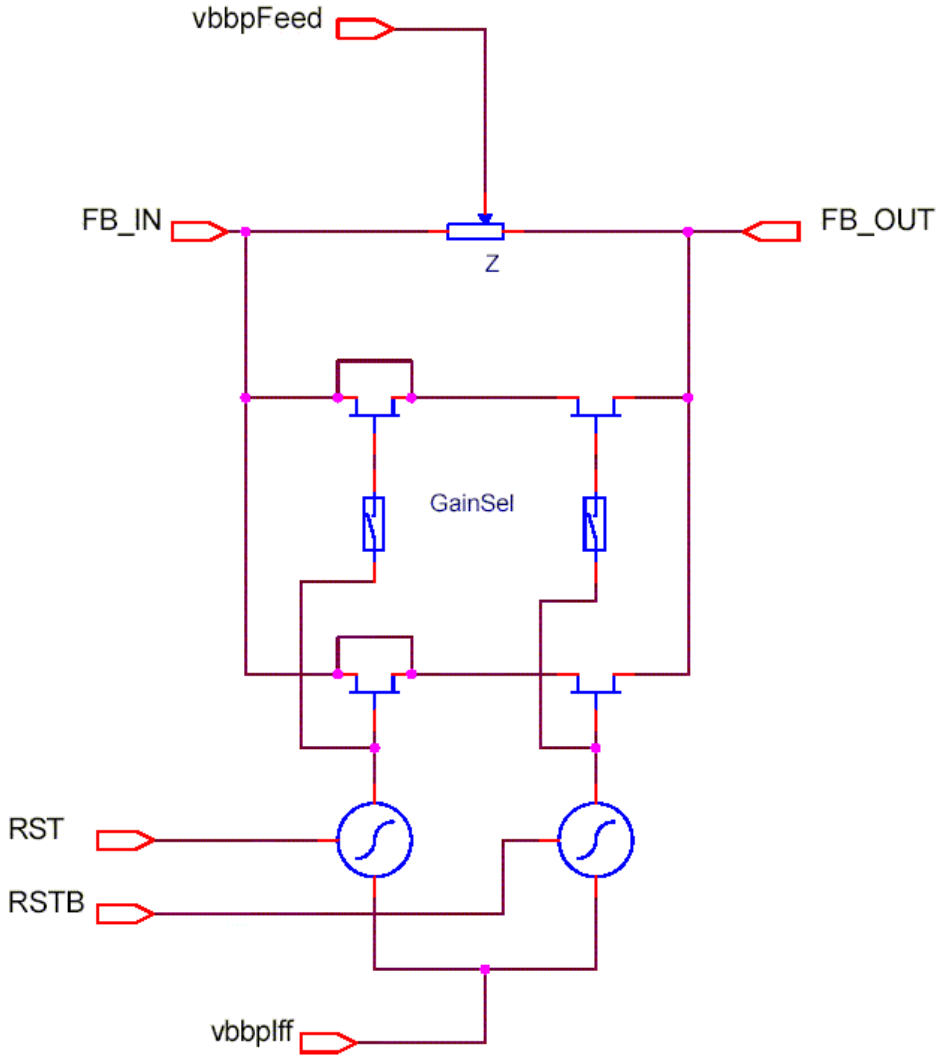
TriP Chip

The chip (cont.) – feed back details



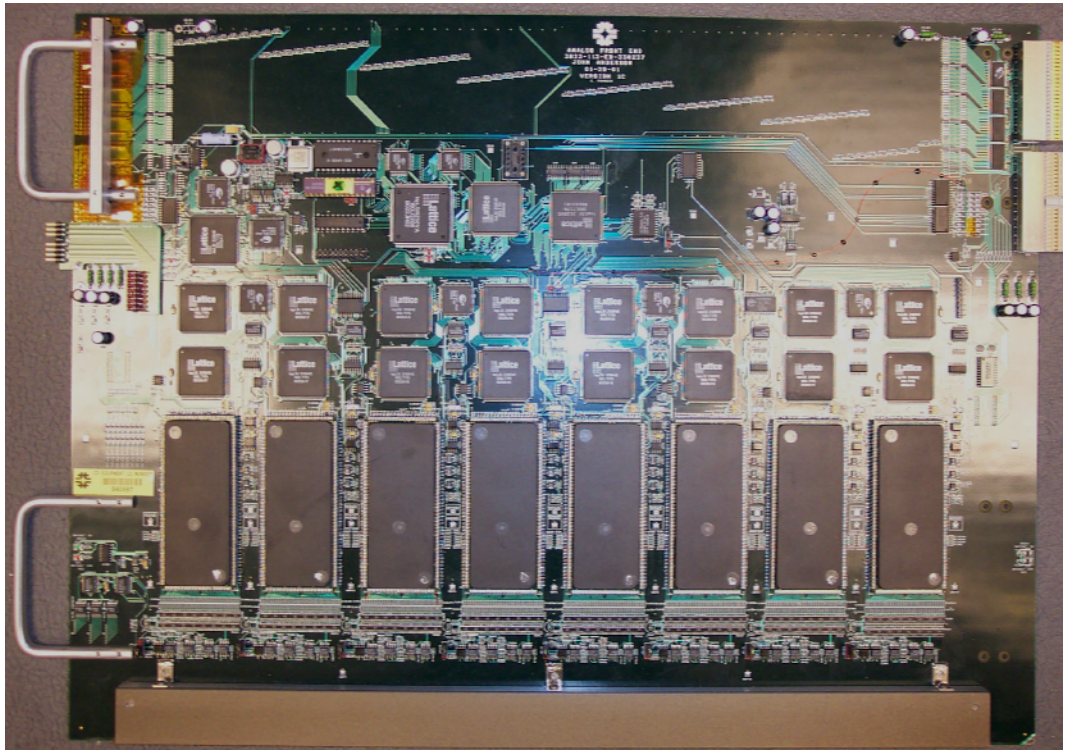
TriP Chip

The chip (cont.) – feed back details



System Design

- Big advantage- already have system installed
  - Boards exist
  - Testing infrastructure exists



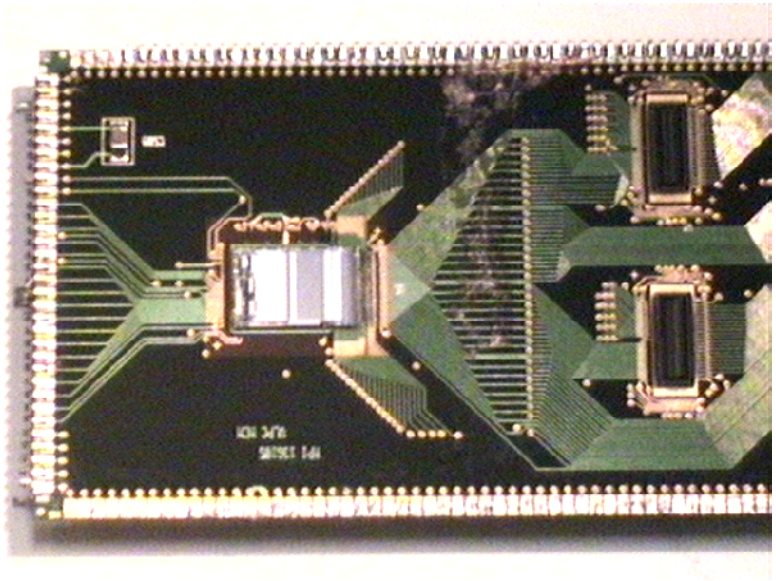
For testing, adapt the TriP to existing boards

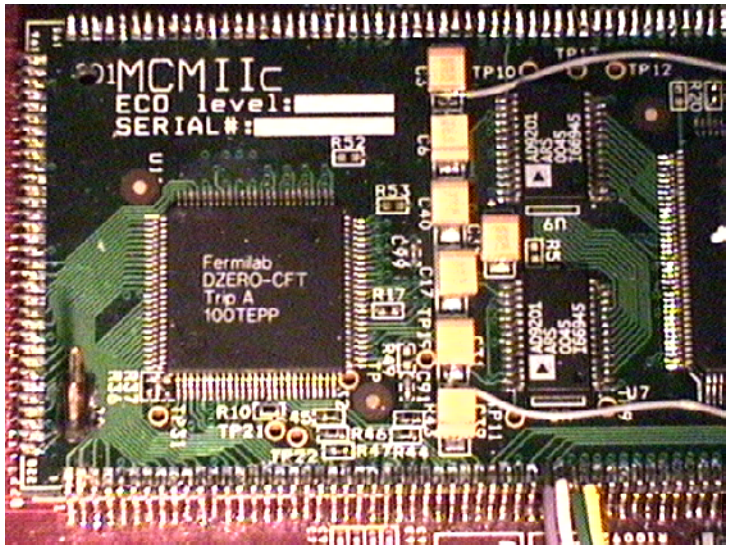
Build new MCMs, mount on existing boards – for testing

Full replacement- new boards (200 boards)

System Design

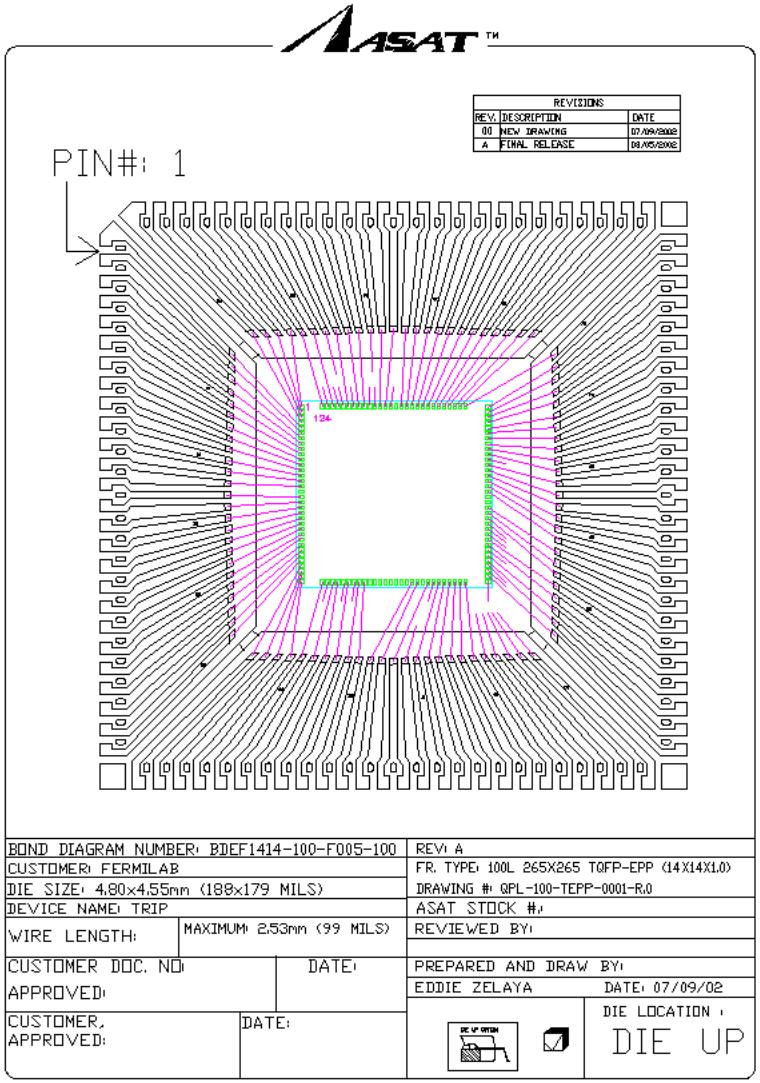
- **System concept critical (for cheap and fast)**
  - Do only what must be done in custom silicon
  - Use commercial chips where possible (ADC,FPGA)
  - Package the chips



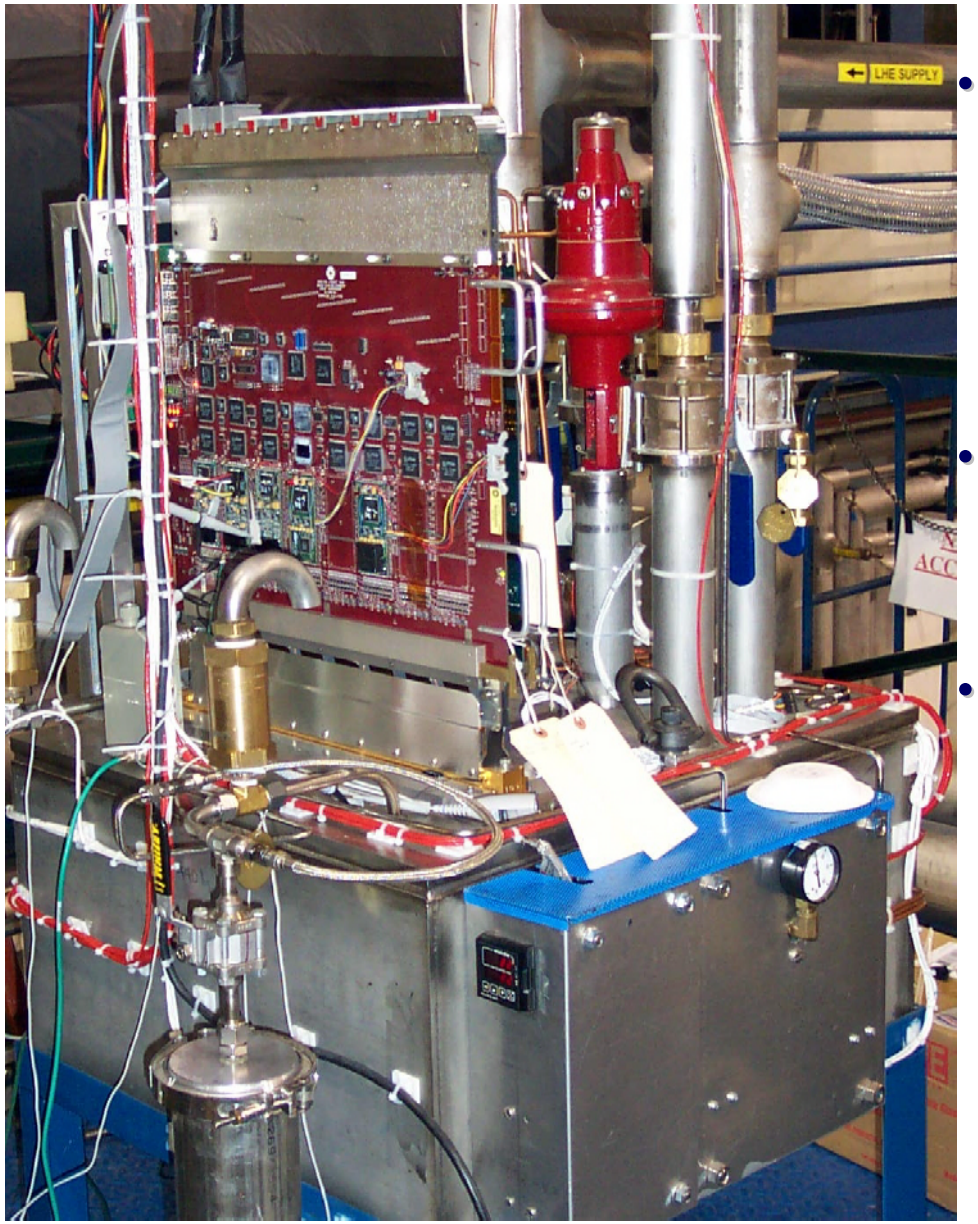


Packaging

- Chip packaging
  - 124 pins on the die
  - 100 pins on the package
  - Electrical performance in testing so far is no diff. between packaged part and wirebonded bare die
- ASAT ExposedPadPack (other companies have similar technology)
  - large metal pad on which die sits exposed on bottom
  - attached with conductive epoxy: very low L ground



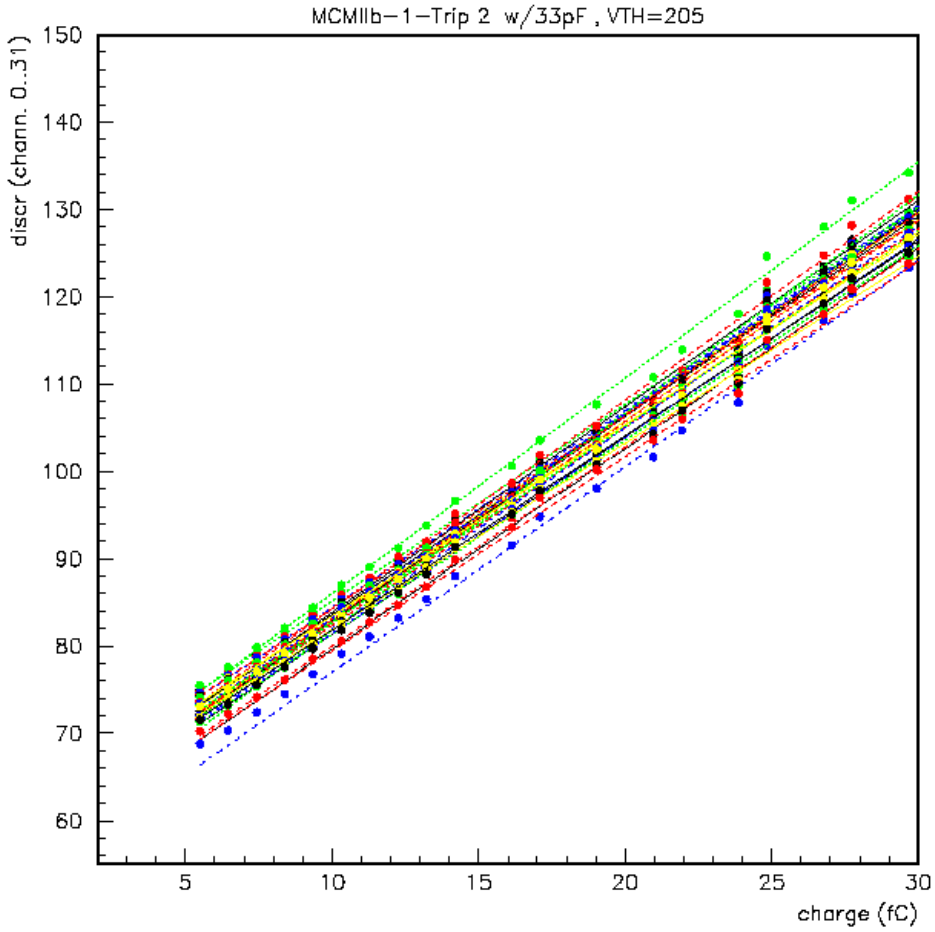
Evaluation

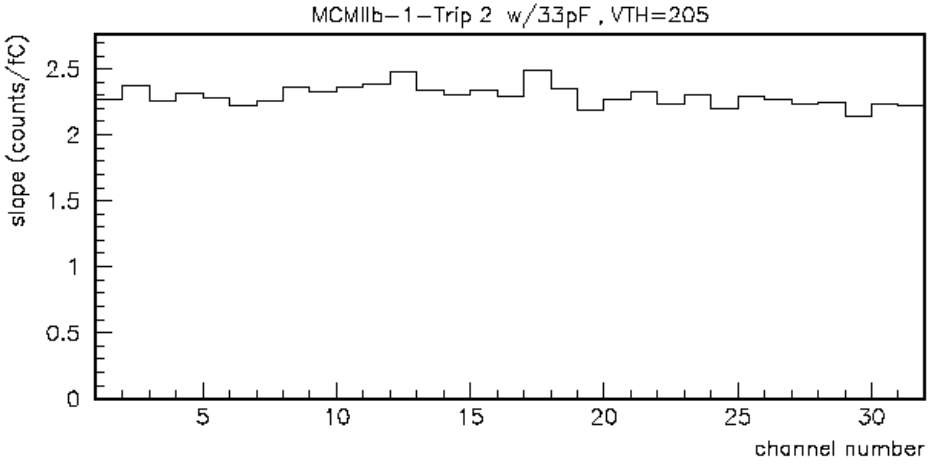


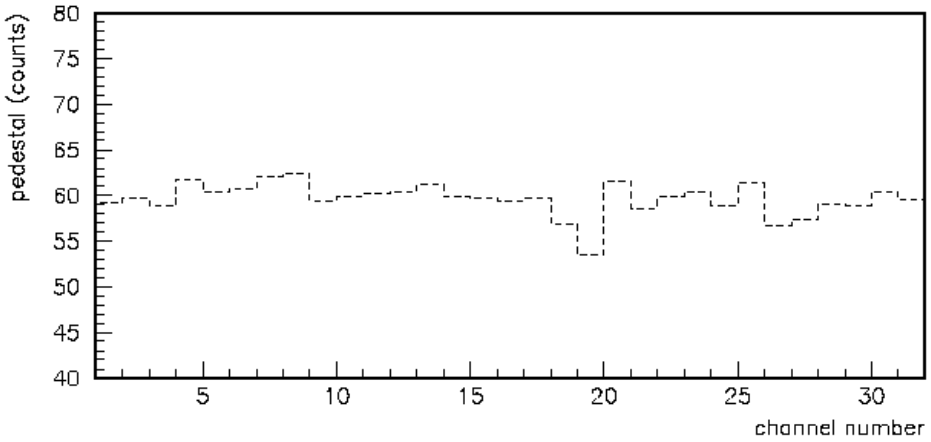
- Made new MCMs compatible with existing system
  - Two versions:
    one with single packaged chip
    one with two wire bonded chips
- Tested extensively on bench (D0Note 4009 and 4076)
- Now started testing with VLPCs

Evaluation

Performance: ADC scan

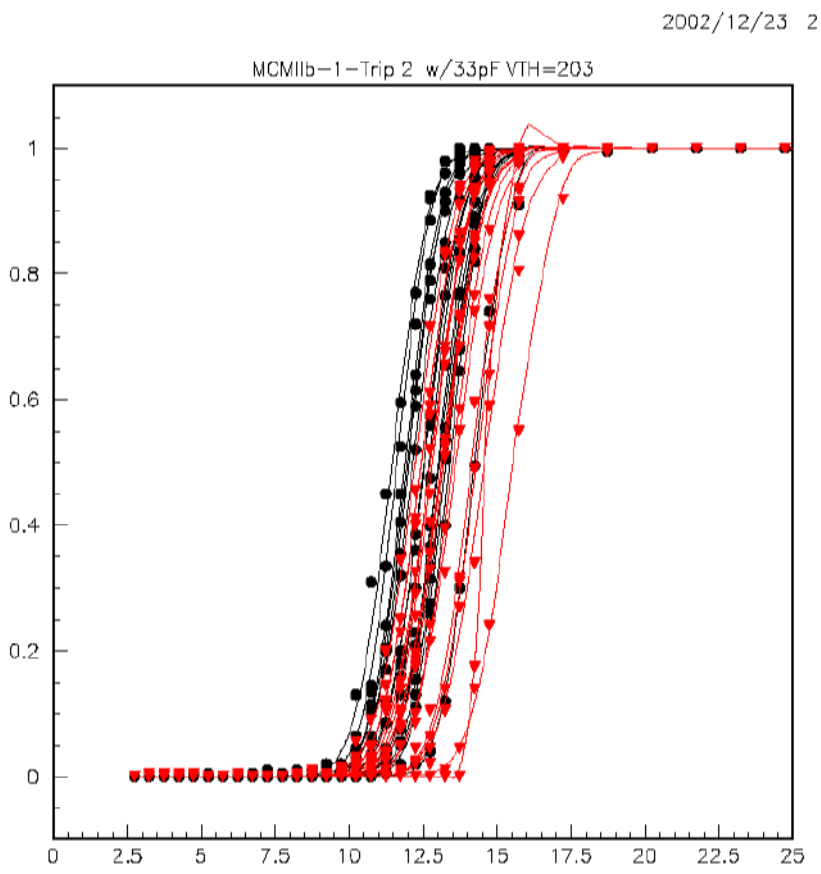


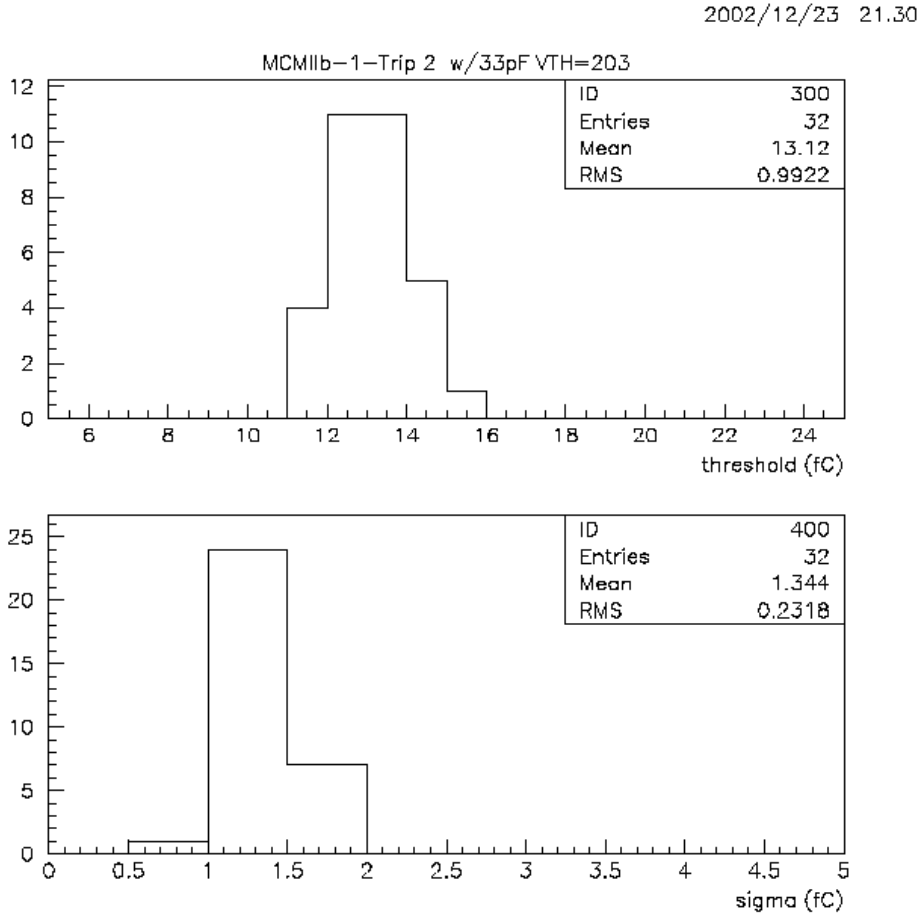




Evaluation

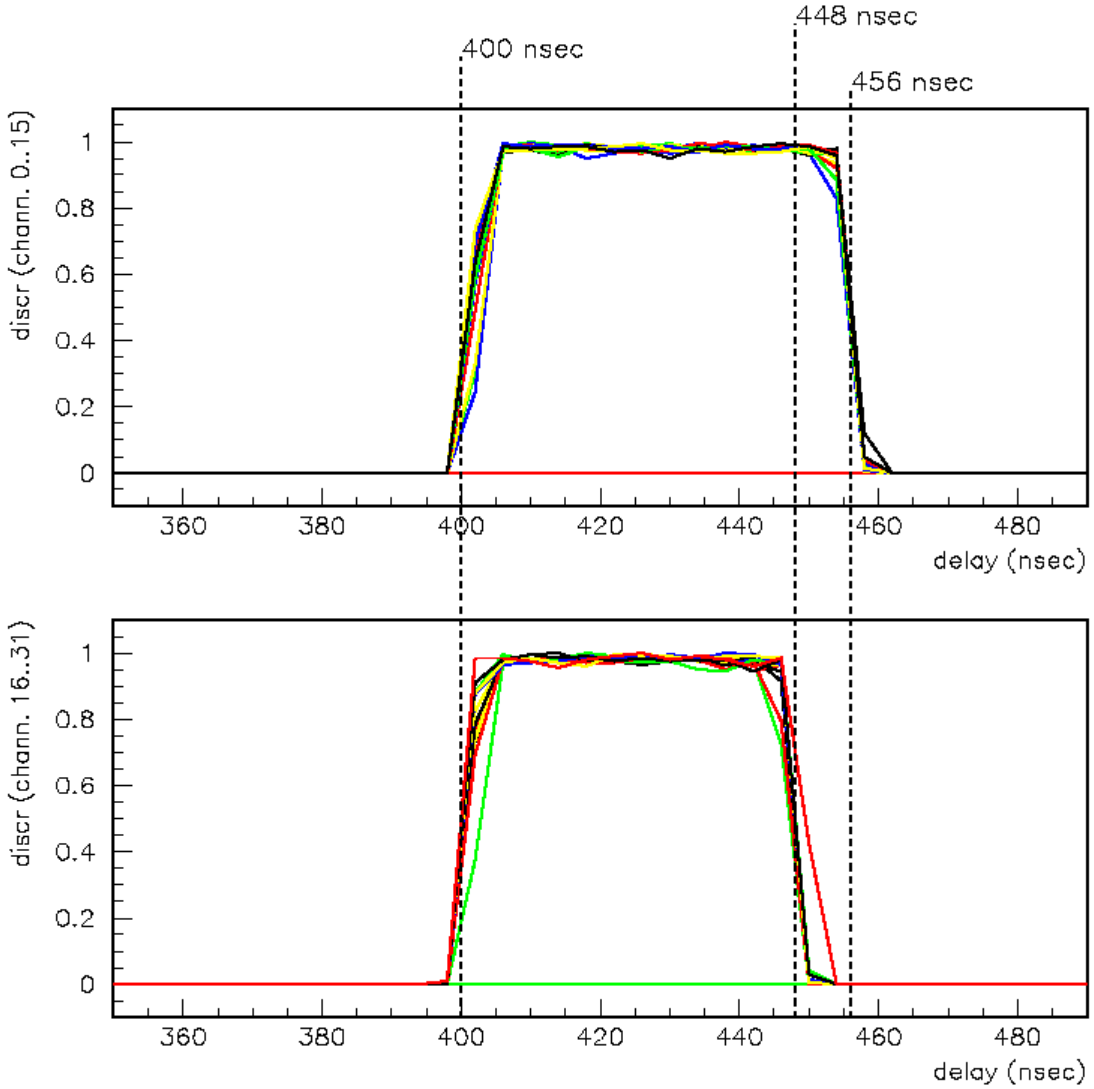
Performance: DISC scan





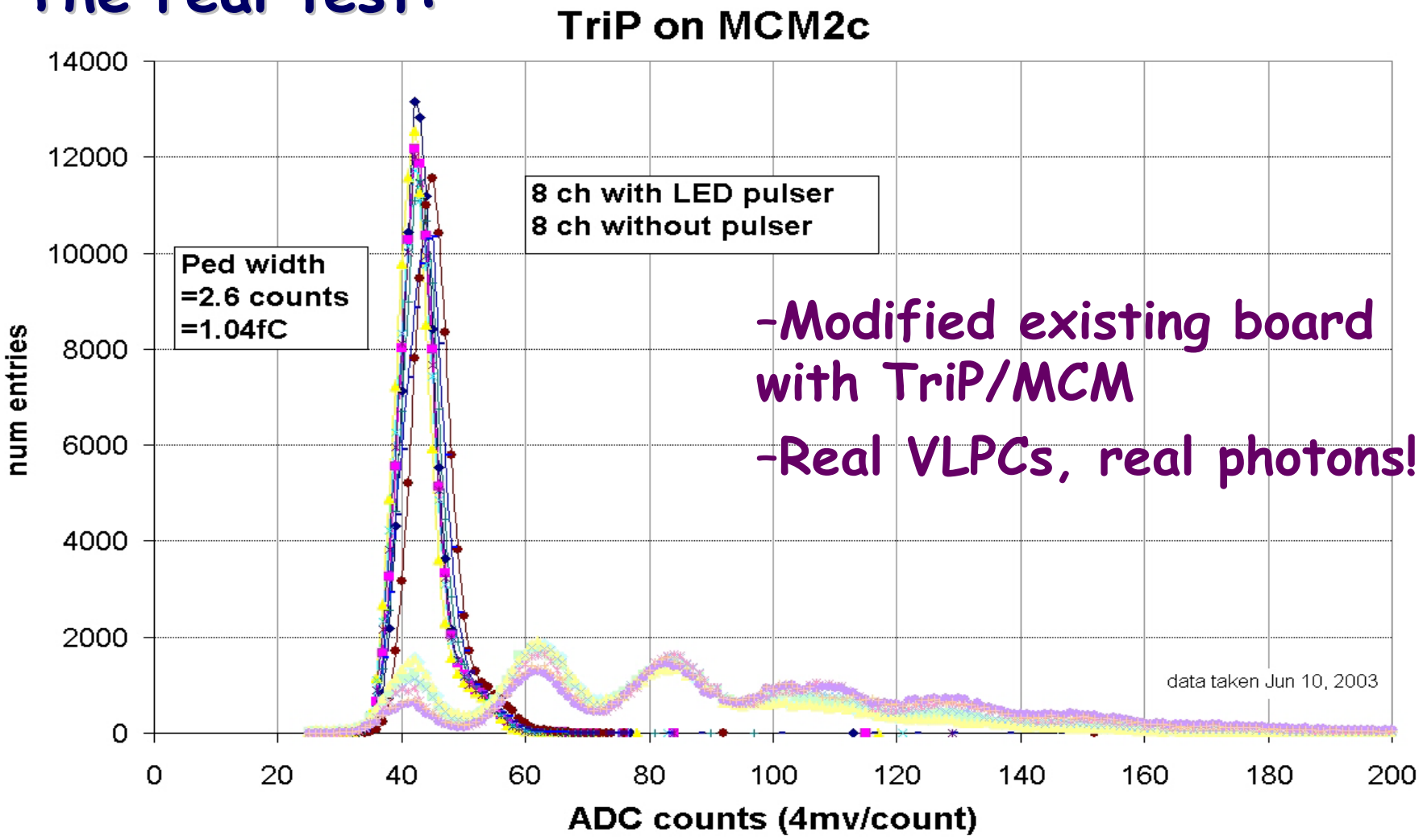
Evaluation

Performance: timing scan



Evaluation

- **The real test:**

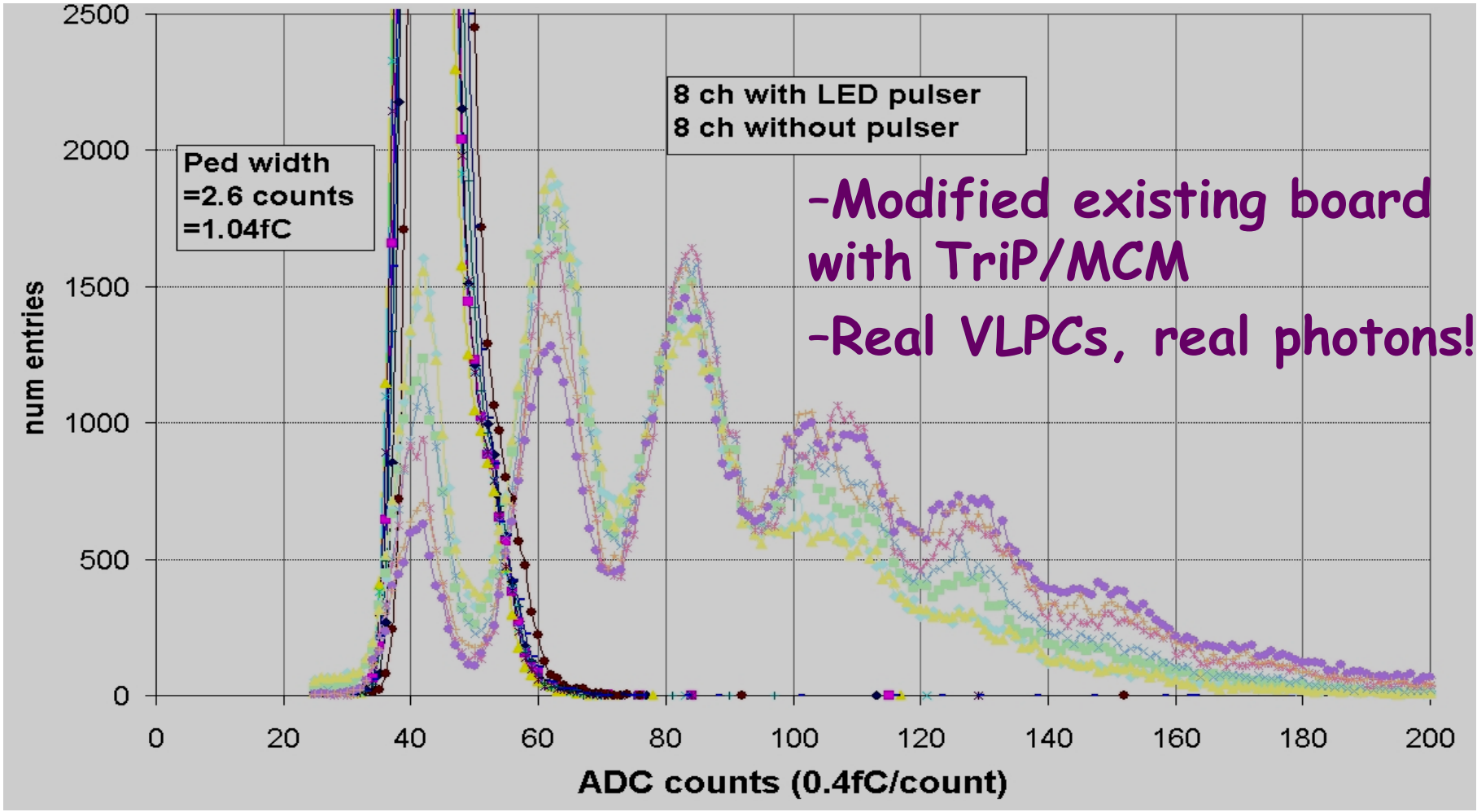


-Modified existing board with TriP/MCM

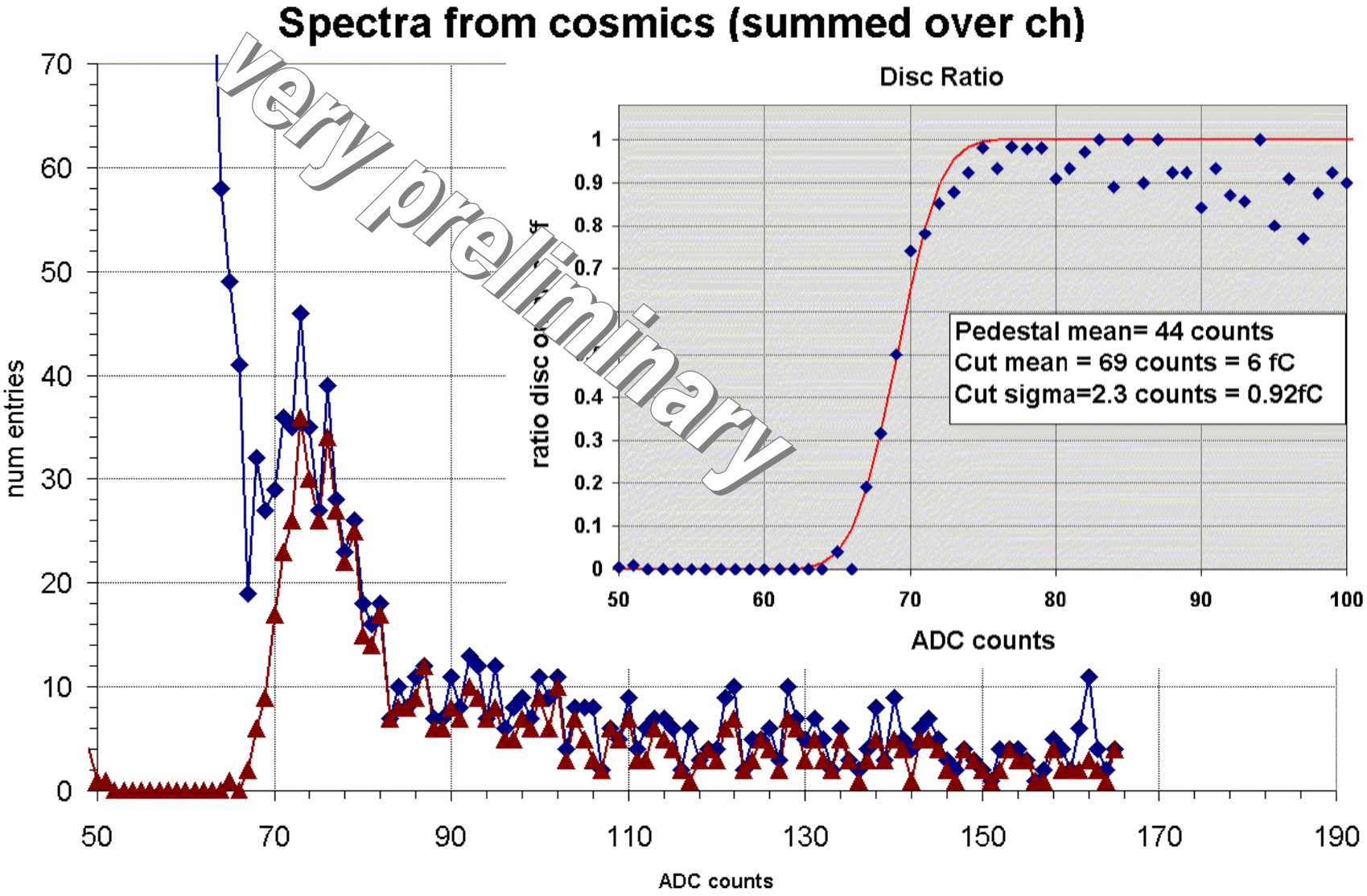
-Real VLPCs, real photons!

Evaluation

- It works!

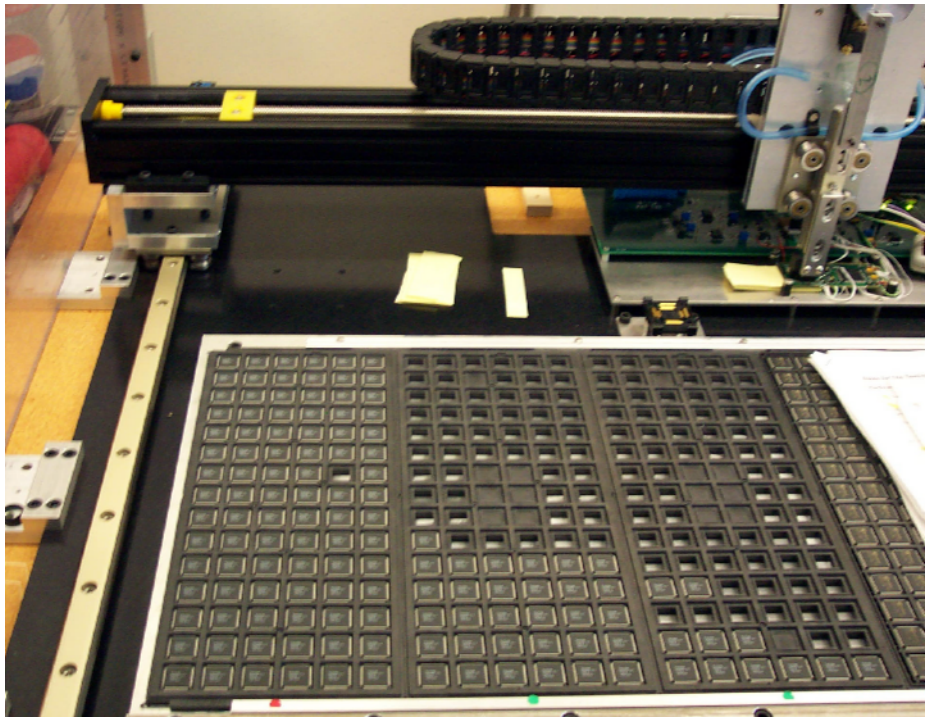


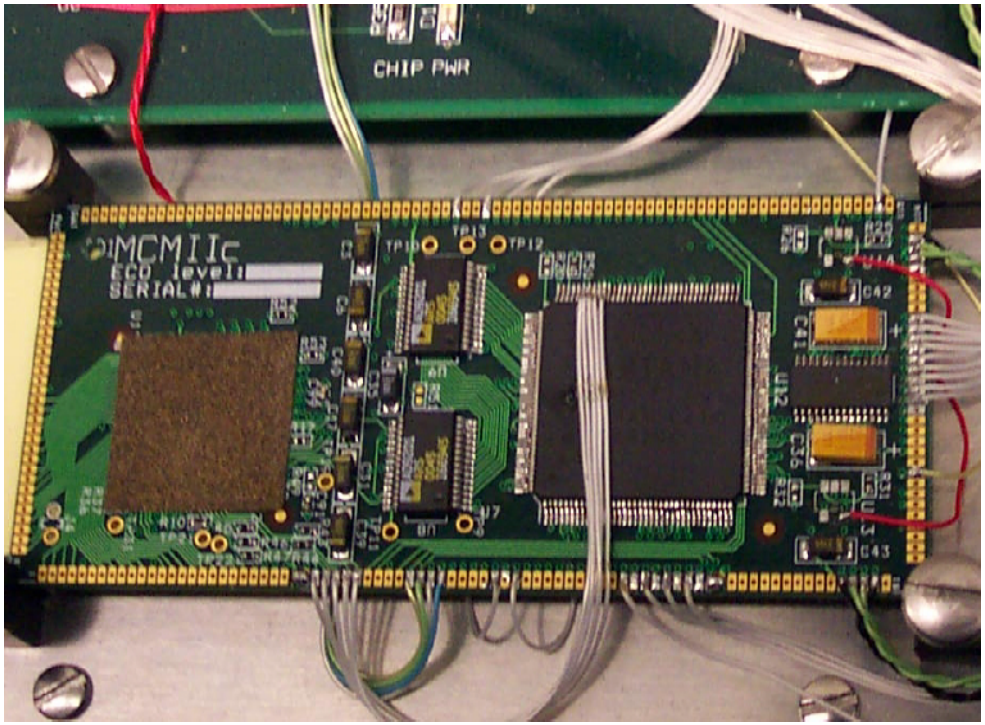
Evaluation


Spectra from cosmics (summed over ch)
very preliminary
num entries
ADC counts
Disc Ratio
ratio disc of
Pedestal mean= 44 counts
Cut mean = 69 counts = 6 fC
Cut sigma=2.3 counts = 0.92fC
ADC counts

Chip Testing

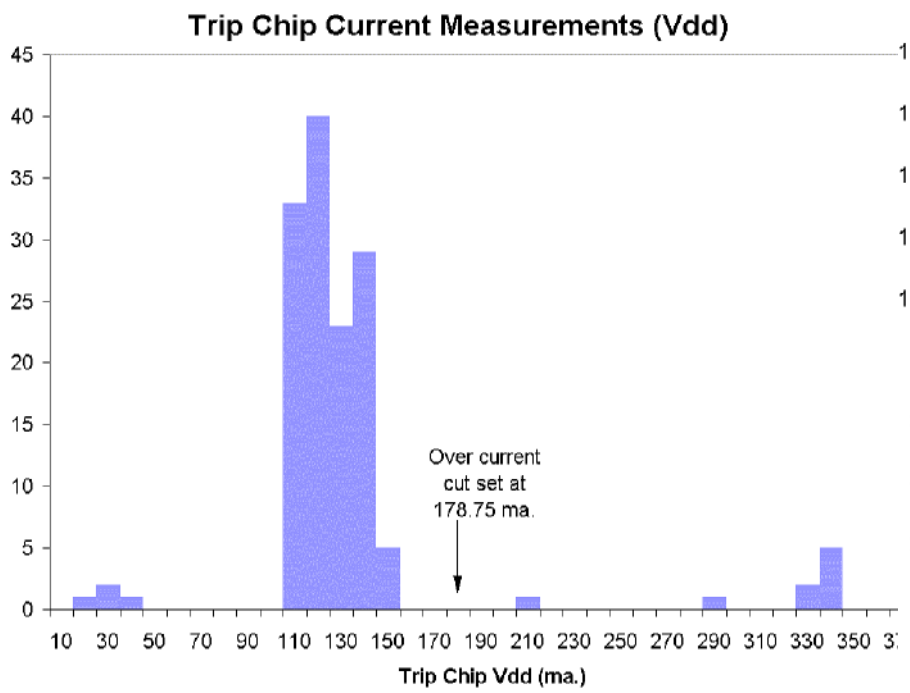
- Do it fast, do it cheap
  - Chip testing robot/tester box connected to MCMIIc using ShinEtsu MAF2-8 conductive mat

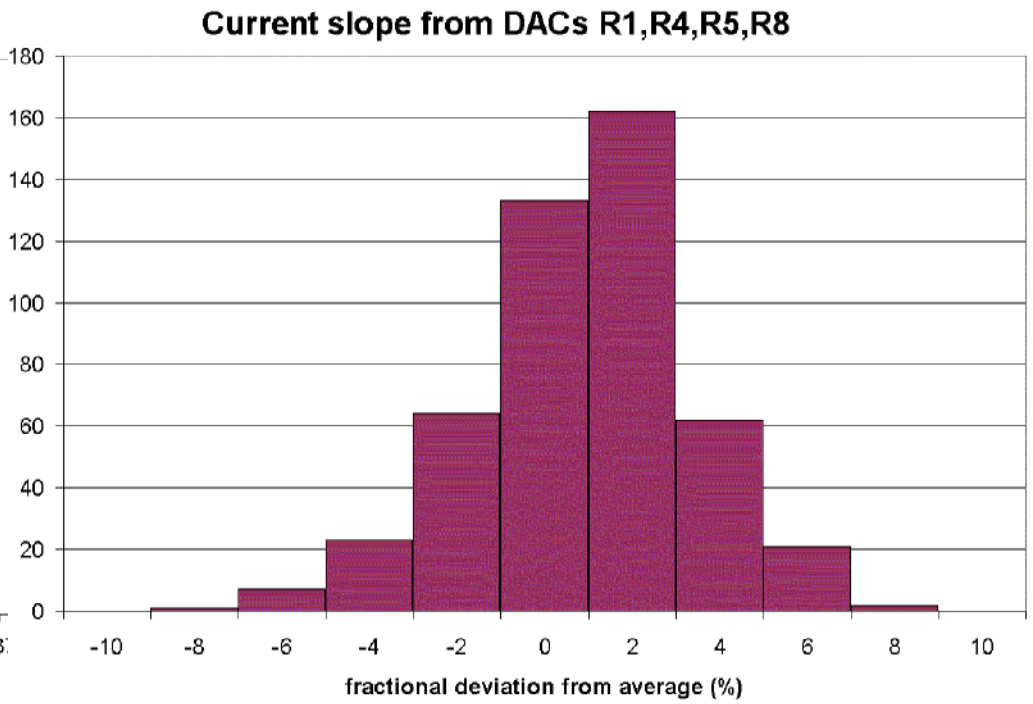




Yield

- 132 packaged chips tested
  - 10 chips failed Vdd current test, 2 failed register R/W
  - Functional testing of chips underway
- 90% are ok… so far





Conclusions

From Dzero note 4076

Window for charge collection:	40 to 45ns	Not optimized yet. Probably ok.
50 to 70ns.		
Digital outputs:		
risetime controlled active only during reset	no no	No, but work around was found.
Threshold setting:(high gain)		
0 to 100fC with 7bit control	satisfied (prelim)	More testing, especially with larger inj charges would be usefull.
99% of channels within 4fC	4fC w/o caps 5fC w/33pF acceptable	Packaged part, no load.
rms noise <1fC	<1fC w/o caps 1.3fC w/ 33pF acceptable	Packaged part, no load. 33pF load.
Threshold setting:(low gain)	not yet tested	
Analog outputs:		
16:1 analog mux at 7.6MHz ch to ch uniformity within +-3%	satisfied 6% slope, 3% peds 8% slope, 5% peds satisfied	Packaged part, no load. 33pF load. Some spread is due to layout of MCM.
rms noise <1fC	0.6fC RMS w/o C satisfied 1.2fC RMS w/ 33pF acceptable	Packaged part, no load.

Conclusions

From Dzero note 4076

Window for charge collection:	40 to 45ns	Not optimized yet. Probably ok.
50 to 70ns.		
Digital outputs:		
risetime controlled	no	No, but work around was found.
active only during reset	no	
[illegible]		
0 to 100fC with 7bit control	satisfied (prelim)	More testing, especially with larger inj charges would be usefull.
[illegible]	4.2fC w/ caps	Packaged part, no load.
	5fC w/33pF	
	acceptable	
rms noise <1fC	<1fC w/o caps	Packaged part, no load.
	1.3fC w/ 33pF	33pF load.
	[illegible]	
Threshold setting:(low gain)	not yet tested	
[illegible]		
16:1 analog mux at 7.6MHz	satisfied	
ch to ch uniformity within +-3%	6% slope, 3% peds	Packaged part, no load.
	8% slope, 5% peds	33pF load.
	satisfied	Some spread is due to layout of MCM.
rms noise <1fC	0.6fC RMS w/o C	Packaged part, no load.
	satisfied	
	1.2fC RMS w/ 33pF	
	acceptable	

- Chip worked on the first try.
- Its not perfect but it is, in our judgment, good enough.
- We want to continue development because the requirements have changed*.

*Ask me later if you are interested in an energetic discussion of accelerator physics

Evaluation

Performance (from Dzero Note 4076)