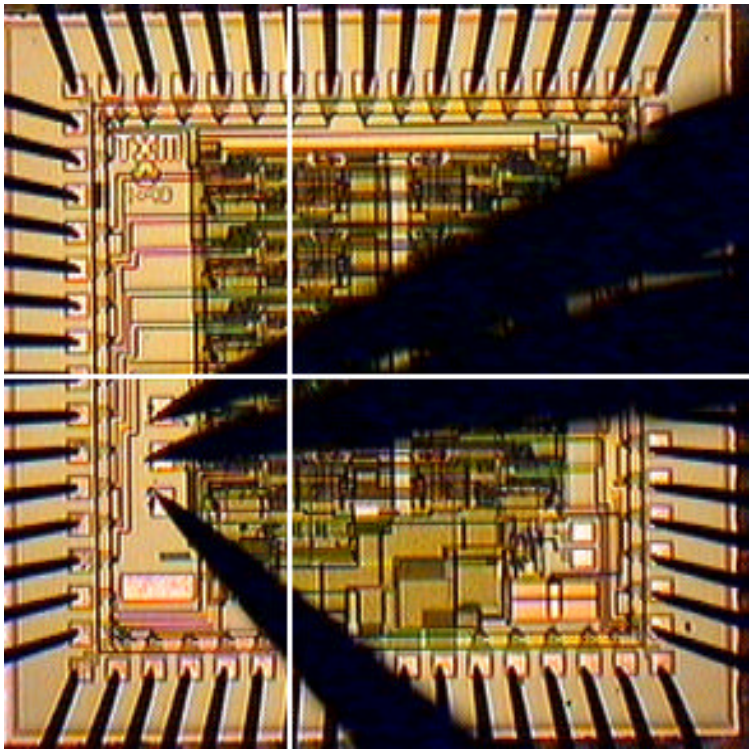
Wafer level Testing of ASICs for Silicon Strip Detectors



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Introduction

All chips are tested at some time

- On board test – least information about part
- Bare die or package test – can check parameter space
- Wafer level test – gives additional information but may not be sufficient due to dicing loss, etc

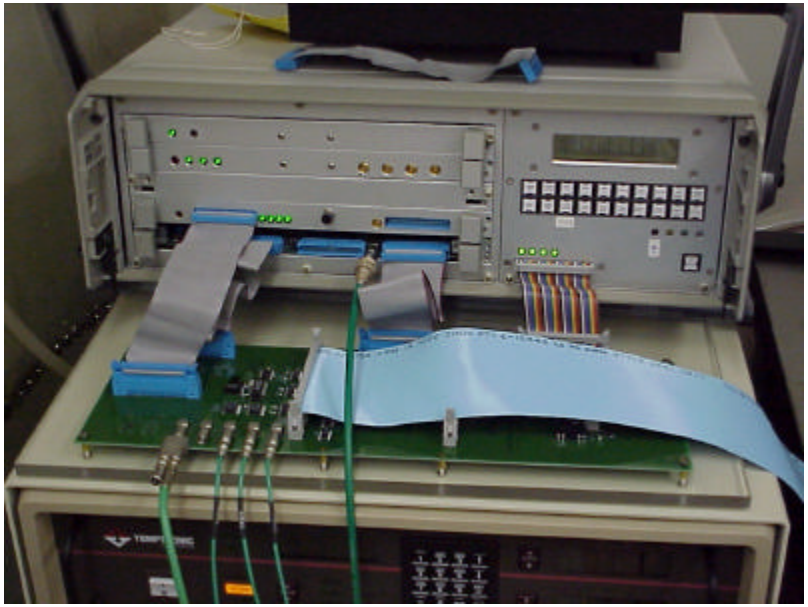
Wafer level testing – powerful tool

- Can help identify design problem
- Can help identify processing problems

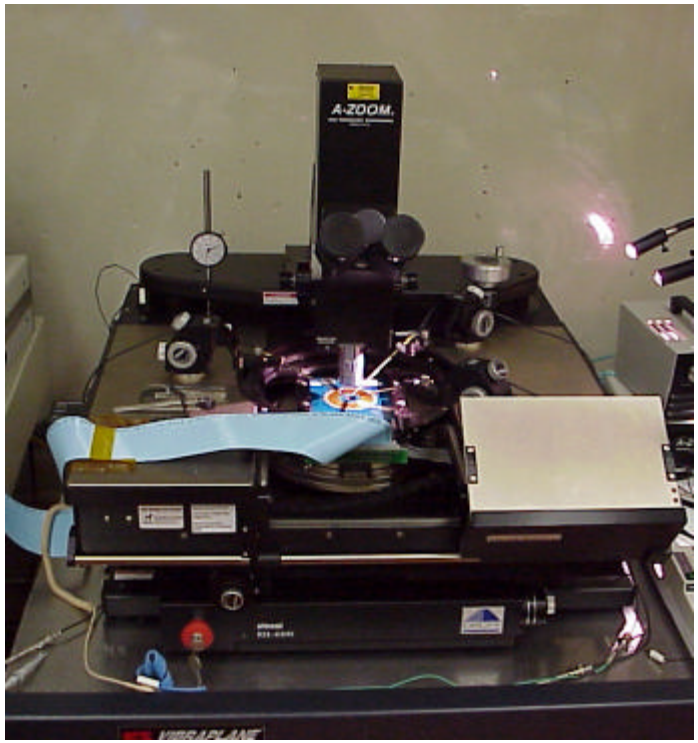
Presentation to cover Fermilab experience with 3 different chips

- 10 channel Transceiver
- DAC, Decoder, and Regulator
- 128 channel silicon strip readout chip

Equipment Used



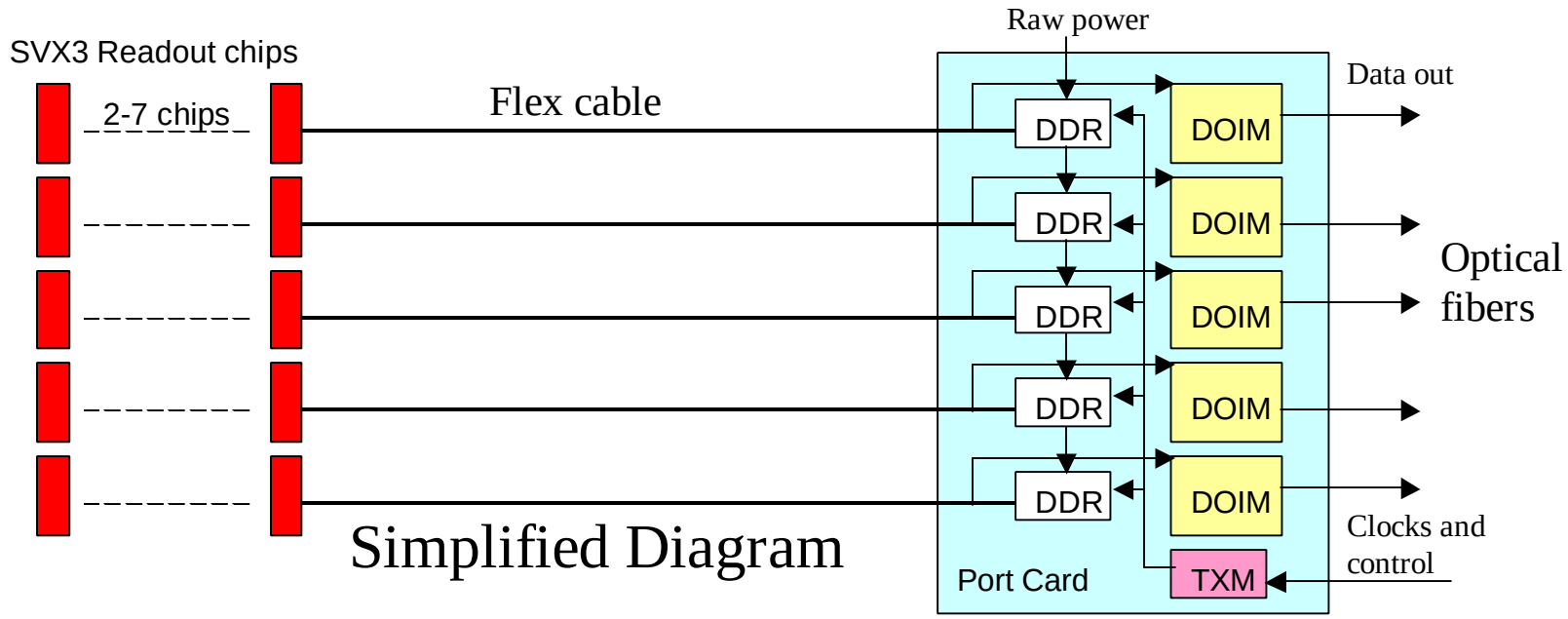
Test and data acquisition package.
Computer not shown.



Wafer level testing requires an automated probe station and a custom probe card along with an automated test/data acquisition system. The entire system is under computer control. The above photos show the automated data acquisition package and the probe station used for 2 of the chips at Fermilab. A similar system was used at LBNL to test the third chip.

Silicon Strip Readout Chips

- TXM – bi-directional transmitter and receiver chip for communicating with the SVX3.
- DDR – DAC/Decoder/Regulator chip. Decodes commands to SVX3, Regulates power to SVX3, and provides analog reference to SVX3
- SVX3 – 128 channel CMOS device with integrator, analog pipeline, ADC, and sparcification for each channel.



TXM and DDR Wafer Tests

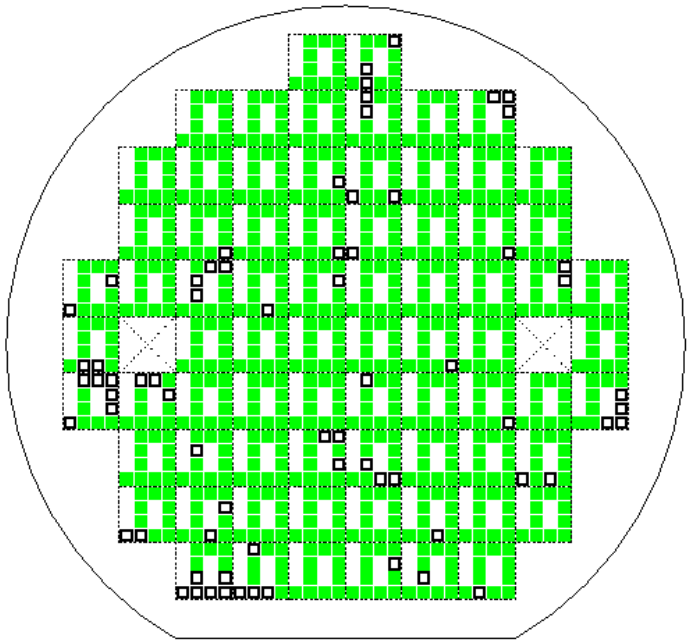
Reticule Layout

- The DDR and TXM chips were placed in the same reticule as shown to the left and manufactured at the same time.
- Two lots were run
- The second lot was run due to problems found during testing of the first lot.

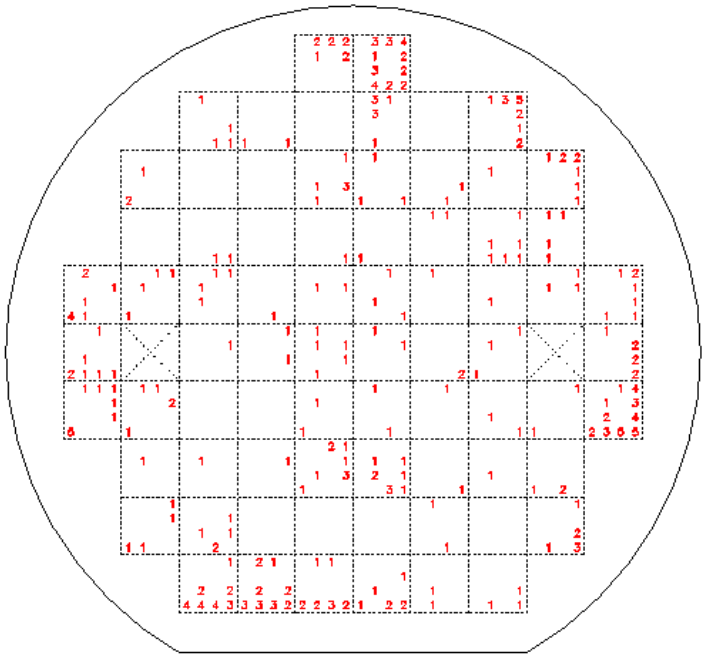
TXM Chip Tests

- TXM is a digital transceiver chip. Tests are primarily digital.
- Digital tests – measure transmitter performance and receiver performance under various conditions. Feed data through chip and check integrity.
- Analog tests – measure power supply current and internal bias voltage under various digital conditions

TXM Test – Lot 1



Typical wafer plot showing good (green) and bad (white square) TXM dice.



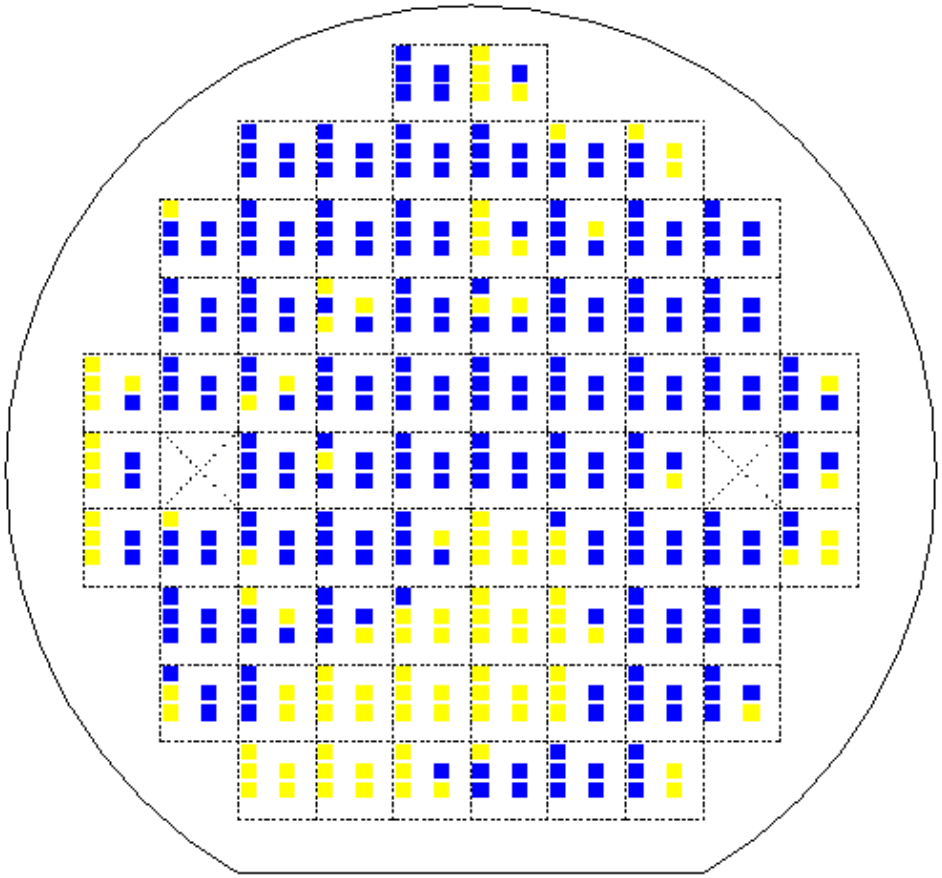
Summary plot showing number of bad TXM in each location for lot 1.

- Five wafers in lot 1
- High yield – 92 % over 5 wafers
- Bad chips clustered primarily around edge of wafer as to be expected

DDR Chip Tests

- The DDR is comprised of several separate analog and digital sections.
- Analog sections have op amps (there are 4 on the chip) for DACs and regulators.
- Analog tests include power supply current, DAC, and op amp measurements.
- Digital section is combinational logic
- Digital tests include toggling all bits to be decoded and verifying proper operation.

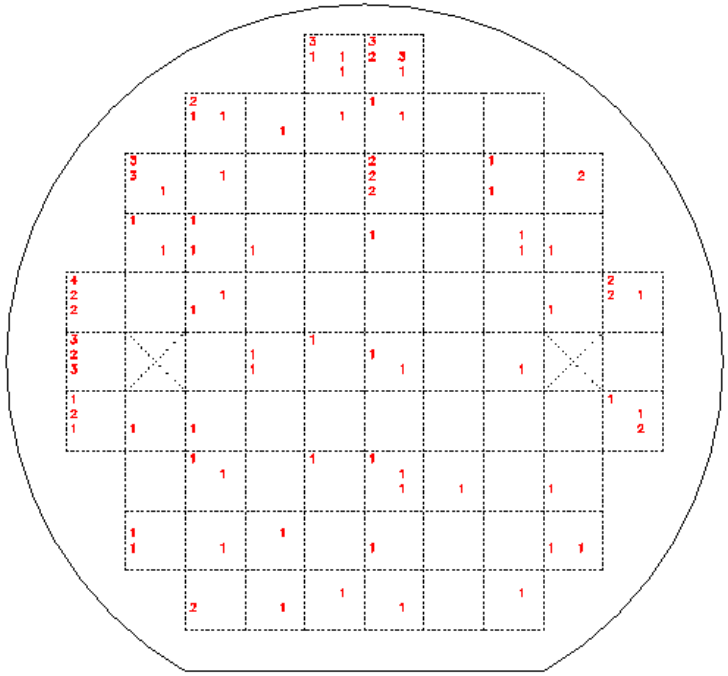
DDR Wafer Tests – Lot 1



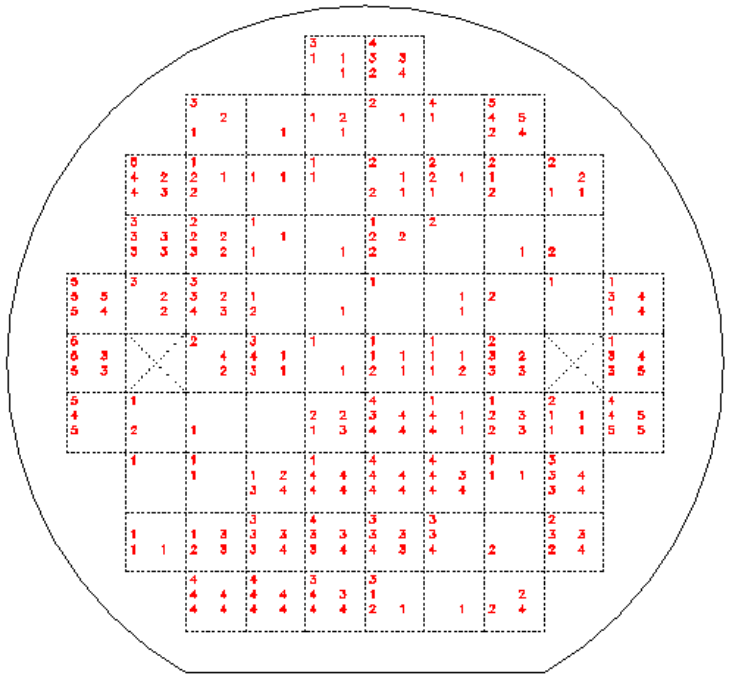
- Wafer yield maps showed an unusual characteristic in lower left portion of all wafers.

Typical DDR yield wafer map showing results of analog and digital tests. Blue = good, yellow = bad.

Summary of Analog and Digital Tests on Four and One Half Wafers of DDRs from Lot #1



DDRs that fail digital test



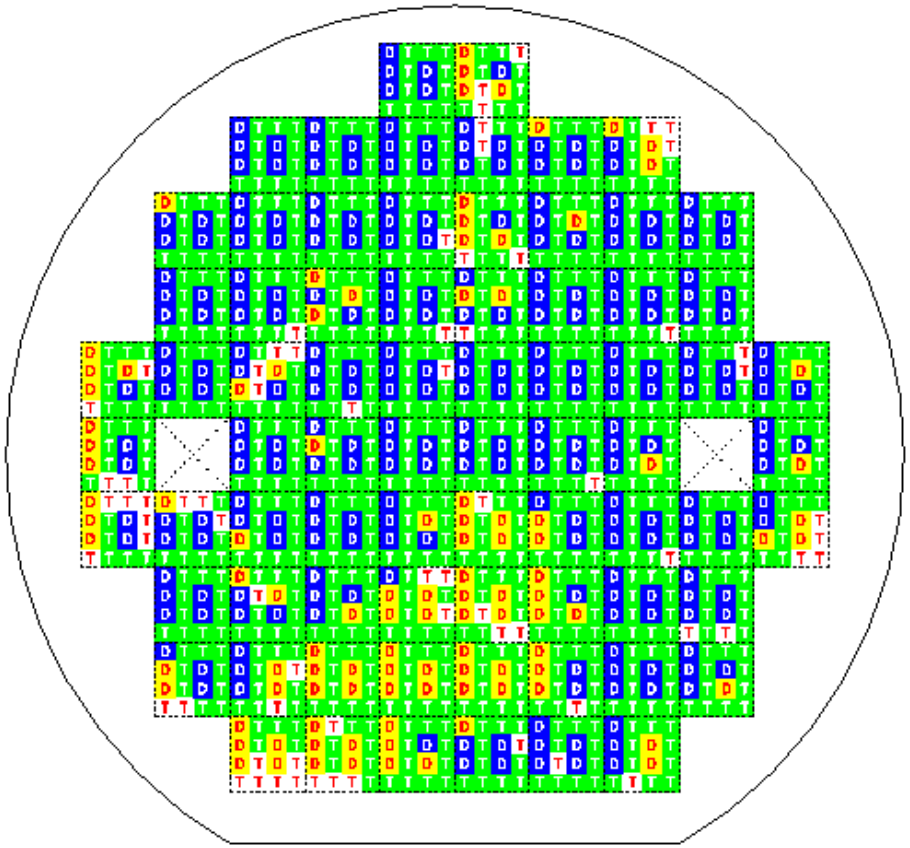
DDRs that fail analog test

- Plots show the number of chip failures in a given location on the wafer for 4 full wafers and the top half of a 5th wafer.
- Digital test results similar to TXM chips – a few failures near the edges.
- Analog test results show location specific anomalies.
- Test pads were added using FIB to allow probing of failed parts.

DDR Failures in Lot 1

- Predominant failure mode is due to gate-drain and gate-source transistor leakage in op amps.
- Leakage currents as high as 20 μa were measured.
- Examination of layout showed a large area of poly connected to gate on leaky transistors.
- Consultant suggested problems caused by plasma etching during processing which damages gates causing leakage current.
- Manufacturers antenna rule spec not violated. (A_r=poly area/gate area < 300). Design A_r = 260.
- Design changed in Lot 2 (A_r = 1.2) to reduce risk of damaged gates on good as well as bad devices.

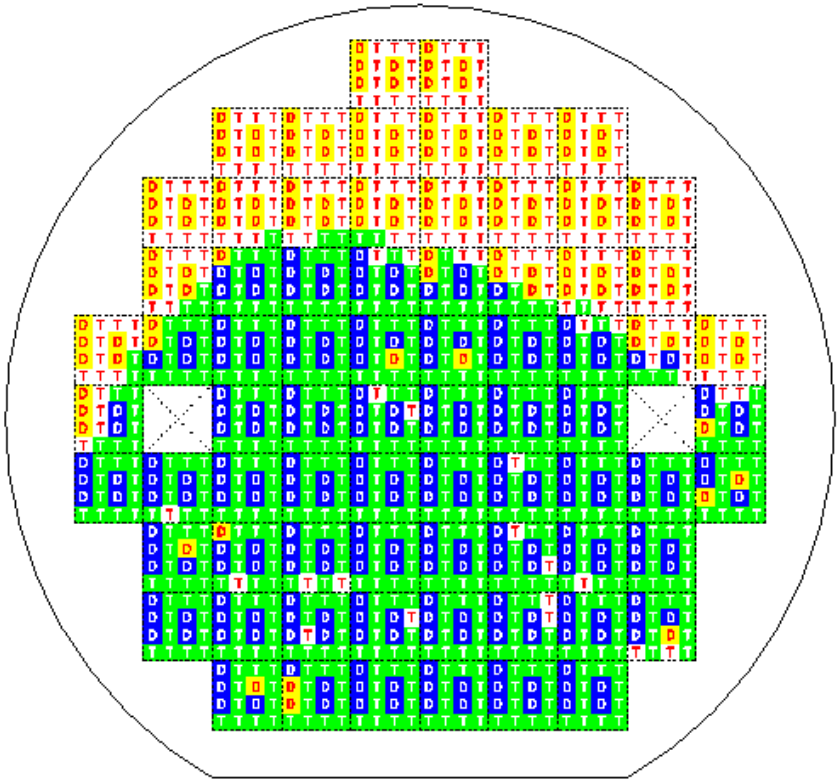
Combined Wafer Map for TXM and DDR (Lot 1)



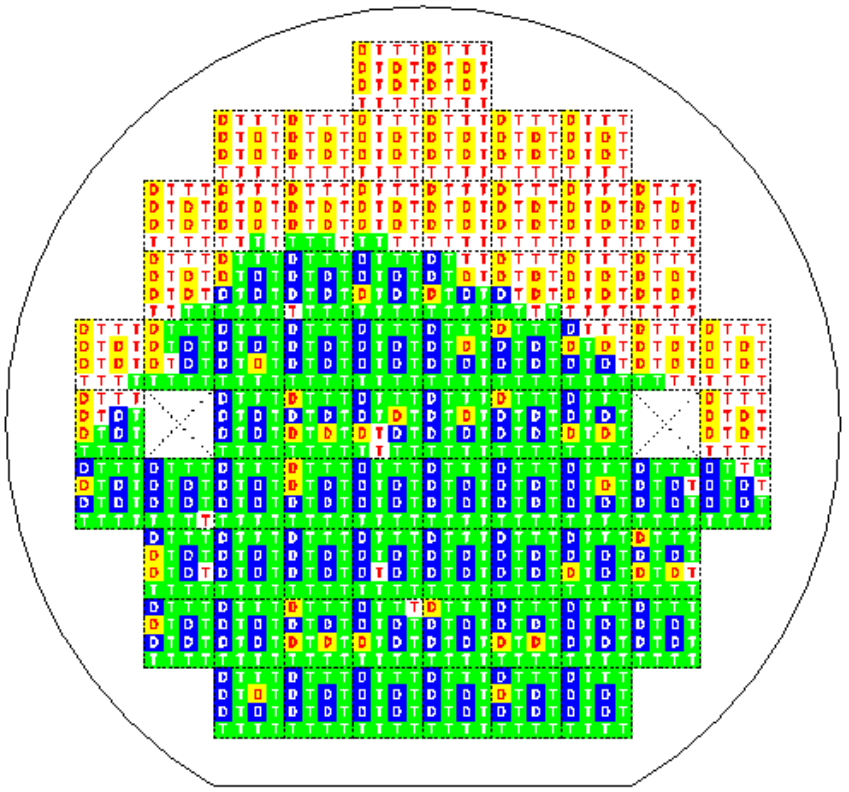
Typical wafer map from lot 1 showing combined TXM and DDR plot. (Yellow/white = bad chip)

- TXM lot 1 yield = 91.7%.
- DDR lot 1 yield = 62.5%.
- If DDR parts were sampled from either the top or the bottom of a wafer, inaccurate yield estimates would occur.
- Additional losses do occur during dicing.

TXM and DDR Lot 2 Wafer Tests



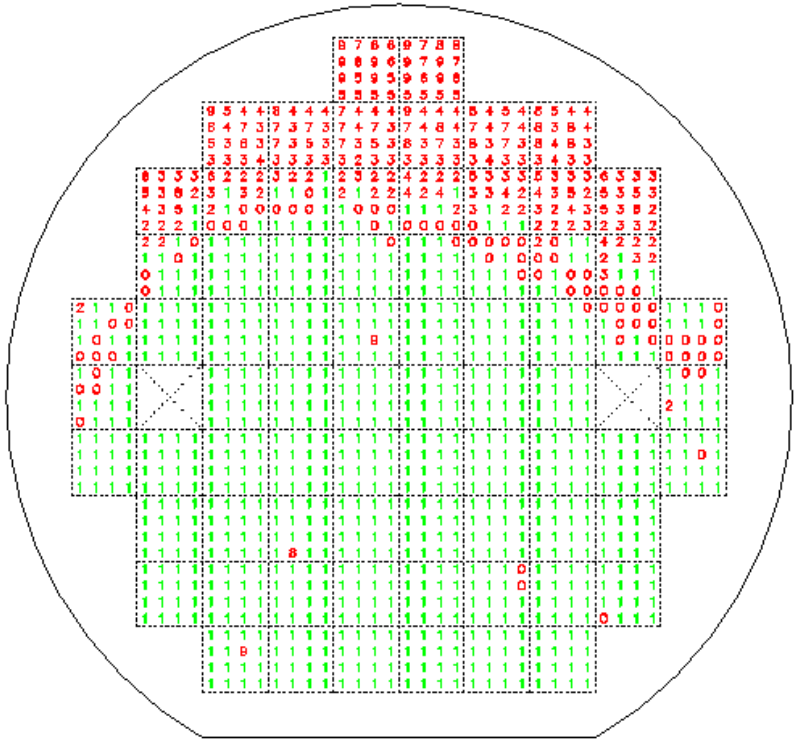
Lot 2, wafer #1



Lot 2, wafer #2

- In lot 2 wafers, the DDR leakage problem is gone.
- A different problem exists at the top of all wafers for both TXM and DDR chips. (Grn/Blu = good, Yel/Wht = bad)

TXM and DDR Lot 2 Wafer Tests



Plot shows relative magnitude of power supply current on one wafer for TXM and DDR chips. (1= normal, 0 = low, 2 and higher show increasing current)

- Power supply currents are increasing dramatically in area with bad TXM and DDR chips.
- Cause of the problem is unknown.
- Testing either the top or bottom of wafer alone gives completely incorrect yield results.

TXM and DDR Summary

- Lot 2 yields lower than lot 1

	Lot 1	Lot 2	Lot 2*
TXM	91.7%	67.7%	93.8%
DDR	62.5%	59.9%	86.8%

* Bad parts near top not included.

- Not well controlled process (RICMOS IV bulk process, 6” wafers)
- For highest reliability, only use parts away from failure border line. Can only be done from a wafer map.

SVX3 Wafer Tests

- SVX3 is complex analog/digital chip for reading out silicon strip detectors.
- 128 channels each with 42 analog pipeline cells and an ADC. Every cell in every channel was tested multiple times.
- 17 different tests performed on each wafer. Some tests quite complex.
- Testing of one 6” wafer took about 8 hours.

Tests Performed

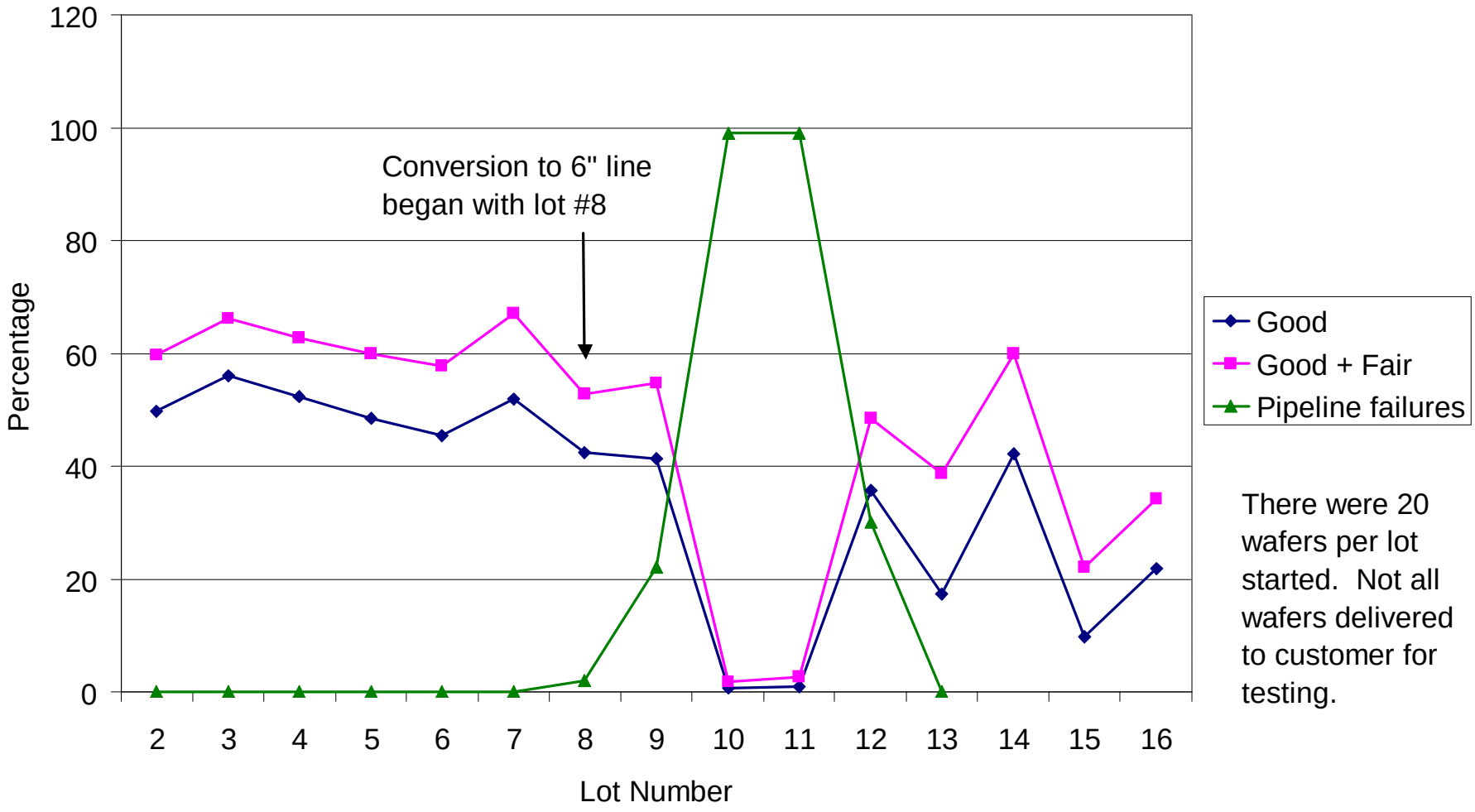
- Analog and digital P.S. currents*
- Programmability (serial input)*
- Basic readout and chip ID*
- Pedestals and noise
- Calibration mask
- ADC limits
- Pedestal adjustment
- Common mode suppression
- Gain
- Sparsification
- Sparsification threshold scan
- Priority passing
- Data valid check
- Gain adjustment
- Multi-hit operation
- Dead-timeless performance

*Essential for further tests

SVX3 Production History

- Production started in 1998 on 4” line
- Production switched to 6” line in 1998 and continued into 1999
- Significant problems encountered with product from 6” line.
- Long period of time to analyze the problem encountered on 6” line product and work out agreement with vendor. During this time wafer production stopped.
- Total of 15 twenty wafers lots produced.
- Wafer level testing was essential in understanding the problem and dealing with vendor.
- All product has now been delivered and is now being assembled.

SVX3 Lot to Lot Yield Summary



There were 20 wafers per lot started. Not all wafers delivered to customer for testing.

Typical SVX3 Wafer Plots from an Acceptable 4” and 6” Wafer

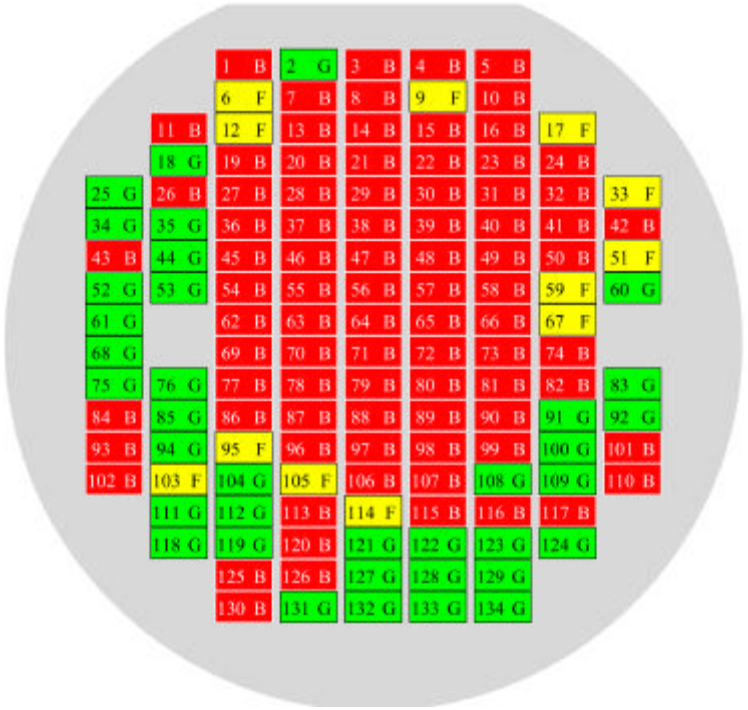
Lot 6 wafer 12

Lot 8 wafer 8

- Number on the wafer indicates die location
- Green = all channels good, yellow = 1 bad channel, red = more than 1 bad channel.

Unacceptable SVX3 Wafers

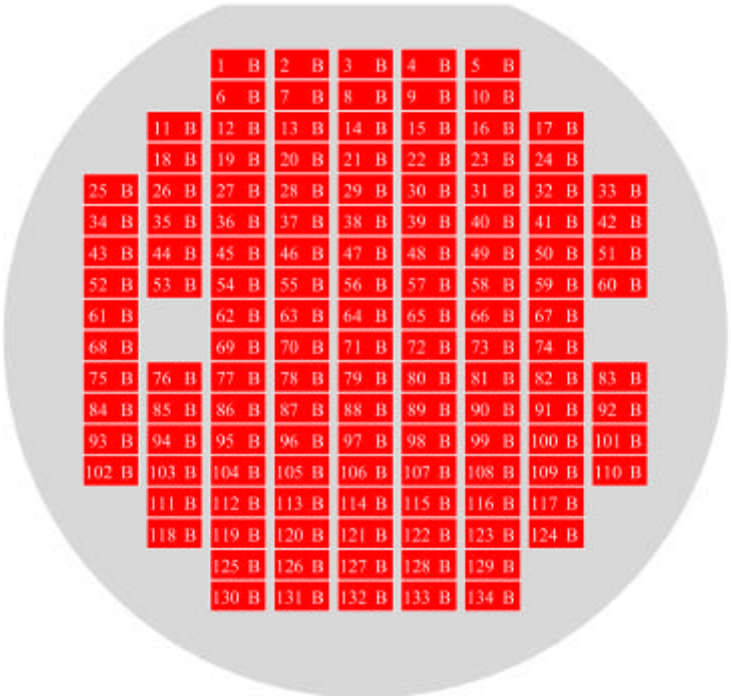
Lot 9 wafer 14



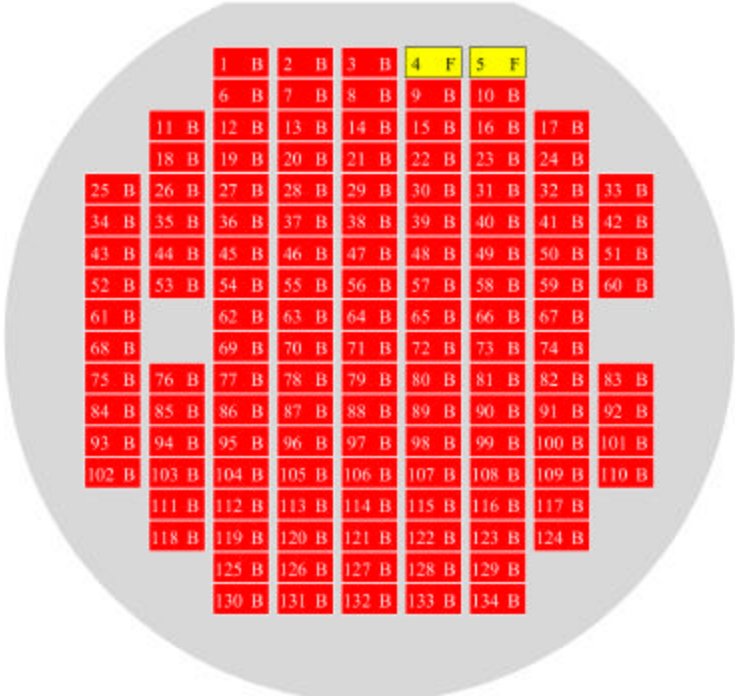
Lot 12 wafer 1

- Lots 9 and 12 generally show all bad chips in the center and good chips around the edge – very unusual.
- Die failure pattern suggests a processing problem.

Unacceptable SVX3 Wafers



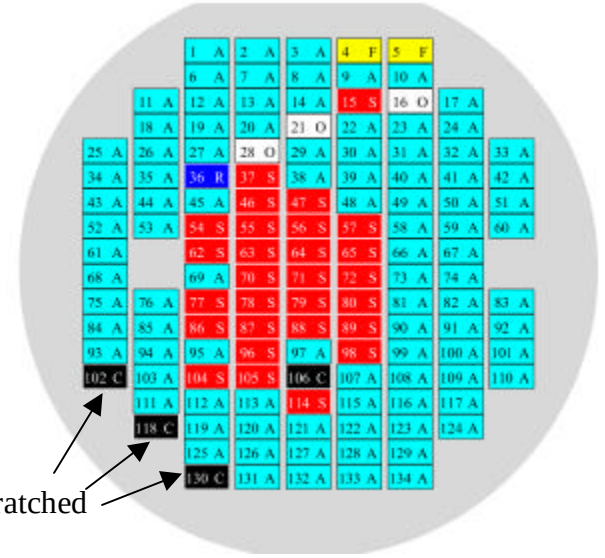
Lot 10 wafer 2



Lot 11 wafer 11

- Nearly every chip on every wafer failed in lots 10 and 11.
- The chip failures on lots 9, 10 ,11 and 12 were studied.
- Identifying the problem was difficult.

SVX3 Failure Types



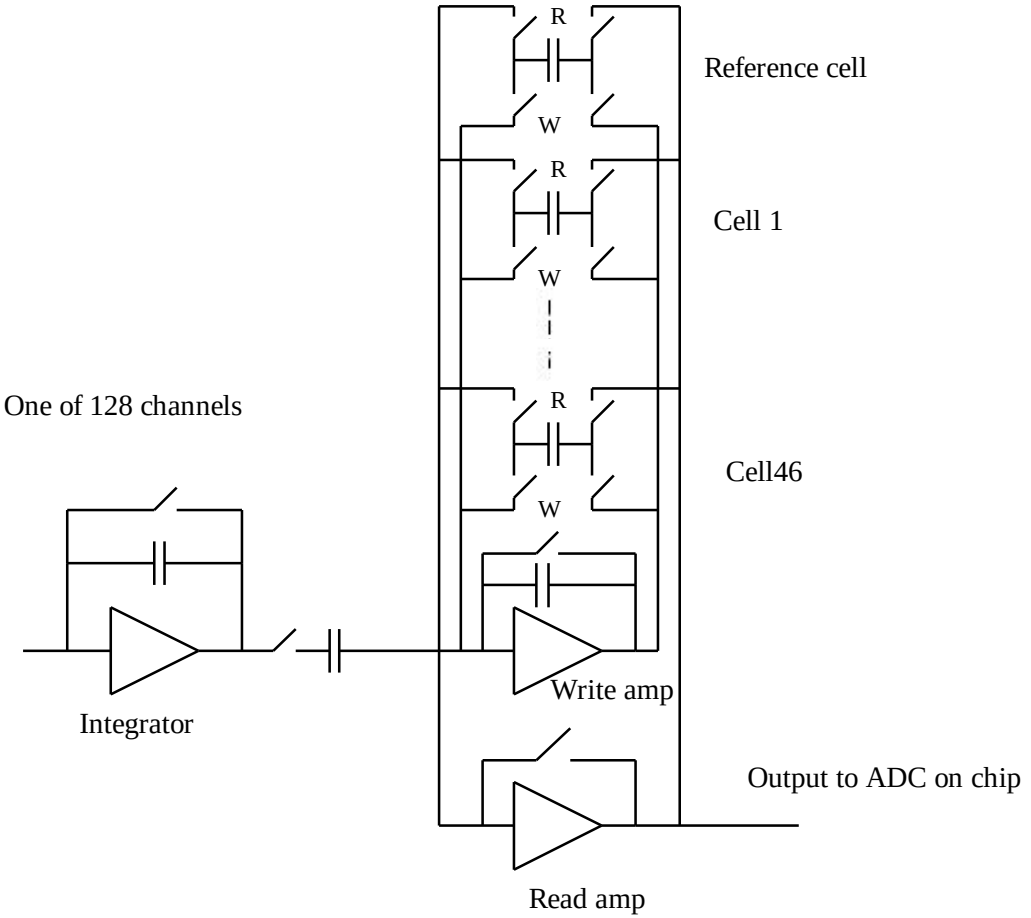
Lot 9 wafer 14

Lot 11 wafer 11

- Lots 9 and 12 showed yield “holes” in the middle of the wafers due to out of tolerance pedestals from the pipeline (as shown on left).
- Lots 10 and 11 show out of tolerance pedestals over the entire wafer and in some cases serial shift register failures in the middle (on right).
- The failure mechanism is the same in both cases.

Understanding the Problem

- Lots 8-12 all arrived at the same time. Testing showed there was a serious problem.
- Serial shift register problem too difficult to isolate.
- Studied the pipeline pedestal problem since a bad cell could be identified and isolated.
- FIB used to add test pads on numerous chips.



Analog Pipeline

Understanding the Problem

- Tests showed high resistance M2-M3 vias in series with feedback storage capacitor in the pipeline.
- Problem shows up in pipeline because pipeline has largest number (23552) of non-redundant M2-M3 vias on the chip.
- Testing the bad via was difficult since a small test current could cause the via to heal itself (become a short).
- Bad vias had resistances up to 100 Megohms.
- The next largest number of M2-M3 vias occurs in the serial shift register (1057).

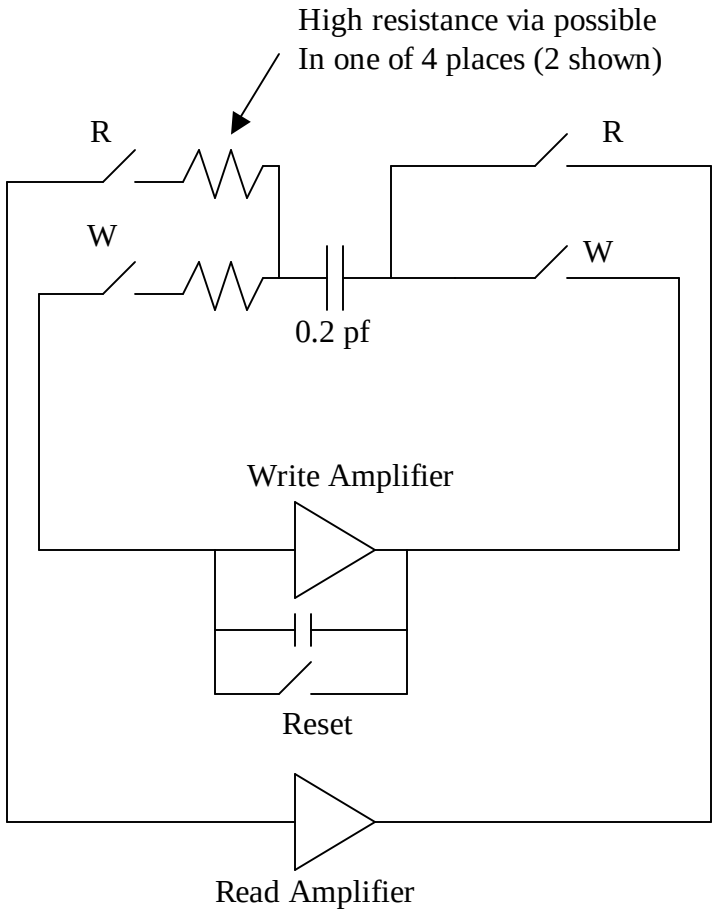
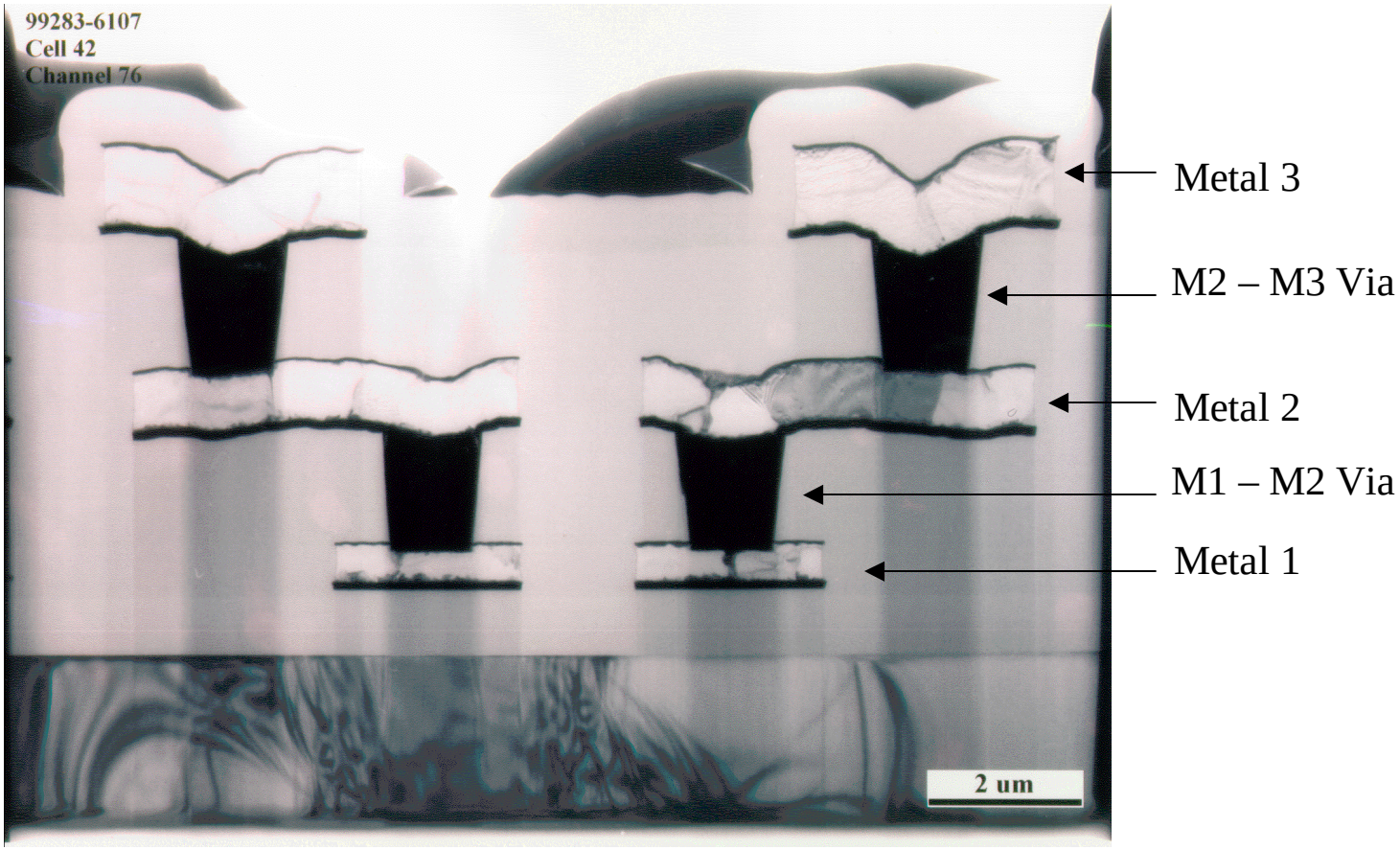


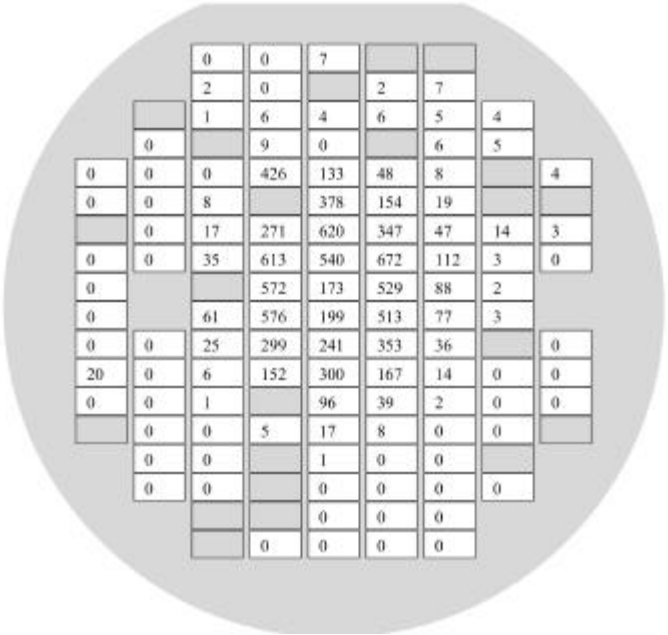
Diagram of high resistance via in series with storage capacitor.

Via Cross Section

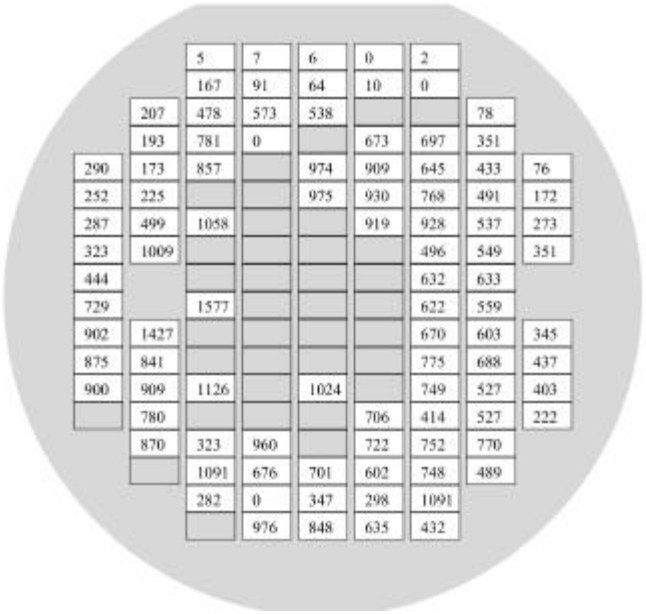


- Via problem believed to be due to inadequate oxide etching at the bottom of the M2-M3 via during a plasma etch step. Our consultant said his etcher etches the outside edge of the wafer faster than center.

Understanding the Problem



Lot 12 wafer 1



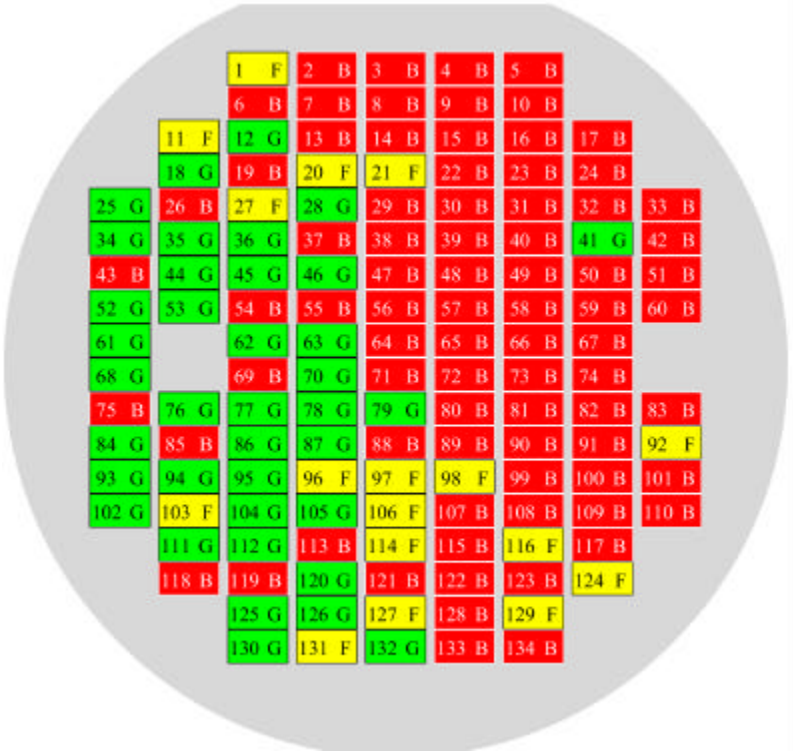
Lot 11 wafer 11

- A bad via in a storage cell causes a pedestal offset.
- There are 5888 storage cells on chip.
- The above plots show the number of bad storage cells for each chip on two different bad wafers.
- The hole in the center of wafer 11 on the right is due to failed shift register cells which prohibits further chip testing and finding bad cells.

Understanding the Problem

- Maximum via failure rate found was about 1 in 25.
- Manufacturer's PCM did not have via strings. Only tested single vias for resistance.
- Problem would probably been much reduced if redundant vias or vias conducting larger currents were used in the design.
- After problem was understood, additional lots started with no changes in processing or design.

Wafers from Lots 13-16



Lot 16 wafer 16 yield plot

- The via problem was gone in the later lots.
- Yields were much lower ranging from 10% to 42%.
- Yields inconsistent compared to 4” wafer lots.
- Cause of lower yield is unknown at this time.

SVX3 Summary

- Processing of SVX3 in RiCMOS IV was inconsistent.
- Highly incorrect yield results could be projected from a given wafer or given lot.
- 8 months lost studying the yield problem.
- Had to prove manufacturing problem which was not easy.
- All wafers have now been delivered to Fermilab
- Vendor will only guarantee 5% yield on future lots.

Conclusion

- Wafer level testing requires fairly expensive equipment ($200K) and trained personnel.
- Wafer level testing is essential for bare die applications.
- Wafer level testing can help identify design and processing problems which may be difficult to identify without knowledge of die location on the wafer.

Acknowledgements

The authors would like to thank Igor Volobouev at Lawerence Berkeley National Laboratory for testing the SVX3 wafers and developing the wafers maps shown in this talk. We would also like to thank Tom Zimmerman at Fermilab for the SVX3 analysis work which identified M2-M3 via problem. The data acquisition package along with the necessary software was developed by Al Baumbaugh at Fermilab.