Fermilab Silicon Strip Readout Chip for BTEV

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The Experiment

- BTEV - new experiment
  - Due to run in 2009
  - Designed pixel readout
  - Designed SSD readout (w/INFN)
- Silicon Strip Detector
  - 21 planes
  - Each plane is 30.6 x 31.6 cm
  - Total of 129,000 strips
  - FSSR (Fermilab Silicon Strip Readout) chip wire bonded to SSD
    - Full custom
    - Mixed signal device
    - TSMC 0.25 μ CMOS
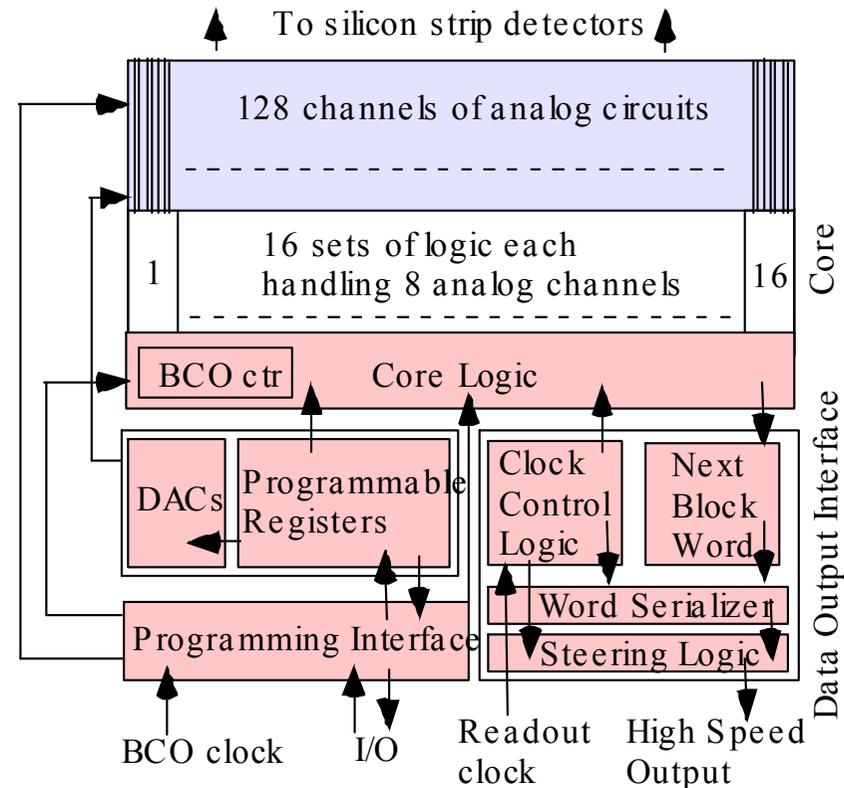

BTeV Detector Layout
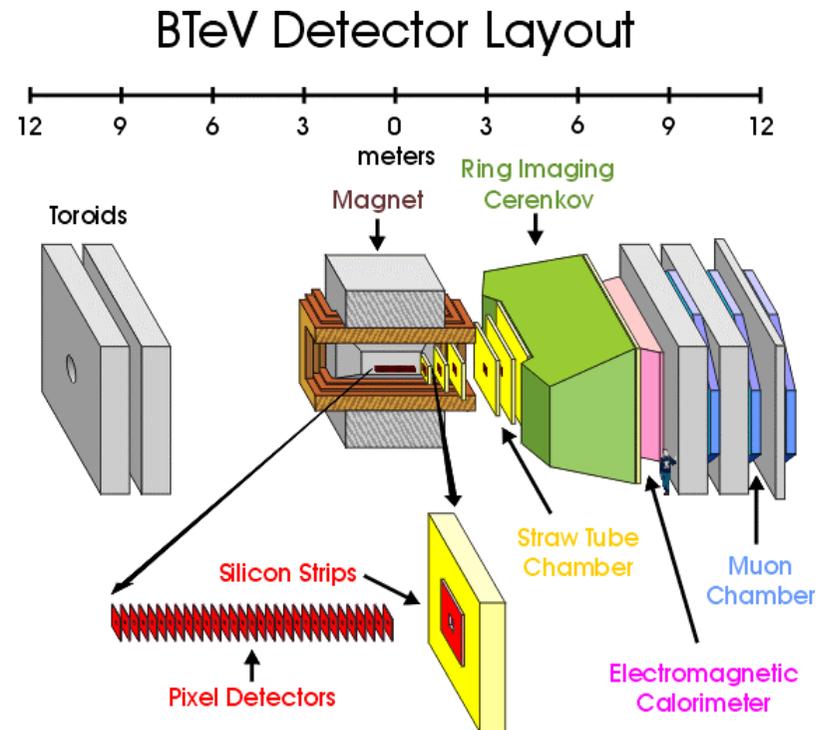
Major Requirements

- Data driven architecture – no trigger
- Can operate at 132, 264, or 396 nsec beam crossing
- Over 10 years FSSR can see 5 Megarads
  - Designed for TID and SEU
- Equivalent Noise Charge (ENC) < 1000erms @ C_{det} = 20 pF
- Threshold dispersion < 500 erms
- Power < 4 mW/channel

FSSR Block diagram

- FSSR Core
  - 128 analog channels
  - 16 sets of logic, each handling 8 channels
  - Core logic with BCO counter
- Programming Interface (slow control)
  - Programmable registers
  - DACs
- Data Output Interface
  - Communicates with core logic
  - Formats data output
 - Same as BTEV FPIX chip
    - Allows common DAQ

To silicon strip detectors

128 channels of analog circuits

1   16 sets of logic each handling 8 analog channels   16   Core

BCO ctr   Core Logic

DACs   Programmable Registers   Clock Control Logic   Next Block Word

Word Serializer
Programming Interface   Steering Logic

BCO clock   I/O   Readout clock   High Speed Output

Data Output Interface

Chip Layout

- Chip has128 channels with all digital blocks
  - 50 micron pitch
  - Double row of bond pads
- Chip features for testing
  - One block of 64 channels has 32 with Baseline Restorer and 32 without
  - Different input transistor sizes were used on a few of the channels
  - A few of the analog front ends were removed to add multiple test points for adjacent channels
  - Individual transistors were added to characterize and compare their performance to operation in the preamplifier.
- Size is 7.27 mm x 4.46 mm
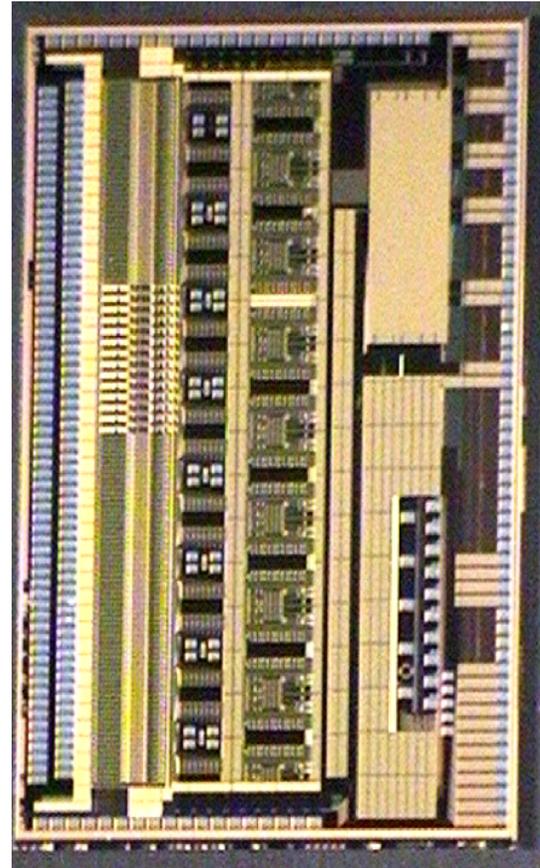
Analog Channels

- Preamplifier
  - Positive charge input
  - Gain of 5 mV/fC
- Integrator and shaper
  - CR-(RC)^2
  - Four programmable shaping times (65, 85, 105, 125 nsec)
- Base Line Restorer
  - Stabilizes base line
  - Blocks DC offset
  - Affects noise, threshold dispersion, gain (more info later)
- Discriminator
 - Comparator
  - Programmable threshold (chip wide)
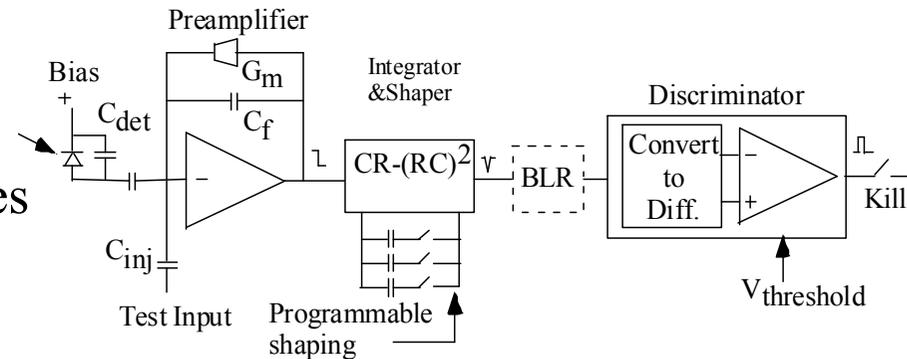
- 1 bit of 128 bit Serial shift register
  - Controls switch to provide Test Input
  - Controls switch to Kill discriminator output

Digital Section

- **Programming Interface**
  - Receives 13 bit of serial data
    - 5 bits for chip ID
    - 5 bits for programmable address
      - CapSel – set shaping time
      - Kill – disconnect discriminator
      - Inject – control test pulse
      - AqBCO – store BCO value
      - Alines – select # of output serial lines
      - SendData – enable core
      - RejectHits – reject new hits
      - Three types of resets

DACs

Programmable Registers

Programming Interface

BCO clock   I/O
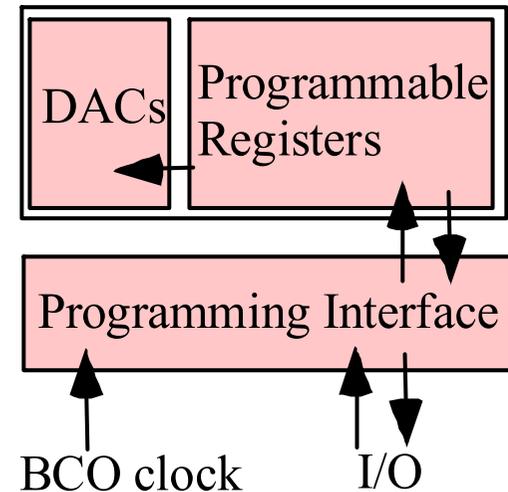
- 3 bits for instructions
  - Write – download 2, 8, or 128 bits to register
  - Read – output bits in register
  - Set – set all register bits = 1
  - Reset – set all register bits =0
  - Default – set register bits to default value
- Chip ID set by wire bonds

Digital Section (cont.)

Readout clock High Speed Output

- Data Output Interface
  - Serial data output
  - Number of output lines is programmable (1, 2, 4, 6)
  - LVDS output
  - No output buffering
  - Interfaces to Core Logic
  - Formats the data
  - Max data rate = 840 Mb/sec (6 lines)
  - Readout clock (70 MHz) independent of BCO clock
 - Data output is not time ordered
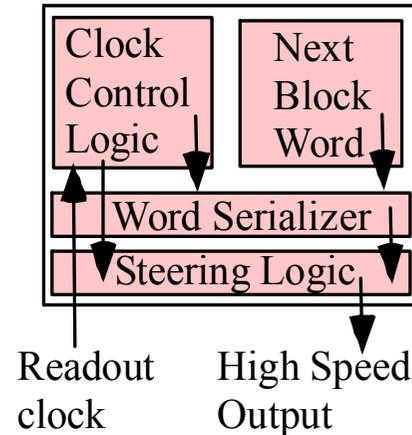
- Two types of 24 bit readout words
  - Sync/Status
    - 10 bits status
    - 13 bits for synchronization
    - 1 bit for word mark
  - Data word
    - 4 bits for strip number (1 of 8)
    - 5 bits for logic set number
    - 8 bits for hit BCO number
    - 6 bits are currently unused
    - 1 bit for word mark

Test Results

- The analog and digital sections along with all test structures functioned properly allowing extensive testing of the chip.

- Noise performance is close to predicted values.

- Overall gain is about 80 mV/fC.

- Wide dynamic range of about 12 fC

- Power dissipation is 3 mW/channel

- The chip has been operated operated with a 70 MHz readout clock to provide 840 Mb output data rate.

- Threshold dispersion = 440 erms (with BLR)

- ENC (C_{det} = 20 pF, shaping time = 125 nsec, with BLR) is 790 erms.

- All specifications met.

Averaged Waveforms at Shaper Output Showing Different Shaping Time Settings

- Shaping time can be programmed (65, 85, 105, 125 nsec)

- Adjustment allows for
  - Foundry process variations
  - Different beam interaction times.

- Has small tail lasting for several microseconds that might cause a problem.
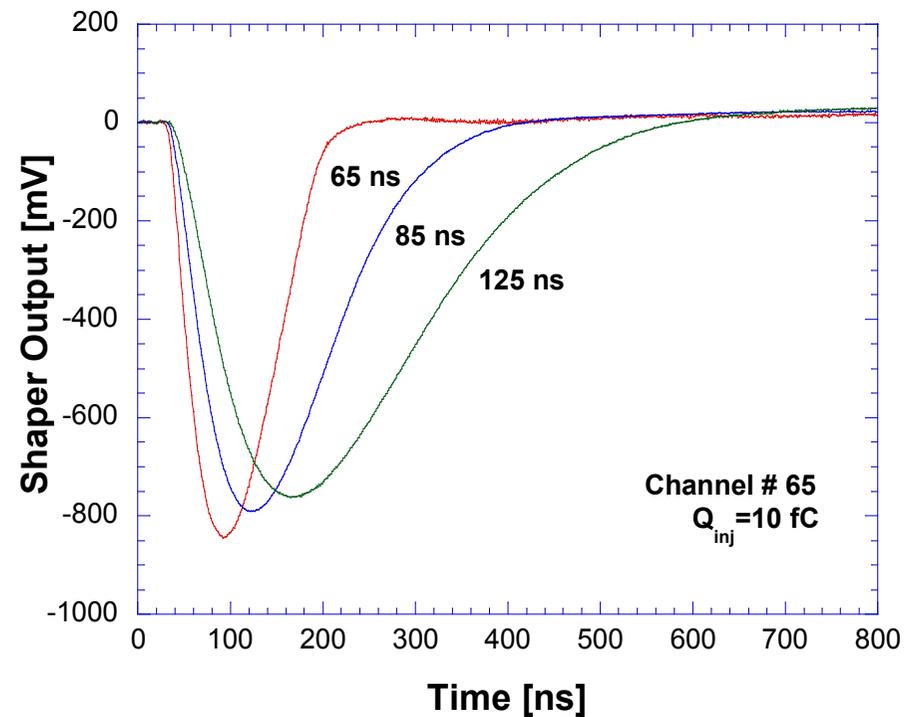
Equivalent Noise Charge Measurement at Shaper Output

- Close to simulated value

- Noise depends on shaping time

ENC = 220 e + 26.5 e/pF
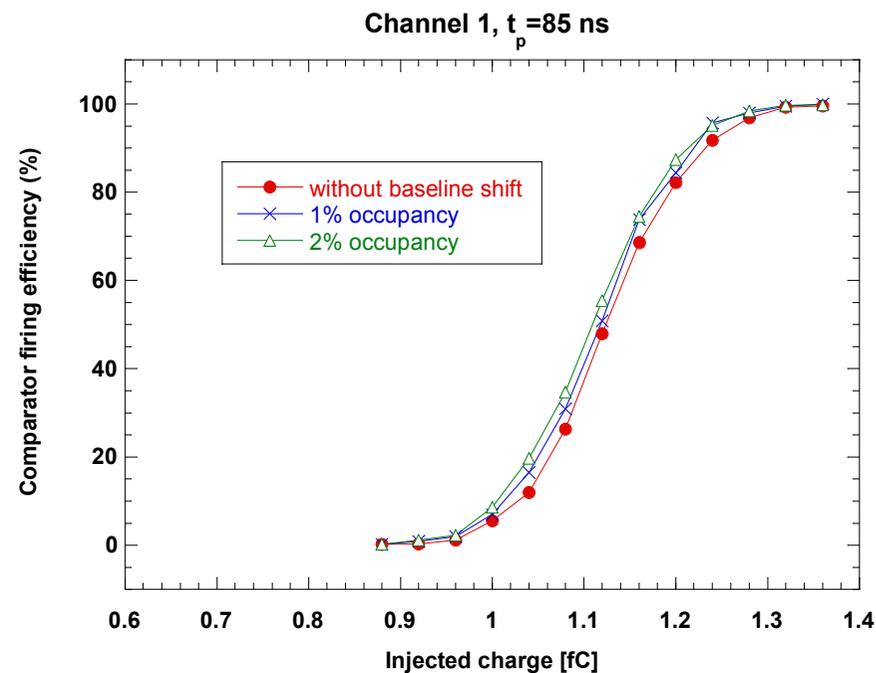
NMOS, W/L = 1500/0.45

t_P = 85 ns
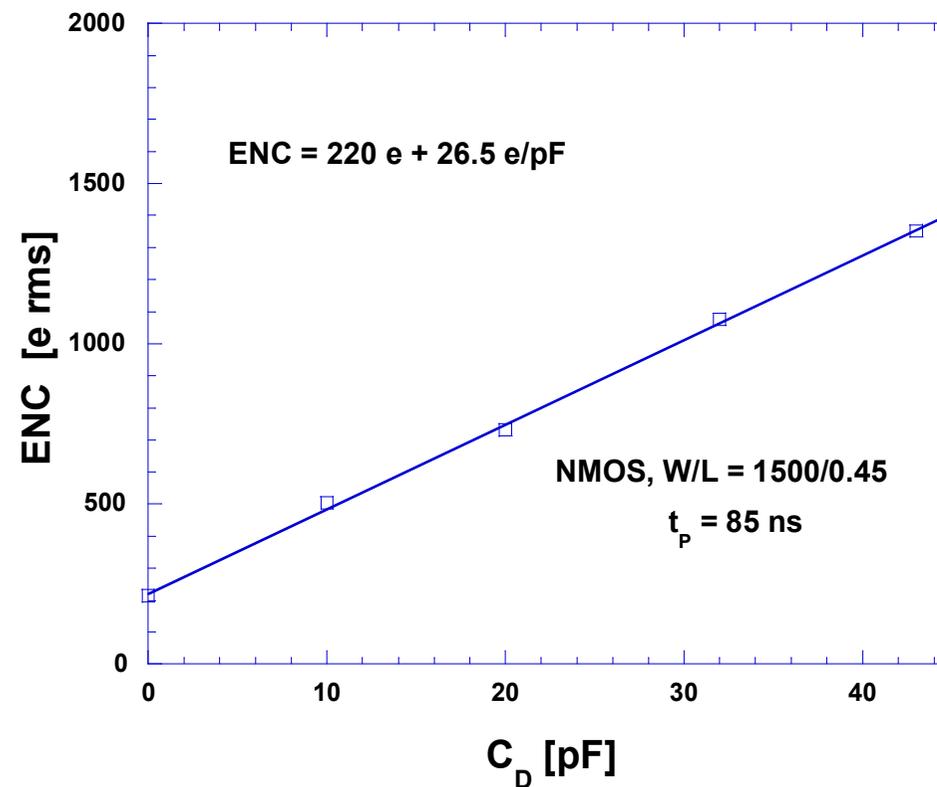
Base Line Restorer Test Results

- Shaper output has small overshoot.
- Overshoot causes unwanted variable offset at discriminator input.
- BLR removes variable offset.
- BLR also improves threshold dispersion (AC coupling), but increases noise.
- BLR is needed to remove variable offset and improve threshold dispersion
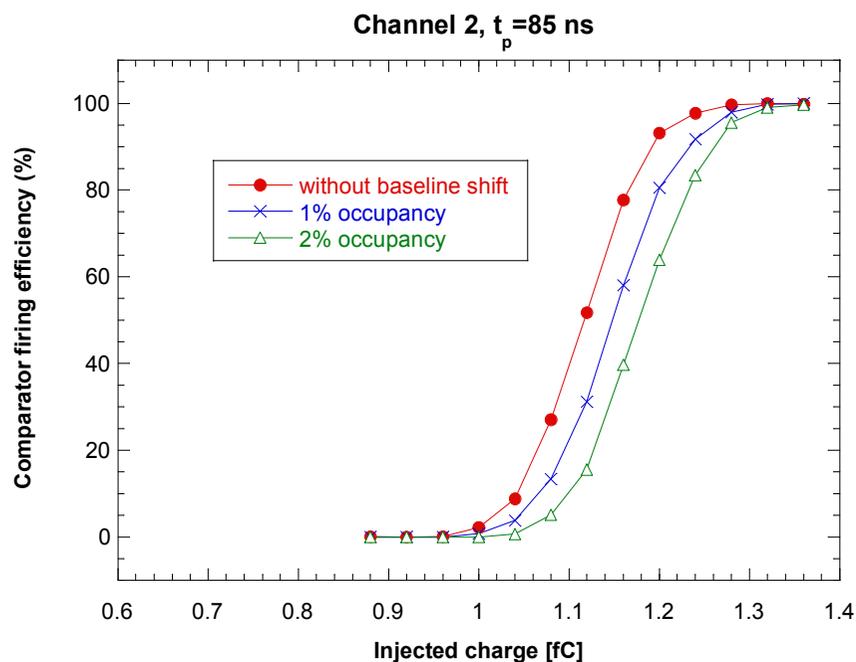
Input signal discriminator scan <u>without</u> BLR   Input signal discriminator scan <u>with</u> BLR

Future Changes

- Since the current chip has unnecessarily wide dynamic range, the gain will be increased by decreasing the size of the preamplifier feedback capacitor from 200 fF to 150/100 fF. This will cause a further reduction in threshold dispersion.

- It was recently decided that a simple discriminator output will not satisfy the need to calibrate the detector as radiation changes its characteristics.
  - A 3 bit ADC, similar to the one used in the BTEV FPIX chip, will be added to each channel– considered low risk.
  - The 3 bits will be inserted into the data word to replace 3 of the 6 unused bits. Thus there is no impact on the data rate.

Conclusion

- A full size prototype of the silicon strip readout chip for BTEV has been designed and tested.

- The device was found to be fully functional.

- With the presence of the BLR all initial requirements were met.

- The final design will include a gain change and addition of a three bit ADC.

- Work is progressing toward a submission in January 2005.

Back up Slides

Averaged Waveforms at the Shaper Output for Different Input Charges

- Output is well behaved

- Gain is about 80 mv/fC

- Gain becomes non-linear above 12 fC.
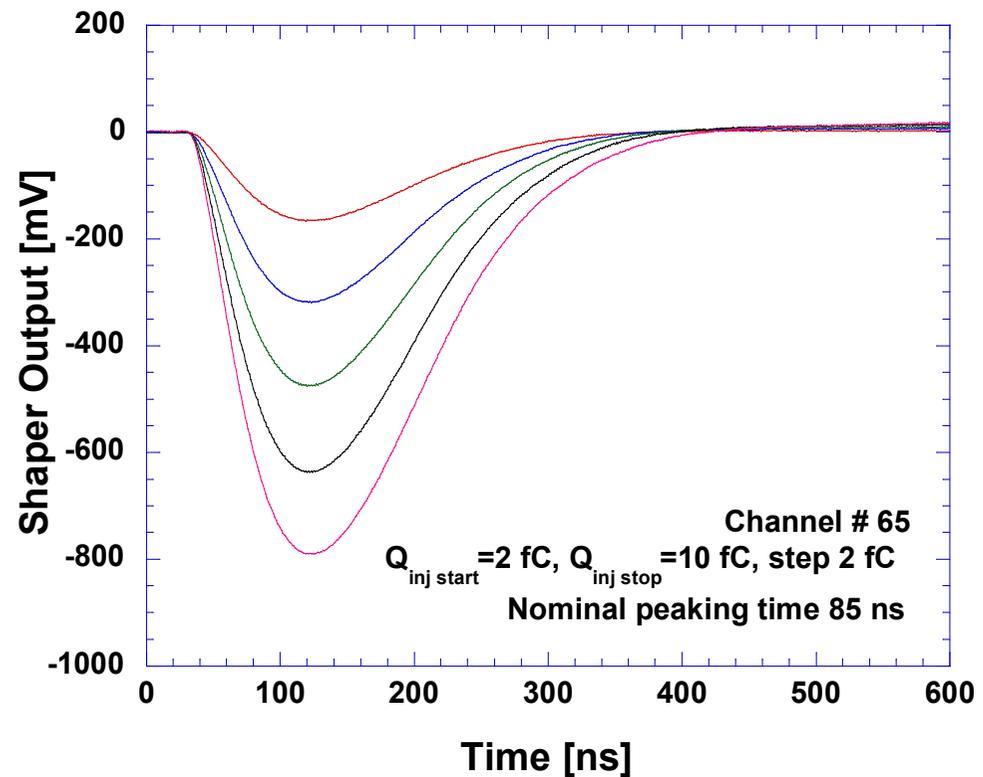
Output Data Format

b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

(a) One output pair

b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12

(b) Two output pairs

b5	b4	b3	b2	b1	b0

b11	b10	b9	b8	b7	b6

b17	b16	b15	b14	b13	b12

b23	b22	b21	b20	b19	b18

(c) Four output pairs

b3	b2	b1	b0

b7	b6	b5	b4

b11	b10	b9	b8

b15	b14	b13	b12

b19	b18	b17	b16

b23	b22	b21	b20

(d) Six output pairs

Base Line Restorer Circuit

From shaper

I

To discriminator

−

Ref

+

2I
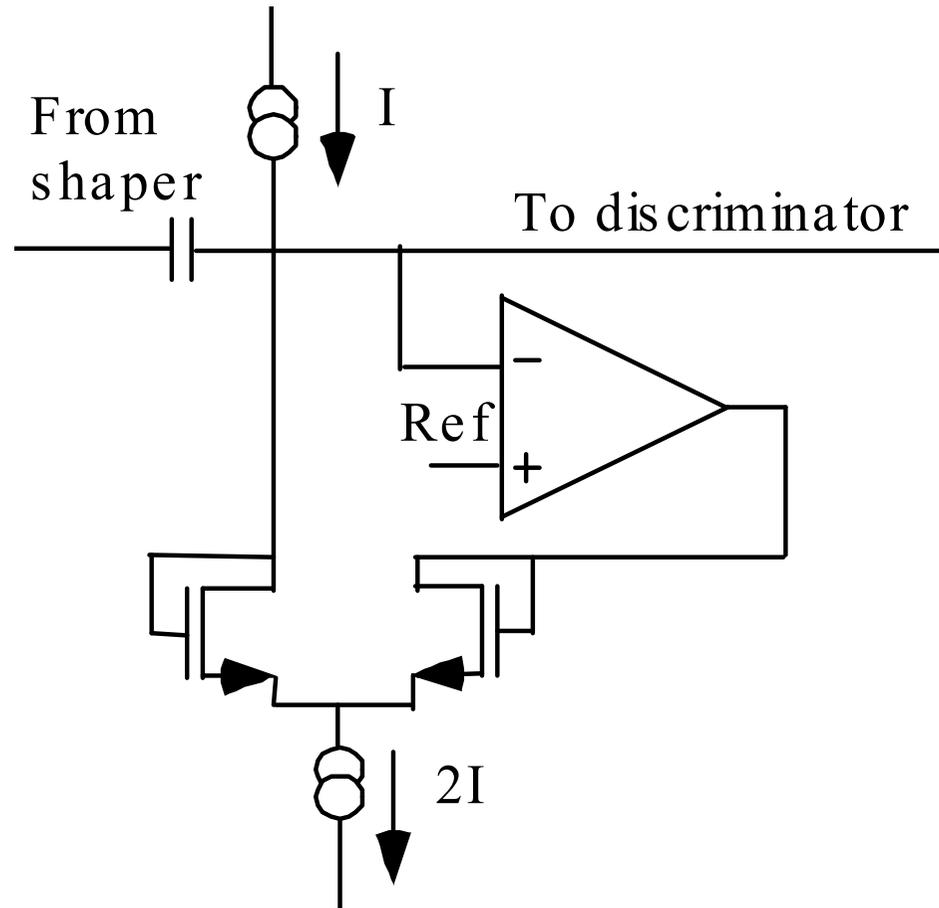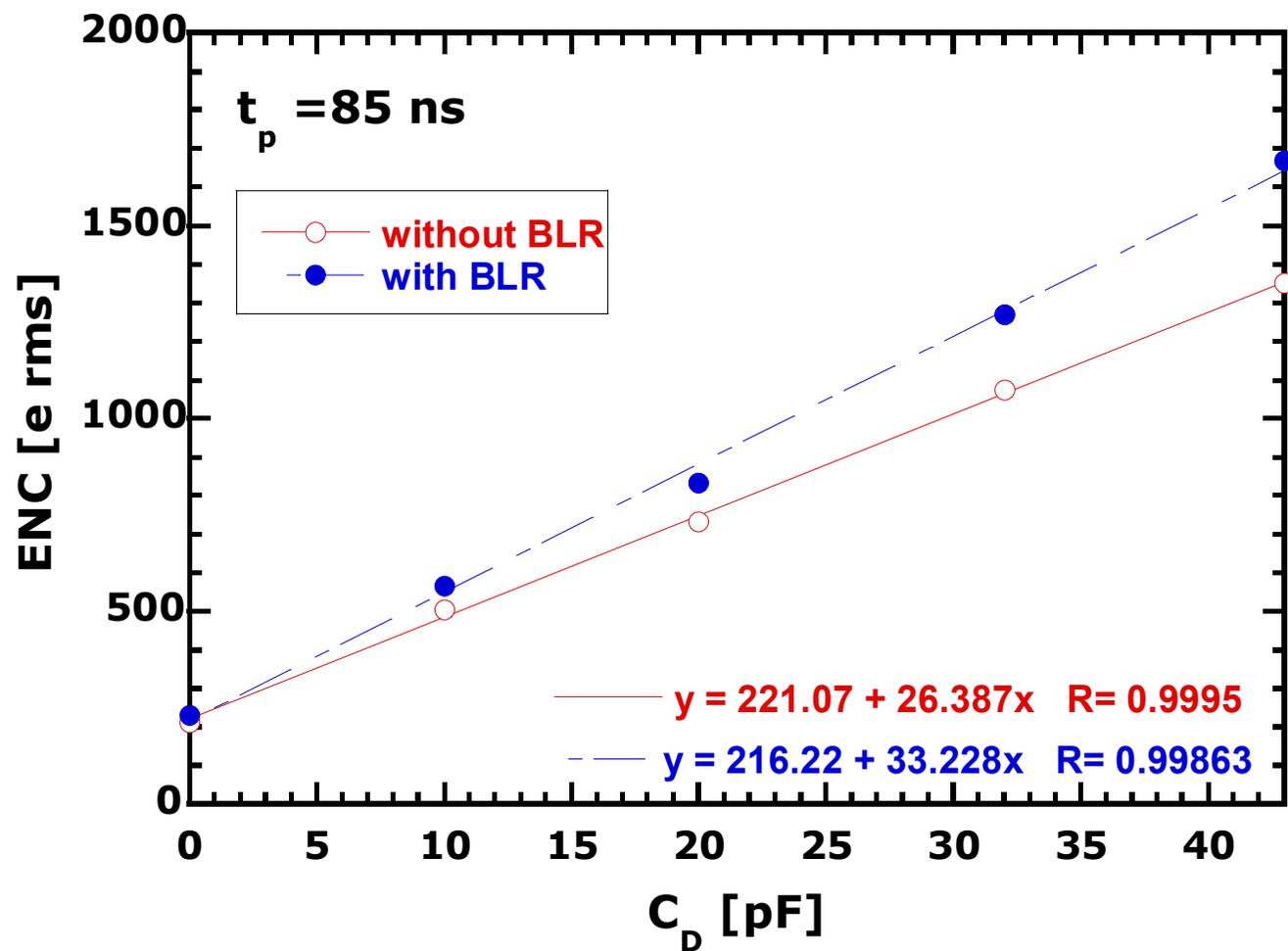
Detector Plane with FSSR Readout Chips
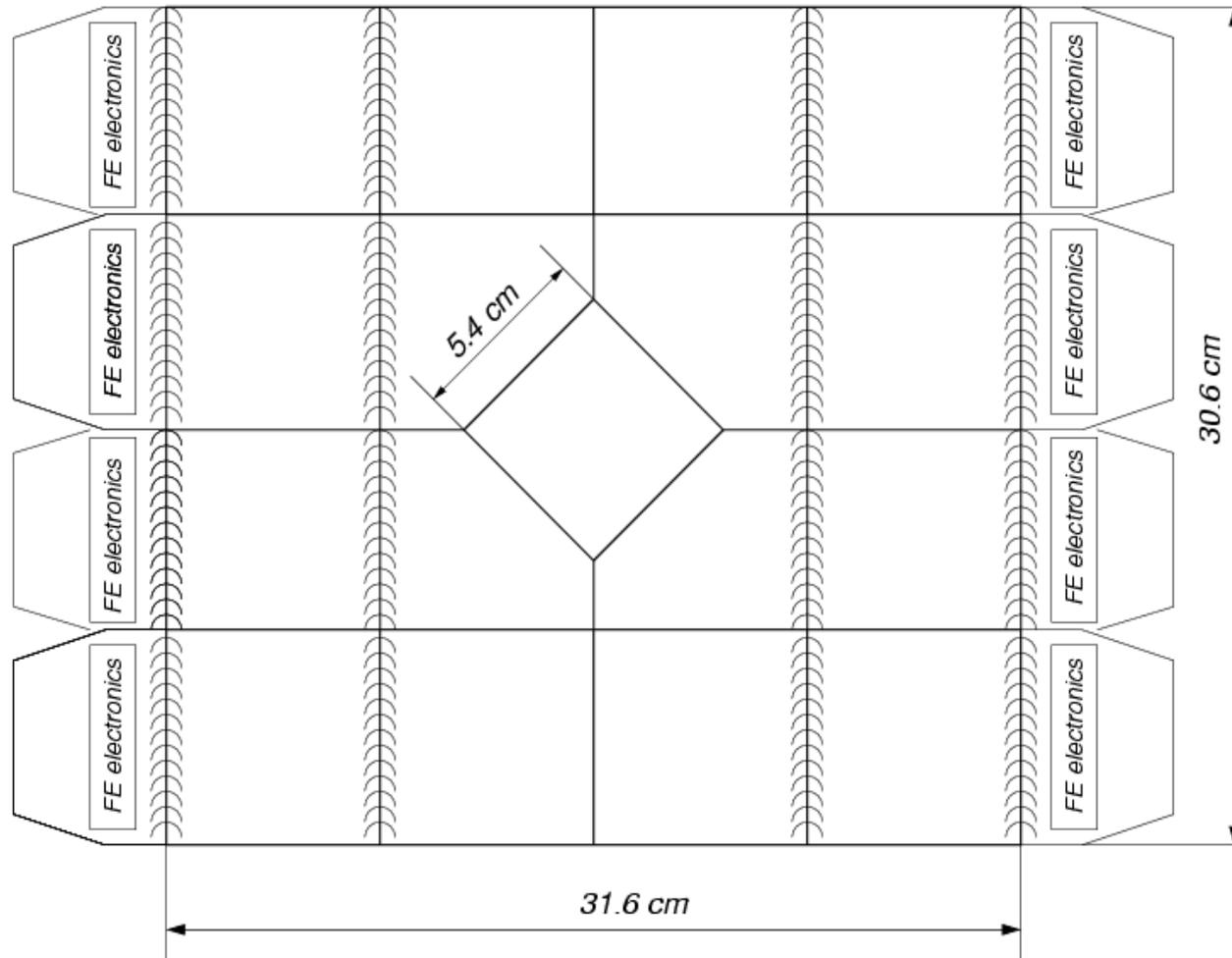
ENC with and without a BLR

Typical threshold dispersion and equivalent noise charge with and without a Base Line Restorer circuit for a shaping time of 85 nsec.

	Threshold Dispersion	ENC
W/O BLR	790 erms	760 erms
W BLR	440 erms	890 erms
Specification	500 erms	1000 erms