The Design of a Charge Integrating, Modified Floating Point ADC Chip for Calorimeters

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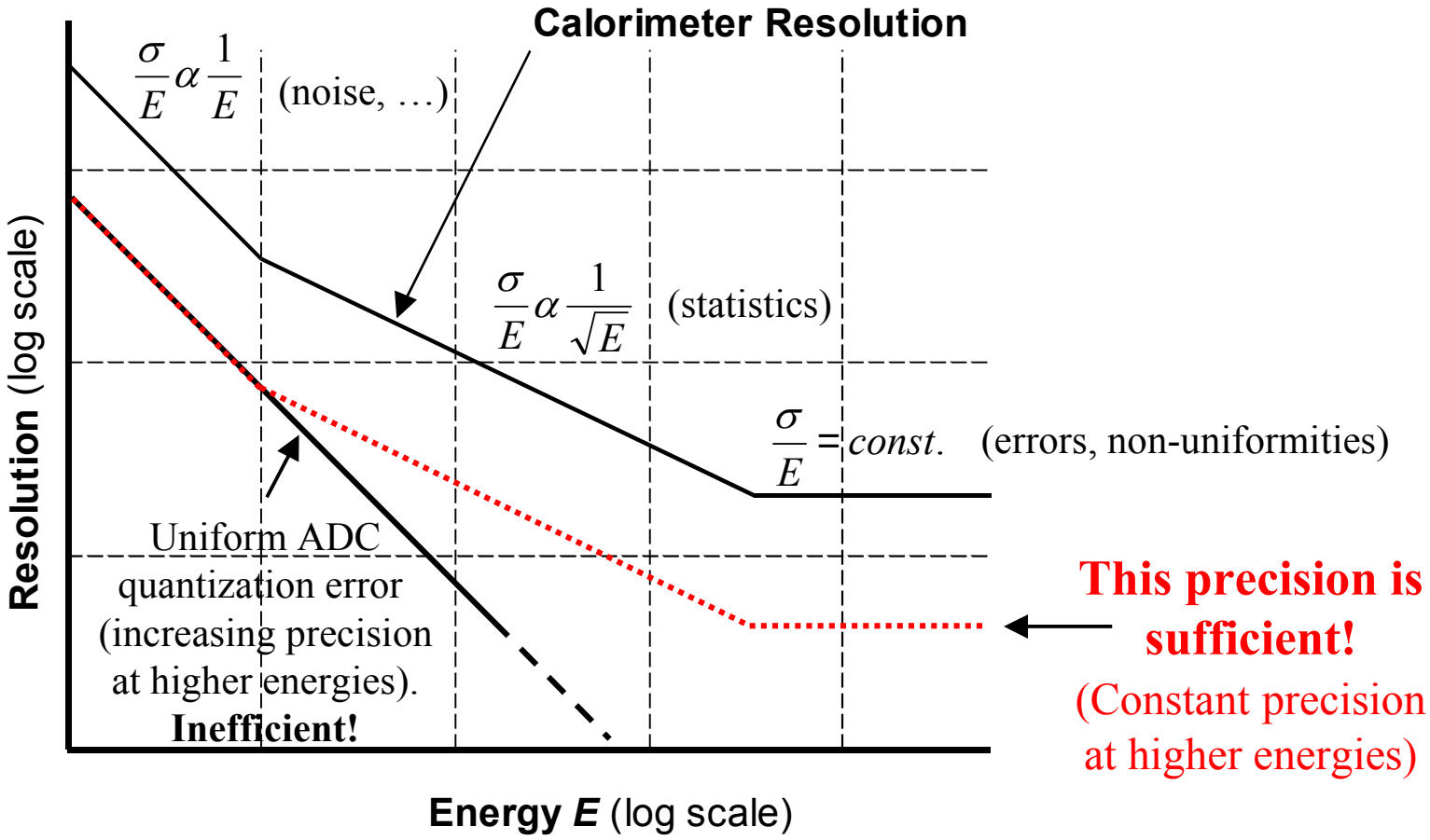
Outline

- The problem
- QIE (Charge Integrator and Encoder) concept
- Previous QIE chip designs
- New QIE8 design for CMS (HF and HCAL)
- Practical stuff -- some important practical tips for obtaining the best performance from sensitive mixed mode designs of this type

The problem: digitizing photodetector charge pulses

1) over wide dynamic range (typically 13-18 bits)
2) with negligible quantization error
3) at high rate (typically around 50 MHz)



A solution: a floating point system

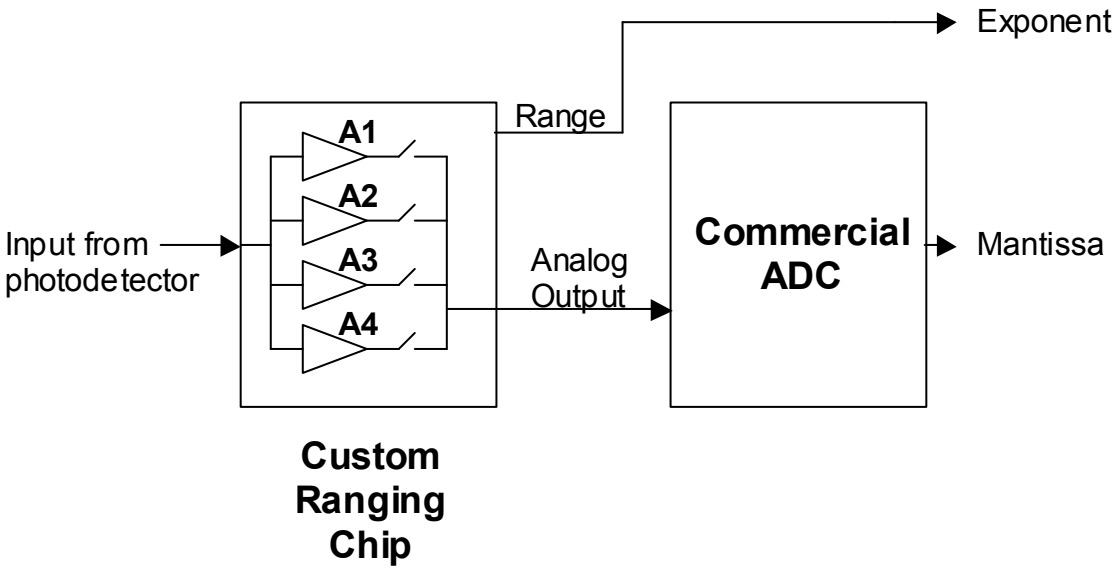
Multi-ranging concept:

- Signal feeds multiple ranges with different gains
- Select one range to route to an ADC
- ADC output: Mantissa, digital range code: Exponent
- "Floating point" output achieves more constant precision

Examples:

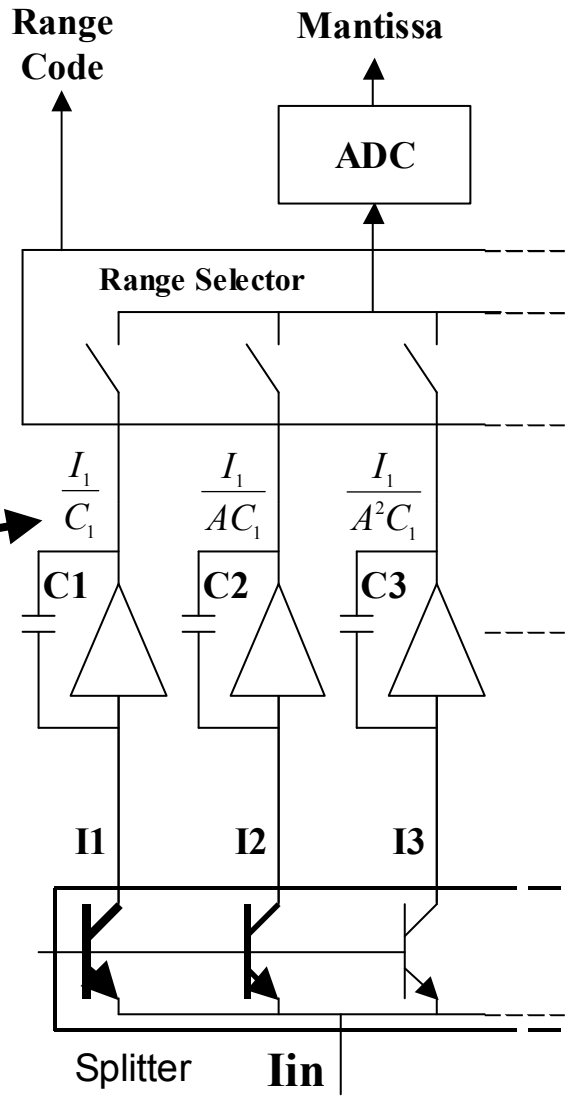
- CARE Chip (Babar)
- FPPA/MGPA Chip (CMS)
- Previous QIE5-7 Chips (KTEV, CDF, MINOS)

All are multi-ranging chips which feed a commercial ADC.



The QIE Concept

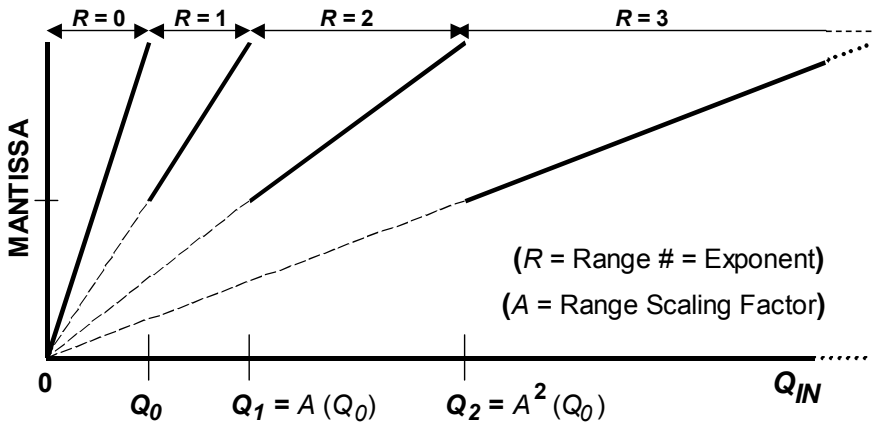
- 5) The range code forms the exponent.
- 4) For a given input charge, one appropriate range output is selected and digitized by an ADC, forming the mantissa.
- 3) Splitter ratios and integration C ratios are chosen to achieve range-to-range scaling of the transfer gain (I/C) by factor *A*.
- 2) Each splitter range output feeds a charge integrator. The current fractions are integrated simultaneously on all ranges.
- 1) Input current pulses are divided into weighted fractions by a current splitter



Transfer Characteristic

Multiple ranges, scaled by factor *A*:

If range integrators **not** offset:
all ranges intersect at the origin

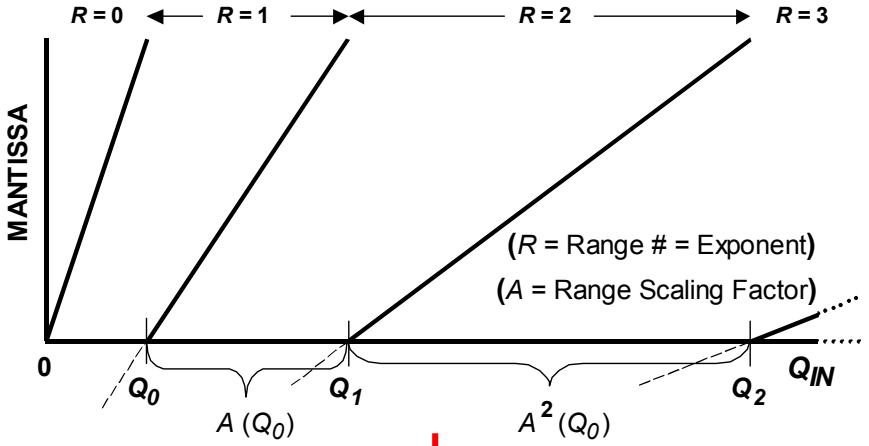


$A = 2$: standard floating point

(All ranges except the lowest use half the ADC span)

QIE scheme:

Range integrators are offset

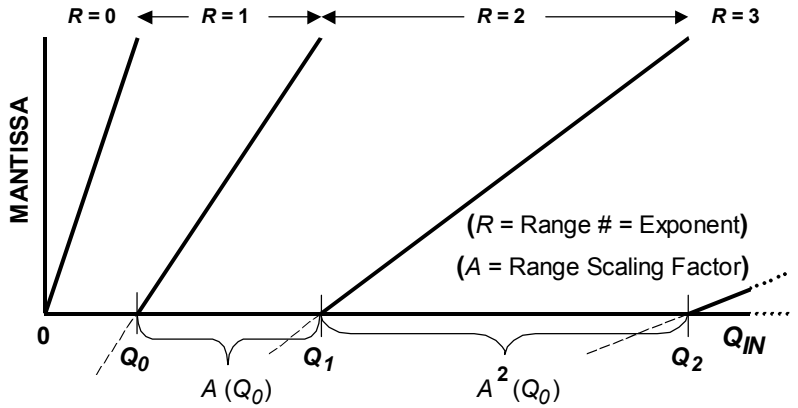


"**Modified**" floating point format

More efficient: each range uses the full ADC span)

Modified Floating Point Analysis

Most important specs:
Least count input charge (Q_{LSB})
Maximum input charge (Q_{MAX})
Relative quantization error (e_{qr})



The range scaling factor A is a design parameter, optimized for a given application. For arbitrary A:

$$\longrightarrow \text{Relative quantization error } e_{qr} = \frac{(bin\ size)/\sqrt{12}}{(input\ amplitude)} = \frac{A^R Q_{LSB}}{\sqrt{12} Q_{IN}}$$

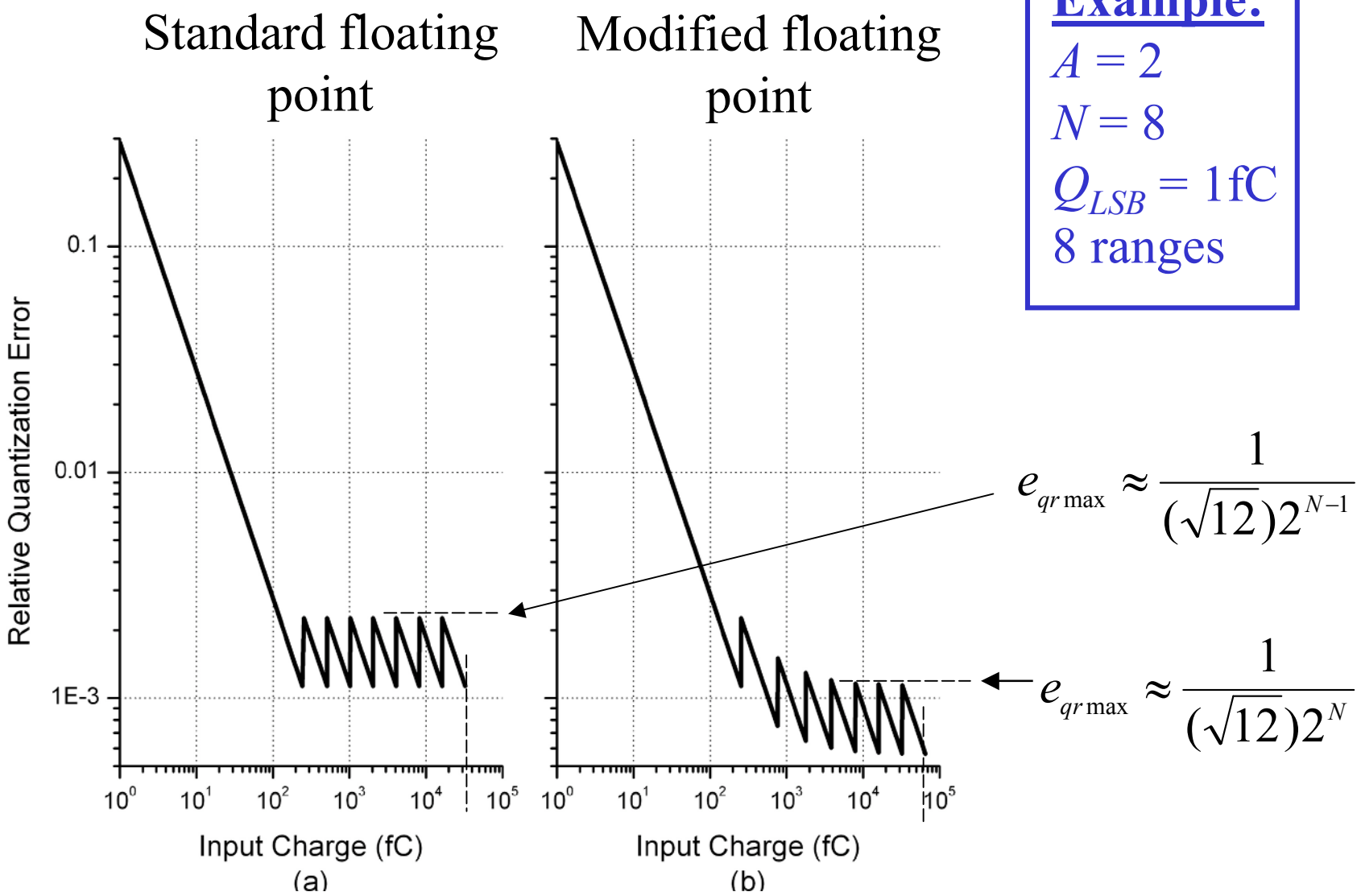
Approximations for # of ADC bits, # of ranges

A	**# of ADC bits (*N*)**	**# of ranges**
$A = 2$	$N \geq \log_2 \frac{1}{\sqrt{12} e_{qr\max}}$	$\log_2 \frac{Q_{MAX}}{2^N Q_{LSB}}$
$A > 2$	$N \geq \log_2 \frac{A^2}{\sqrt{12}(A+1) e_{qr\max}}$	$\log_A \frac{A Q_{MAX}}{(A+1) 2^N Q_{LSB}}$

(See Appendix A for more details)

In general, for a given *A*:

- The required precision (max. relative quantization error) determines the number of ADC bits, *N*.
- Once *N* is set, the dynamic range determines the necessary number of scaled ranges.
- With a larger range scaling factor *A*, fewer ranges are required but more ADC bits are needed to achieve a given precision.



Example:

$A = 2$

$N = 8$

$Q_{LSB} = 1\text{fC}$

8 ranges

Modified floating point with $A = 2$: 2x smaller error, 2x more range!

Previous QIE chip designs

QIE5-7 (for KTEV, CDF, MINOS):

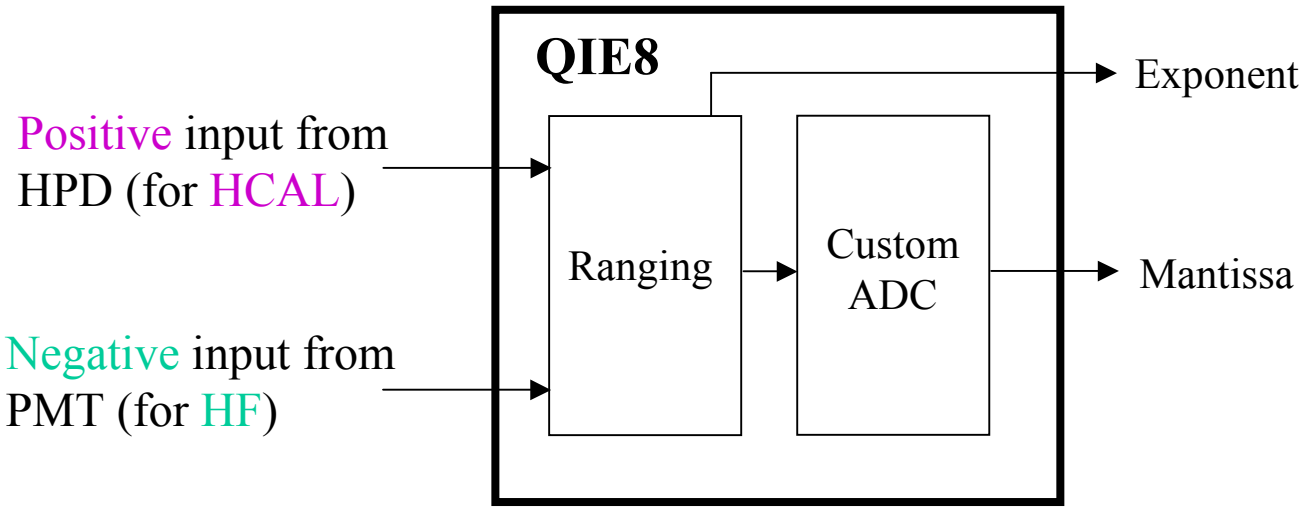
- ORBIT 2u "pseudo" BiCMOS process
- Range scaling by factor of 2, scaled by splitter ratios
- 4-deep integrator pipeline for deadtimeless operation
- Analog outputs, to drive external buffer/ADC
- Pseudo-differential input/output configuration

Disadvantages of QIE5-7:

- Commercial opamp and ADC required
- Power: 700 mW + opamp + ADC = 1-2 W/channel
- Not a true BiCMOS process
- Dual supply required (infrastructure, sequencing)
- Process reliability: problems with foundry and reliability

Newest QIE chip: QIE8

- Designed for 2 applications (HCAL and HF) at CMS
- AMS 0.8u BiCMOS process
- Major changes from earlier QIEs – new design



Single chip solution: analog in, digital out
Selectable input polarity
Single 5V supply

QIE8 Specifications

Max. relative error e_{qr} (upper ranges) = 2%
Q_{MAX}/Q_{LSB} = 10,000 (>13 bits)
Beam crossing time = 25 ns
ADC DNL (low end) < 0.05 LSB

HPD (positive) input

Q_{LSB} = 1 fC (normal mode)
Q_{LSB} = 0.33 fC (cal. mode)
Input Impedance < 40 ohms
Input analog BW > 20 MHz
ENC (Cin = 30 pF) < 0.5 fC

PMT (negative) input

Q_{LSB} = 2.7 fC (normal mode)
Q_{LSB} = 0.9 fC (cal. mode)
Input Impedance = 50 or 93 ohms
Input analog BW > 40 MHz
ENC (5m, 50 ohm cables) < 2 fC

QIE8 Design Challenges

- Very sensitive controlled impedance inputs (1 fC/LSB for HCAL)
- CAL mode: even higher sensitivity (1/3 fC/LSB) to track detector response shifts with known signal source (200e/bucket from radioactive source)
- Custom ADC with very low DNL
- Mixed mode single chip design
- Must accept either input signal polarity
- Single supply operation for simplicity

QIE8 Design Approach

Requires sensitive, fast input → **minimize # of splitter NPNs!**

- Use fewer ranges (thus large range scaling factor *A*)
- Scaling mostly with integration cap ratios instead of splitter ratios

Pick $A = 5$

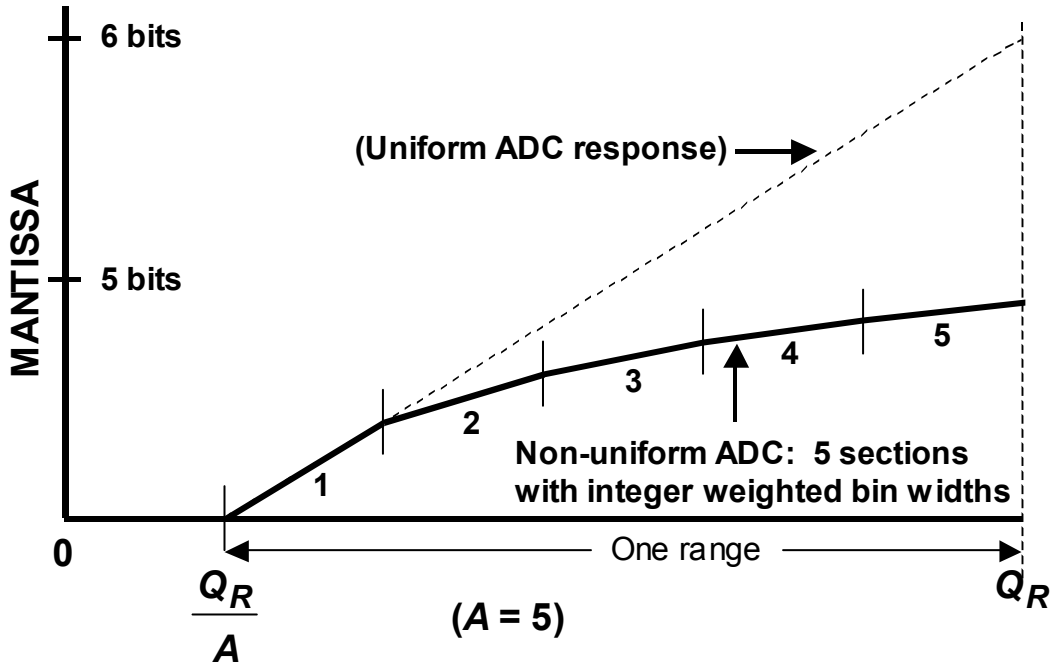
- For quantization error $e_{qr} = 2\%$, $N = 6$ ADC bits
- For 10,000:1 dynamic range, 4 ranges are required
- 4 splitter outputs in 5:1:1:1 ratio ⟶ only 8 NPNs

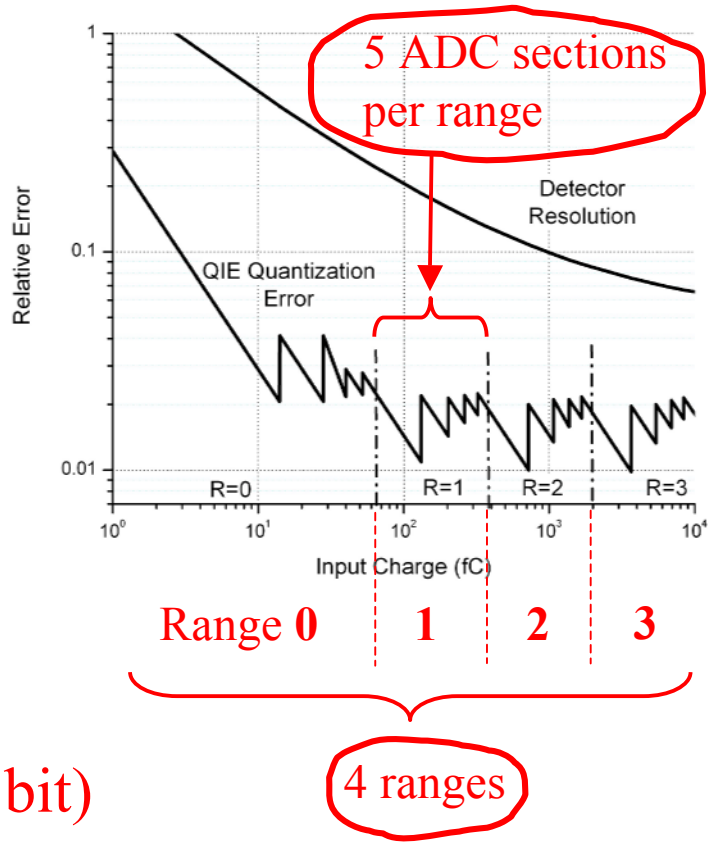
6 bit ADC is not bad, but…

- If $A = 5$, there is a factor of 5 variation in quantization error across any range – inefficient. ⟶ Use non-uniform ADC!

A Custom Non-uniform ADC

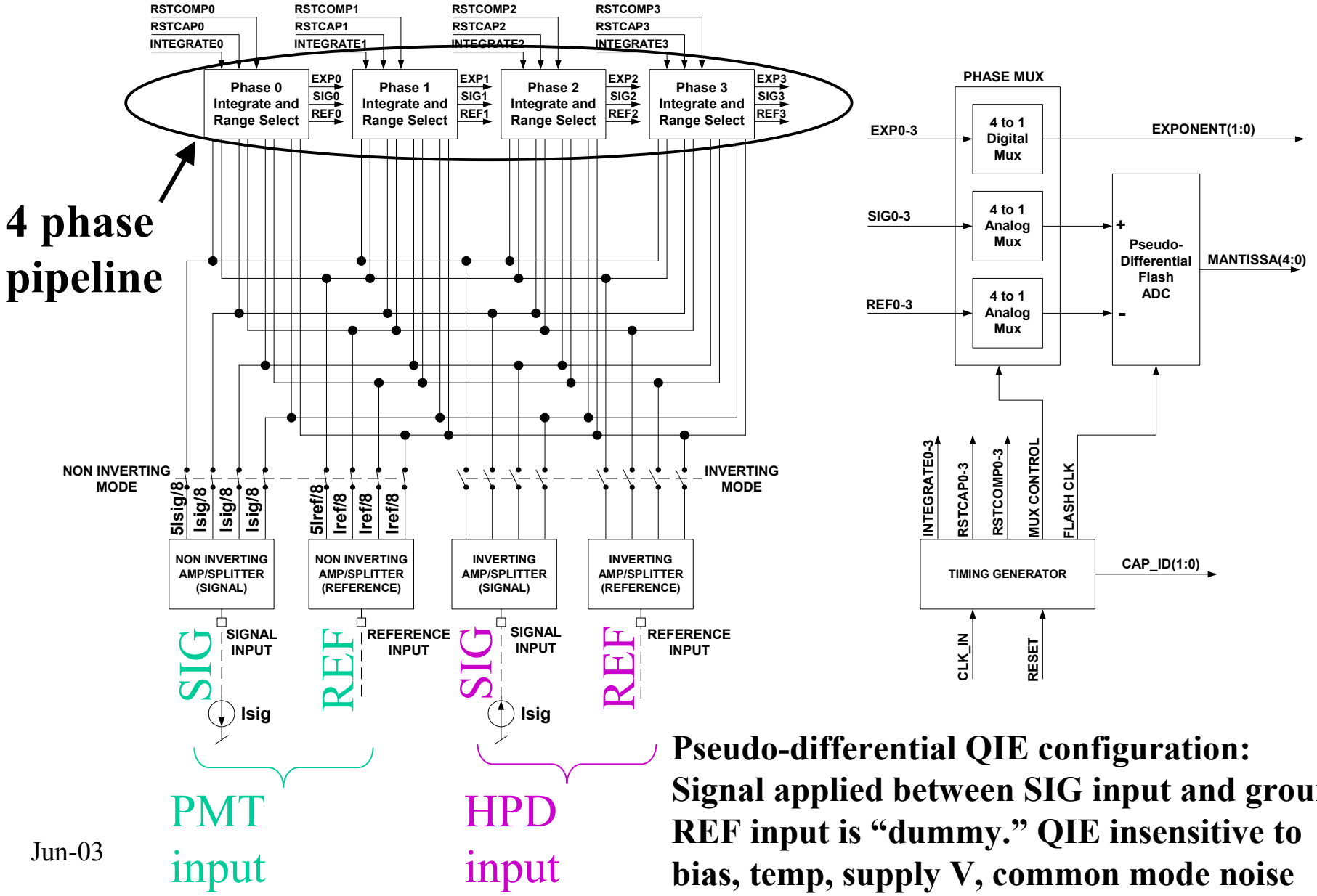
4 range QIE8 with non-uniform ADC





- Stabilized quantization error
- 5 bit ADC sufficient (instead of 6 bit)

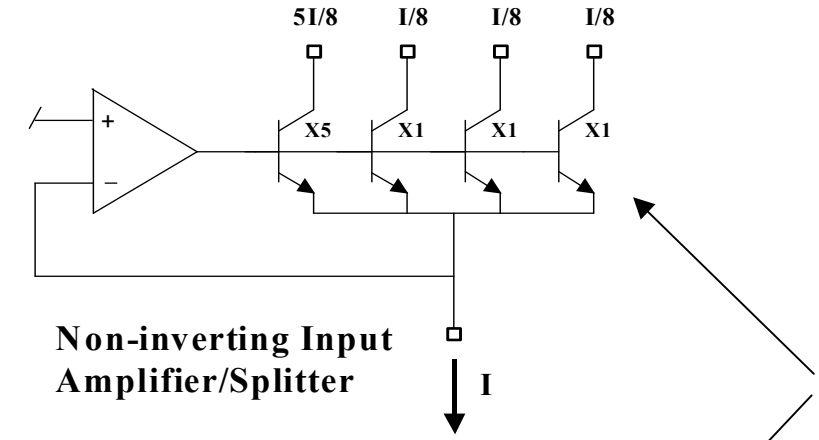
QIE8 Block Diagram



Pseudo-differential QIE configuration: Signal applied between SIG input and ground, REF input is "dummy." QIE insensitive to bias, temp, supply V, common mode noise

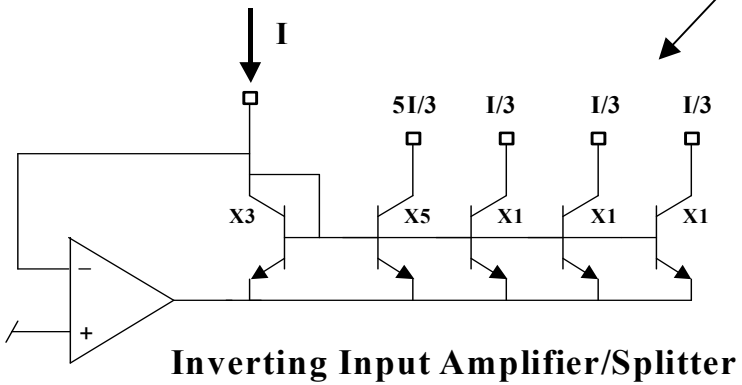
Separate input amps for PMT, HPD

Negative input
(PMT)

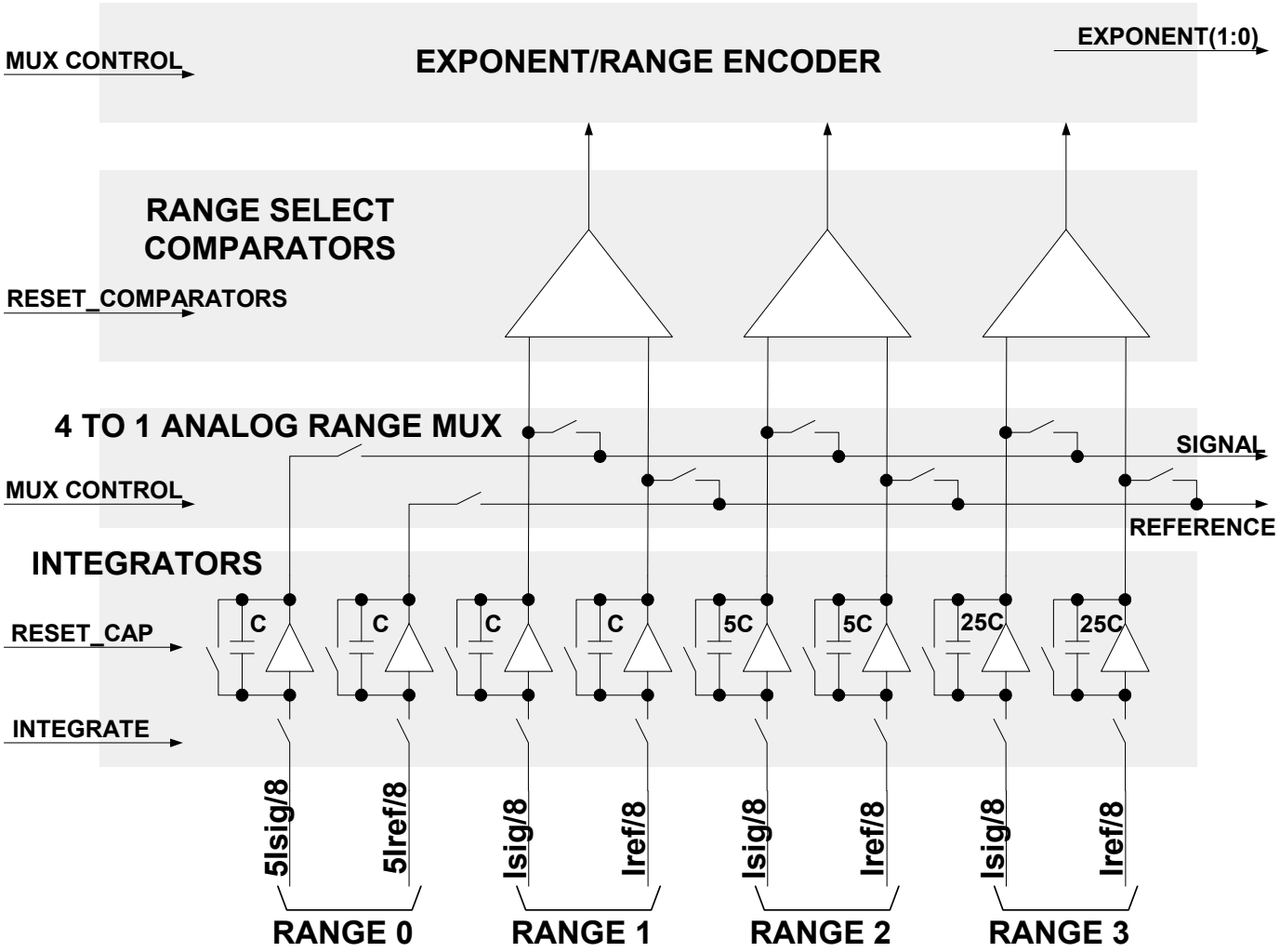


4 range splitter:
only 8 NPNs

Positive input
(HPD)
(gain = -2.7)



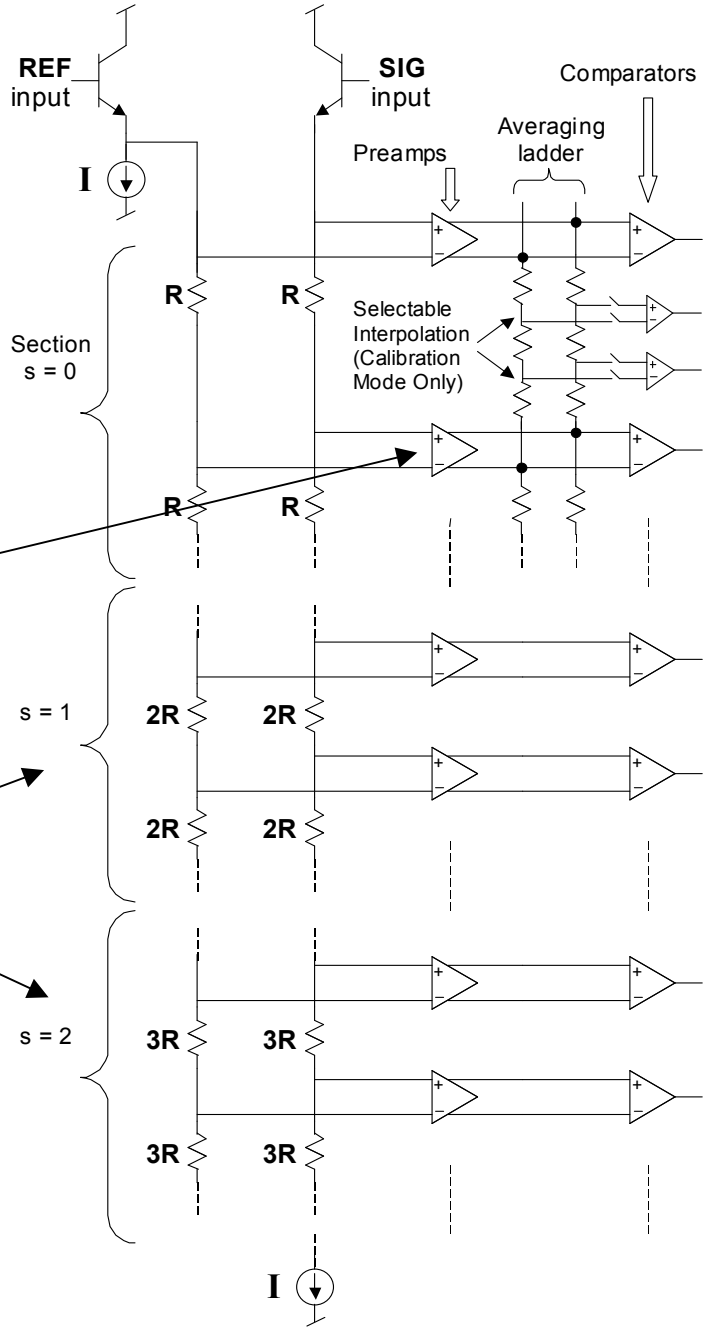
Integrate and Range Select Circuits



Custom pseudo-differential non-uniform ADC

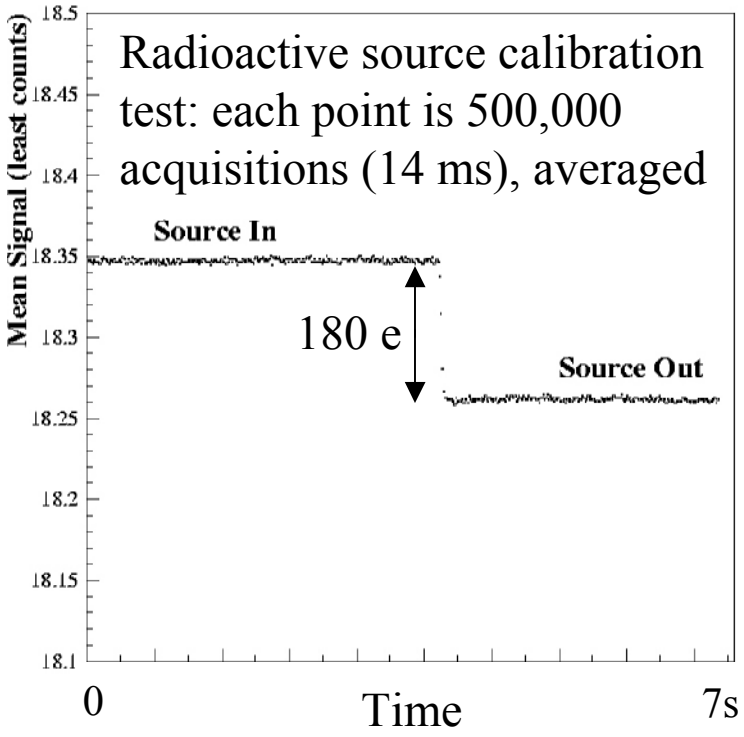
Preamps with output averaging for low DNL

5 sections with integer weighted bin widths



QIE8 Results

- Meets all specs
- Runs at > 70 MHz
- 2 constants (slope + offset) required per range
- Low DNL (< 0.05 LSB in normal mode)
- Power = 330 mW with a single 5.0V supply
- Stable against shifts in bias, temp, clock, Vdd, etc.
- No digital coupling to inputs, but ONLY if lots of things are done right… ⟶



Practical Stuff

("How to get good mixed mode performance with very sensitive inputs," *OR*, "You have to do everything right to get the best performance.")

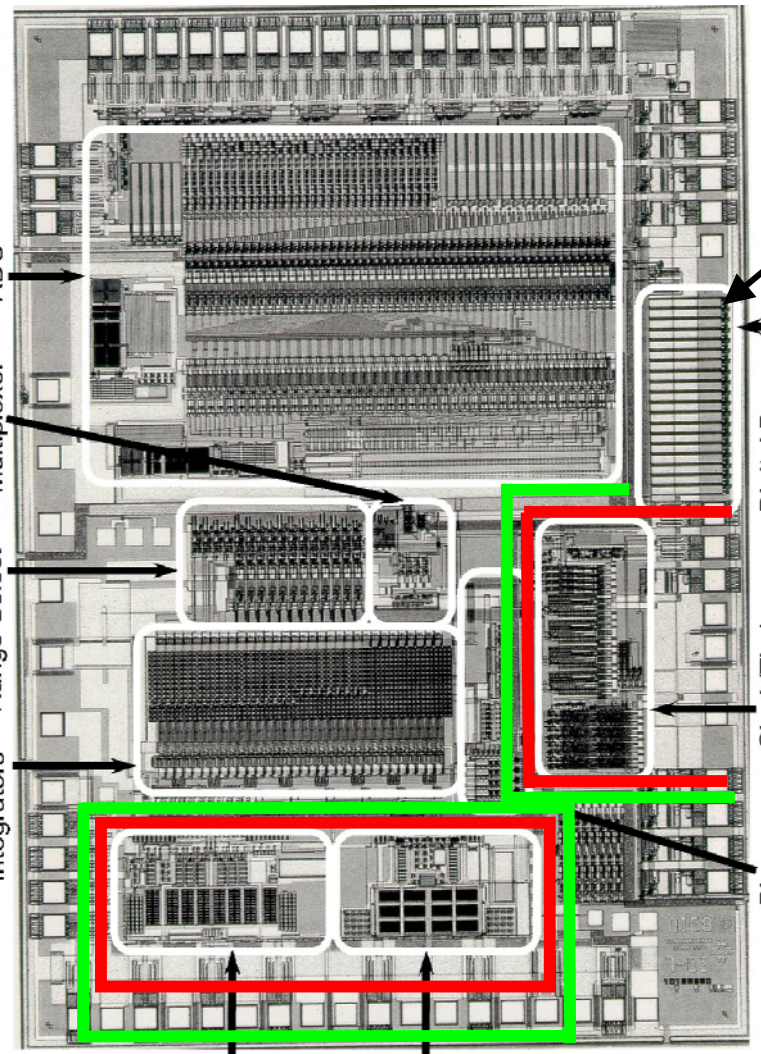
- Chip level
- Package level
- Board level

(Some of these things were learned by the method of "first not doing")

Chip Level

- Completely pseudo-differential design
- Inputs and outputs on opposite sides
- Low-level differential digital outputs
- On-chip digital supply bypass cap (to limit high frequency transients)
- Substrate isolation between analog input section and digital sections

Digital outputs (low level differential)



Digital bypass caps (650 pF total)

Digital power, control inputs

Analog power, bias

Analog/digital substrate isolation technique:

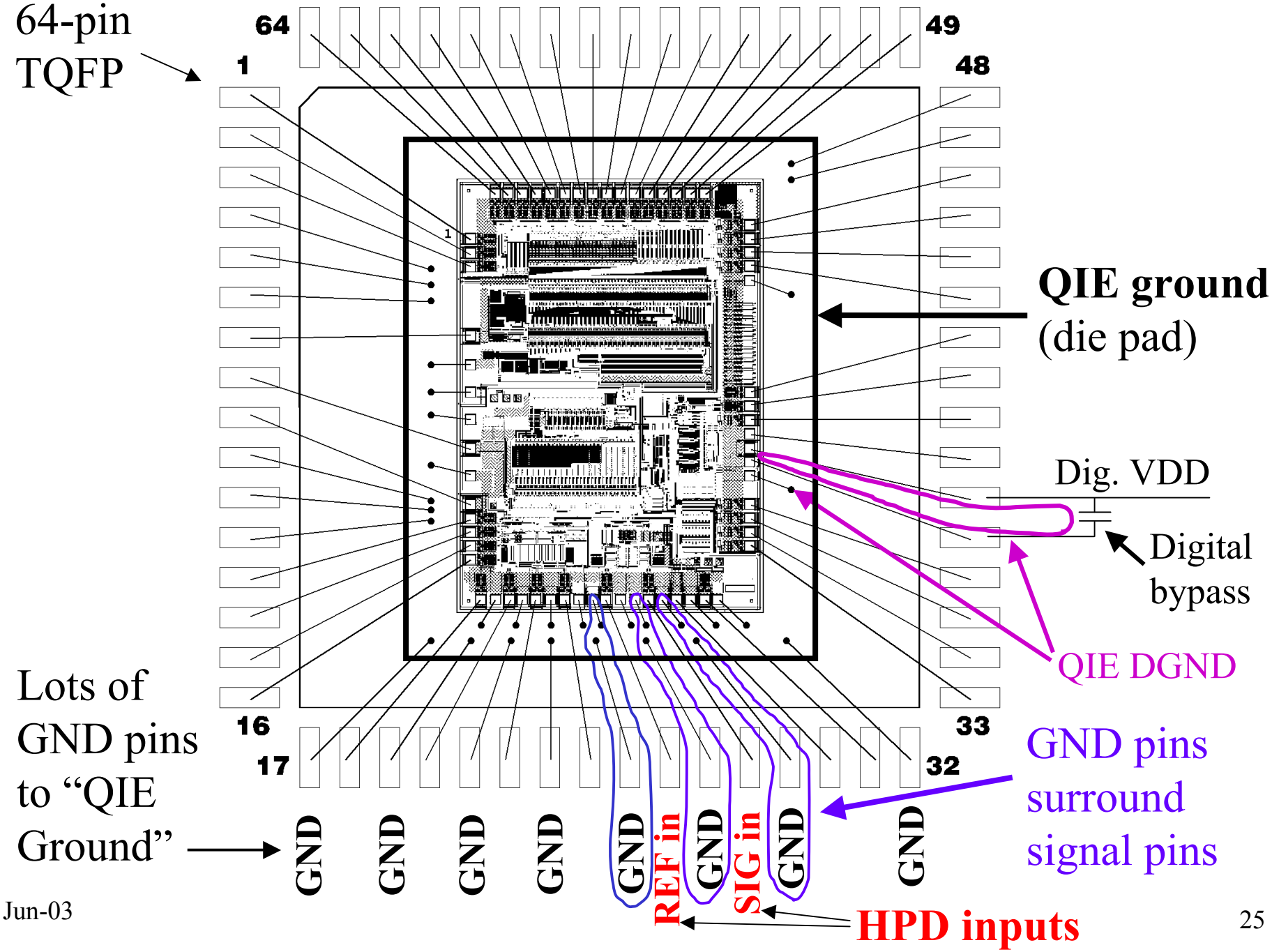
N collector implant (connect to +5V)

Substrate contact (dedicated gnd pin)

Analog inputs (pseudo-diff.)

Package Level

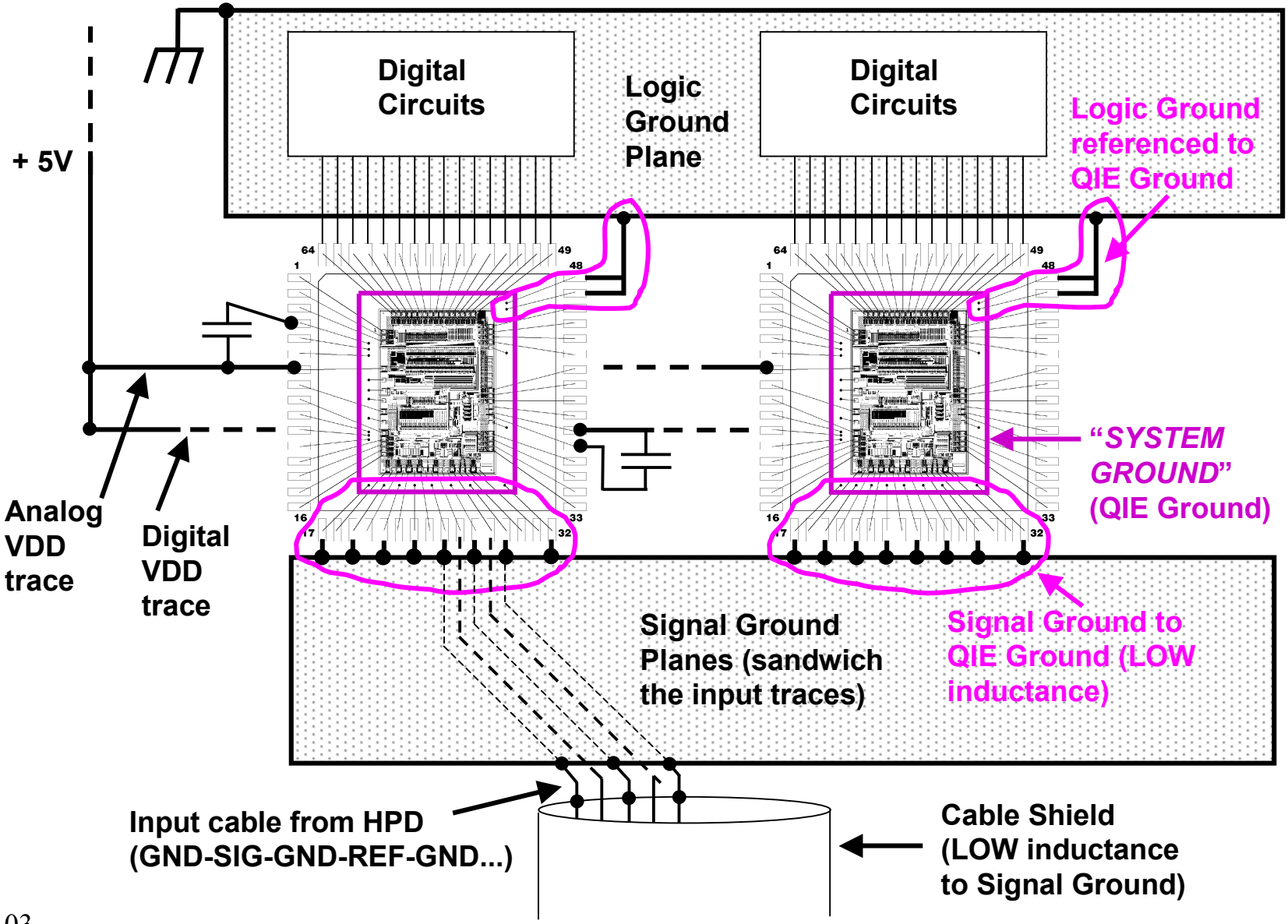
- Small 64-pin TFQP
- Internal metal die pad is God's "**QIE ground**"
- QIE digital ground (and all other chip grounds) are referenced to "**QIE ground**" inside the package
- Separate pin used to return digital bypass ground current to the chip only – transient bypass cap current doesn't flow through any ground plane.
- Lots of package GND pins from the die pad to facilitate the transfer of "**QIE ground**" to the PCB
- Use input amplifier ground pins on BOTH sides of SIG and REF input pins (more on this later)


64-pin
TQFP
64
49
1
48
1
QIE ground
(die pad)
Dig. VDD
Digital
bypass
QIE DGND
Lots of
GND pins
to "QIE
Ground"
16
33
17
32
GND
GND
GND
GND
GND
REF in
GND
SIG in
GND
GND
GND pins
surround
signal pins
HPD inputs

Board Level

- Follow the principle of "connect the grounds only at the ADC" (in this case, "ADC" is the QIE chip)
- Separate planes for **Signal ground** (QIE inputs) and **Logic ground** (digital support chips)
- **Signal ground** well connected to **QIE ground** (the die pad) with many pins (low inductance)
- **Logic ground** referenced to **Signal ground** only at **QIE ground** (digital currents stay on **Logic ground** and away from **Signal ground**).
- Single 5V QIE power supply with separate trace runs for analog and digital VDD
- GND-SIG-GND input configuration all the way up to the chip pads: 1) shields against capacitive coupling, 2) minimizes input loop areas, magnetic coupling to loop areas tends to cancel (like a coax)

QIE8 PC Board



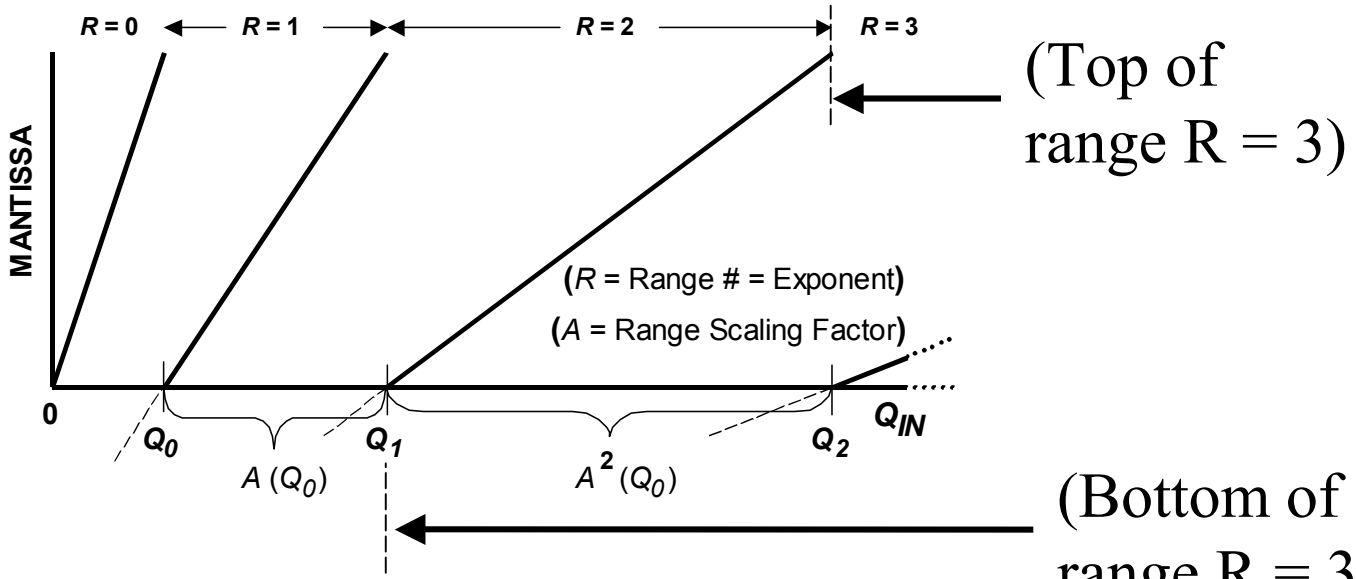
Conclusion

- Earlier QIE chips:
  - ORBIT process
  - $A = 2$
  - External opamp + ADC
  - Dual +/- supply
- QIE8:
  - AMS 0.8u BiCMOS (much better process)
  - Higher range scaling to optimize front end ($A = 5$)
  - Single chip with custom non-uniform ADC
  - Simple: 1 supply + a few external passive components
  - Excellent performance!

Appendix A: Modified Floating Point Analysis

→ Charge at the top of range R: $Q_R = \sum_{x=0}^{R} A^x 2^N Q_{LSB}$
(N = # of ADC bits)

→ Relative quantization error $e_{qr} = \frac{(bin\ size)/\sqrt{12}}{(input\ amplitude)} = \frac{A^R Q_{LSB}}{\sqrt{12} Q_{IN}}$



Case 1: "Small" scaling factor ($A = 2$)

(Charge at top of range R)

$$Q_R = \sum_{x=0}^{R} A^x 2^N Q_{LSB} \longrightarrow \begin{cases} Q_R \approx 2^{R+N+1} Q_{LSB} & \text{(top of range } R\text{)} \\ Q_{R-1} \approx 2^{R+N} Q_{LSB} & \text{(bottom of range } R\text{)} \end{cases}$$

Since the max. relative quantization error occurs at the range bottoms:

$$e_{qr} = \frac{A^R Q_{LSB}}{\sqrt{12} Q_{IN}} \longrightarrow e_{qr\max} \approx \frac{1}{(\sqrt{12})2^N} \longrightarrow N \geq \log_2 \frac{1}{\sqrt{12} e_{qr\max}}$$

(# ADC bits)

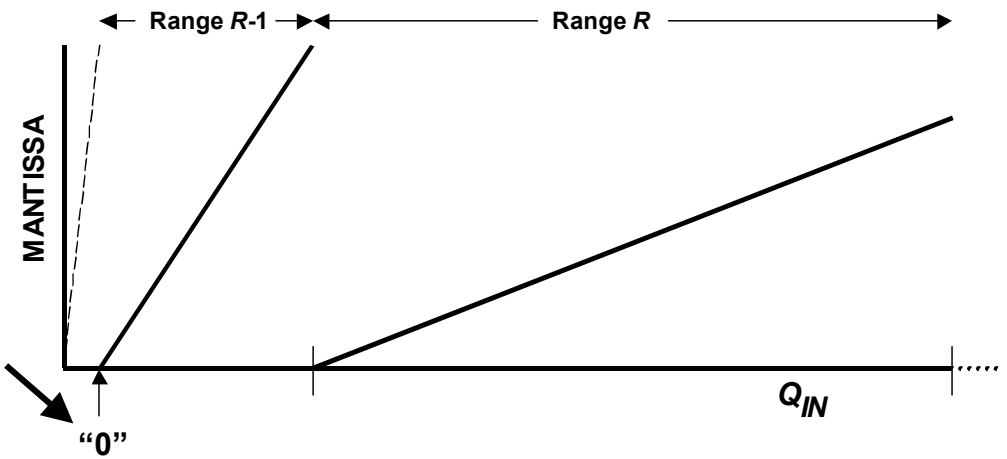
Number of ranges required: $\log_2 \frac{Q_{MAX}}{2^N Q_{LSB}}$

Case 2: "Large" scaling factor ($A > 2$)

An approximation: the total charge span is covered by the 2 most significant ranges. Then:

$$Q_R = (A^R + A^{R-1})Q_0 = \frac{A+1}{A} A^R 2^N Q_{LSB} \quad \text{(top of range } R\text{)}$$

$$Q_{R-1} = (A^{R-1} + A^{R-2})Q_0 = \frac{A+1}{A^2} A^R 2^N Q_{LSB} \quad \text{(bottom of range } R\text{)}$$



The input charge (and thus e_{qr}) varies by a factor of A across a range. Again, the max. relative error occurs at the range bottoms:

(For $A > 2$)

$$e_{qr} = \frac{A^R Q_{LSB}}{\sqrt{12} Q_{IN}} \longrightarrow e_{qr\,\max} \approx \left(\frac{A^2}{(A+1)} \right) \frac{1}{(\sqrt{12}) 2^N} \longrightarrow N \geq \log_2 \frac{A^2}{\sqrt{12}(A+1) e_{qr\,\max}}$$

(# ADC bits)

Number of ranges required: $\log_A \frac{A Q_{MAX}}{(A+1) 2^N Q_{LSB}}$