SOI Detector with Drift Field due to Majority Carrier Flow - an Alternative to Biasing in Depletion

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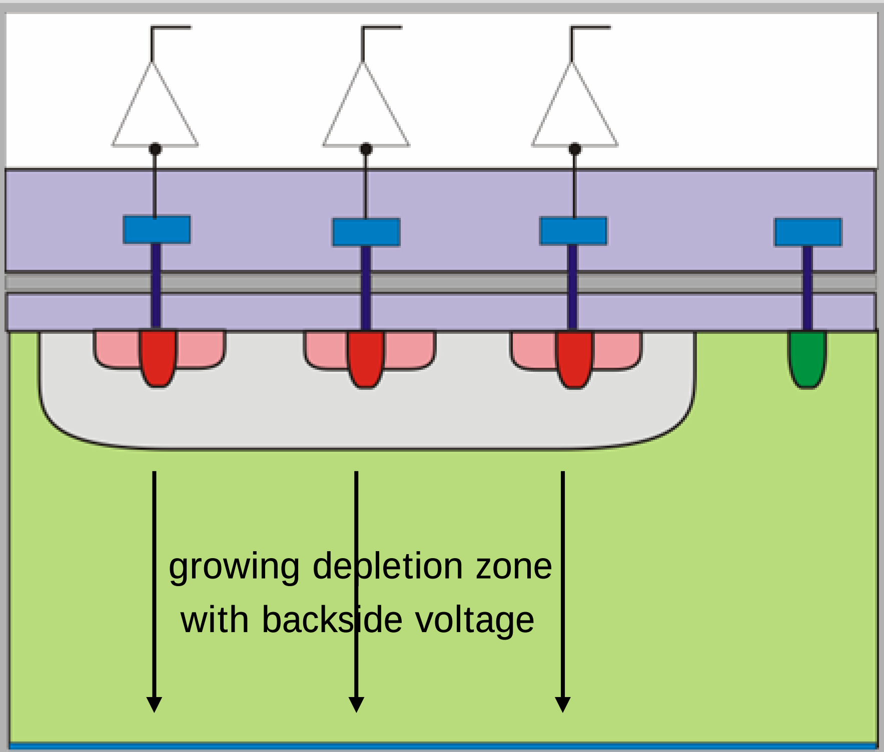
Outline

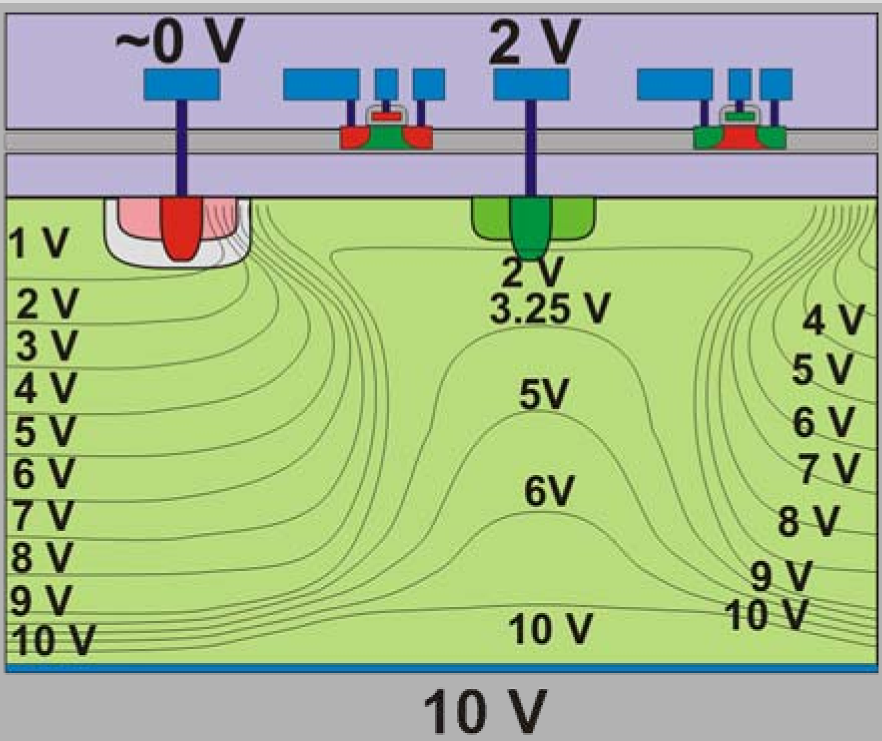
- standard depletion vs. drift biasing in OKI SOI
- August 2009 chip using drift structures
- first results with Fe55 source
- comparison drift vs. no drift, BPW diode vs. normal diode
- summary and outlook

standard depletion vs. drift biasing



up to ~100V

- p-diode in n-substrate (e.g. here)
- reversed biased by applying backside voltage
- voltage needed to fully deplete high resistivity (1kOhm) 250um thick material in the order of 100V



- diode still p-in-n (e.g. here)
- **moderate voltage (around 10V) applied to backside**
- additional n-in-n rings biased to create drift field

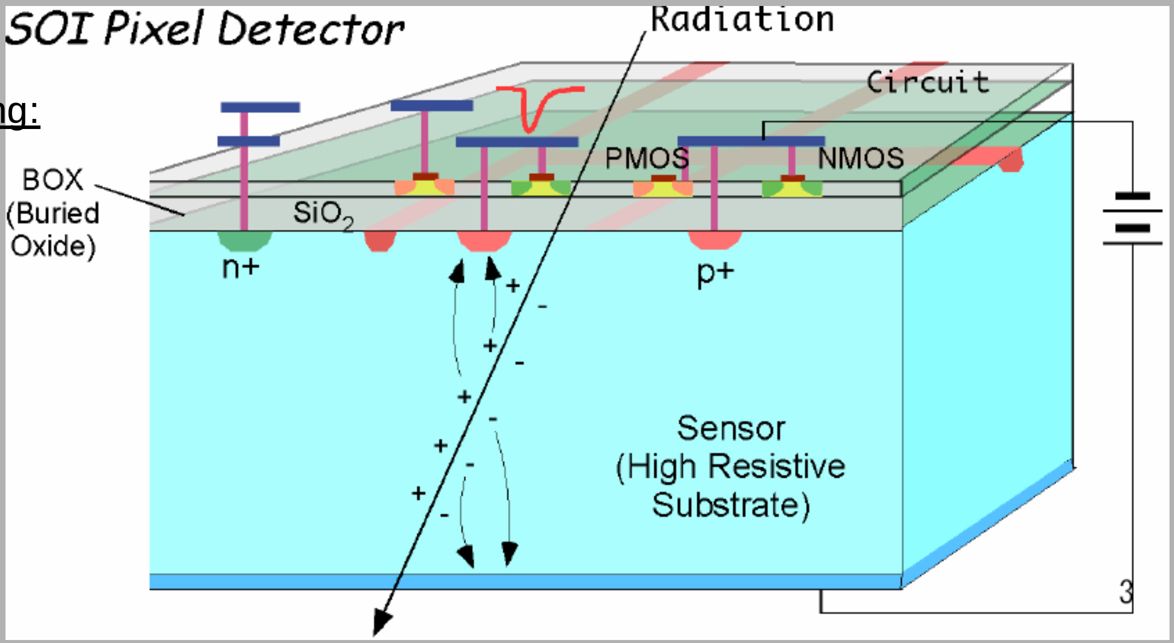
$$U = \frac{d^2}{t \cdot \mu}$$

- collection time of 100ns in 250um detector: 10-15V on backside sufficient
- n-ring(s) at front side create(s) additional **lateral drift field** to improve charge collection

SOI pixel detector (in unidepleted(*) scheme)

(*) CMOS detector 'in unidepleted mode' proposed by P.Rehak et al.

using this approach in **SOI technology**
on high resisitvity substrate is especially appealing:
- vertical drift field generation possible
  due to low biasing current:
  [500 Ωcm and 13V: 4uA per pixel (20um pitch)]



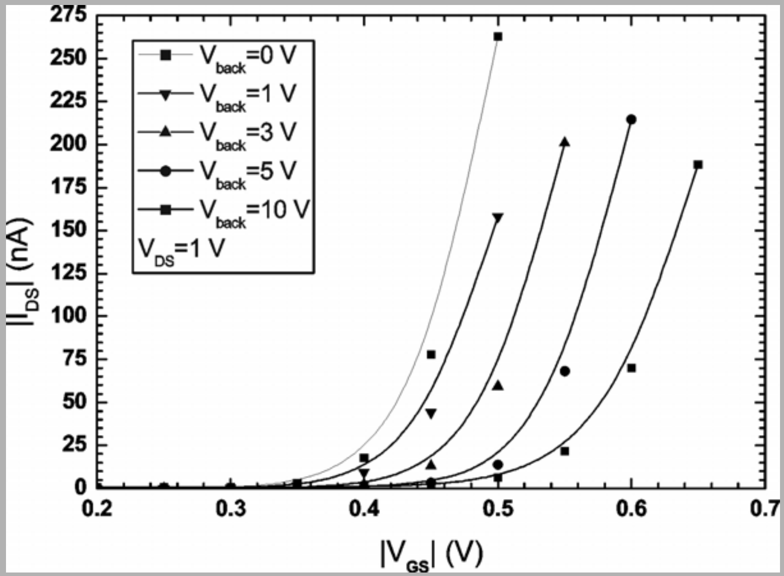
general advantages of SOI detector:

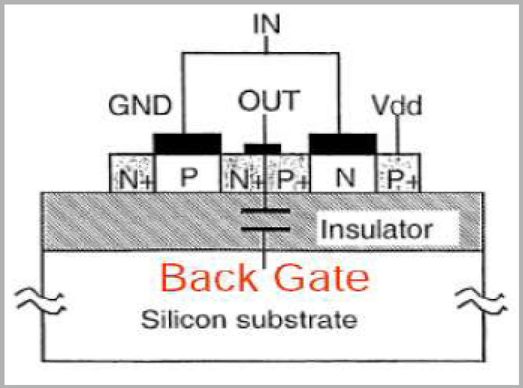
- monolithic approach (prime example)
- small diode input capacitance
- access to full CMOS (nmos/pmos)
- no bumping: low mass, low cost

Process	0.2μm Fully-Depleted Low-Leakage, SOI CMOS, tox=4.5/7 nm, 1P4M, MIM, DMOS, Vcore=1.8 V (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick, Handle wafer: Cz、700 Ω-cm (*n-type*), 650 μm thick (SOITEC)
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

back gate effect / advantage of drift biasing

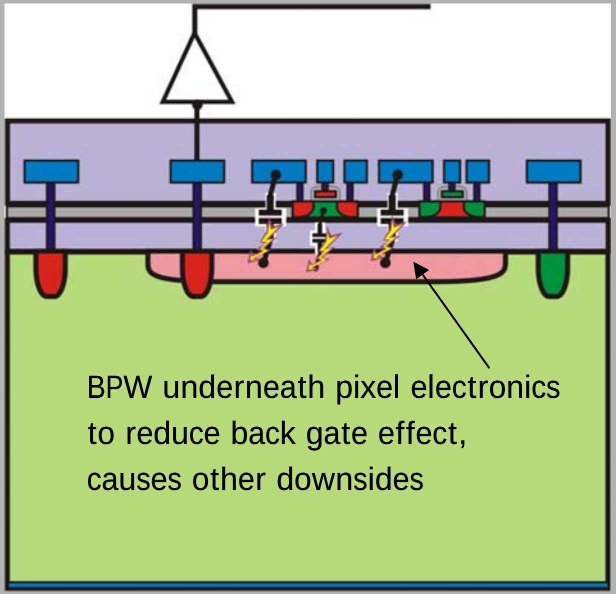
test transistor from the MAMBO II submission:



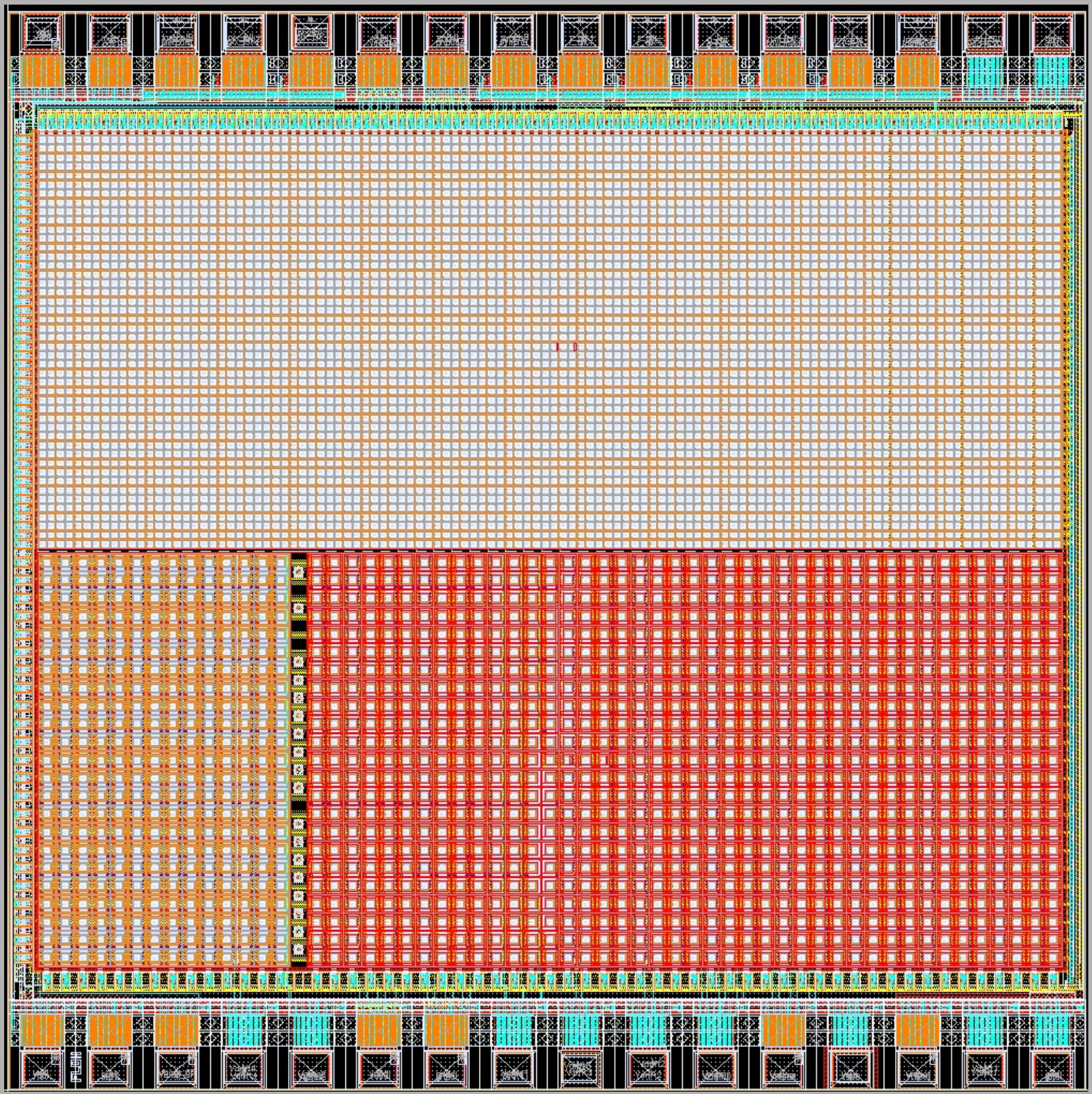


back gate effect causes significant threshold voltage shifts, up to failure of more complex analog designs

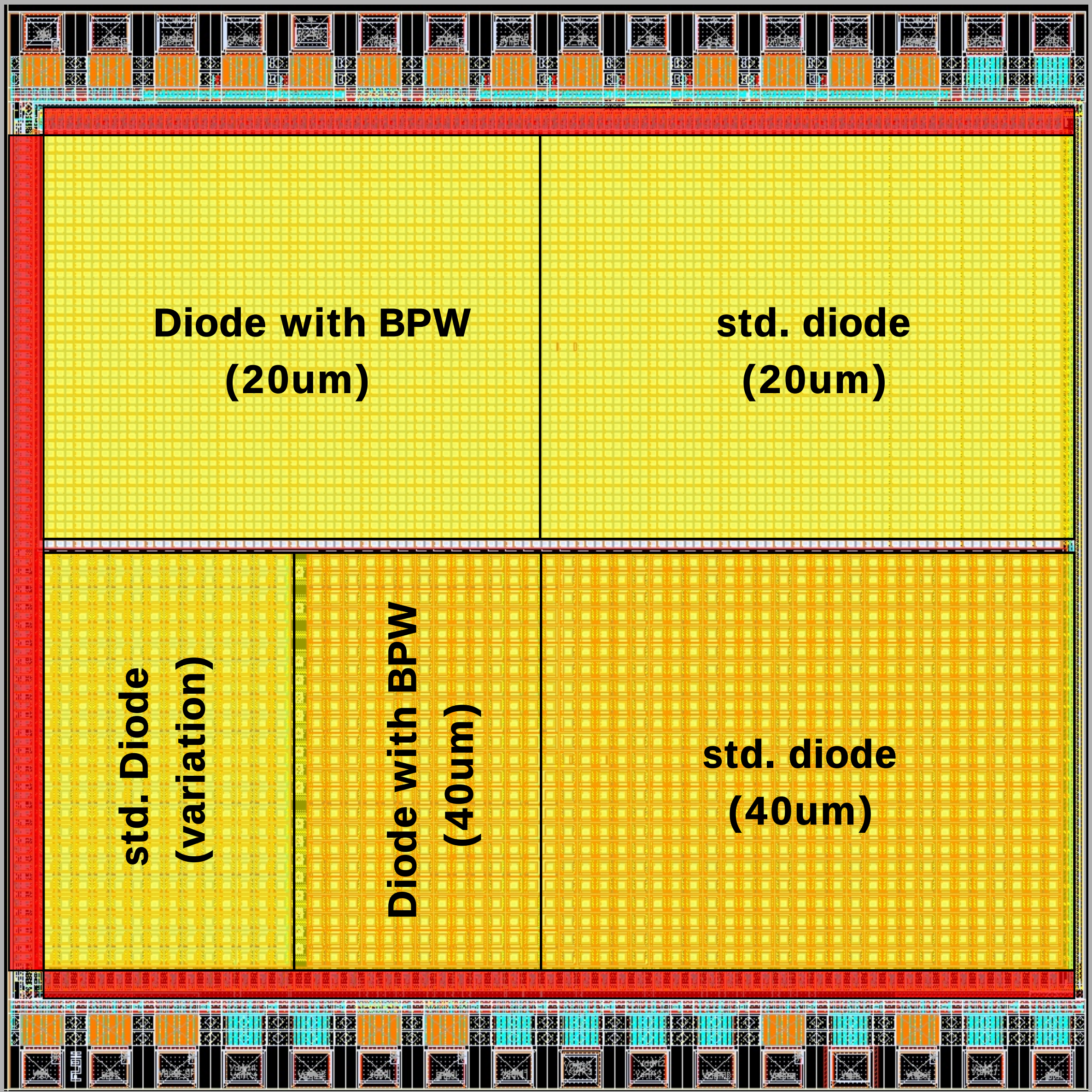
- BPW has been proposed to reduce back gate effect: deep p-well shielding the entire pixel electronics
- However, much larger diode increases noise & decreases gain
- also, coupling of CMOS activity into large collecting diode through thin (200nm) BOX likely and severe!



August 09 - Chip overview



August 09 - Chip overview

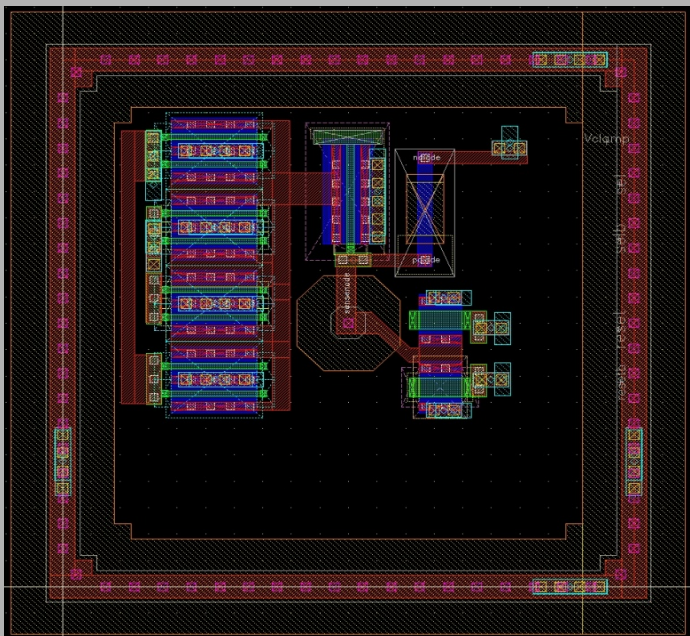


- 2.5 x 2.5mm chip size
- prototype for drift structures
- pixel pitches: 20um, 40um
- various designs, most importantly normal diode and diode with BPW

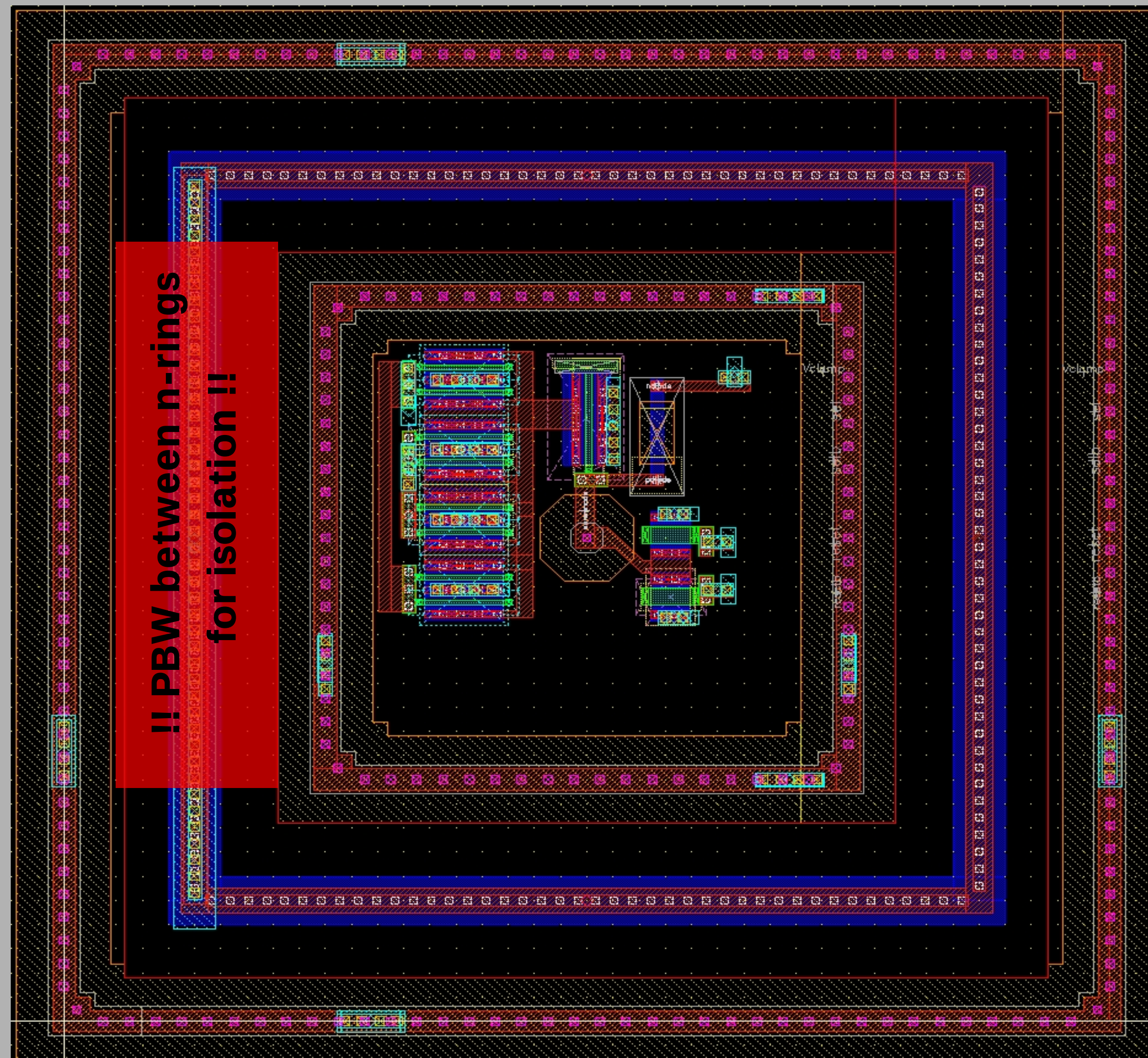
yellow: sensor area
red area: control logic and multiplexing

pixel designs

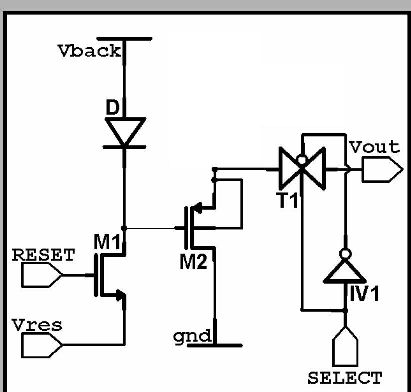
20um pixel layout (1 drift ring):



40um pixel layout (2 drift rings):

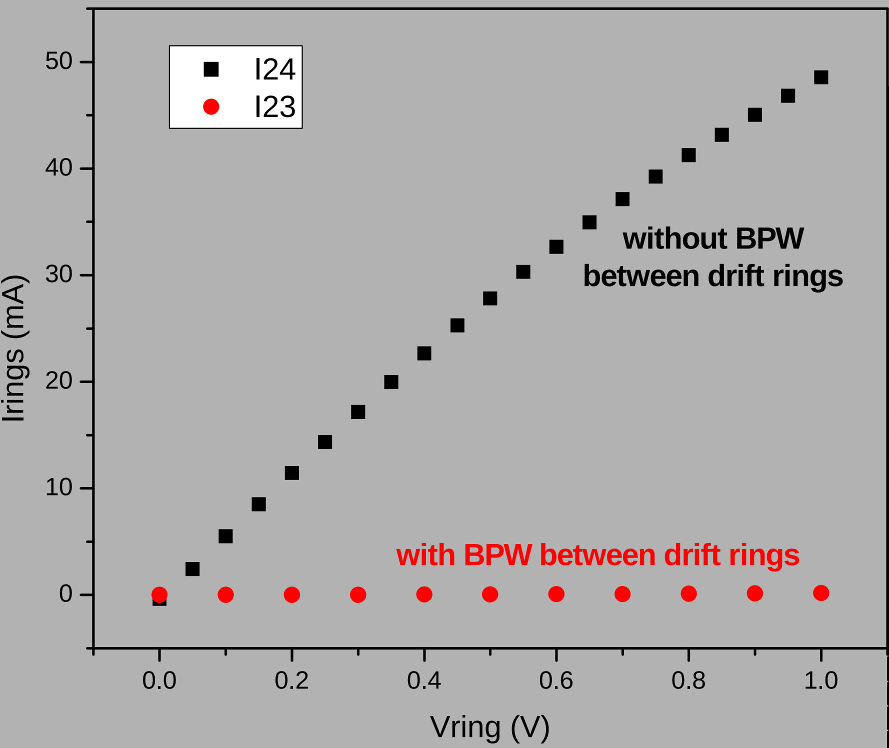


schematic (3T-like pixel architecture):



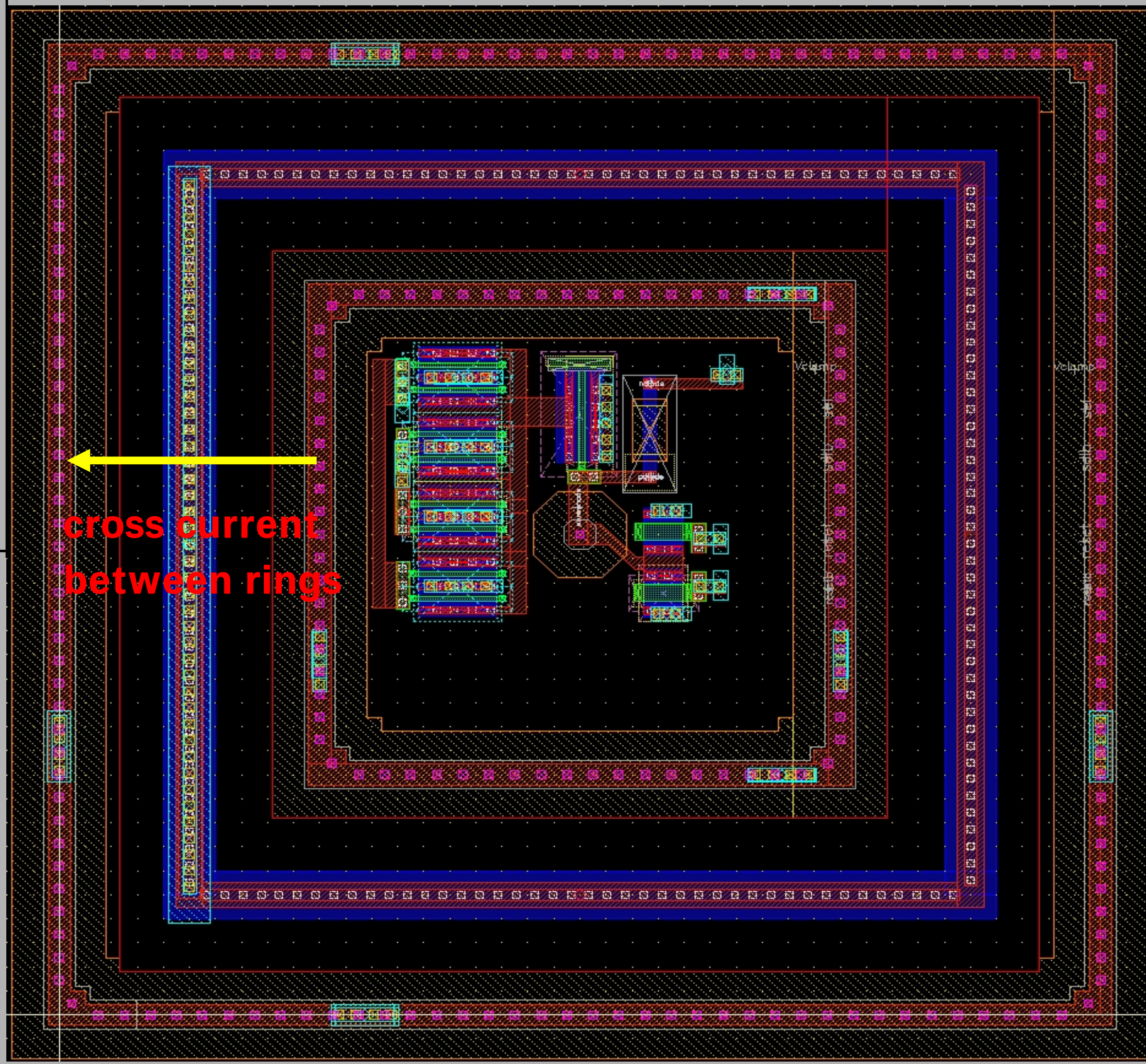
- SF, reset, select, clamp
- emphasis on studying detector properties

pixel designs (cont'd)



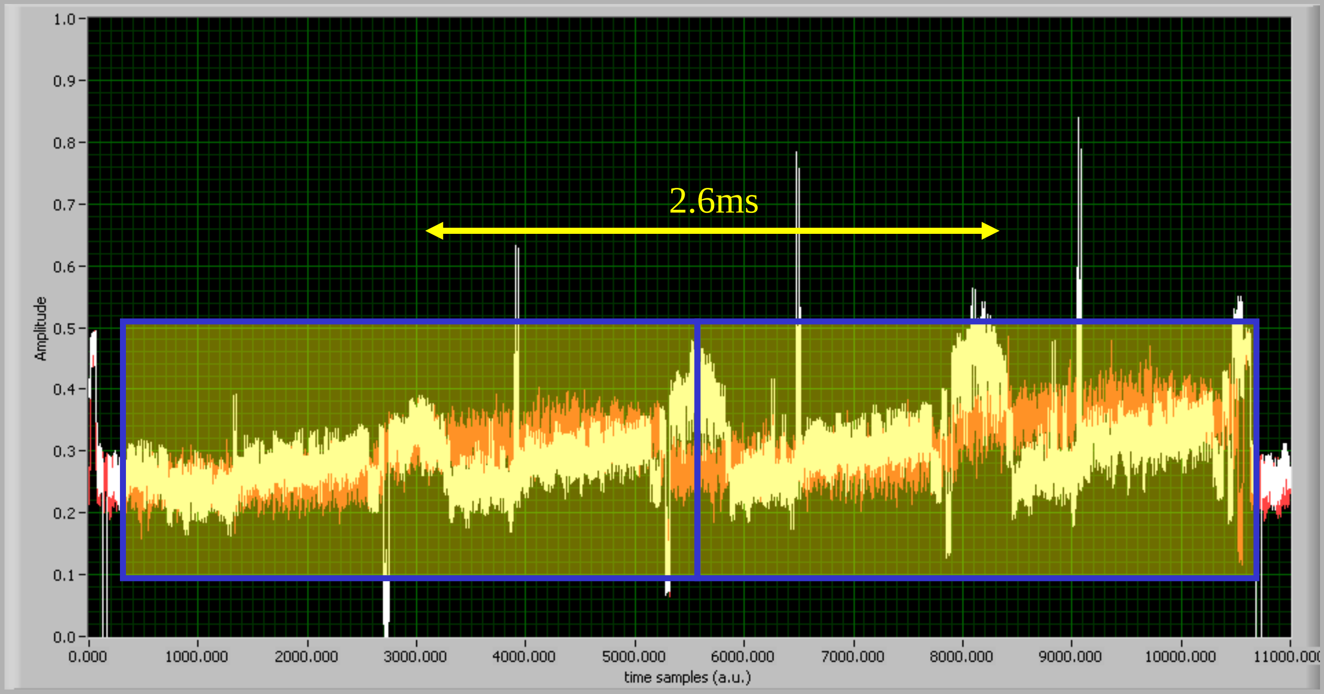
BPW between n-rings
'eliminates' cross current

40um pixel layout (2 drift rings):

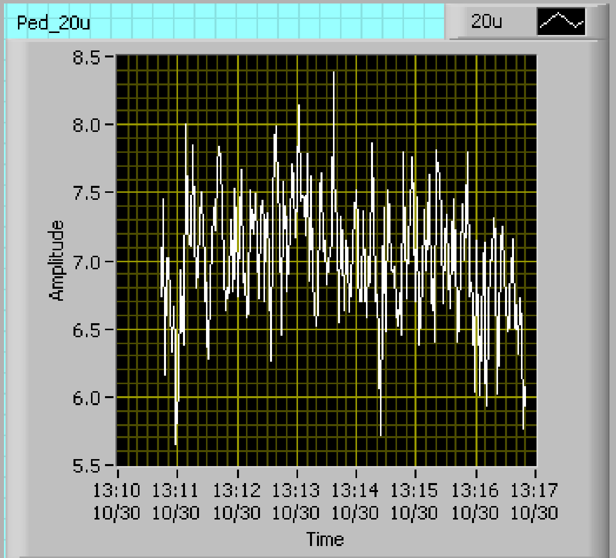


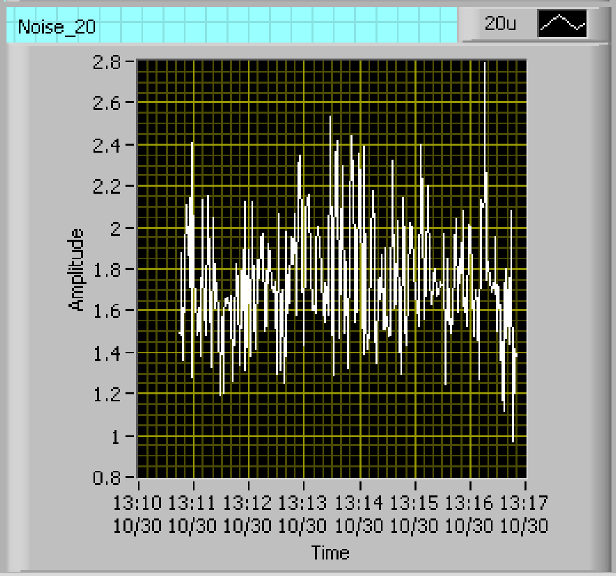
readout / matrix operation

raw data of two successive frames:



mean pedestal and noise over time:





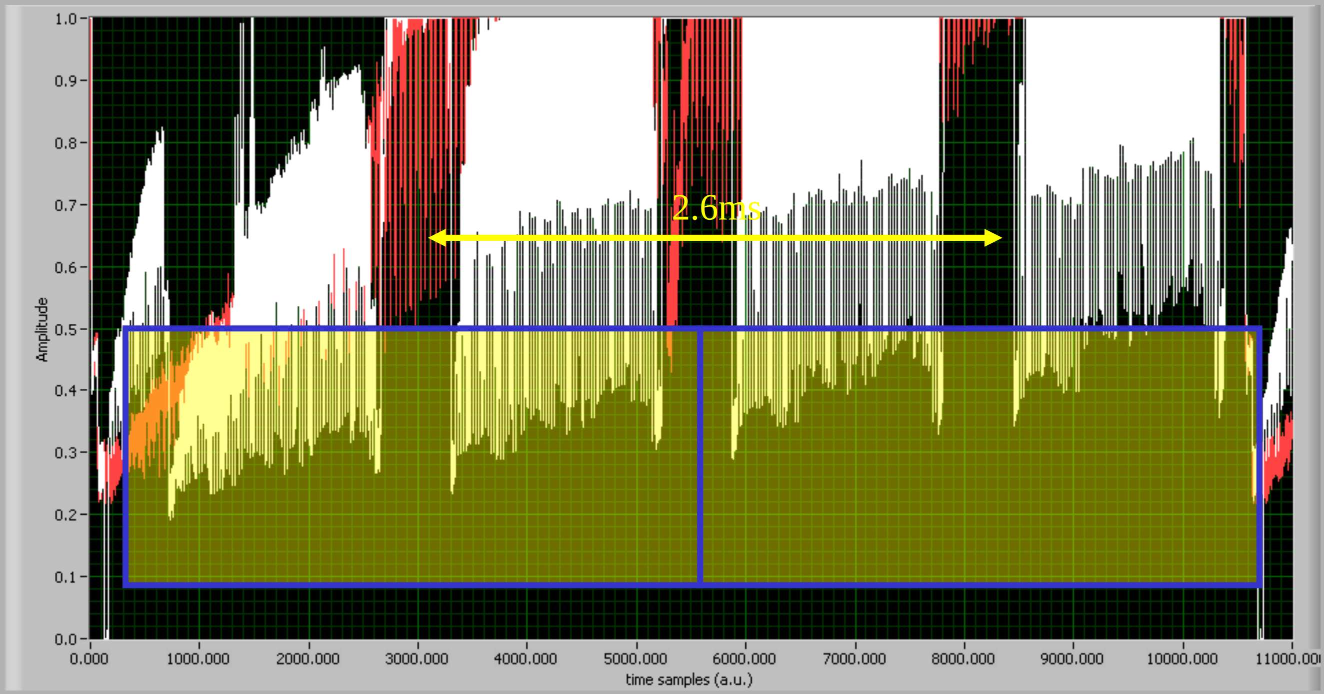
drift operation: 3V backside, 1.5V and 2V drift rings,

moderate cooling (using peltier element at 6W) to **15.2 ºC**

- matrix read out: 2.6ms
- CDS between two successive frames
- continuous (average over 25 frames) pedestal computation and subtraction

current biasing limitation

raw data of two successive frames:



- current limitation is to run at **drift voltage** with respect to backside at **1-2V**
- more aggressive cooling may help in future to go to higher drift voltages
- use Fe55, front side illuminated for tests

drift operation: 3V backside, 1.5V and 2V drift rings,
without cooling, chip temperature: **30.5 ºC**

- currently, even with moderate cooling bias **drift voltage of 2V** (3V backside , 1V inner ring) **cannot be exceeded**,
- this kind of leakage **DOES NOT** occur in **standard depletion** bias (even at 8V),
- assumption is that in drift biasing scheme, charge is collected from the entire volume **including the backside** of the chip, which is not specifically treated (implantation and annealed) -> increased carrier generation

Radiogram with Fe55

tungsten Fermilab-Logo placed on top of chip

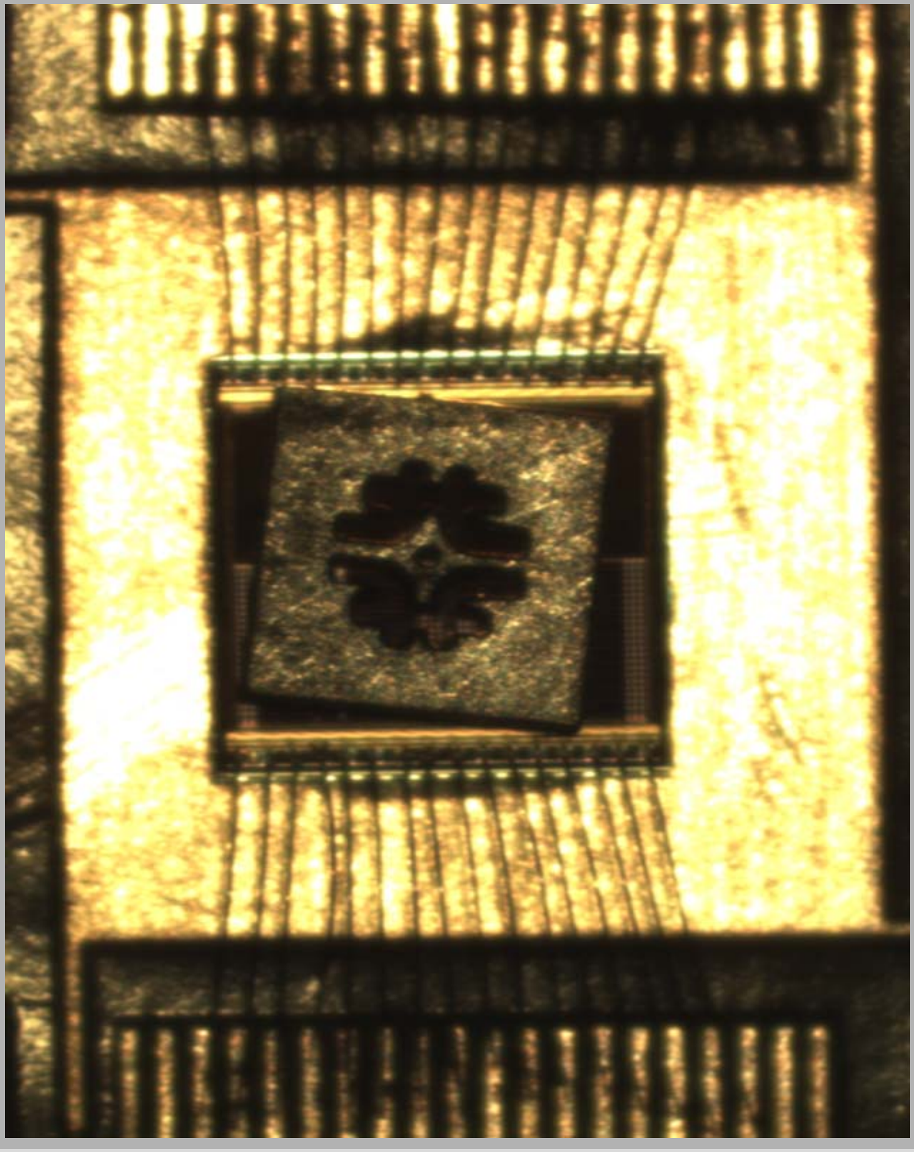
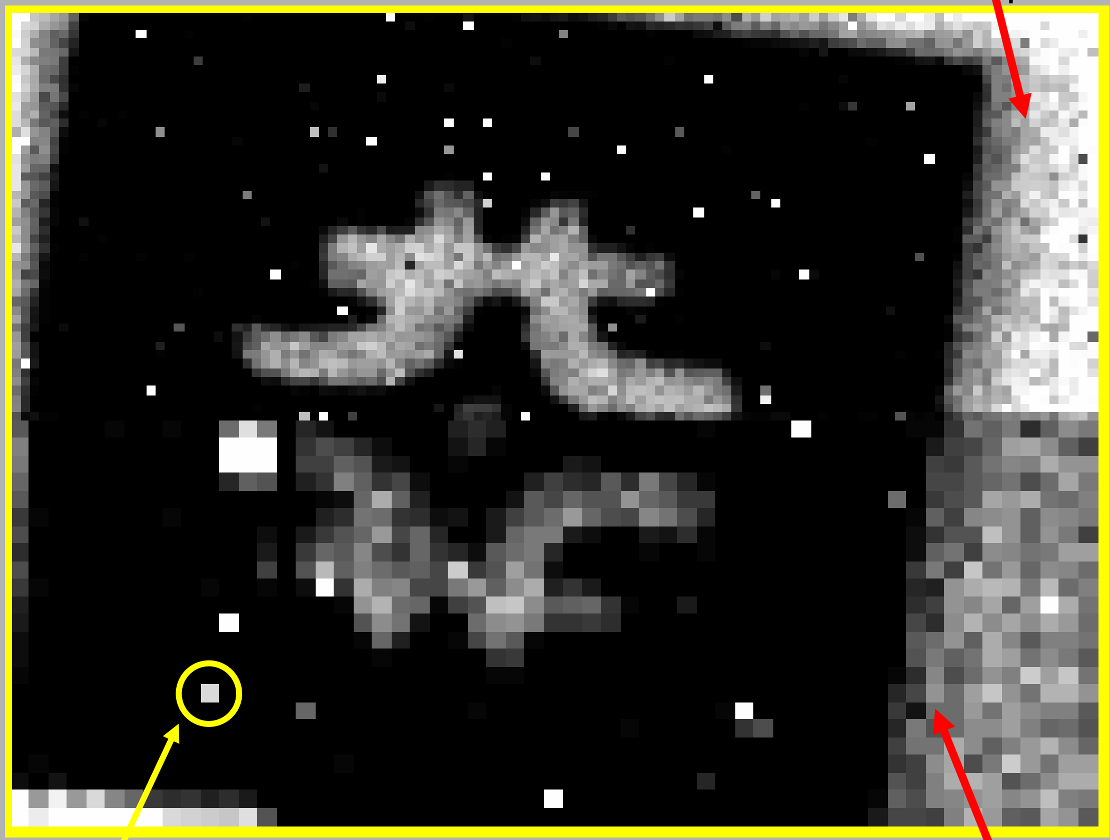
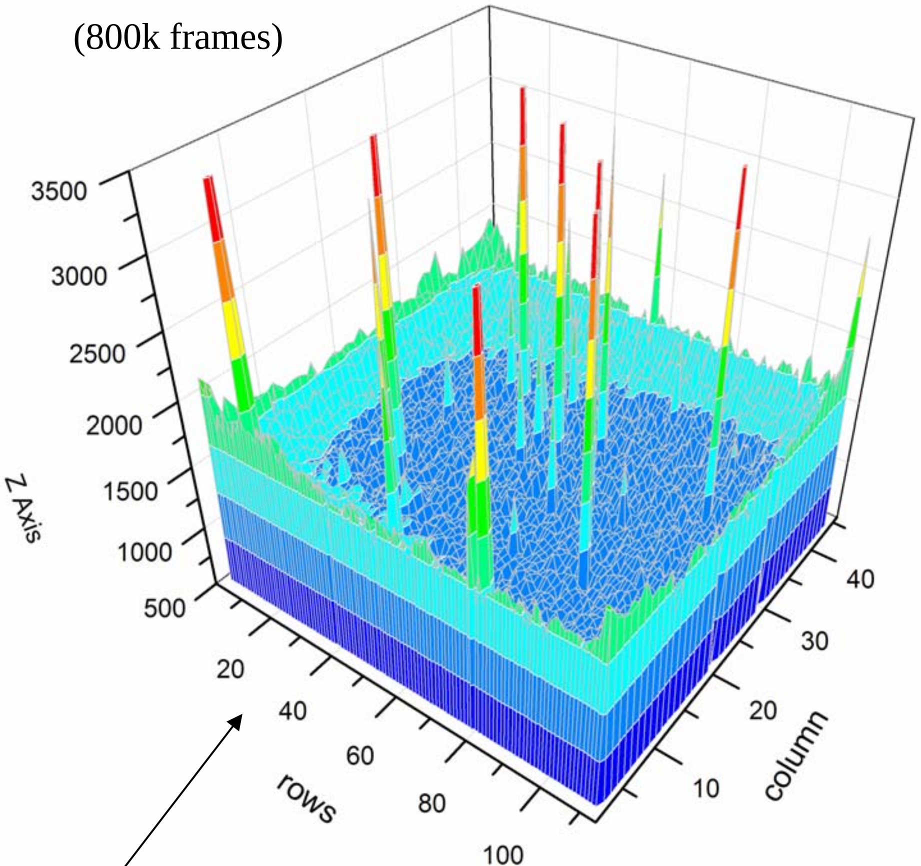


Image obtained in **drift configuration** (8σ cut on hits)

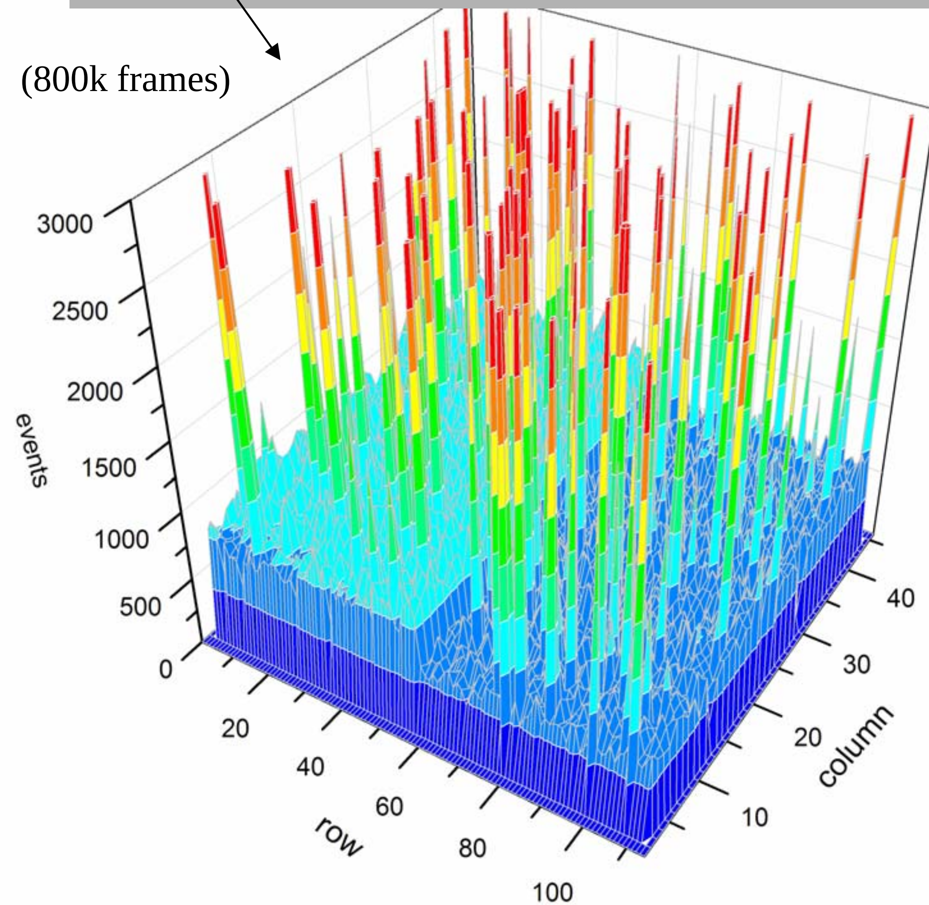
- 3V backside,
- 2V, 1V for 40um pixel rings
- 1.5V for 20um pixel ring



flatfields (drift vs. no-drift) – 20u pixels

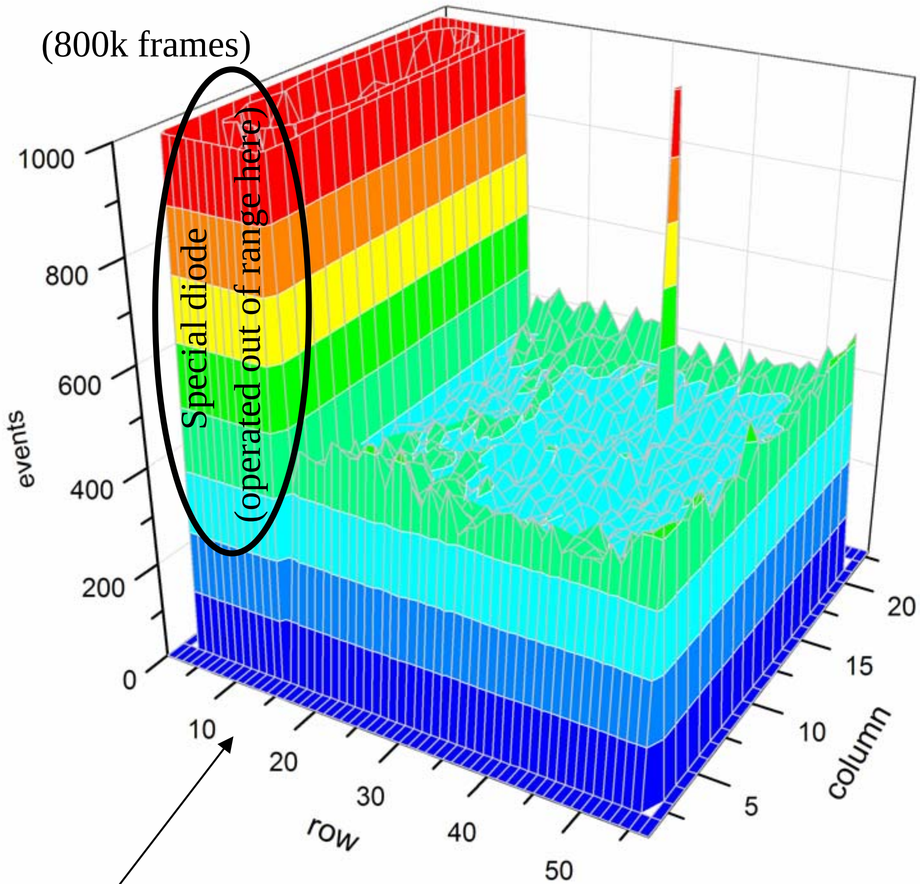


no drift:
- distinct hit rate for BPW, normal diode
- average: ~ 600 hits (normal), ~800 hits (BPW)



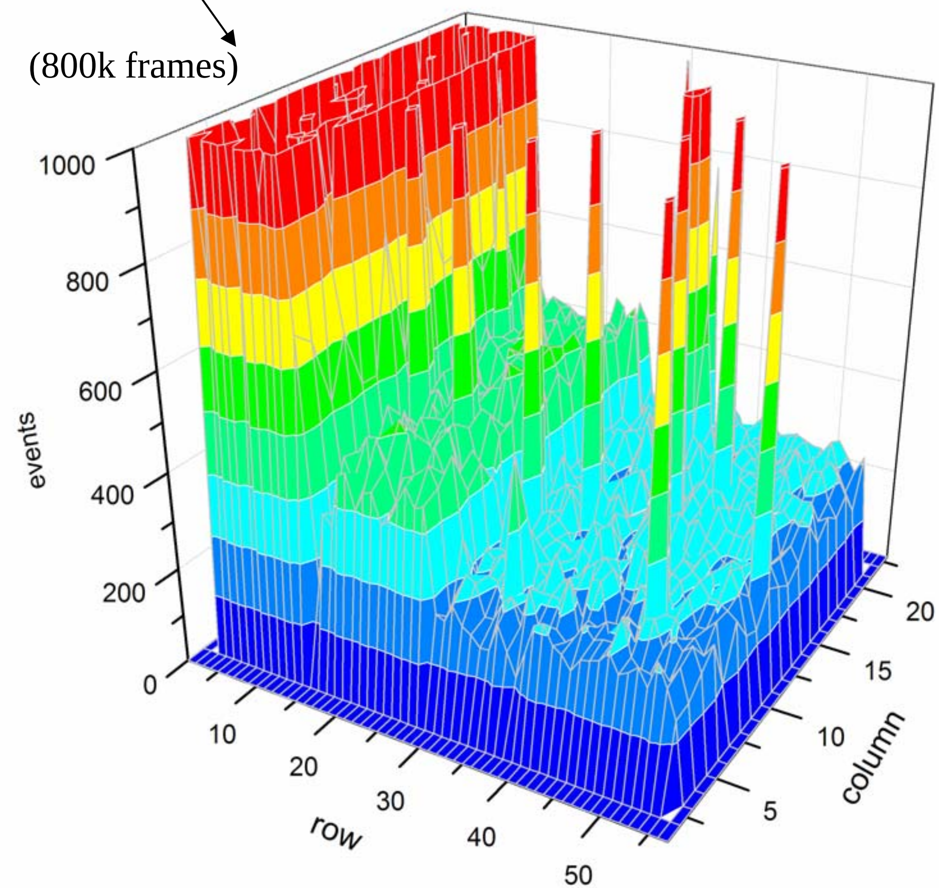
drift configuration:
- more homogeneous (BPW, normal)
- average hit ~ 1200 hits
  (about twice as much hits compared to no drift)
- much less ghost pixels

flatfields (drift vs. no-drift) - 40u pixels



no drift:

- distinct hit rate for BPW, normal diode
- average: ~ 300 hits (normal), ~400 hits (BPW)

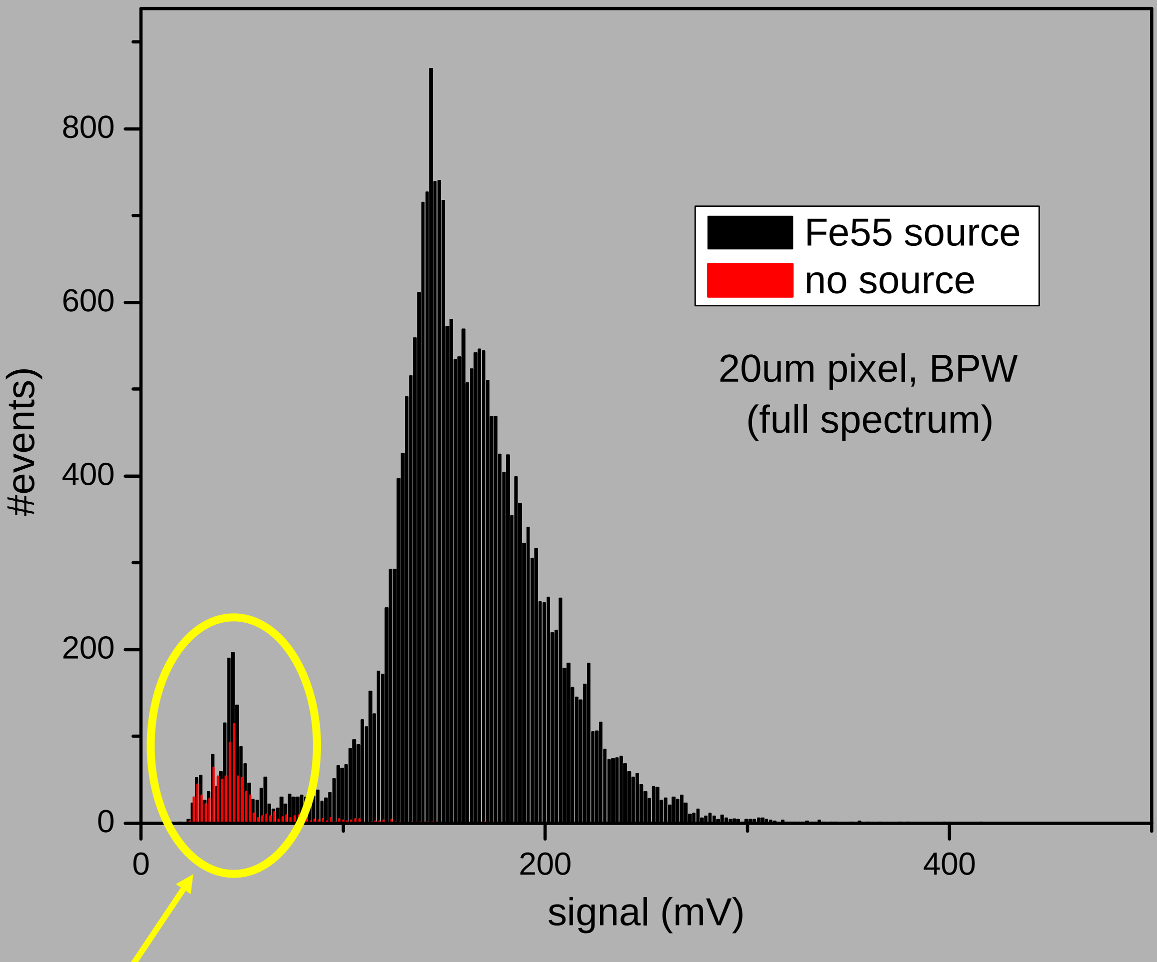


drift configuration:

- more homogeneous (BPW, normal)
- average hit ~ 400 hits
- much less ghost pixels

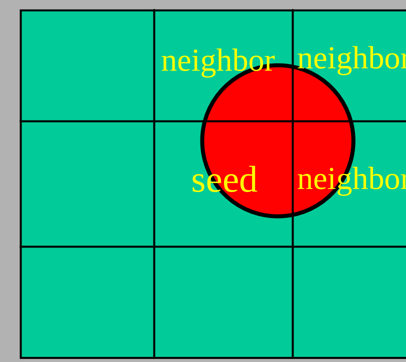
Fe55 spectrum (preliminary)

Full Spectrum (no cluster separation),
in drift operation (3V backside, 1.5V ring)



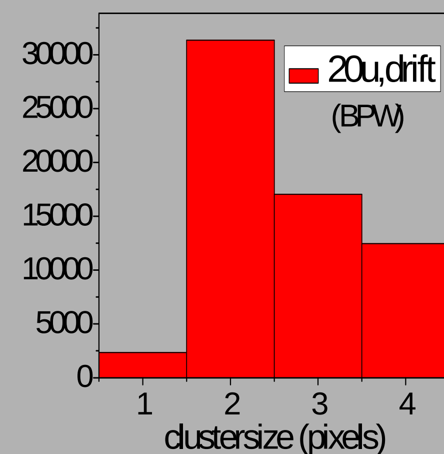
Ghost hits with and without source

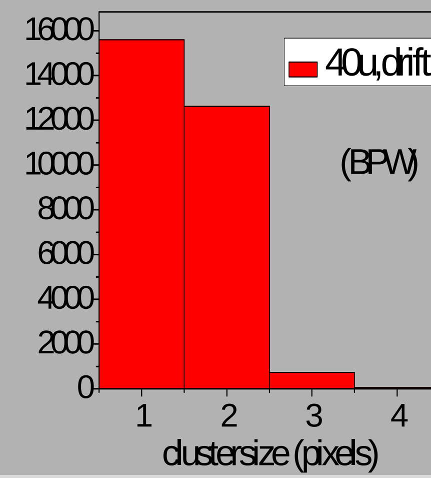
cluster reconstruction:



- max. signal/noise
- 8σ cut on seed
- 3σ cut on neighbor pixel

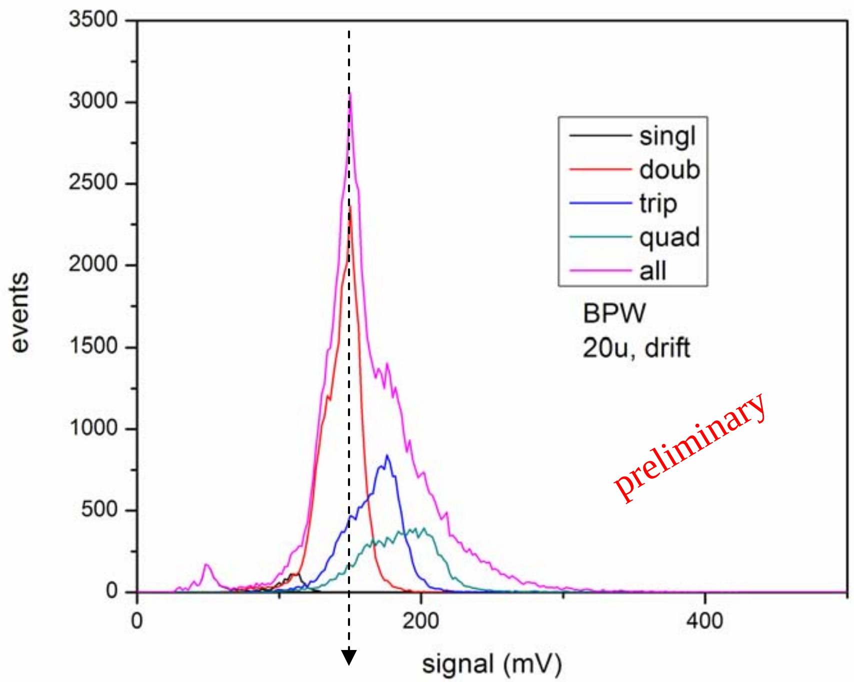
(electronic noise ~ 2mV, eq. ~20e)



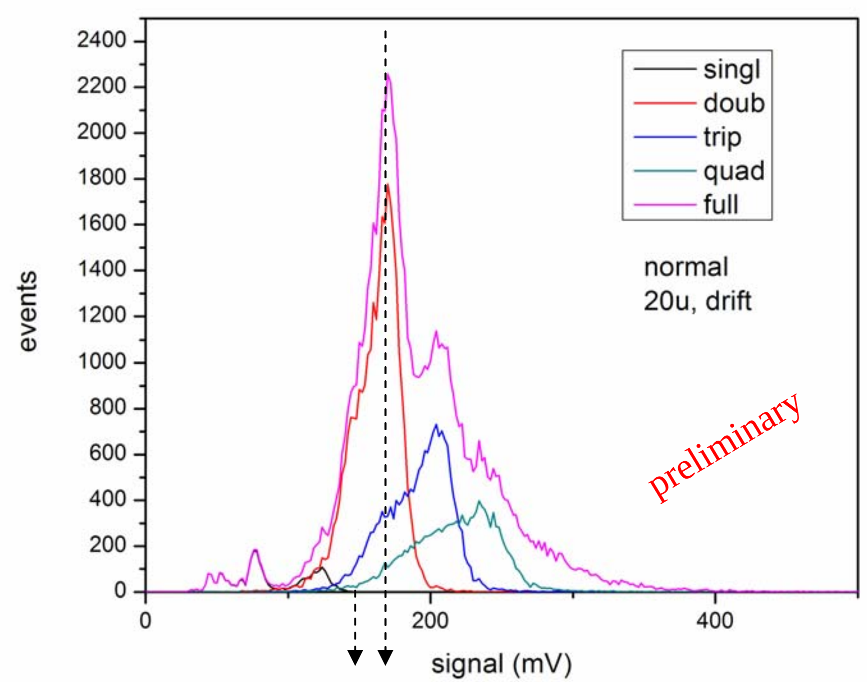


pixel gain: PBW / normal diode

BPW diode (in drift operation), 20um pixel

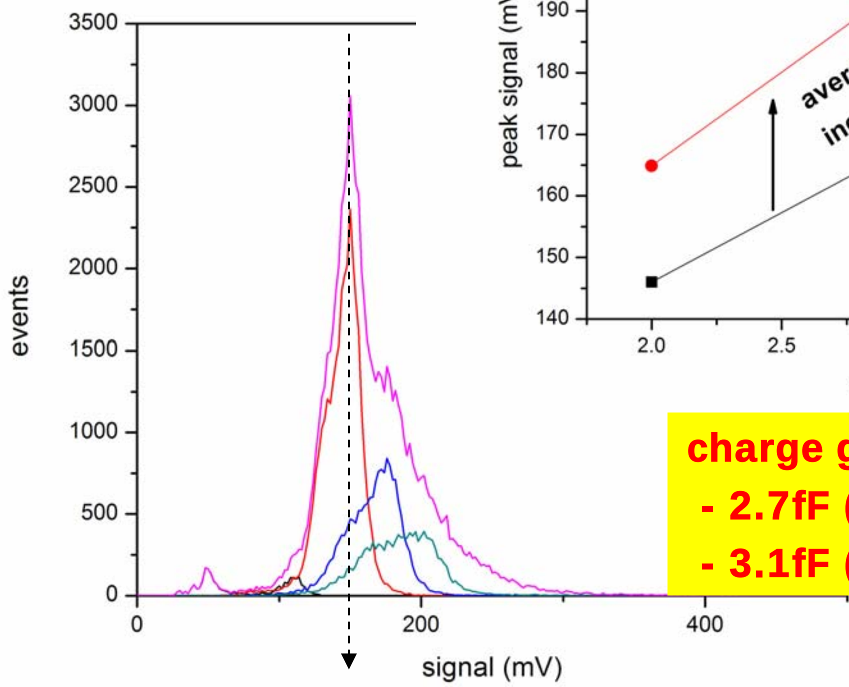


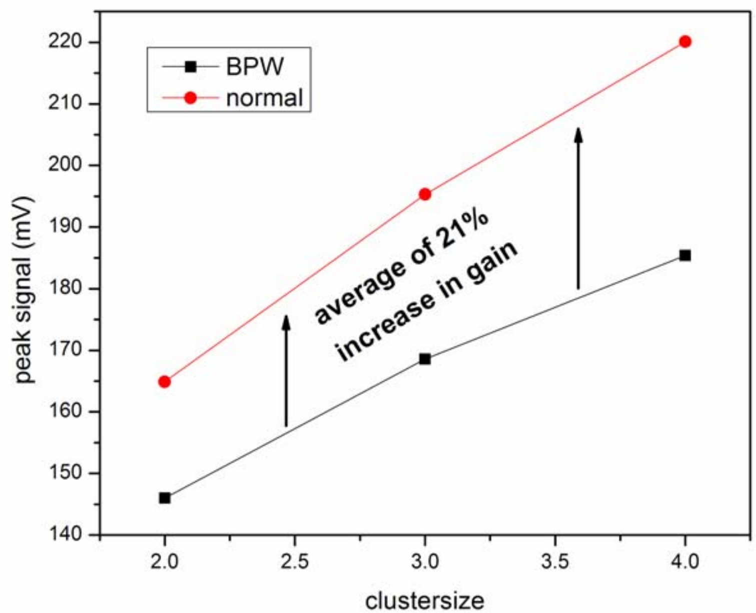
normal diode (in drift operation), 20um pixel

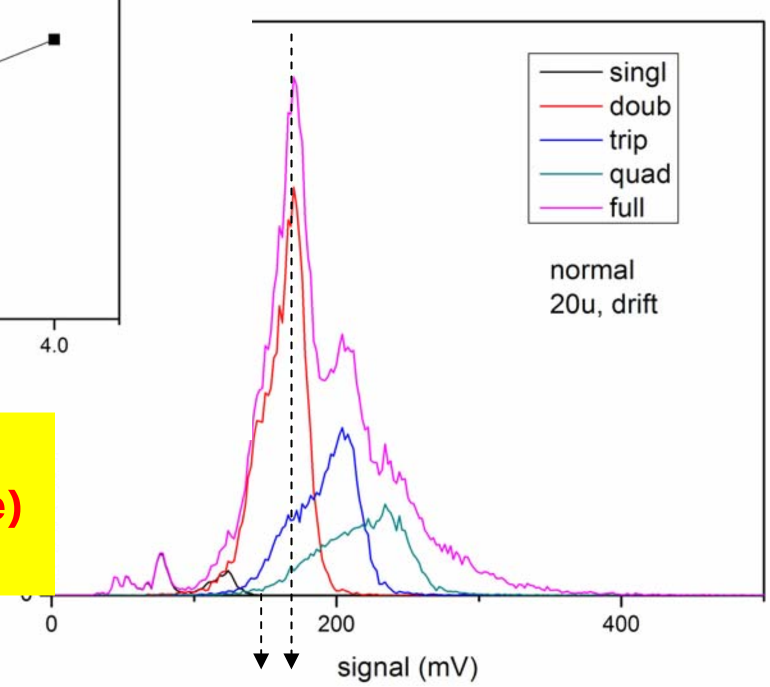


pixel gain: PBW / normal diode

BPW diode (in dr ... de (in drift operation), 20um pixel





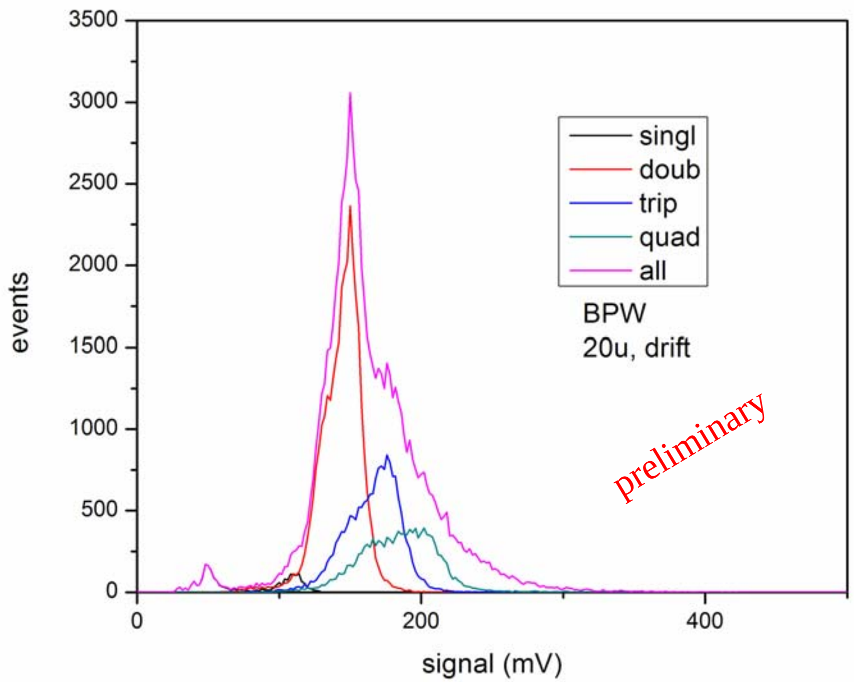


charge gain:
- **2.7fF (normal diode)**
- **3.1fF (BPW)**

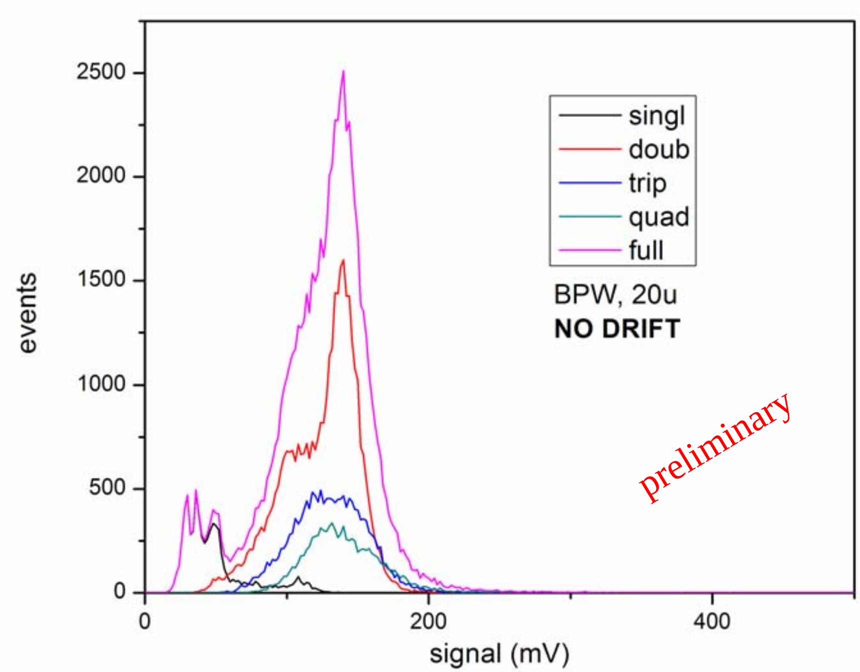
also observing **higher gain for** normal **40um pixel** compared to BPW version

drift vs. no drift

BPW diode **(in drift operation)**, 20um



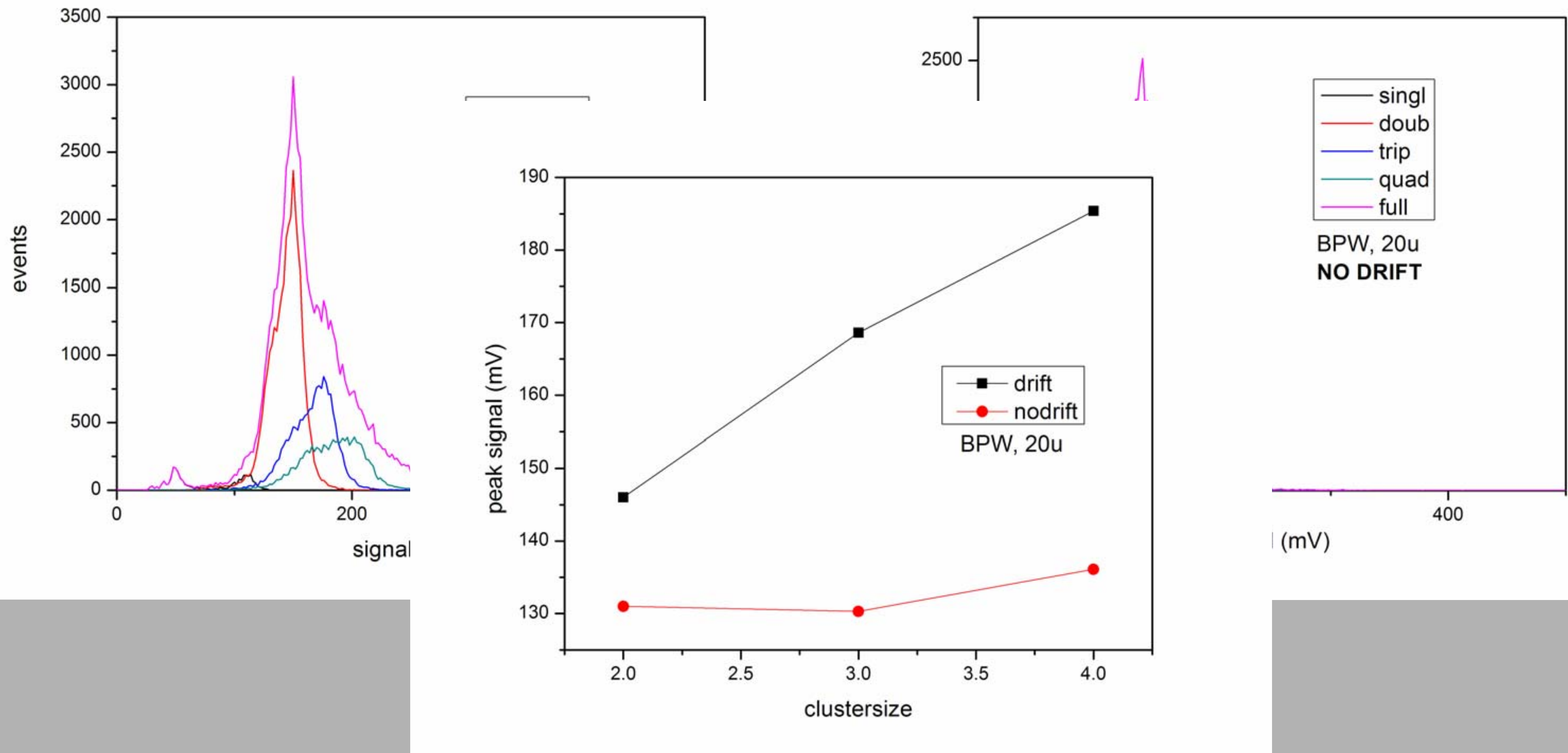
BPW diode (**NO Drift field),** 20um pixel



drift vs. no drift

BPW diode **(in drift operation**), 20um

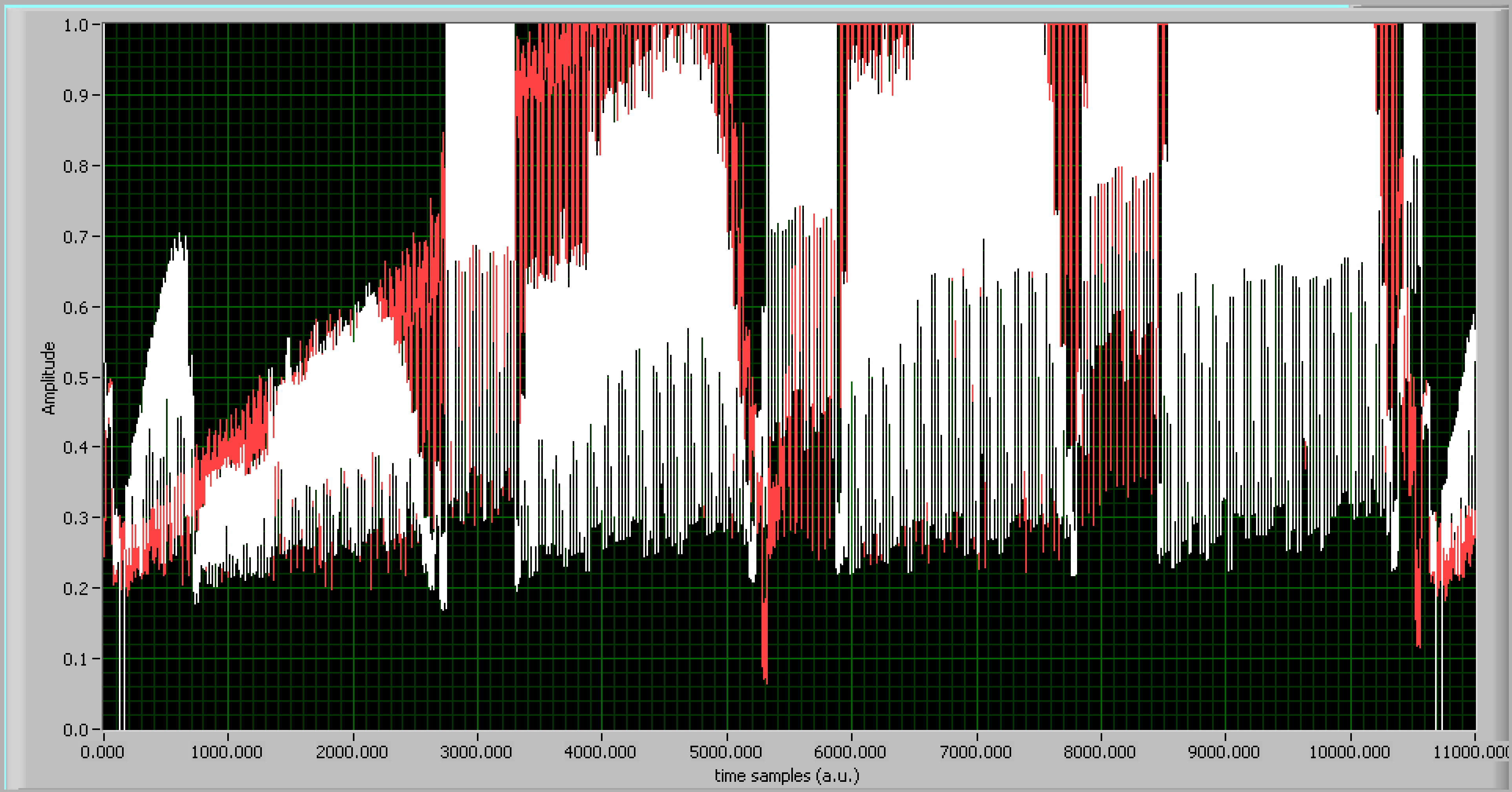
BPW diode (**NO Drift field),** 20um pixel



summary / outlook

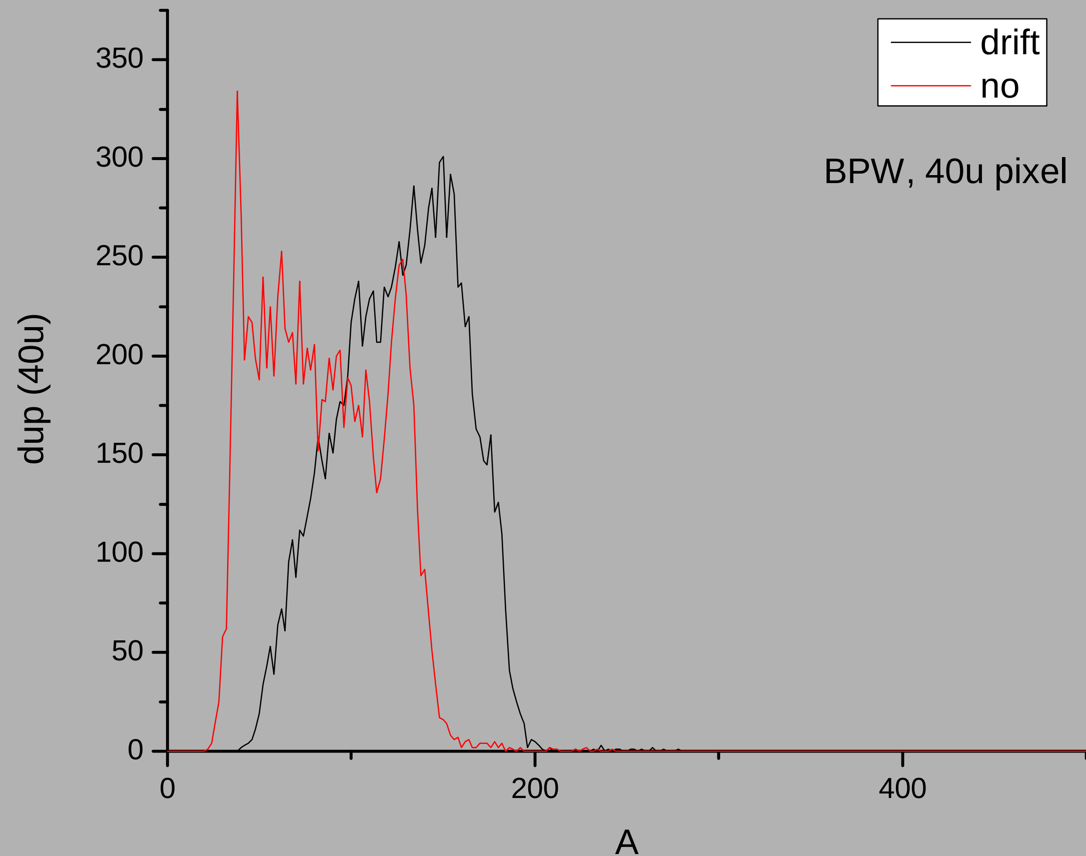
- **Realization of drift biasing scheme in high resistivity SOI process** (OKI semiconductor)
- SOI detector as **true monolithic device** offers many advantages (compact, low cost)
- Drift biasing scheme naturally eliminates back gate effect (being one issue with SOI detectors at the moment)
- **Full operation of the detector using drift scheme demonstrated**
- First results are promising, however not fully conclusive (to favor drift over standard depletion)
- **Bias limitation of 1-2V** drift voltage currently limits exploration of full potential of the scheme
- More aggressively cooled operation is planned for current prototype
- Recent process / thinning options with more advanced back side treatment might open new opportunities for future submissions

Backup slides

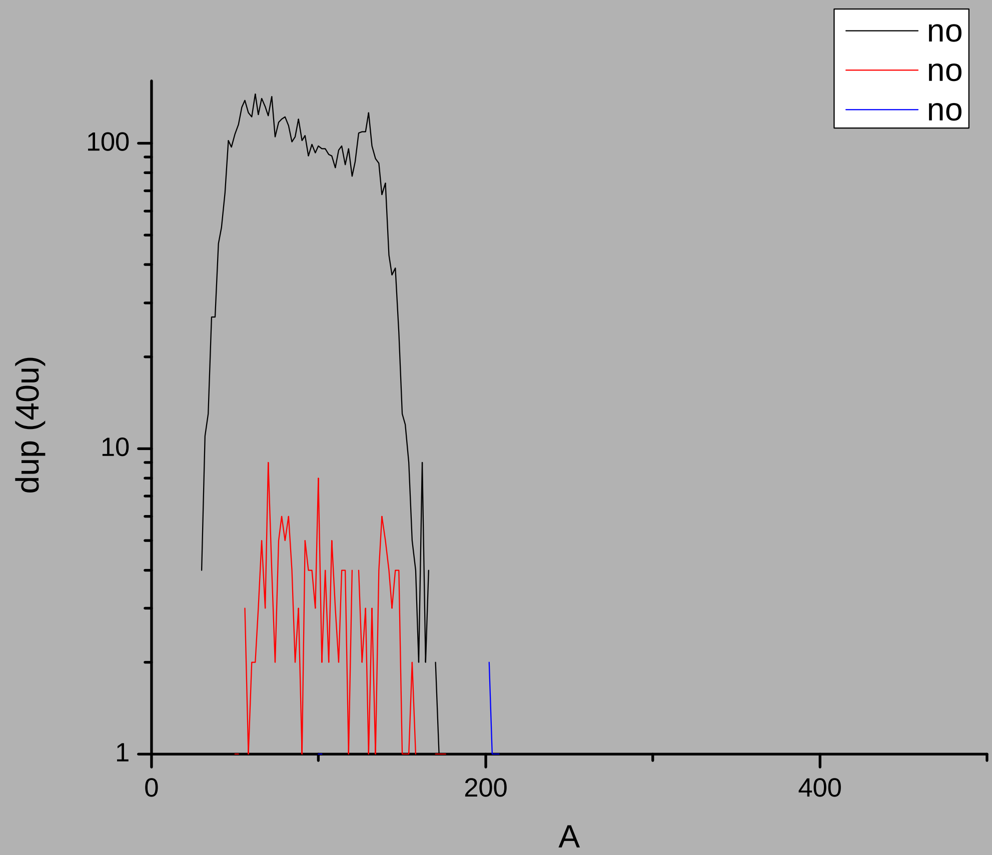


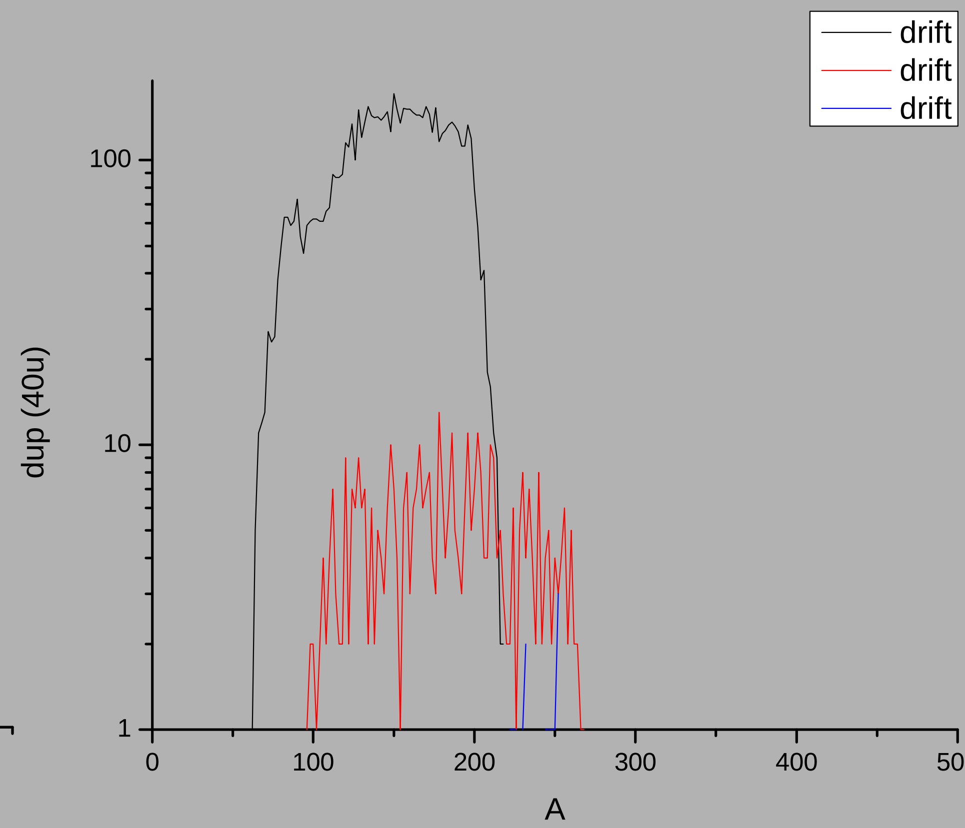
Cooling (15C), 4V Backside, Driftrings at 2V 1.5V

40u pixel -> backup

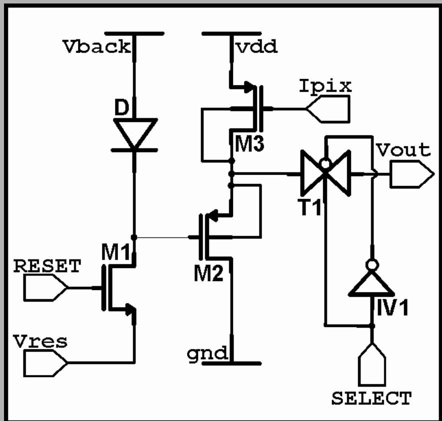


40u pixel -> backup



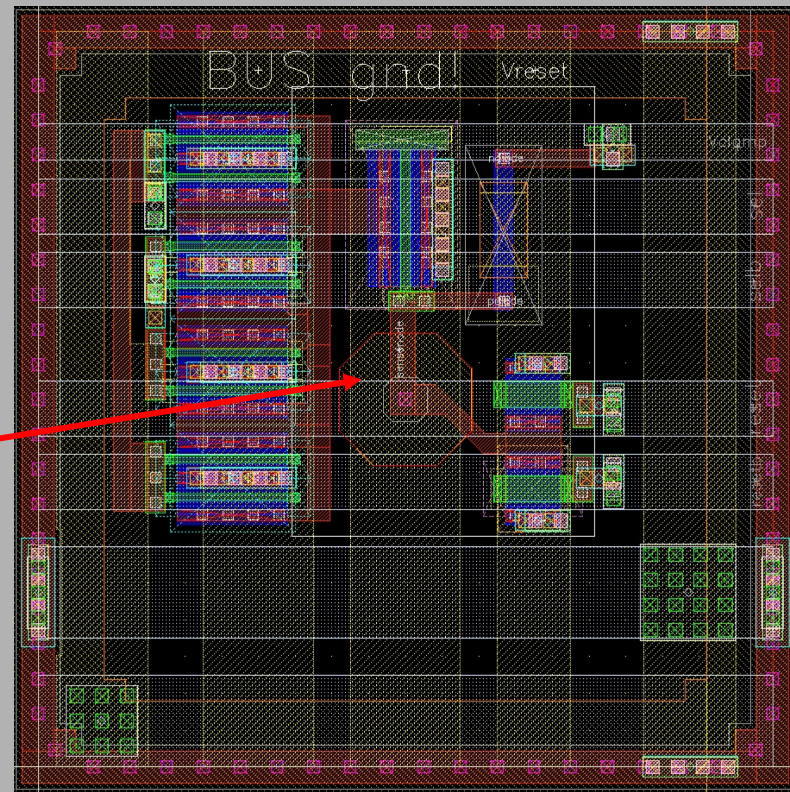


pixel architecture



3T-like pixel architecture

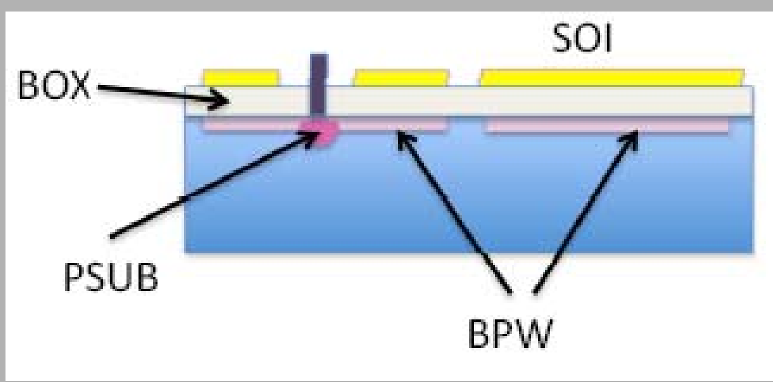
- emphasis on studying detector properties



20um

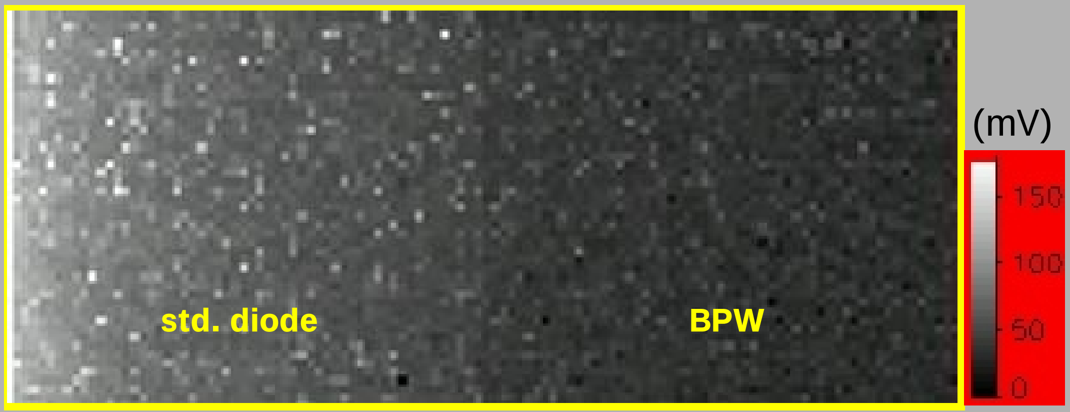
20um

- Use of BPW in one matrix to study effect on gain (capacitance) and leakage current
- However, BPW is of size of IMB, hence very small (no shielding purpose, study of capacitance only)



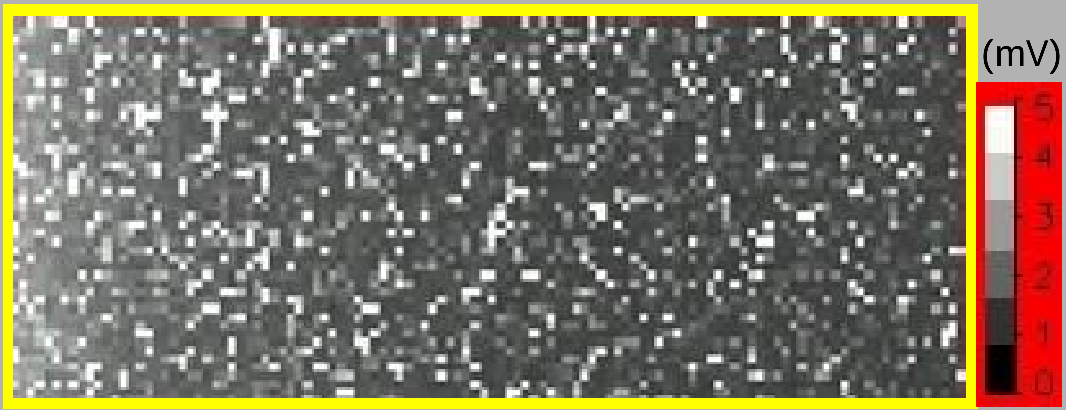
(preliminary) result using Fe^{55} source

Pedestal map



- Pedestal map shows difference of BPW and std. diode
- BPW more homogenous and less leakage

Noise map



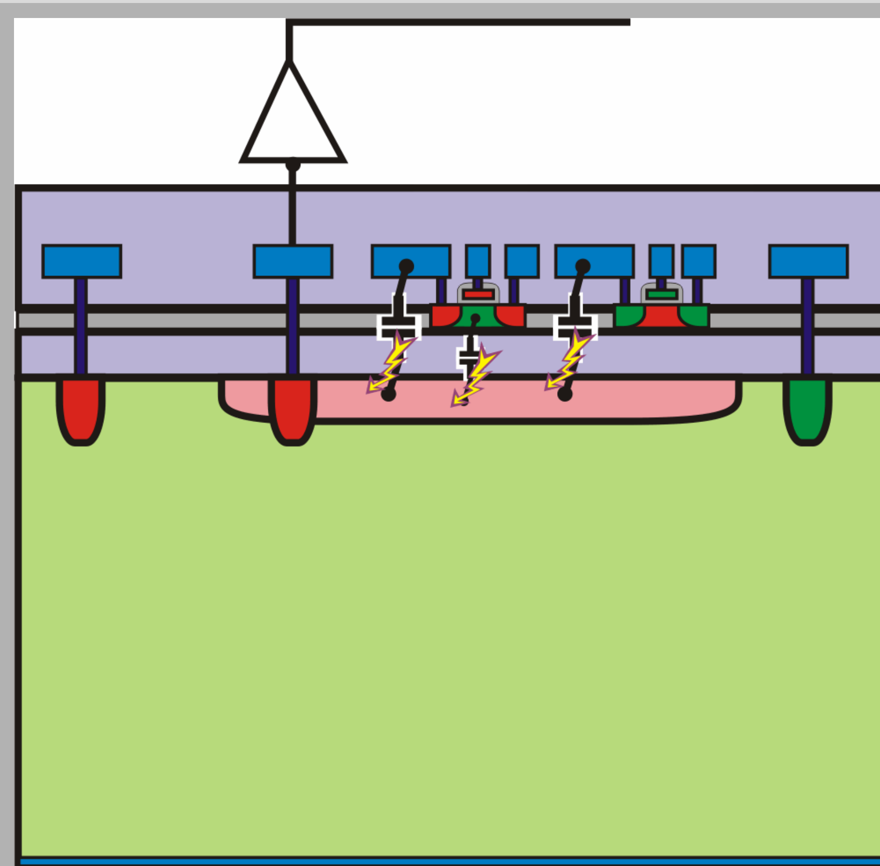
Mean Noise: ~44e-, (eq. ~2.2mV after amplification)

Review role of BPW in current OKI process

- **current process** features **BPW** to reduce back gate effect
- this can be used to shield transistors outside the pixel, e.g. at periphery
- **In pixel**, use of **BPW** as screening purpose **is dangerous** as it will make cross talk coupling stronger

-> limited use to cure back gate!!!!, worsening of cross talk effect

(note, BPW to reduce leakage and to decrease capacitance in pixel is still an interesting and attractive feature)



BPW over PSUB in pixel offers ideal platform for direct/strong coupling into the collecting diode is not bringing any good inside pixels,
direct coupling paths sending all transient interferences to the input of an in-pixel amplifier, additionally multiple capacitive feedback paths are created that may lead to instability feedback chain