3D Technology Issues and On-going Developments at FNAL

Ray Yarema
Fermilab

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Overview

- First talk on 3D circuits for the ILC took place at the ILC Vertex meeting at Schloss Ringberg, Tegernsee, Germany in May of 2006.[1]
- This talk will present some of the highlights from the meeting on Vertical Integration Technologies for HEP and Imaging which took place at Schloss Ringberg April 7-9, 2008.
- The talk will be supplemented with additional information where appropriate.
- Most of the talk will focus on 3D activities at Fermilab.
- 3D activities related to the ILC will be highlighted.

Vertical Integration Technologies for HEP and Imaging Meeting

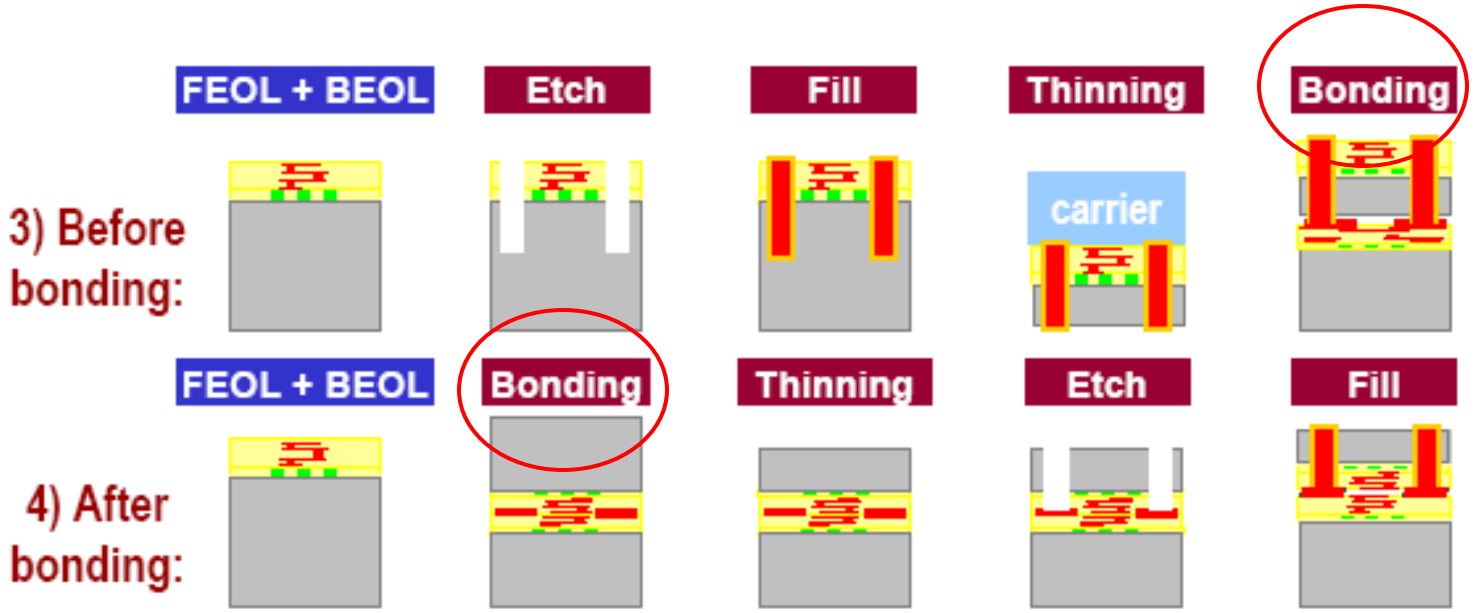
- The one clearly stated goal of this meeting was to develop a common platform for the R&D of vertically integrated pixel detector systems which would then provide the opportunity to share the experience and open new possibilities for the organization of common projects for the LHC and ILC.

Emerging 3D Programs

- One program, called DevDET FP7, has been proposed by a large number of institutions in many countries[2]
  - There are many work packages included the proposal
  - One work package includes development of 3D integrated circuits
  - Numerous R&D steps are outlined to develop a 3D circuit
  - The proposal focuses on a "Via last" approach
- Another program was described that uses a commercial vendor[3]
  - Minimizes 3D development issues by HEP groups
  - Offers the ability develop 3D circuits quickly and at low cost.
  - The approach focuses on a "Via first" approach

Via Last Approach

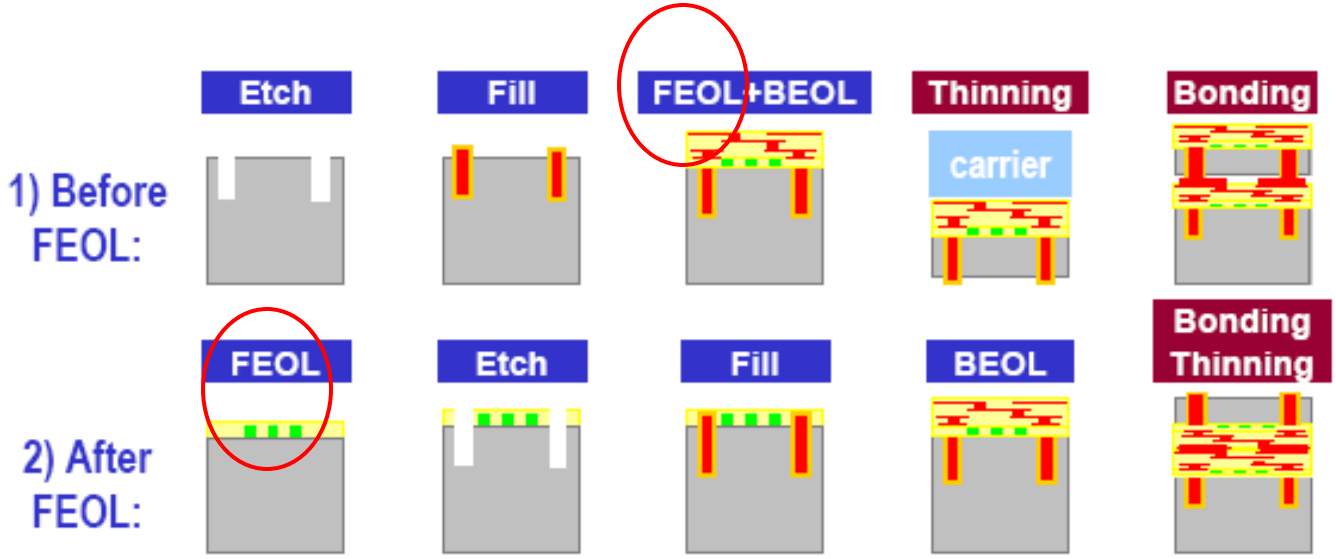
- Via last approach occurs after wafer fabrication and either before or after wafer bonding [4]



Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

Via First Approach

- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing [4]



IBM, NEC, Elpida, OKI, Tohoku, DALSA….

Tezzaron, Ziptronix Chartered, TSMC, RPI, IMEC……..

DevDET FP7 Work Package 3

- 3.1 – microelectronics technology and enabling tools.
- 3.2 – shareable IP blocks for HEP
- 3.3 – 3D interconnection of microelectronics and semiconductor detectors
  - Step 1 – design and production of test and prototype ASICs for 3D R&D in a MPW run with access to full wafers.
  - Step 2 – Production of sensors to be used for 3D R&D.
  - Step 3 – Prestudies including interconnection of special dummy test structures, wafer thinning, and via formation.
  - Step 4 – Interconnection of a pixel sensor to one ASIC layer
  - Step 5 – Sensor to single wafer and ASIC to ASIC interconnection with vias.
  - Step 6 – Full demonstrator with interconnection of sensor to two layers of ASICs
  - Requested funding = 1.2 million Euros over 4 years for development of 3D (not funded yet)

Technology Breakdown

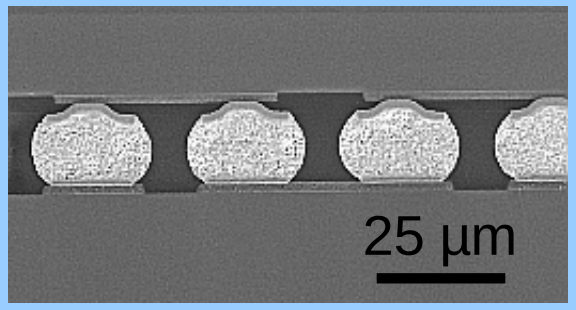
- The DevDET 3D fabrication can be thought of in two parts
  - Development of 3D integrated circuit
    - Via formation
    - Bonding of ASIC layers together
  - Development of 3D bonding to a separate sensor
  - Note – the bonding technology for the 2 parts listed above can be the same or different.
- The bonding technology being pursued for both parts in DevDET FP7 is called Solid Liquid Inter Diffusion (SLID)
  - Based on a CuSn eutectic solder bond
  - Recently Fermilab has completed a study on CuSn bonding

Fermilab Study of CuSn Bonding

- Goal of project was to demonstrate a bump bonding process compatible with pixilated devices having a 20 micron I/O pitch.
- Phase 1 completed –design and fabrication of passive test structures based on 50 um I/O pitch used on ATLAS and BTEV pixel sensors, but using bumps compatible with 20 um pitch.
  - Tests with PbSn solder bumps
  - Tests with CuSn solder bumps
- Work done in collaboration with RTI in North Carolina.

Bump Bond Comparison

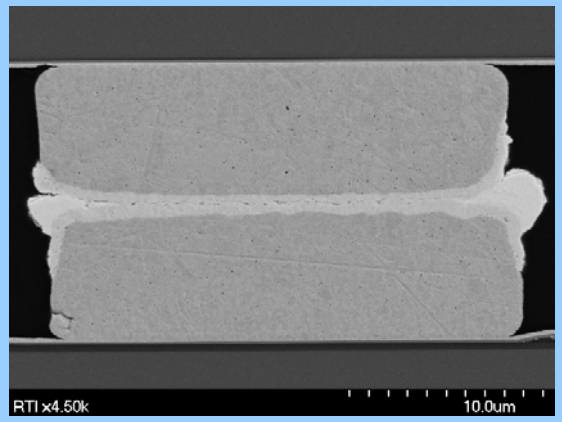
SnPb (60/40) Bump Bonds



25 µm solder bumps on 50 µm pitch, fabricated at RTI

- Currently used for pixilated detector devices
- Demonstrated pitches of 50 mm with >99.9% yields in area arrays of >16K bonds
- Self-aligning
- Bond density limit?

Cu-Sn Bump Bonds



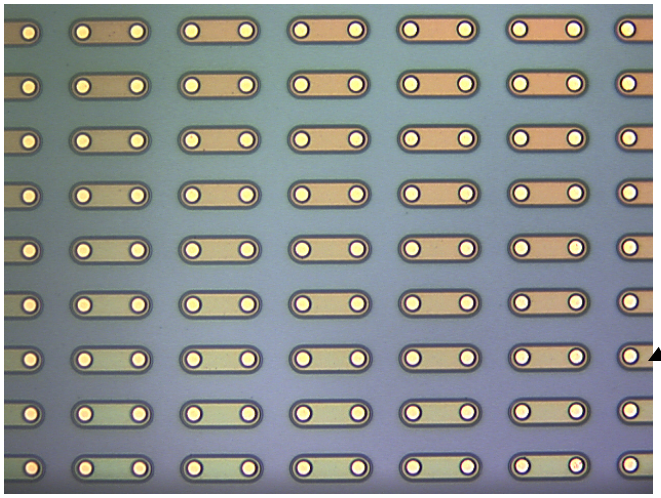
25 µm Cu-Sn bump bond, fabricated at RTI

- Technology at R&D stage
- Yields for large area array interconnects?
- No obvious density limit
- Misalignment tolerance?

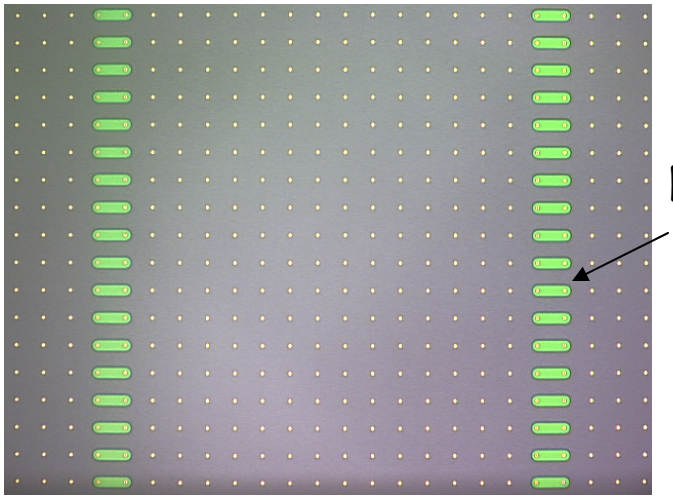
Test Structure Design and Tests

- Full array – 176 x 128 bump array (22528 bumps) on 50 um pitch in X and Y
- Device array to simulate 22 columns of 50 x 400 um pixels in 128 rows
- All bonding done chip to chip.
- Measure resistance and yield of contacts using daisy chains.
- Perform die shear tests to determine failure strength of the arrays.

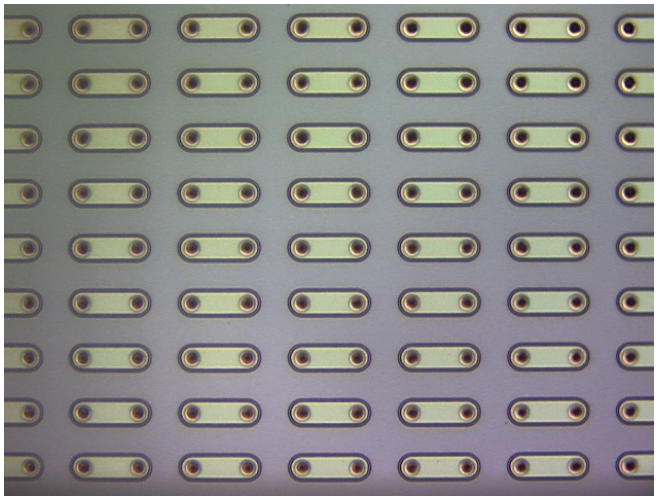
Test Structure Layout



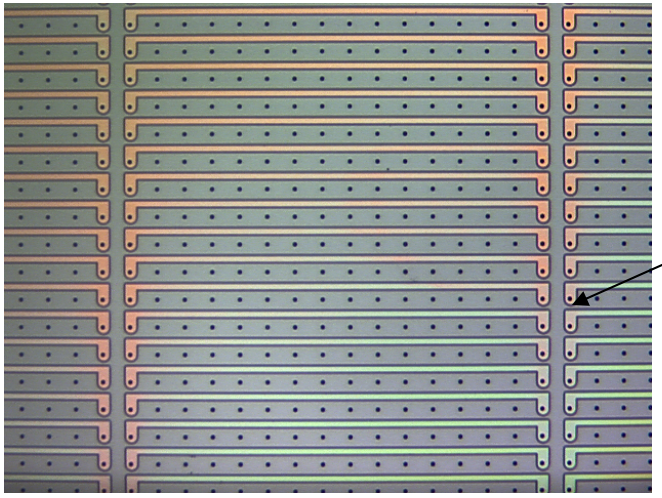
Cu pillar



Ni/Au



CuSn pillar



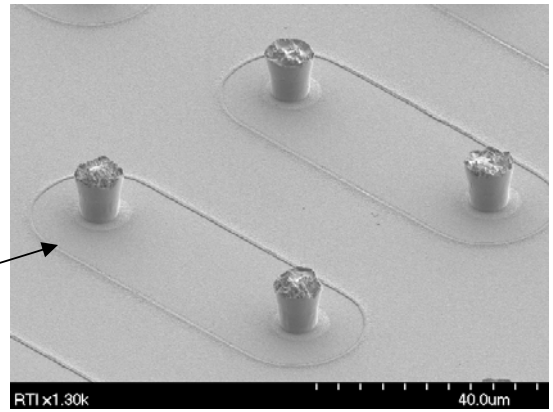
PbSn ball

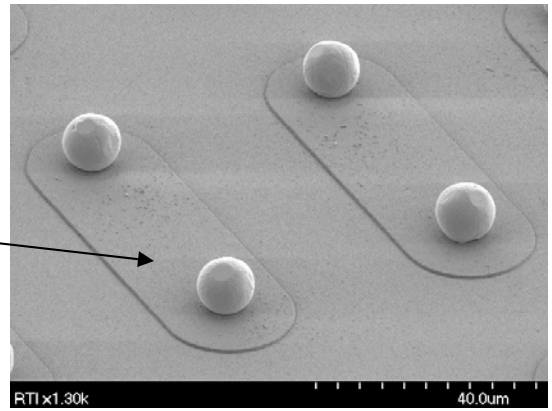
Full Array with CuSn

Device Array with PbSn

SEM of bumps Before Bonding

- Tests performed
  - 7 um CuSn pillar to 11 and 15 um Cu pillars
  - 10 um dia PbSn balls

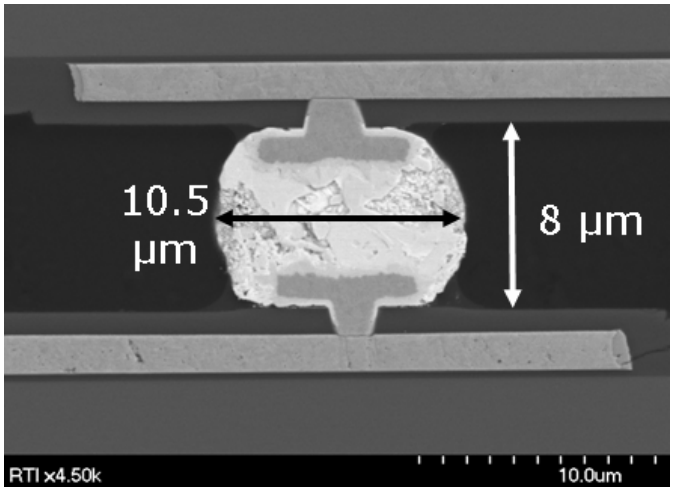




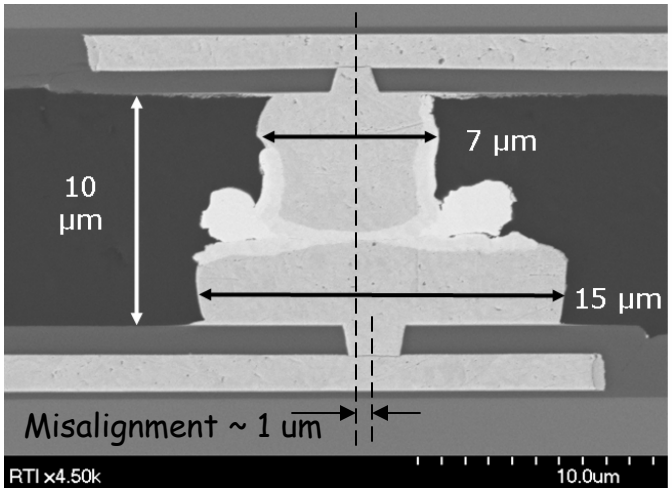
SEM of Bond Connections

- Bond yield of 10 um PbSn balls– poor
- Bond yield of 7 um CuSn on 15 um Cu pad was 99.995%
- Bond yield of 7 um CuSn on 11 um Cu pad was 99.995%
- All CuSn bonded chips (11 & 15um Cu pads) had die shear strengths greater than the strongest PbSn bonded chip.
- Initial tests indicate better yield than for previous HEP hybrid assemblies at RTI using solder bumps.
- Interconnect resistance 10~27 milliohms

PbSn bond



CuSn Bond



Bonding Comments

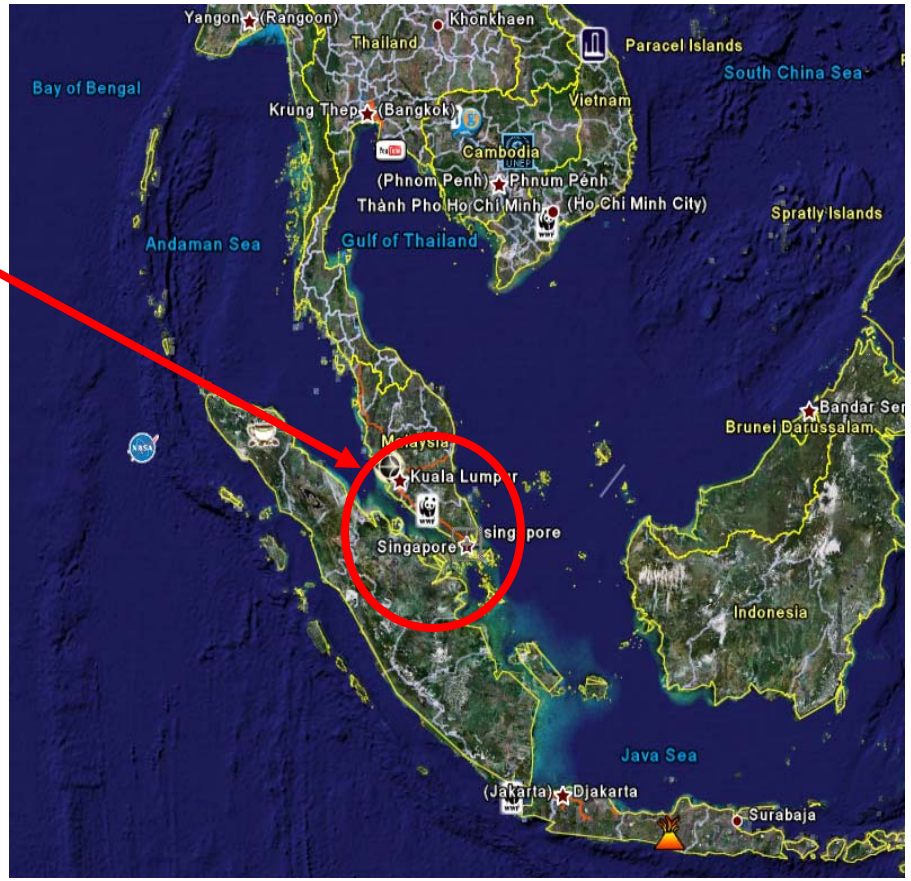
- Fermilab has shown that CuSn bonding can be used for fine pitch (20 um) assembly of 3D circuits.
- Both PbSn and CuSn bonds can have significant mass and represent a high Xo for fine pitch assemblies or high density interconnects.
- CuSn bonding is perhaps better suited to bonding of 3D ASICs to detectors where interconnect density is lower than bonding of ASIC tiers together.

A Program to Use Commercial 3D Vendors

- There are 3 vendors that I know have commercially available (external) 3D processes.
  - Tezzaron – uses CuCu thermocompression for bonding
  - Ziptronix- uses Direct Bond Interconnect (oxide bonding)
  - Zycube – uses adhesive and In-Au bumps for bonding
- Fermilab is working with Tezzaron to fabricate 3D integrated circuits using CuCu bonding.
  - Others developing CuCu bonding include IBM, RPI, MIT
- Fermilab is working with Ziptronix to do low mass bonding with DBI to detectors. (FPIX chips to 50 um thick sensors.)

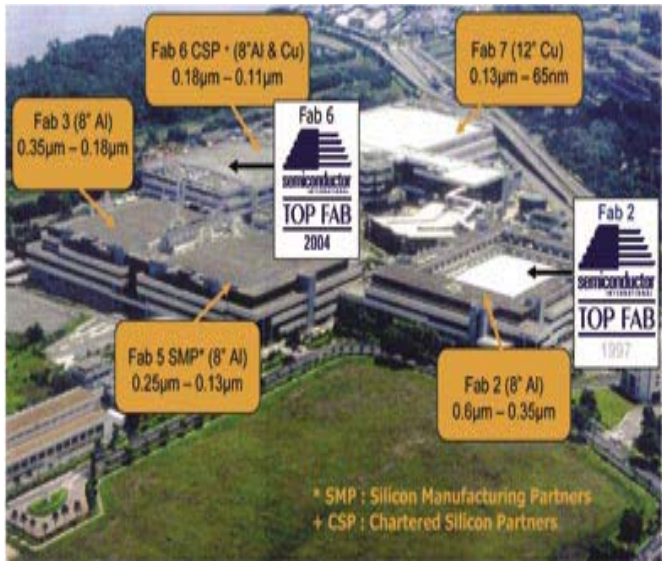
Tezzaron Background

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



Chartered Semiconductor

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Extension to 300mm wafers and 45nm TSVs underway
- Chartered 0.13 um process has different layer arrangement and transistor thresholds than IBM process.
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic

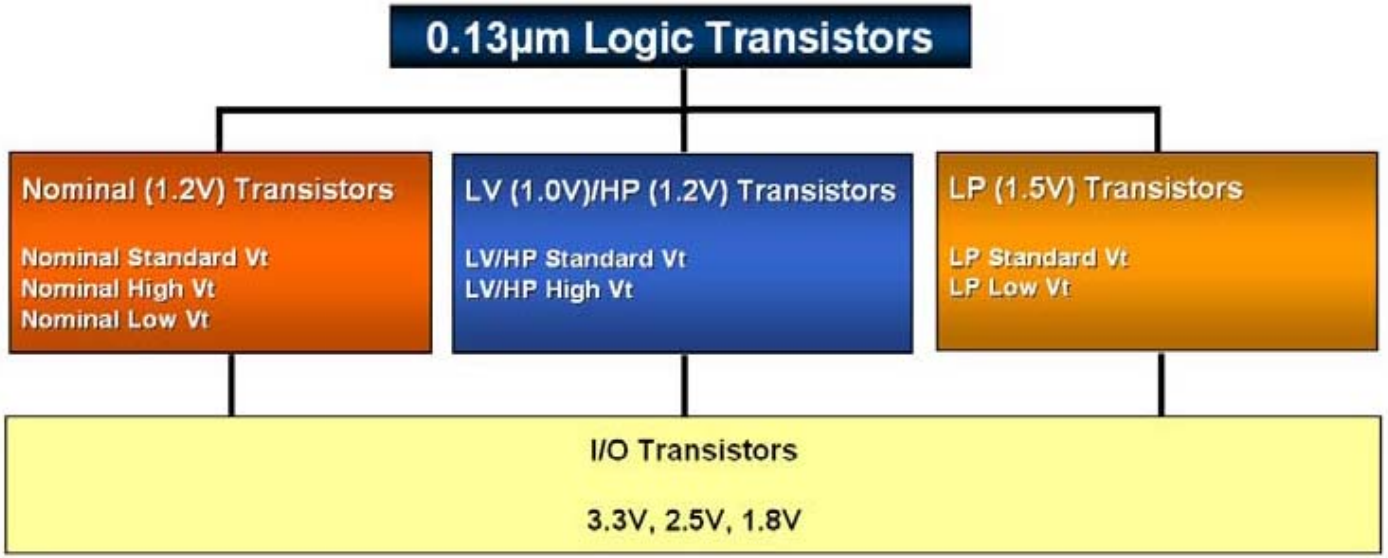


Chartered Campus

Chartered 0.13 um Process

- 8 inch wafers
- Large reticule – 24 mm x 32 mm
- Features
  - Deep N-well
  - MiM capacitors – 1 fF/um^2
  - Reticule size 24 x 32 mm
  - Single poly
  - 8 levels of metal
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously
    - Nominal
    - Low voltage
    - High performance
    - Low power

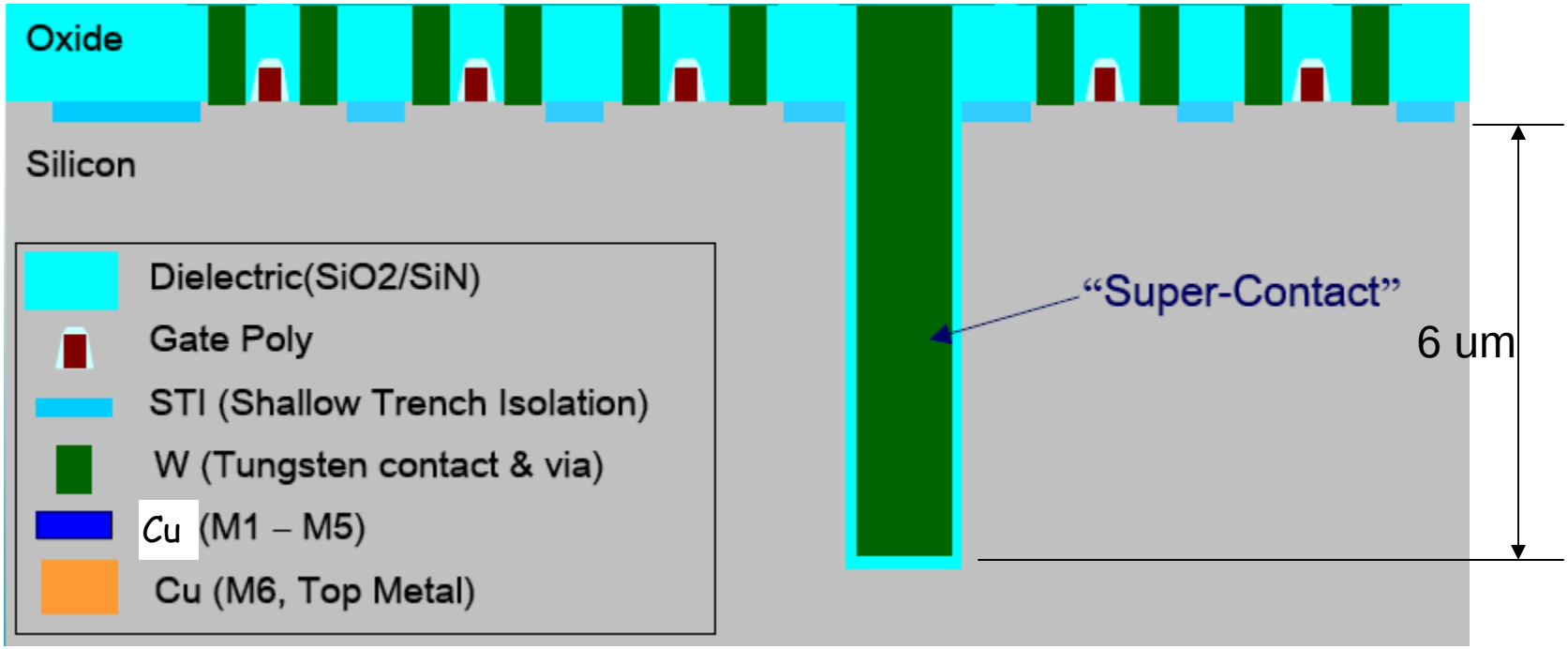
Chartered Transistor Options



Choose one of three processes and one of three I/O transistors types

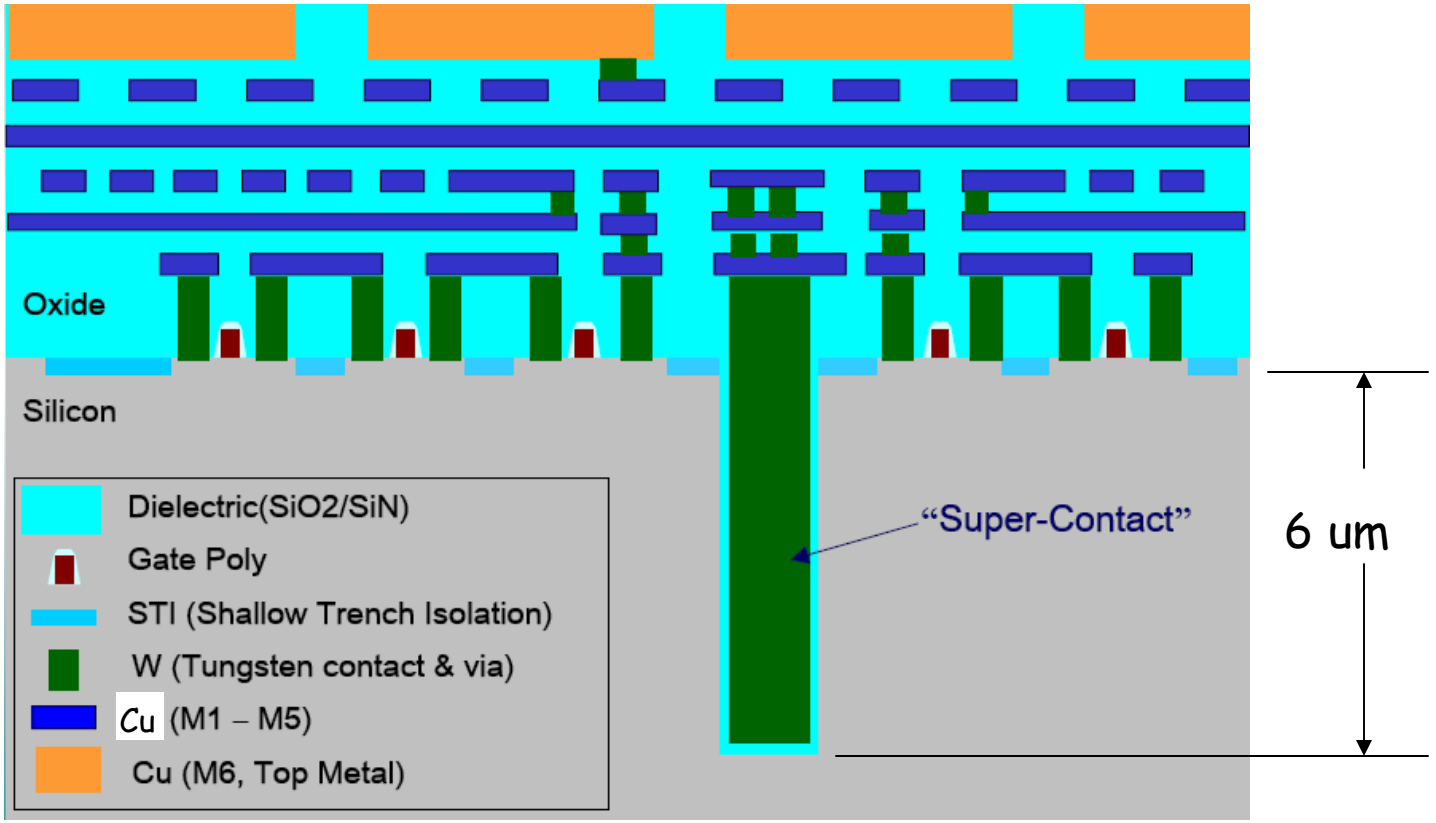
Tezzaron 3D Process[5]

- Complete transistor fabrication on all wafers to be stacked
- Form super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors



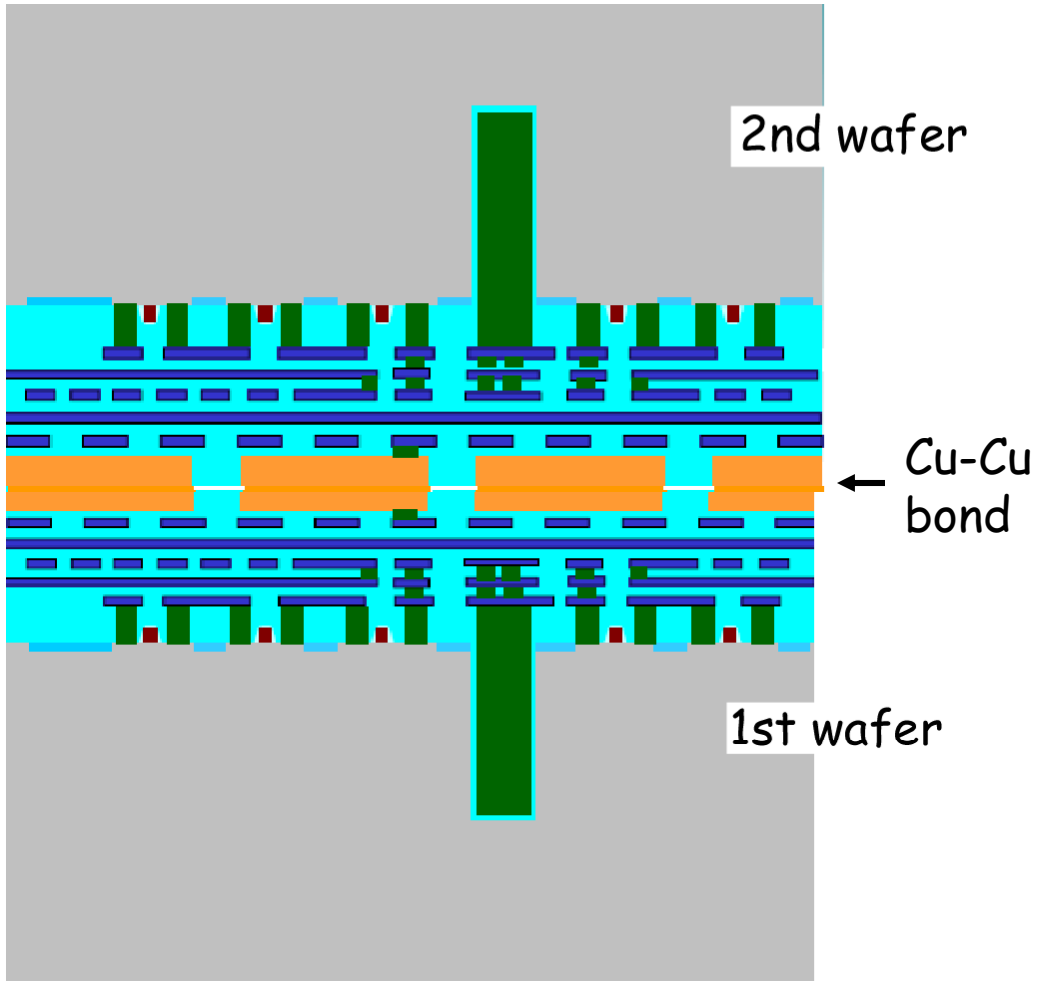
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Cu metal layers and top Cu metal (0.8 um)



Tezzaron 3D Process

- Bond second wafer to first wafer using Cu-Cu thermo-compression bond

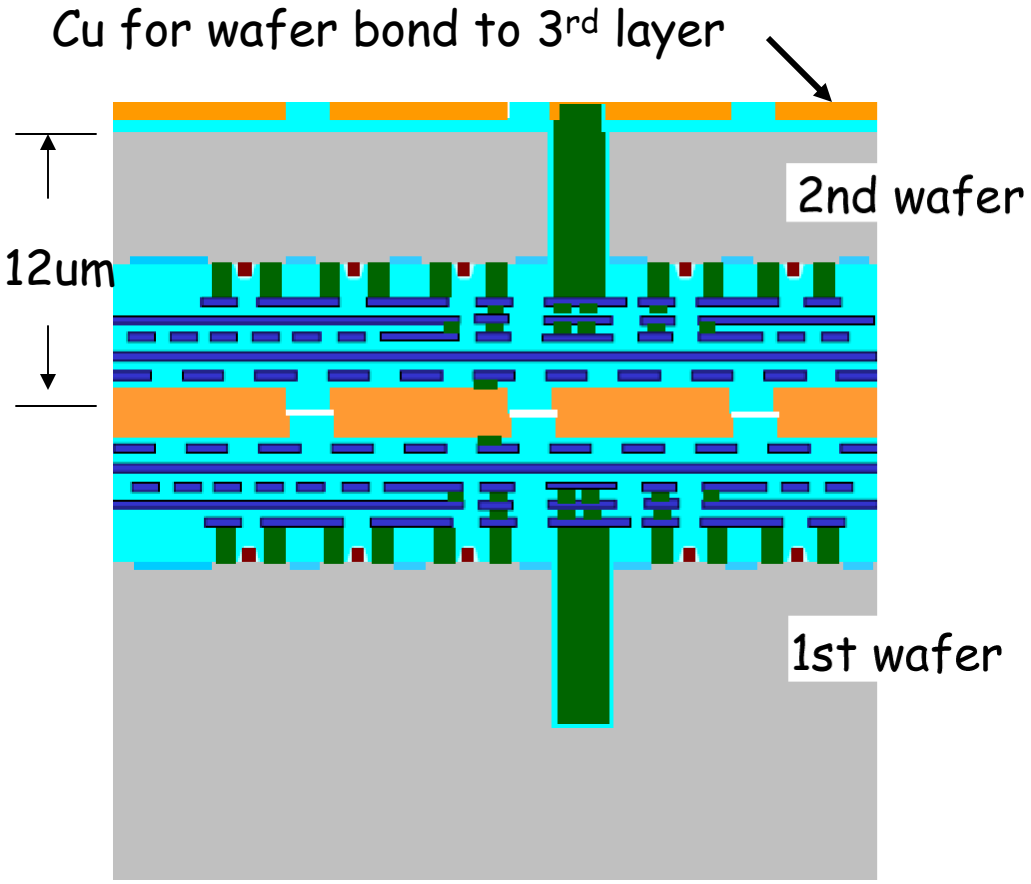


Tezzaron 3D Process

- Thin the second wafer to about 12 um total thickness to expose super via.
- Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer

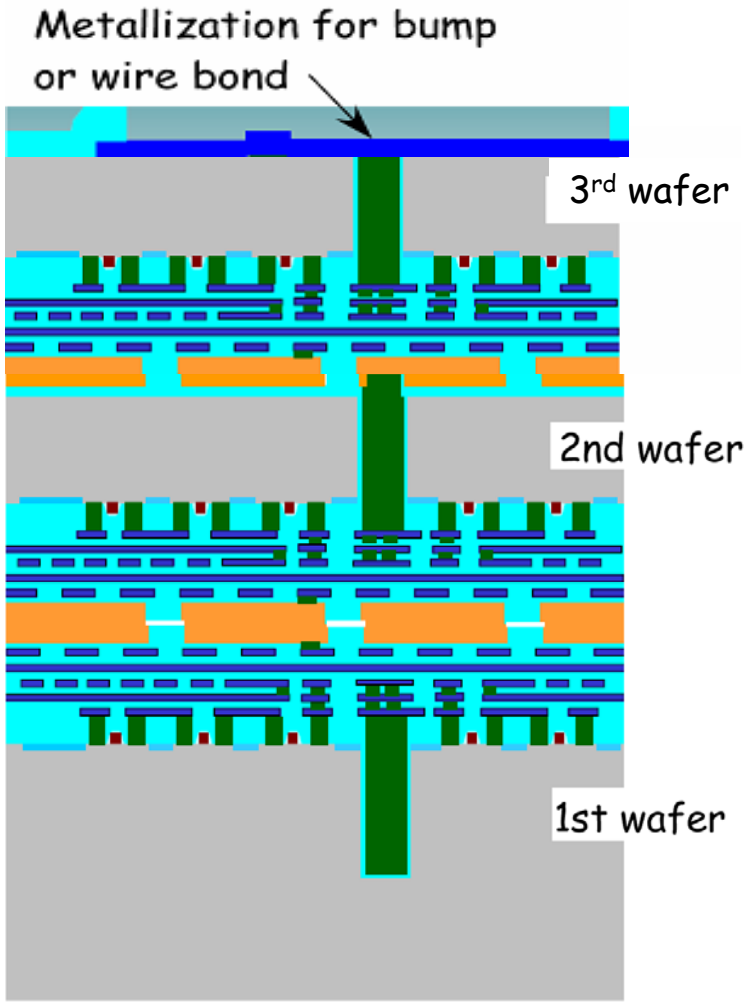
  OR

  add metallization on back of 2nd wafer for bump bond or wire bond.

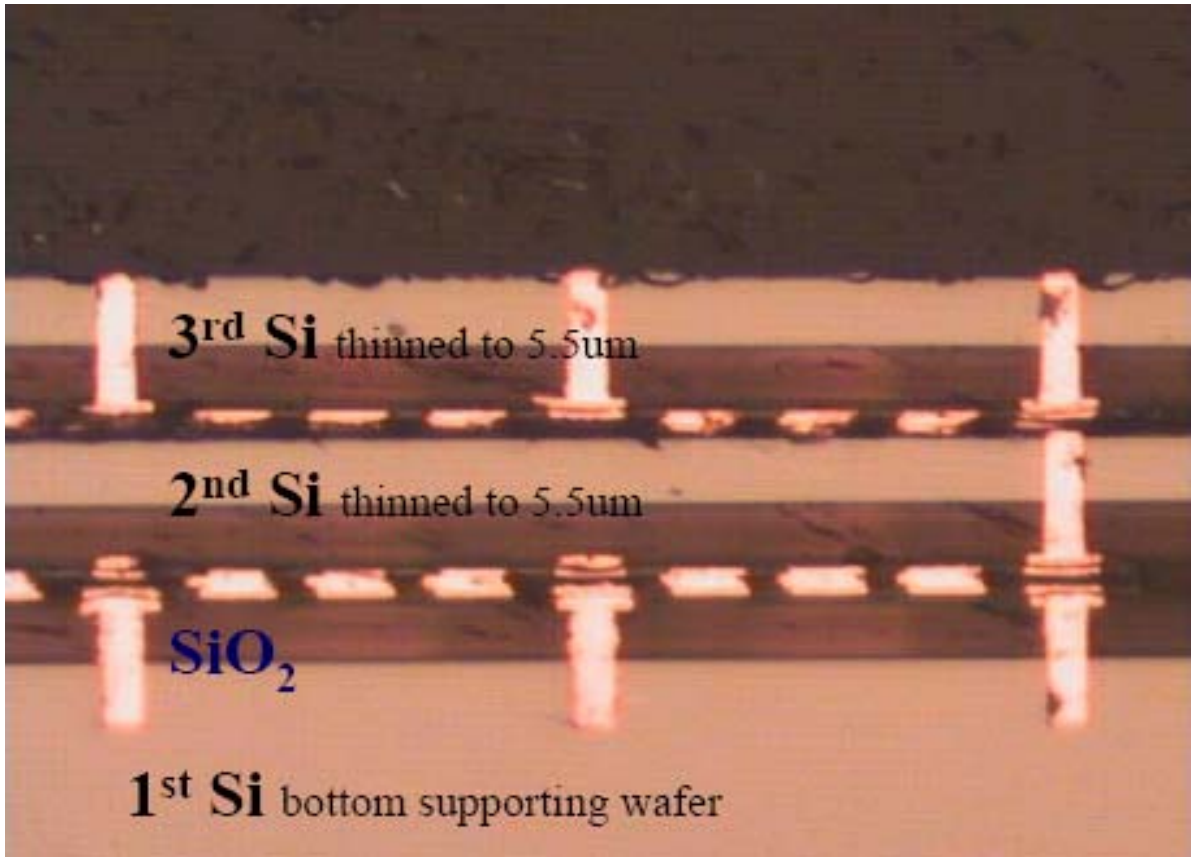


Tezzaron 3D Process

- Stack 3rd wafer
- Thin 3rd wafer (course and fine grind to 20 um and finish with CMP to expose W filled vias)
- Add final passivation and metal for bond pads

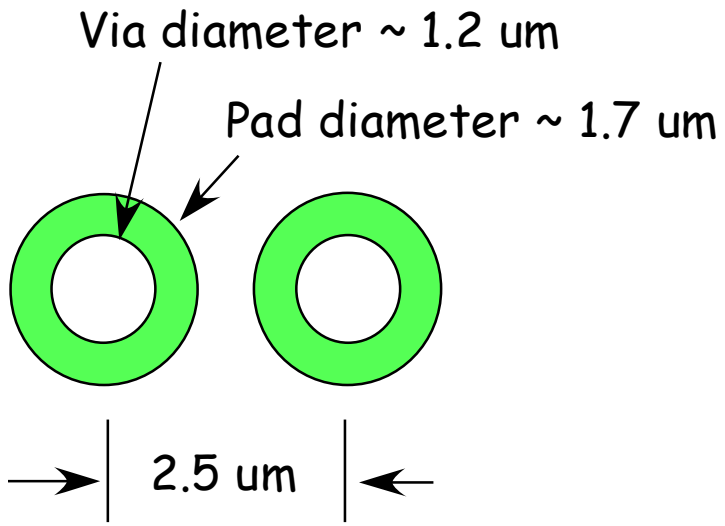


Cross section of Tezzaron 3 layer Stack[5]



Tezzaron vias

- Via size plays an important role in high density pixel arrays
- Tezzaron can place vias very close together

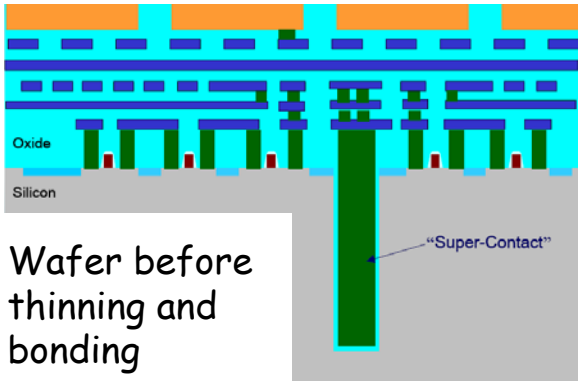


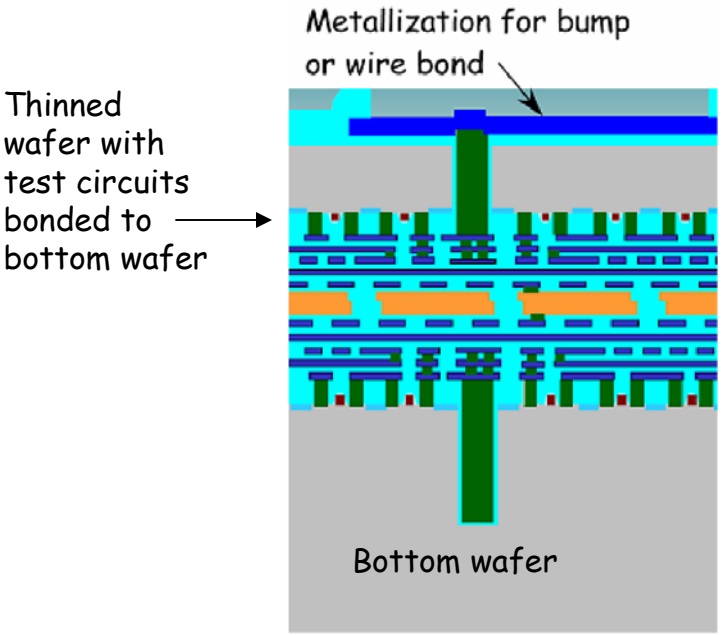
Wafer Bonding

- Bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 um
- Missing bond connections = 0.1 PPM
- Temp cycling of bonds from -65 to + 150 C
  - 100 devices, 1500 cycles, 2 lots, no failures

Circuit Performance

- Circuits tested with full substrate thickness and then after bonding and thinning to 12 um
  - No change in performance between thinned and bonded devices and unthinned/unbonded devices.
    - Bandgap circuit
    - Sense Amplifier
    - Charge pump
  - No change in performance between thinned and bonded devices before and after temperature cycling.
- Transistor measurements on same devices before and after thinning and bonding are shown on the next slide.
  - No noticeable difference in characteristics except small increase in PMOS speed due to strain in silicon as expected





Transistor Performance for Thinned and Bonded Wafers[5]

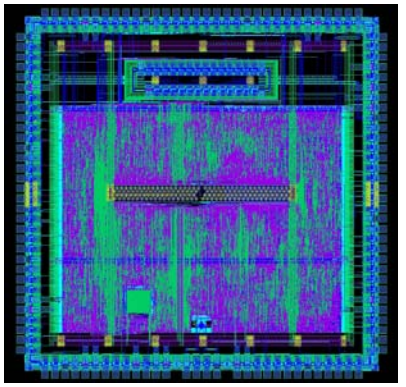
	Threshold Voltage VT0 (V)						Saturation Current Idsat (uA) (Vd= Vg=1.2V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	0.395	0.485	0.479	-0.355	-0.399	-0.398	122.520	5152.000	9696.000	26.940	2061.800	5986.200
Post Ave	0.393	0.484	0.465	-0.357	-0.396	-0.404	121.500	5094.333	9840.333	26.897	1997.333	4473.000

	Breakdown Voltage BVDSS (V) (Ids=2uA)						Leakage Current Ioff (pA) (V=1.4V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	3.380	3.220	3.220	4.100	4.000	2.780	151.820	638.900	3655.000	136.460	1285.120	282050.000
Post Ave	3.377	3.230	3.217	4.147	3.970	3.113	140.433	433.667	3237.667	211.333	910.333	121680.000

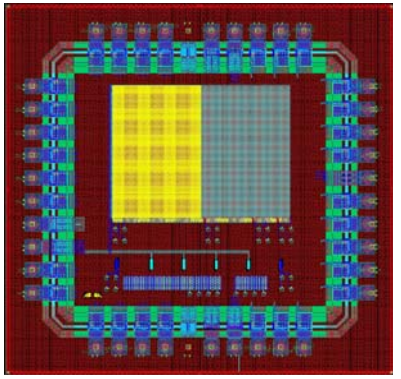
	Subthreshold Slope SUBSLP (mV/dec)						Gate Leakage Current GLEAK (nA)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	75.840	76.820	79.380	-73.040	-76.960	-89.460	1.200	1.172	1.190	0.909	0.883	0.886
Post Ave	74.367	76.100	78.567	-74.733	-76.833	-88.600	1.250	1.287	1.300	1.018	1.011	0.767

Tezzaron Chips

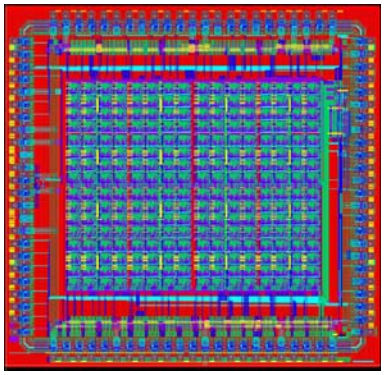
CPU and memory stack
- 80 MHz operation
- 220 MHz memory interface
- Synthesized, placed and routed in 3D with standard Cadence tools



CMOS sensor
- 5 different pixel fields
- Main array 160 x 120 pixels, 5 x 5 um pixels
- 2.4 um pitch interconnect
- 100% array efficiency
- Back side illumination



FPGA
- 12 vertical interconnects/logic block
- Shows tight 3D integration capability

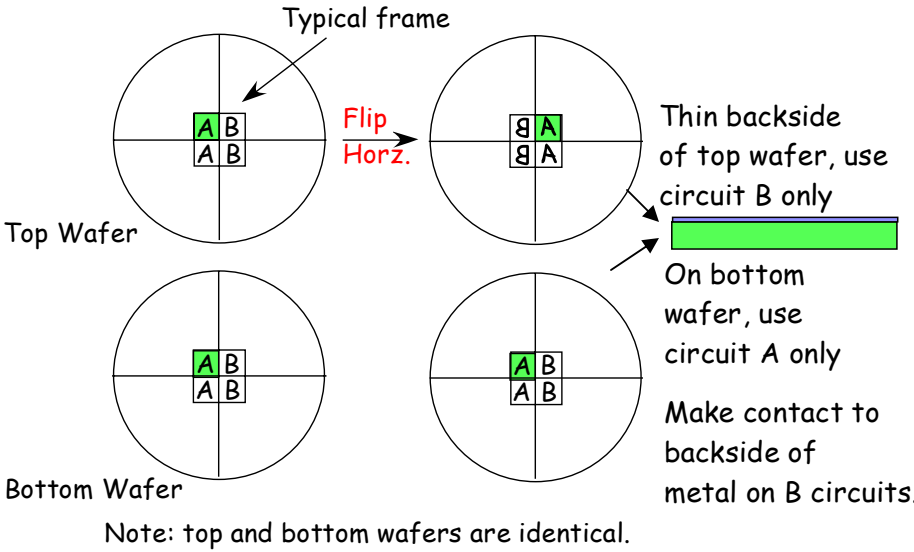


Advantages

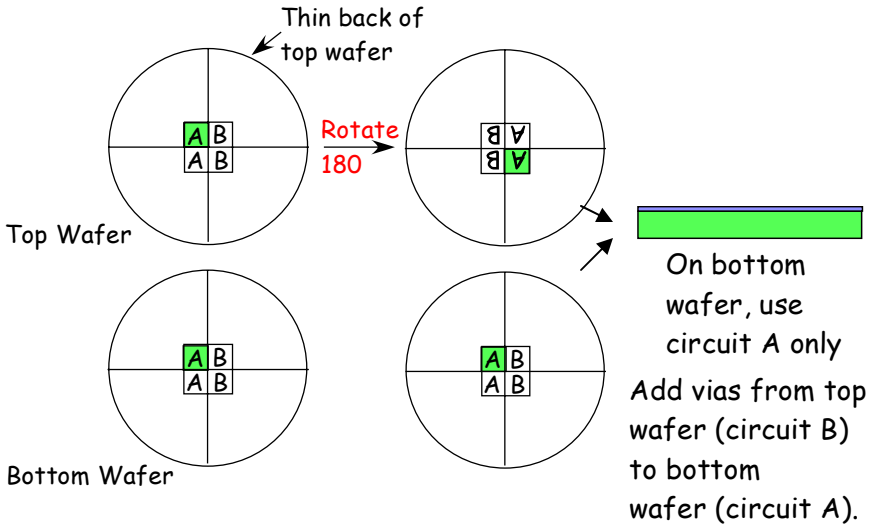
- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Good models available for Chartered transistors
- Thinned transistors have been characterized
- Process supported by commercial tools and vendors
- Fast assembly
- Lower cost

Fermilab 3D Multi-Project Run

- Fermilab will be submitting a 3D multi project run using Tezzaron.
- There will be only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 16 x 24 mm)
- The wafers will be bonded face to face.
- Bond pads will be fabricated for bump bonding to be done later at Ziptronix



Face to Face Bonding



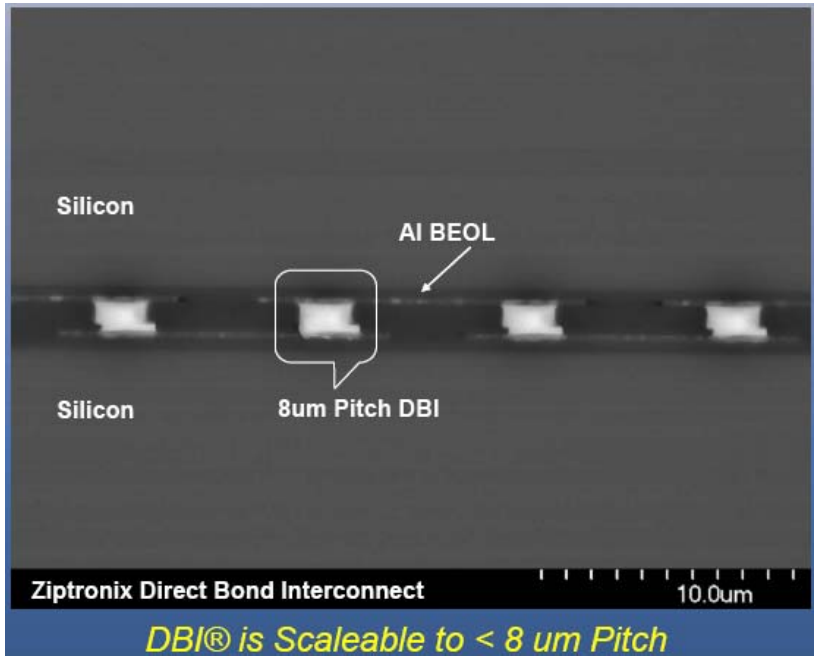
Back to Face Bonding

Cost/Delivery

- We expect to receive 12 fully processed 3 D wafers (made from 25 eight inch wafers).
- We expect the total cost to be less than $250K (~150K Euro)
- We expect delivery to be approximately 12 weeks after delivery of the loaded reticule to Tezzaron.
- Other HEP groups have been invited to join the MPW run.

Ziptronix

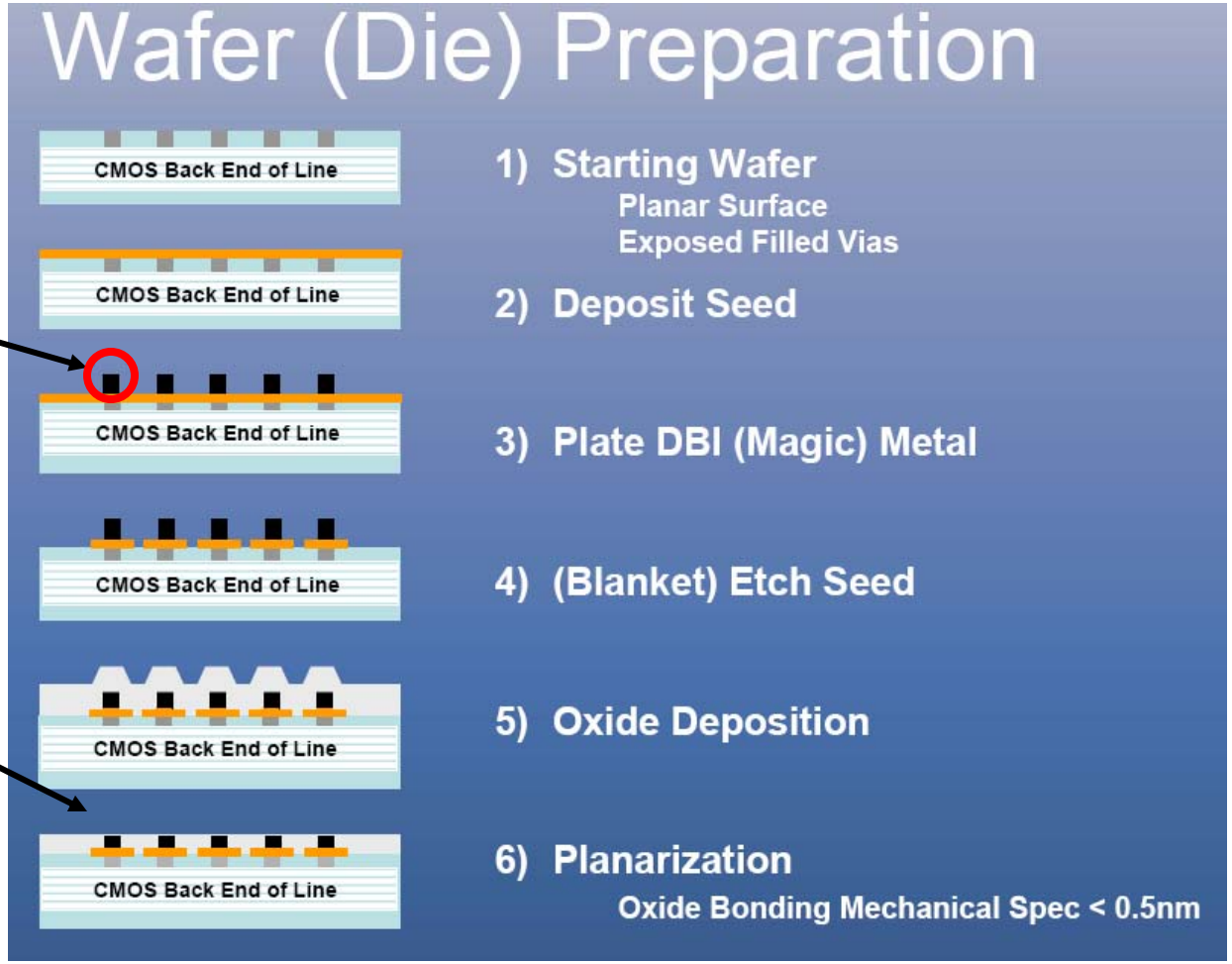
- Some parts received from Tezzaron will be bonded to sensors.
- Fermilab sensors are being made at MIT LL.
- Some 3D bond processes introduce significant material between bonded layers.
  - Conventional solder bumps or CuSn can pose a problem for low mass fine pitch assemblies
- IC bonding to a detector will be done by Ziptronix using the Direct Bond Interconnect (DBI) process.[6]
  - Xo < 0.001%
- Tezzaron and Ziptronix have formed an alliance.
  - Good communication between companies for pad metallization for sensor bonding, etc. now exists.



- Ziptronix is located in North Carolina
- Fermilab has current project with Ziptronix to bond BTEV FPIX chips to 50 um thick sensors.
- Orders accepted from international customers

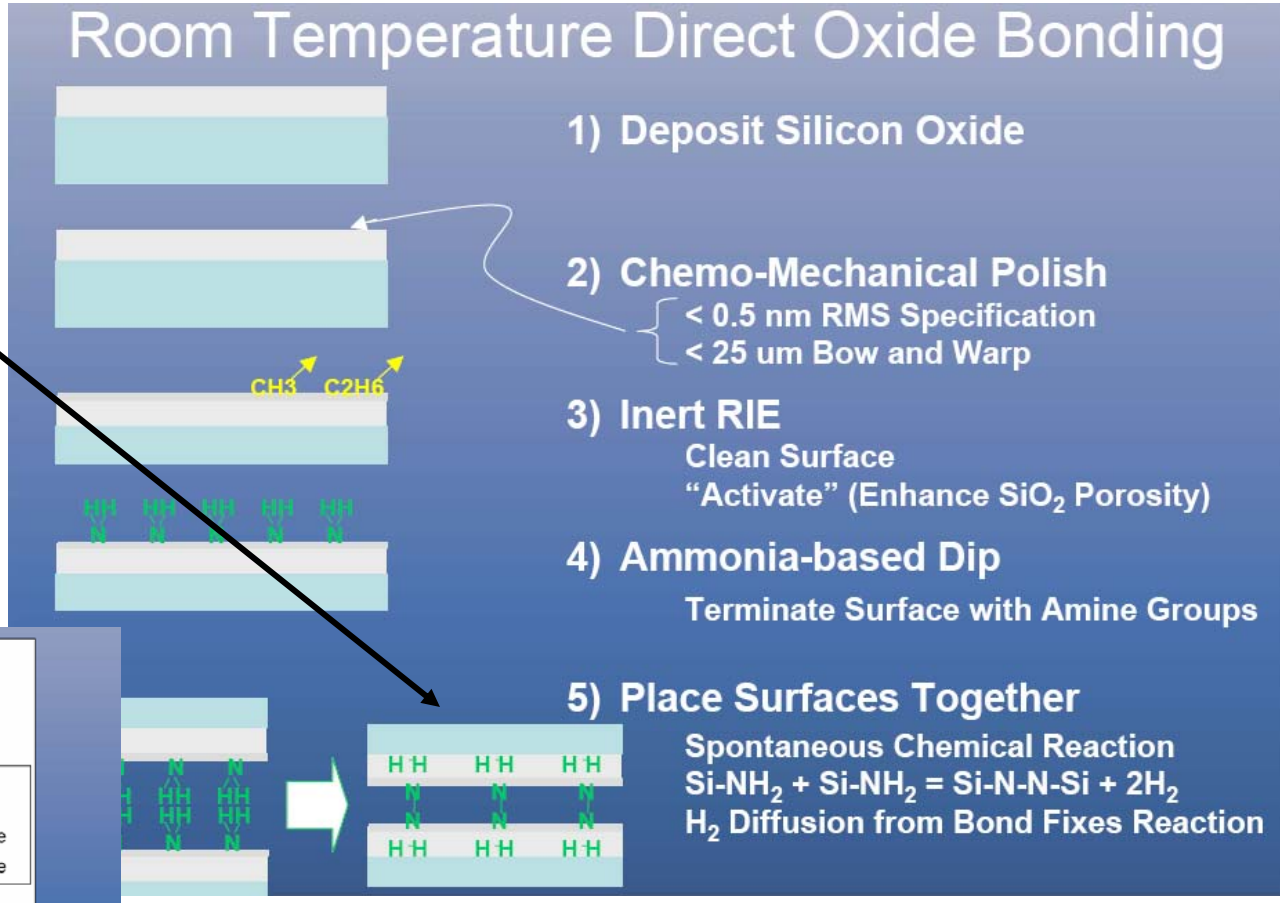
DBI Process

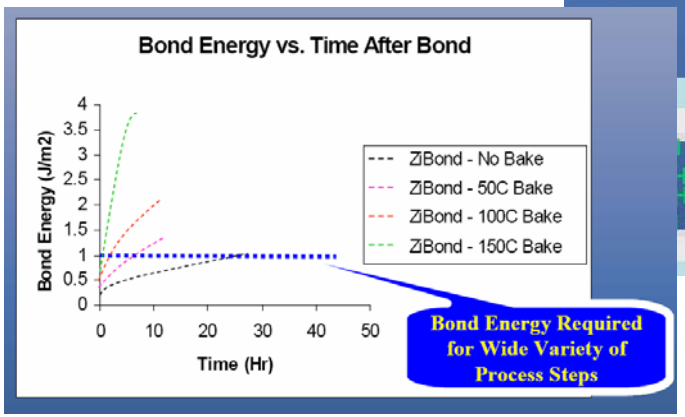
- Add Magic metal for electrical connections
- Prepare surface for oxide bonding



Oxide Bonding

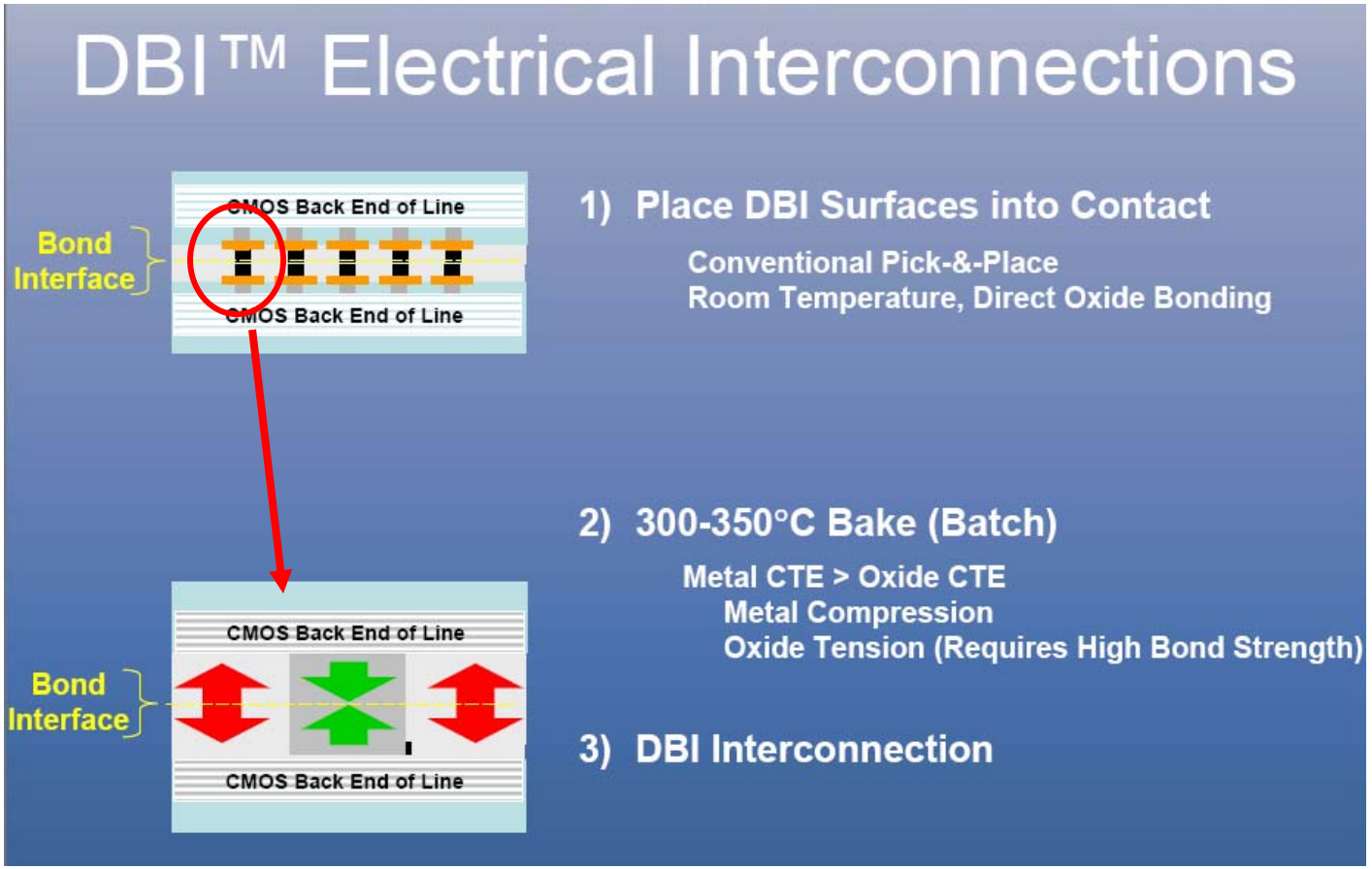
- Surfaces bond immediately due to Van der Waals force.
- Bonding occurs at room temperature
- Bond strength increase with time





DBI Electrical Connections

- After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.

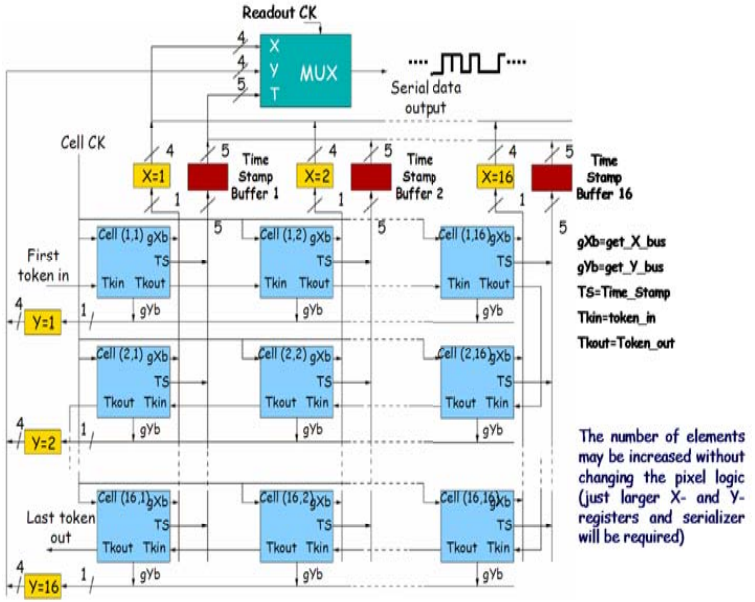


Collaboration Forming

- Fermilab is leading an effort to develop 3D integrated circuits through an MPW run at Tezzaron
- Recently 4 French laboratories have received funding (200 K Euros) to perform 3D electronics development
  - Strasbourg - IPHC
  - Orsay - LAL
  - Paris - LPNHE
  - Marseille - CPPM
  - Received LOI from CNRS/In2P3 to join Fermilab MPW run
- INFN has received 300K Euros for study of MAPS, including 3D circuit design
  - Received LOI from Universita di Bergamo to join Fermilab MPW run
- Other groups have expressed interest but have not made a commitment as yet.

ILC Projects in Tezzaron MPW Run

- Marc Winter (Strasbourg) is intending to work with Fermilab to develop a simple 3D MAPS device with 7 bits of time stamping for the ILC.
- Valerio Re (Bergamo) has designed and built a MAPS device using a deep N-Well, for the ILC with sparsification and 5 bit time stamping.
  - Valerio will work with Fermilab to develop a 3D version of the chip to improve fill factor and pitch and to add features such as expanded time stamping and digitization of analog information



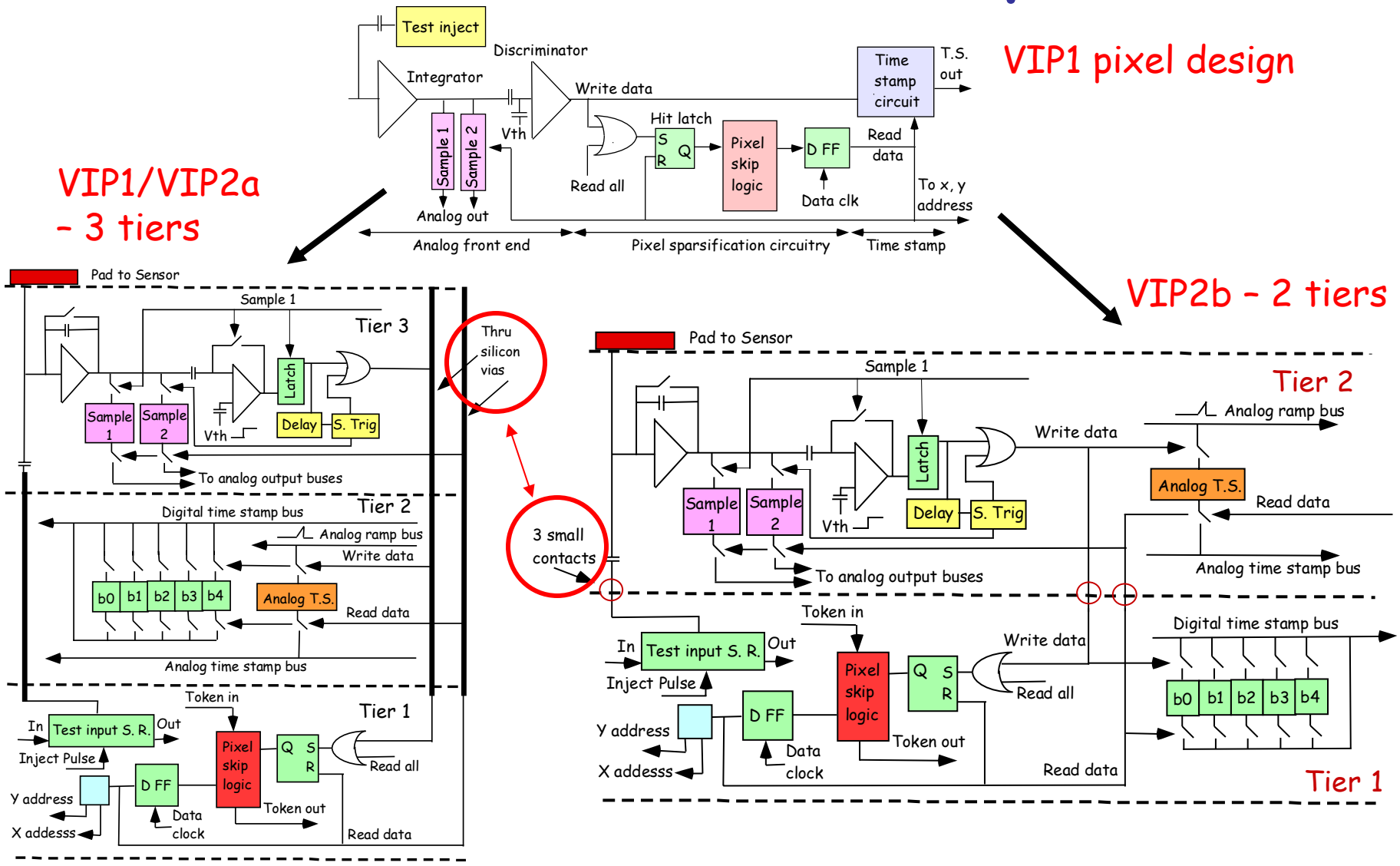
ILC Projects in Tezzaron MPW Run

- Fermilab has previously designed a 4K pixel chip called VIP1 in the MIT LL SOI process for the ILC vertex detector.
  - Features include 3 layers of electronics, sparsification (same readout architecture as Valerio), 10 bit time stamping capability, analog outputs, 20 um pixels.
  - Several problems have been discovered but chip tests are continuing
    - Backup lot being fabricated by MIT LL
  - New submission (VIP2a) to MIT LL in September
  - VIP 2b will be submitted to Tezzaron MPW run

VIP2b design at Tezzaron

- VIP2b design essentially the same as VIP2a.
- Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
- Radiation tolerance of Chartered 0.13 um process is currently being studied by another group.
- Going from 3 layers in 0.18 um technology to 2 layers in 0.13 um technology should reduce pixel size below 20 um.
- Using the via first process at Chartered eliminates the wasted area needed for vias in the MIT LL process.
- Chartered provides fully characterized process and models at commercial foundry along with standard cell libraries.
- VIP2b requires significantly less 3D processing than VIP2a

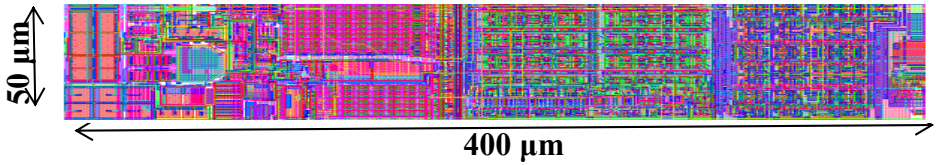
VIP2a and VIP2b Comparison



SLHC Projects in Tezzaron MPW Run

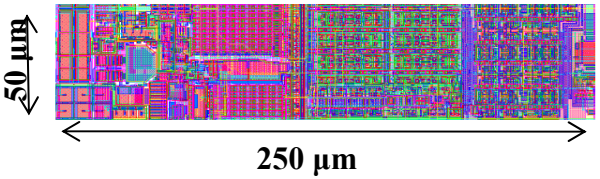
- Jean-Claude Clemens and Alexandre Rozanov (CPPM) have expressed interest in converting the current 0.25 um ATLAS pixel design to a 3D structure with 2 tiers in the Chartered 0.13 um process.[8]
- Fermilab intends to develop a 3D chip with 2 tiers of electronics to explore the advantages of 3D for the Super CMS pixel detector.
  - Going from 1 layer of circuitry in a 0.25um process to 2 layers in a 0.13 um process can increase circuit density by a factor of 7.
  - Circuit density can by traded for smaller pixel size.
  - Features to consider for parallel processing
    - In pixel digitization
    - Large digital storage
    - Triggering capability
    - Sparsification
    - Reduction of peripheral circuitry

Hybrid pixel detectors (Atlas exemple)[8]



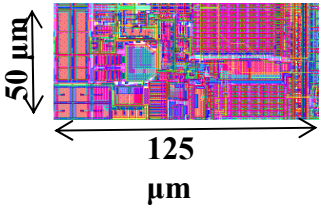
FE-I3 CMOS
250 nm

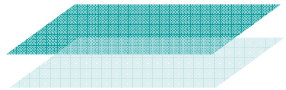
Done : ATLAS



FE-I4 CMOS
130 nm

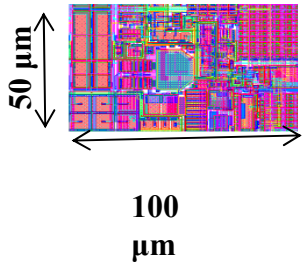
Design

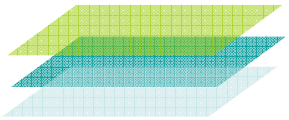




Drastic pixel dimension reduction (*cost effective compared to smallest technologies ?*)

Though





4 sides buttable structures

New mechanical possibilities

Dream ?

Summary

- The Vertical Integration Meeting at Schloss Ringberg brought together members of the HEP community interested in developing 3D electronics for advanced detector systems.
- Various 3D plans in Italy, France, Germany, and the United States were discussed.
- The proposal from Fermilab, to use commercial vendors, received considerable attention and is leading to a collaboration between various groups within HEP to explore the Tezzaron 3D process.
- Groups in Italy, France, and the United States will be designing chips in the Tezzaron 3D process for possible application in the ILC vertex detector.
- If all goes well, we could have 3D ILC chips back in about one year from now.

References

- 1) R. Yarema, *Fermilab Initiatives in 3D integrated Circuits and SOI Design for HEP*, ILC Vertex Workshop, Tegernsee, Germany, May 29-31, 2006
- 2) Hans-Gunther Moser, *3D Interconnection in the DevDET FP7*, Vertical Integration Technologies for HEP and Imaging, April 7-9, 2008, Tegernsee Germany.
- 3) R. Yarema, *3D Circuit Design at Fermilab*, Vertical Integration Technologies for HEP and Imaging, April 7-9, 2008, Tegernsee Germany
- 4) Steve Lassig, Lam Research Corporation, *Etch Challenges and Solutions for Moving 3-D IC to High Volume manufacturing*, 3D architectures for Semiconductor Integration and Packaging, Oct 23, 2007, San Francisco.
- 5) Bob Patti, *3D Scaling to Production*, 3D Architectures for Semiconductor Integration and Packaging, Oct 31-Nov 2, 2006, San Francisco.
- 6) Paul Enquist, *Direct Bond Interconnect (DBI™) – Technology for Scaleable 3D SoCs*, 3D Architectures for Semiconductor Integration and Packaging, Oct 31-Nov 2, 2006, San Francisco.
- 7) G. Traversi, M. Manghisoni, L. Ratti, V. Re, V. Speziali: "Characterization of deep N-well CMOS MAPS with in-pixel signal processing and data sparsification capabilities for the ILC vertex detector", 16th International Workshop on Vertex Detectors (VERTEX2007), Lake Placid (NY, USA), September 23 - 28, 2007, submitted to Proceedings of Science.
- 8) Jean-Claude Clemens, 3D Electronics Activities at IN2P3, Vertical Integration Technologies for HEP and Imaging, April 7-9, 2008, Tegernsee Germany.