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3D SOI Design at FERMILAB

MAMBO III

Monolithic Active Pixel Matrix with Binary Counters

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Presentation Outline

- Target Application
- Previous Work (MAMBO 2)
  - Design
  - Results
- MAMBO 3 development
  - Goals
  - Schematic
  - Layout
- 3D Integration

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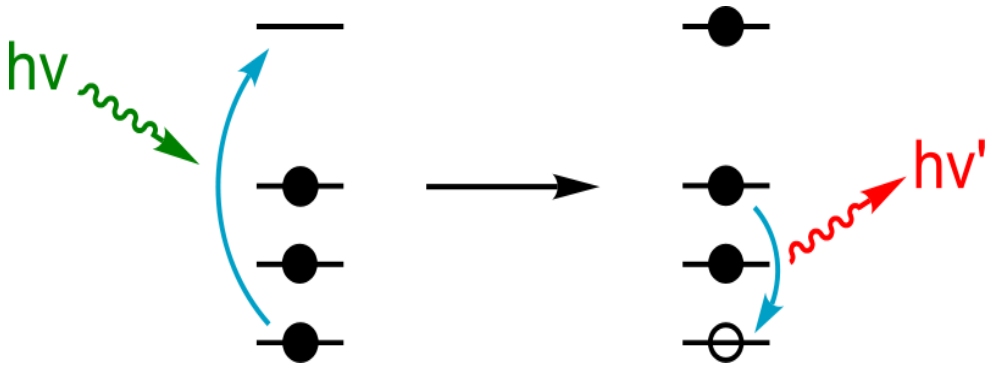
APPLICATION

Possible applications

- Low energy applications up to 12kEv

E.g.

- X-ray autoradiography
- fluorescence X-ray spectroscopy



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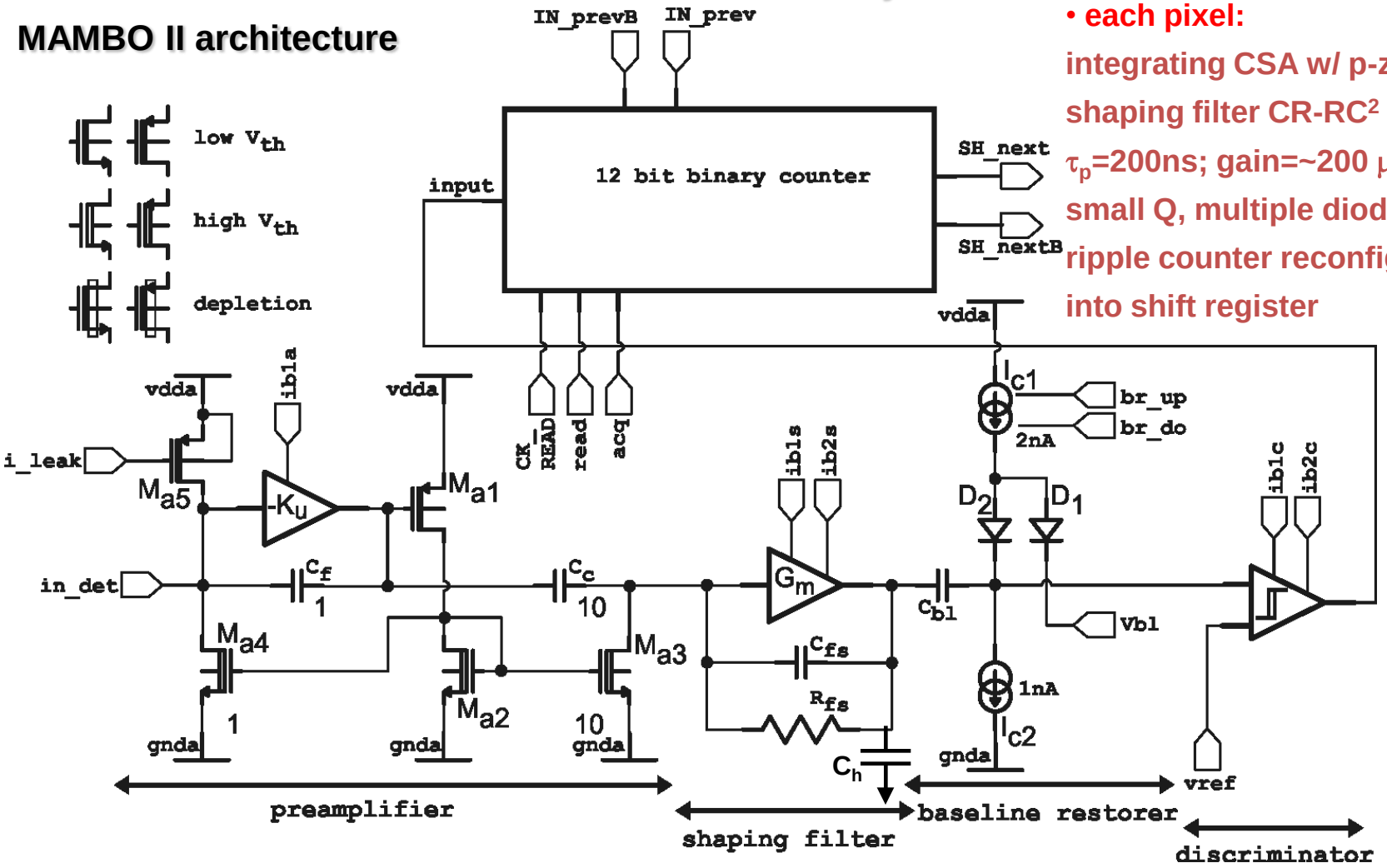
PREVIOUS WORK

MAMBO2: PREVIOUS WORK….

Design details of pixel imaging detector „MAMBO”

MAMBO = Monolithic Active Pixel Matrix with Binary Counters

MAMBO II architecture



- **each pixel:**
  integrating CSA w/ p-z network, shaping filter CR-RC^2 with τ_p=200ns; gain=~200 μV/e$^-$ for small Q, multiple diodes/pixel, ripple counter reconfigurable into shift register

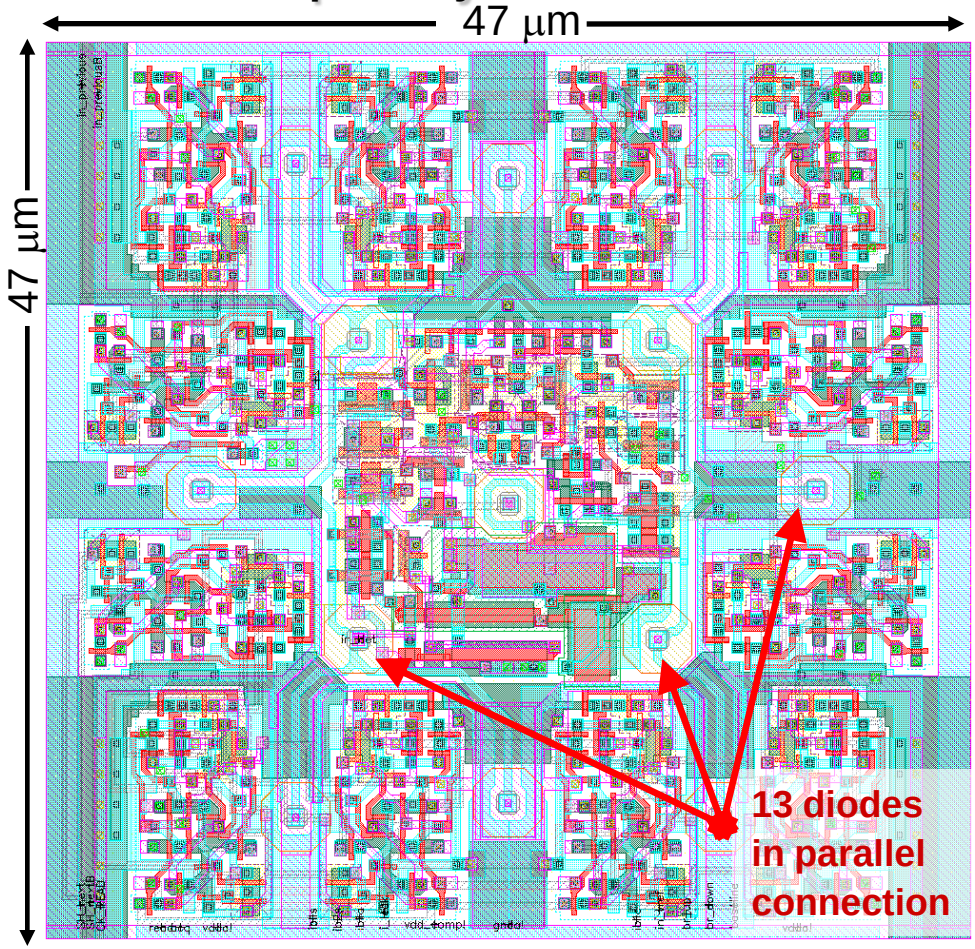
- **compact design excluding use of physical resistors**

C_c=28 fF, C_{fs}=3.3 fF, R_{fs}=50 MΩ, G_m=5.8 μS, C_h=30 fF,

MAMBO2: PREVIOUS WORK….

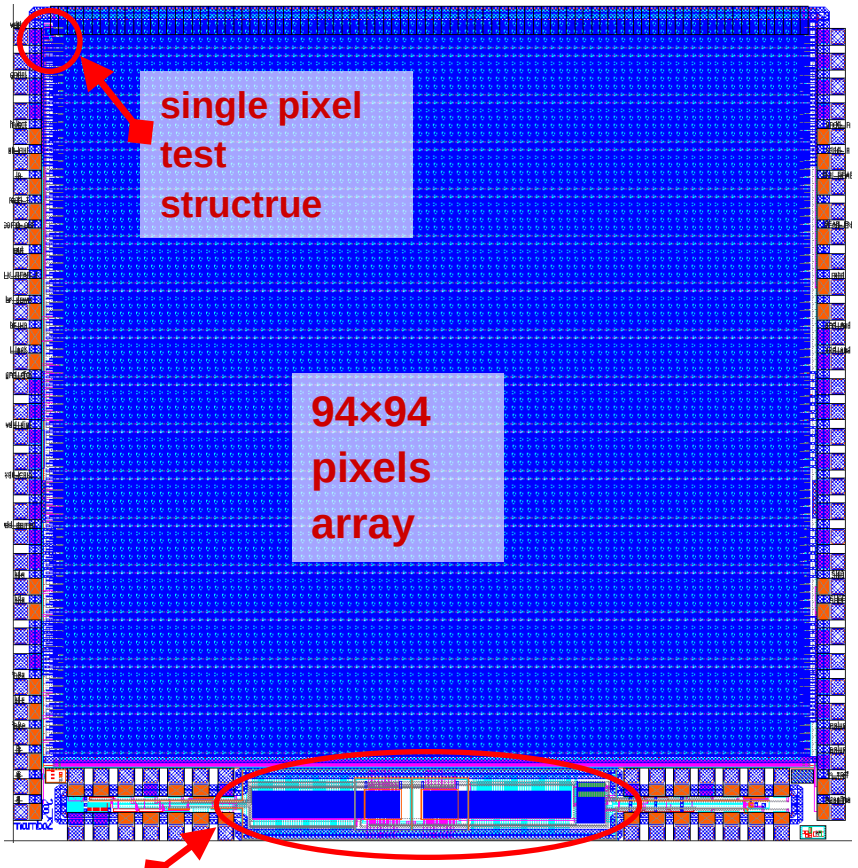
Design details of pixel imaging detector „MAMBO”

- MAMBO II pixel layout



Multiple p-taps (used as signal electrodes) present per pixel for reduction of shifts of threshold voltages.
Partial success: adjustment of bias voltages and currents (referred to V_{GS}) up to several tens of mV still required for V_{back} from the range from 0 to 10V.

- MAMBO II chip layout



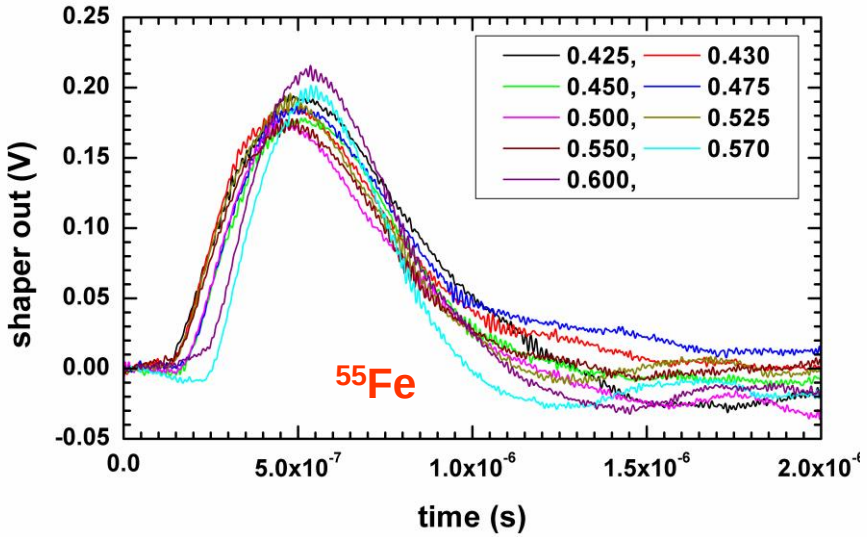
8×10 20×20 μm² 3T pixel matrices for x-talk and test charge collection tests

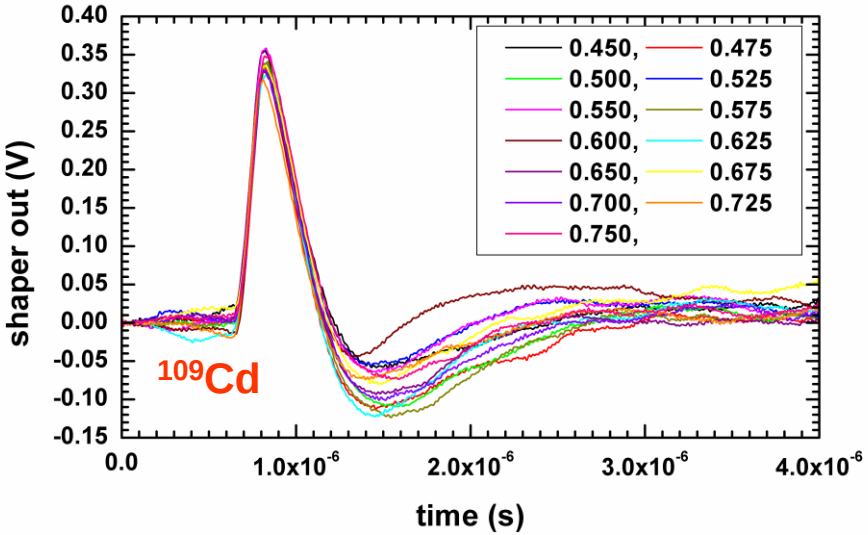
Single pixel test structure is a fully functional ciruit allowing monitoring: **shaper output, discriminator output, counter output**

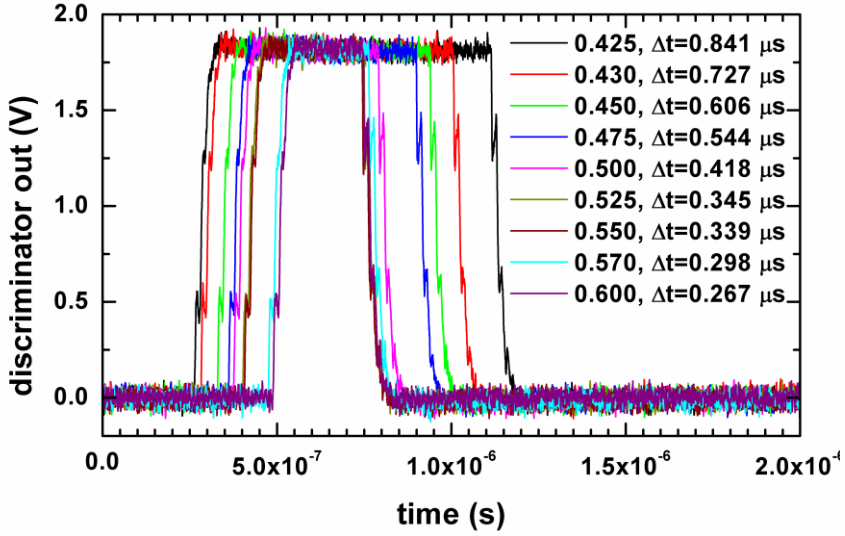
Achievements, observations and investigations

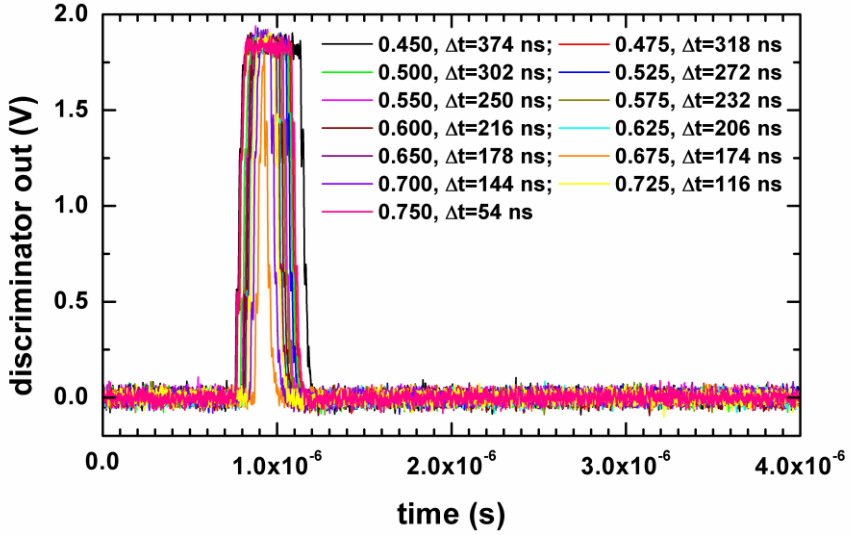
MAMBO II single pixel test

Monitoring of the shaper and discriminator outputs (transient signals)









Analogue Results

Dynamic range	~500 e- to 4000 e-
Noise	~80e-
Sensitivity	100mV/1000e-
Shaping time	250ns

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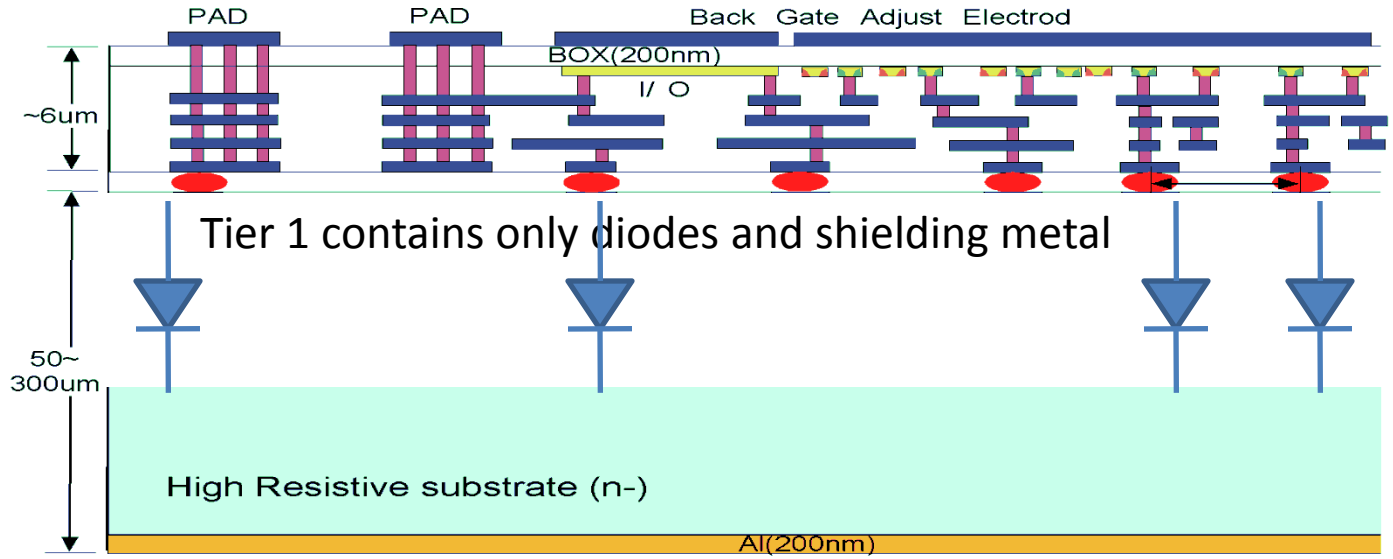
MAMBO 3

Goals

- R&D
- Detector and electronics on different layers (to avoid coupling)
- Diodes with PPLUS with BPW to reduce leakage
- Diode of the same size as the pixel to obtain parallel electric field in active volume, and avoid potential pockets
- Shielding on detector layer
- Possibility of changing gated diode voltage to enhance performance of the diode
- Explore 3D IC technology with Zycube

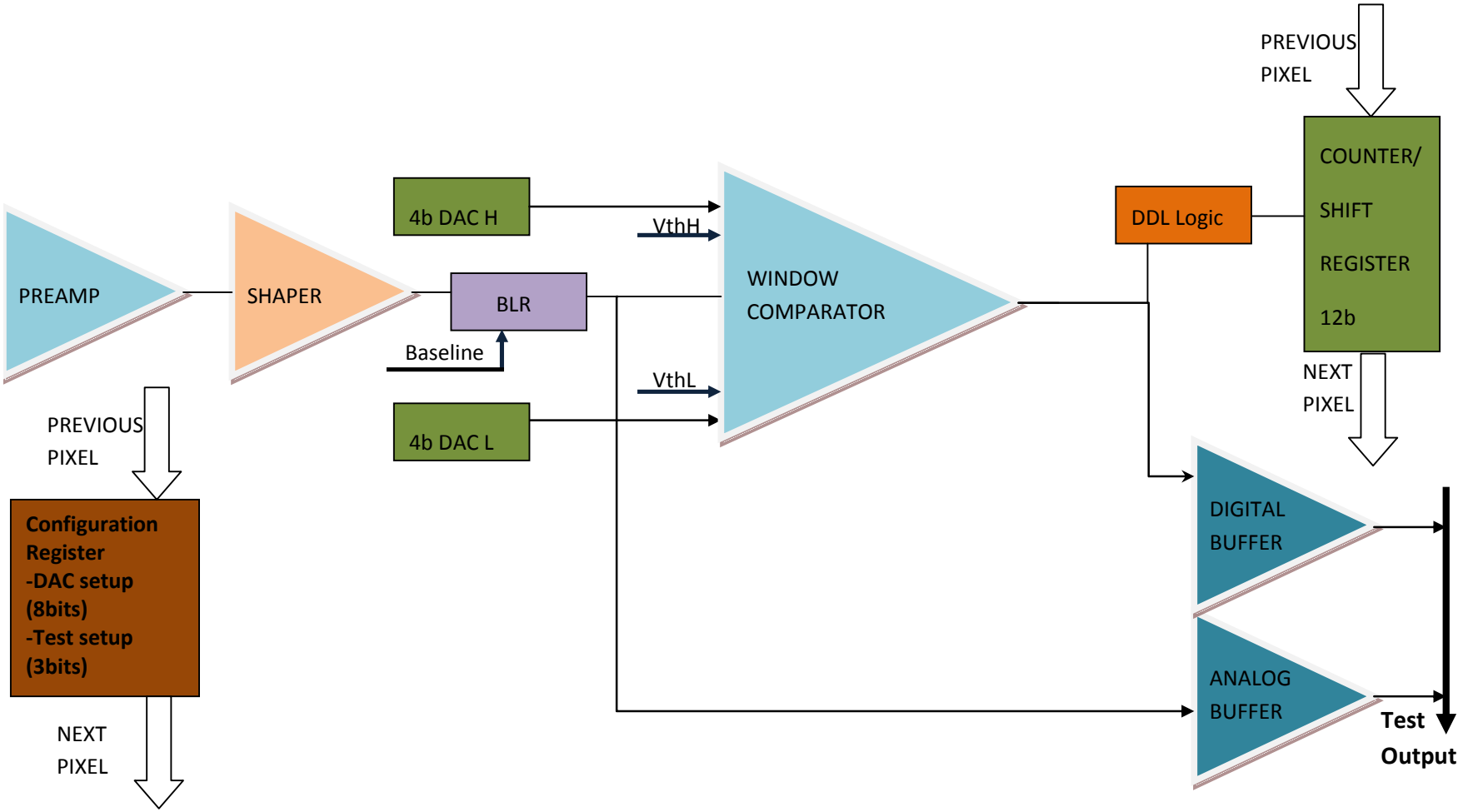
3D : MAMBO 3



MAMBO 3
top ASIC

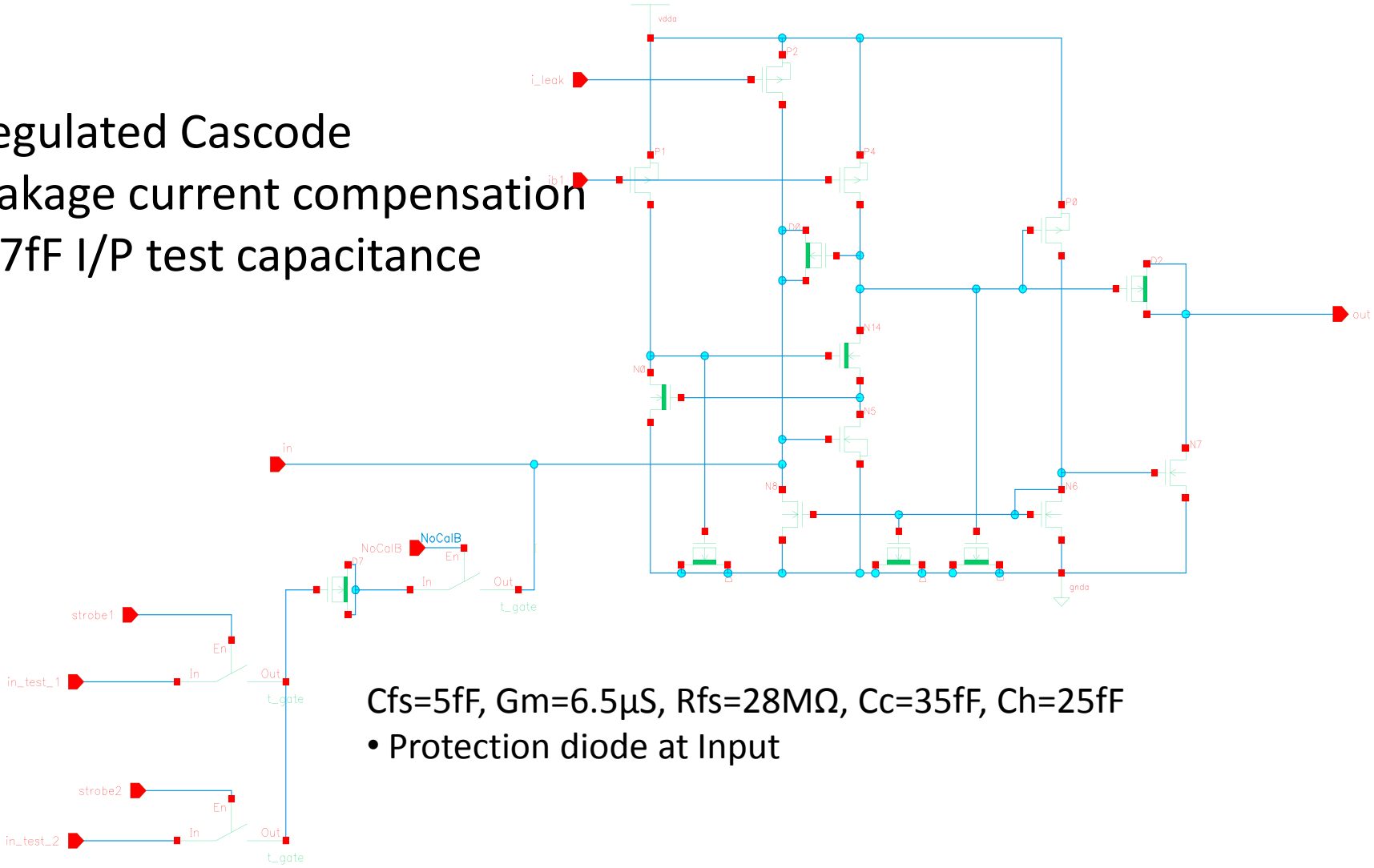
MAMBO 3
bottom ASIC

Top ASIC: PIXEL Design



Preamplifier

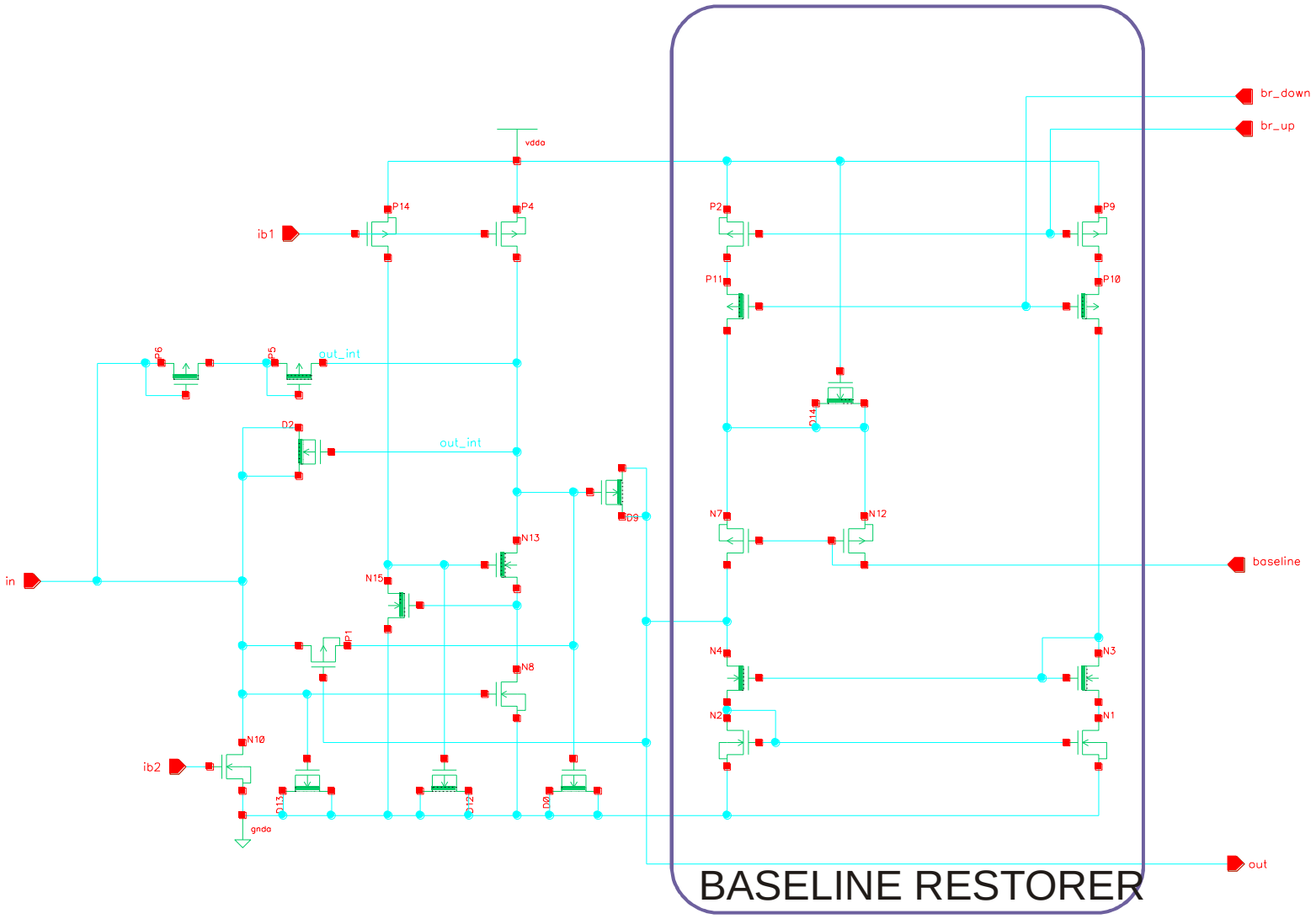
- Regulated Cascode
- Leakage current compensation
- 1.7fF I/P test capacitance



Cfs=5fF, Gm=6.5µS, Rfs=28MΩ, Cc=35fF, Ch=25fF

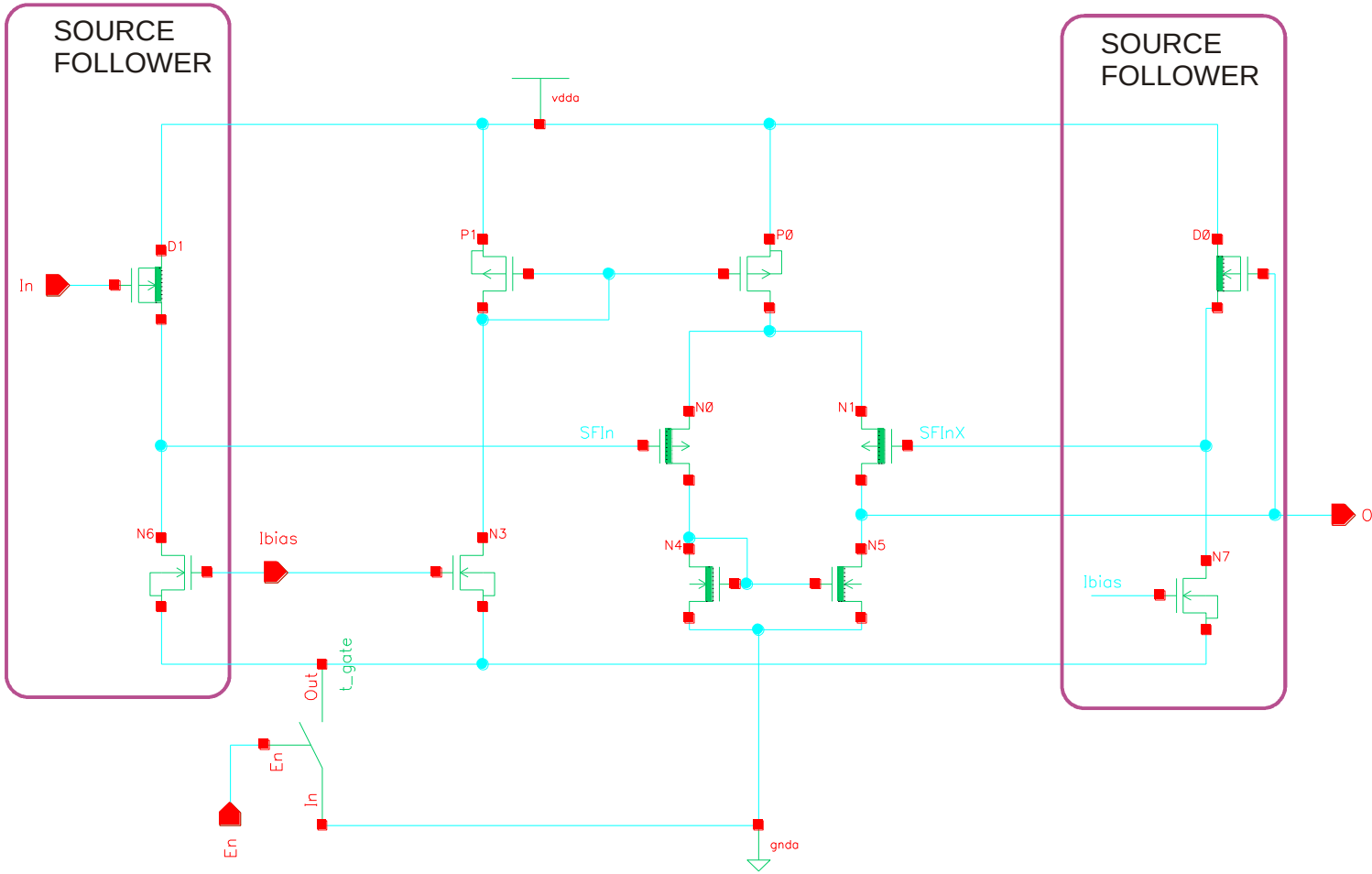
- Protection diode at Input

Shaper and Baseline Restorer

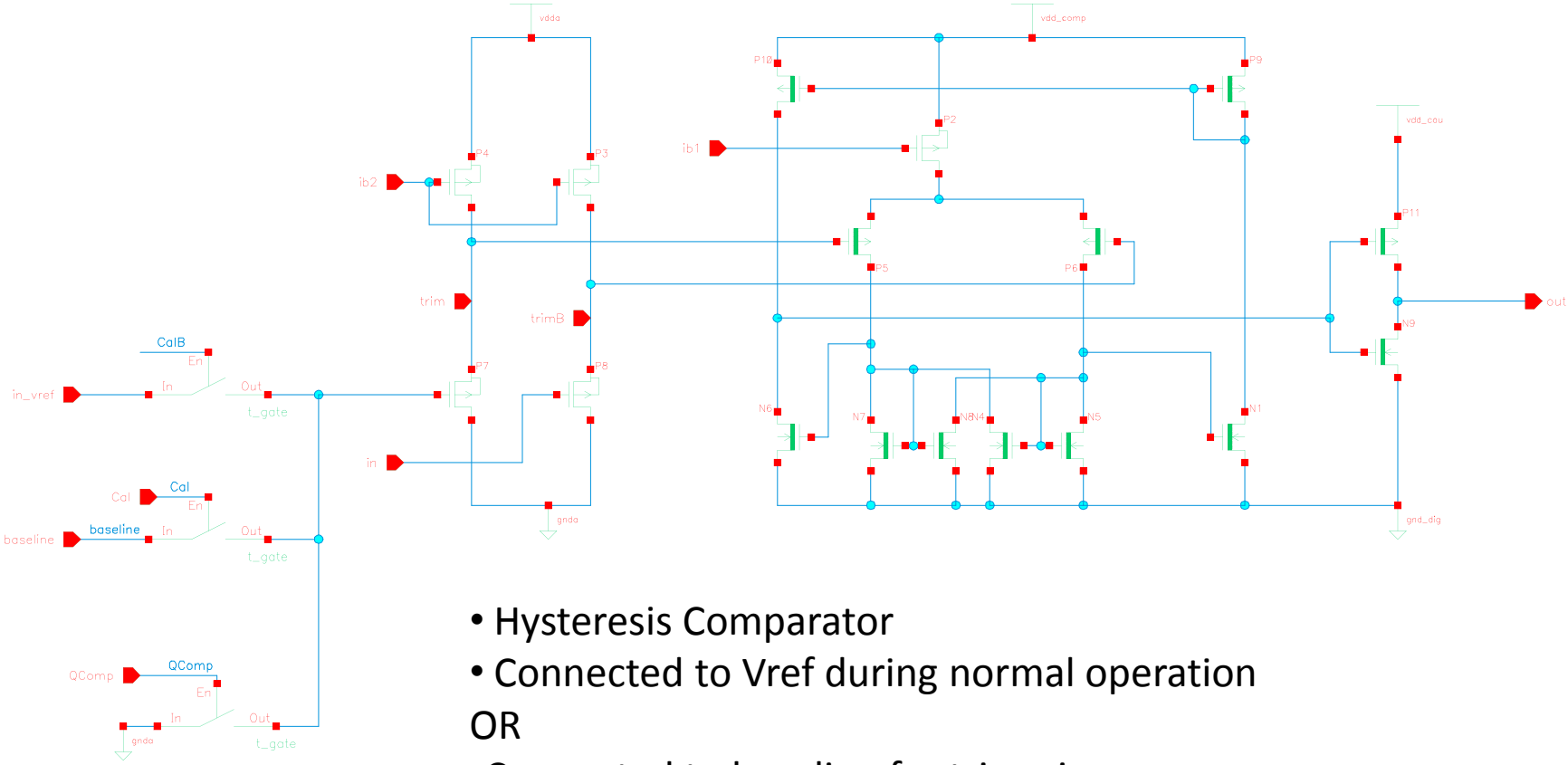


Analog Test Buffer

- Source Followers using Zero Vt DMOS transistors
- Single Stage amplifier
- Disconnected during normal mode of operation
- 10 µA current



Comparator



- Hysteresis Comparator
- Connected to Vref during normal operation

OR

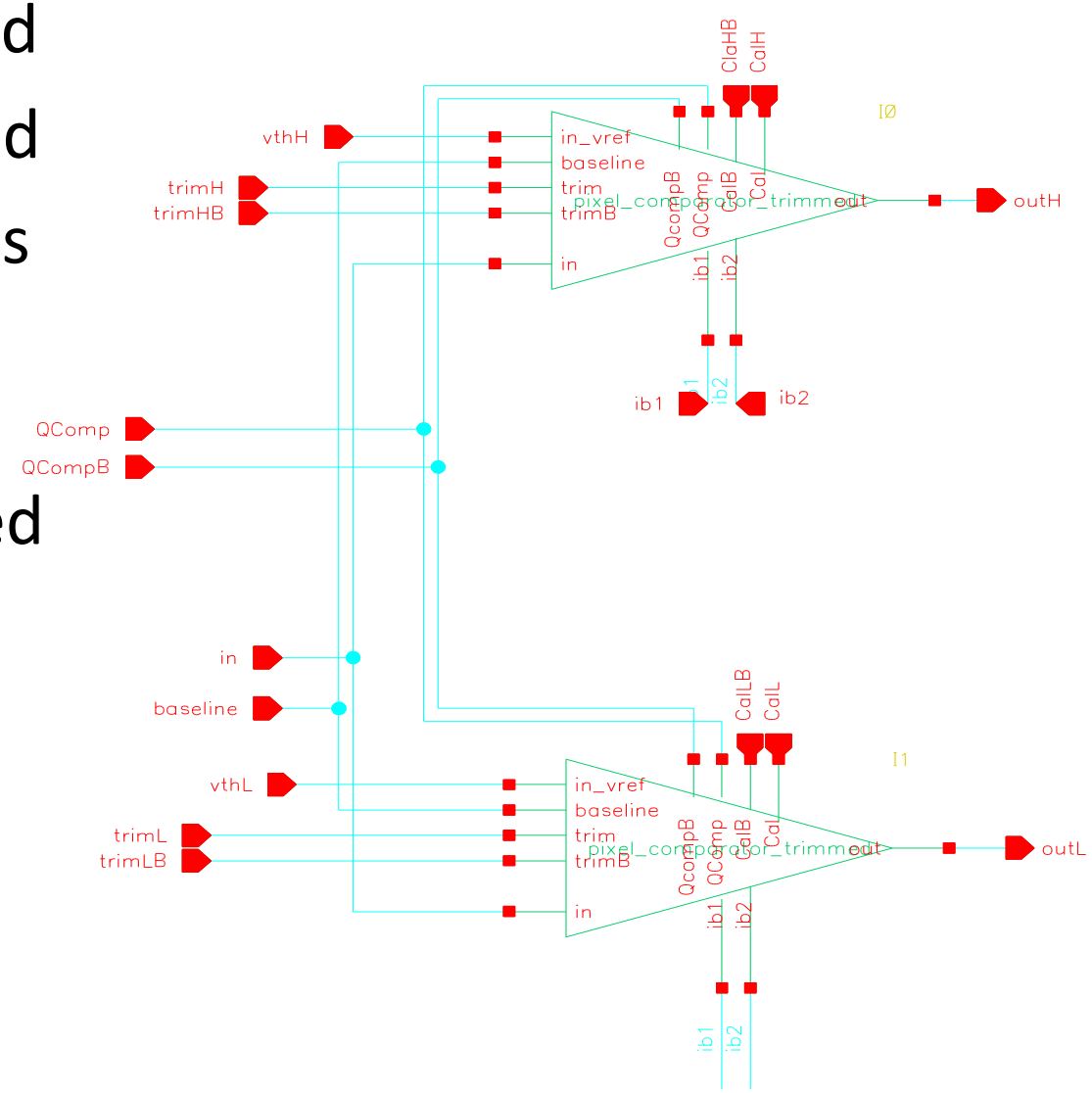
- Connected to baseline for trimming

OR

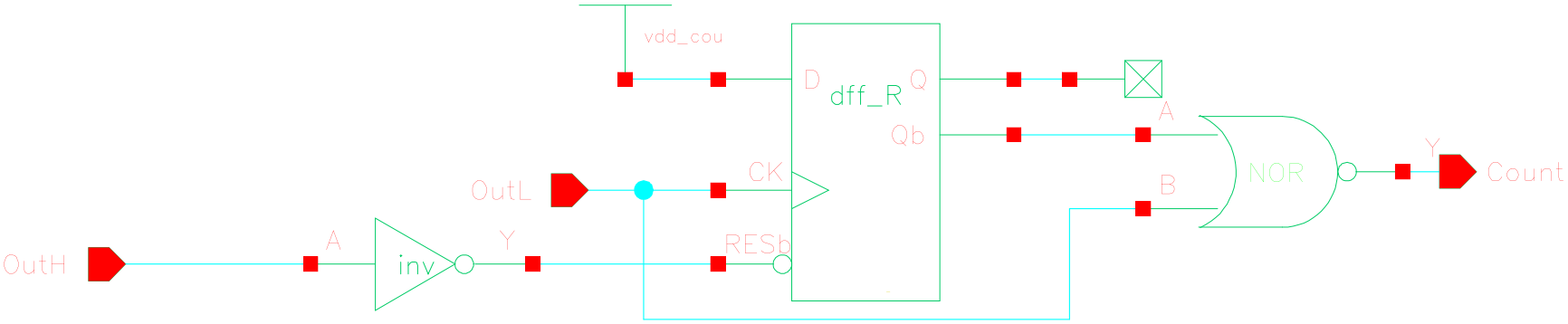
- Connected to gnd! When disabled

Window Comparator

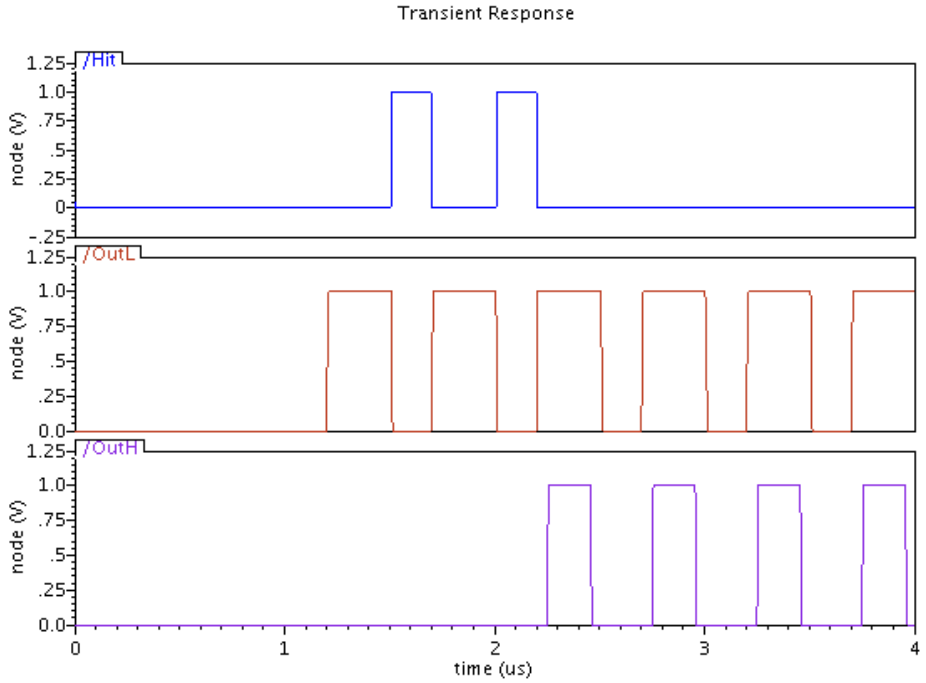
- VthL – Lower Threshold
- VthH –Upper Threshold
- VthL < Signals < VthH is recorded as HIT
- Comparators are independently trimmed to cancel offsets



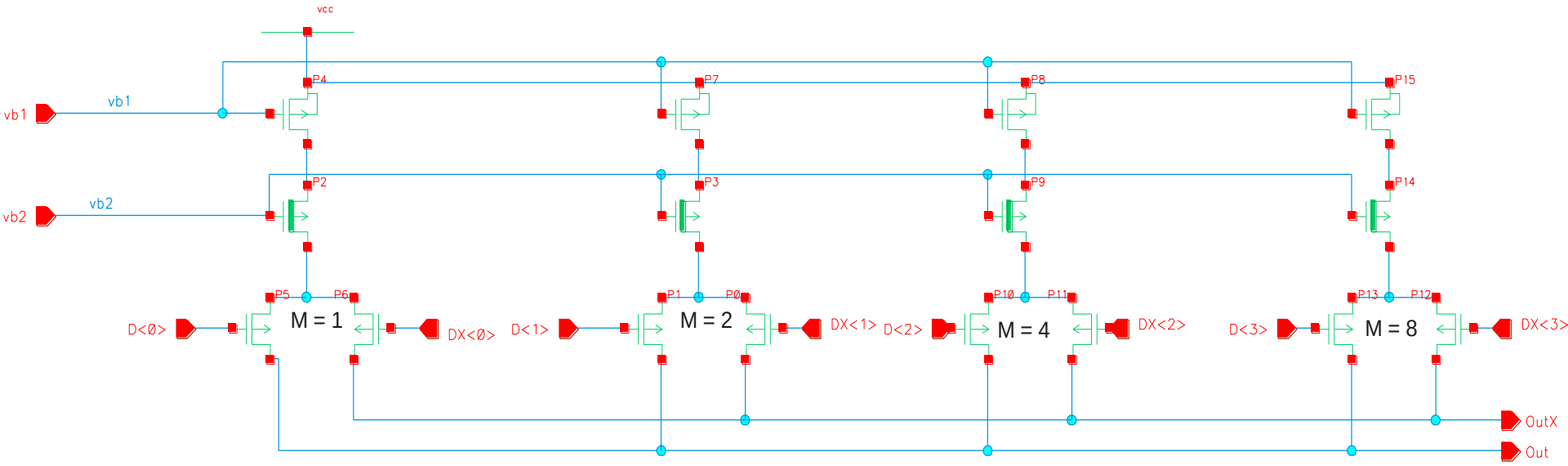
Double Discriminator Logic



- Output of the Lower Threshold comparator behaves as a clock
- Output of the Upper Threshold comparator behaves as a Reset
- When both comparators fire the hit is not counted

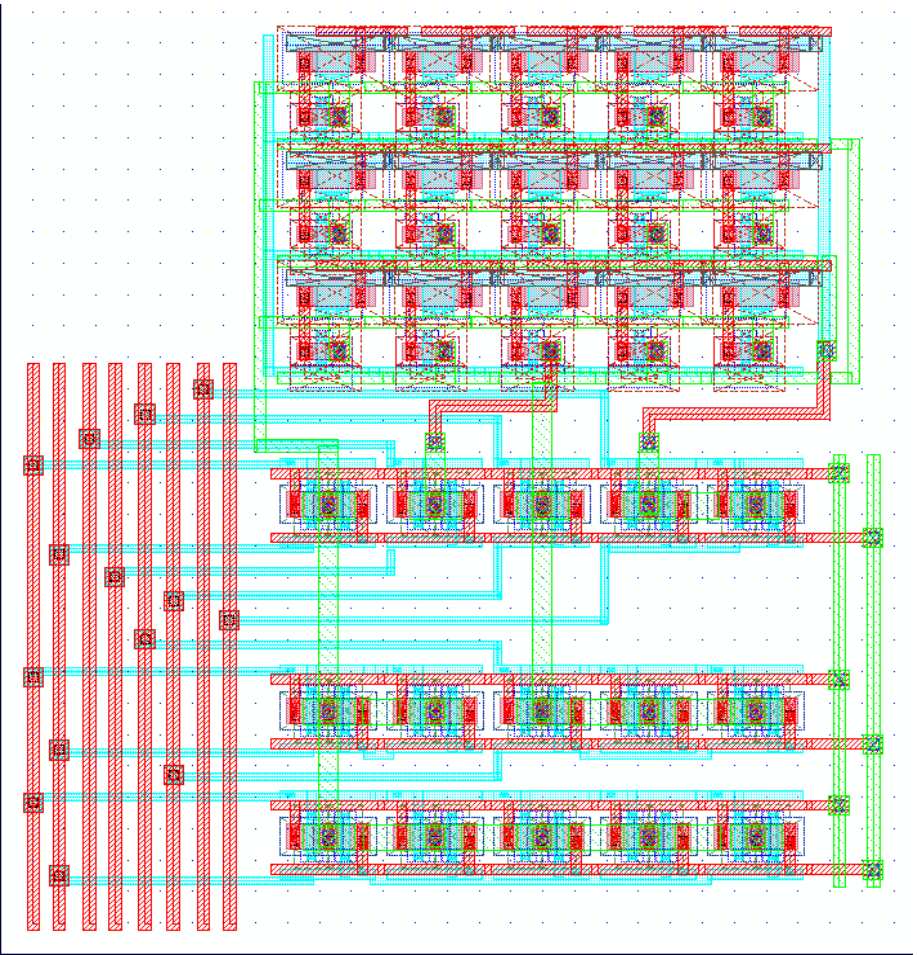


Current Steering DAC (4 bits)



- Binary weighted current mirrors
- Switches are also binary weighted
- Current can be steered either to positive or negative output

DAC Layout



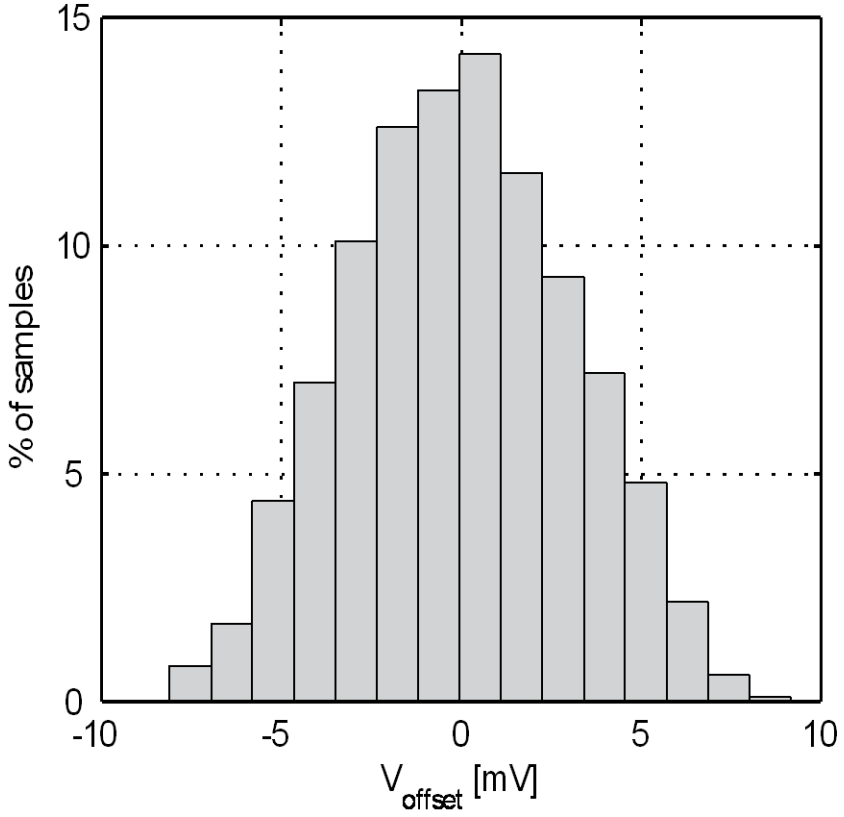
4	3	4	3	4
4	2	1	2	4
4	3	4	3	4

Conventional symmetrical common centroid geometry for current mirrors
Helps to average out global errors
•Matching is critical for monotonic performance

Trimming DACs

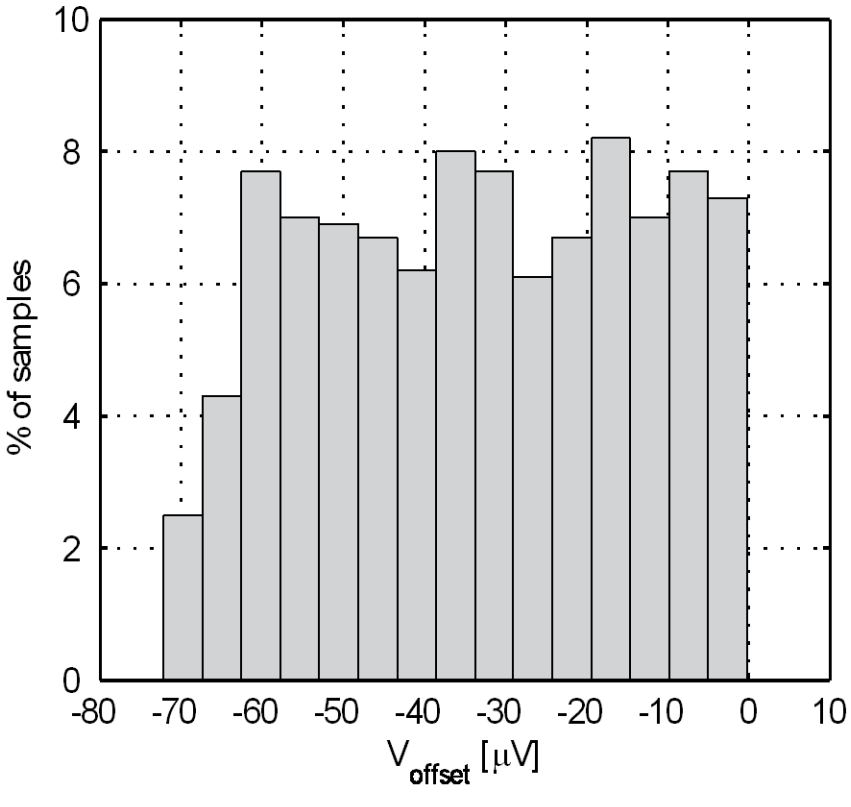
Matching is worse for SOI!, Data here corresponds to a typical bulk CMOS process

Offset distribution before compensation



- Gaussian distribution
- Depends on component matching

Offset distribution after digital compensation

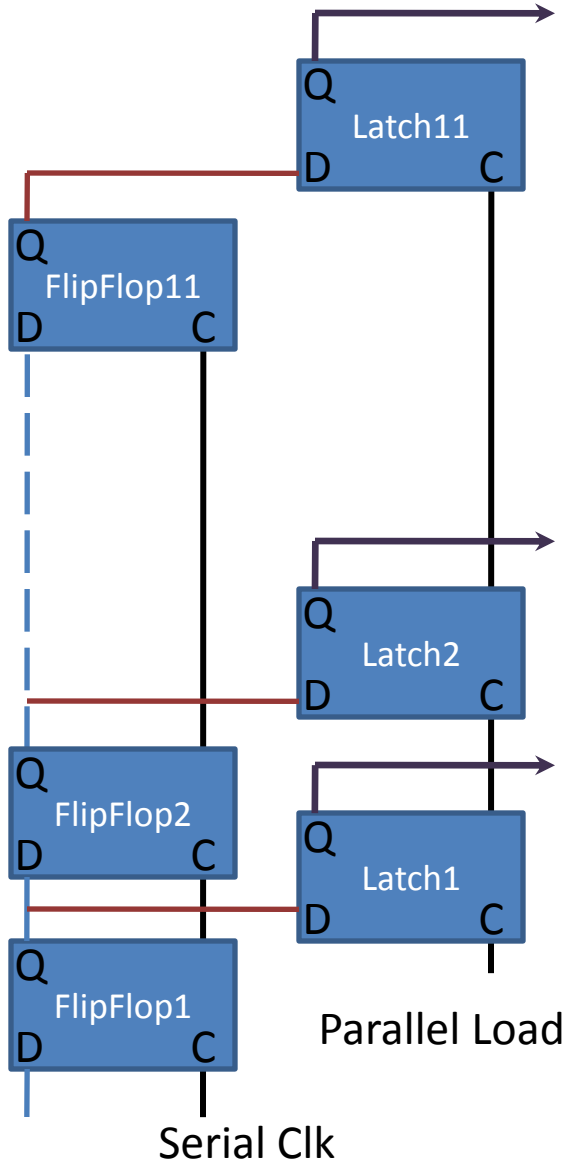


- Uniform distribution
- Residual offset depends on DAC resolution

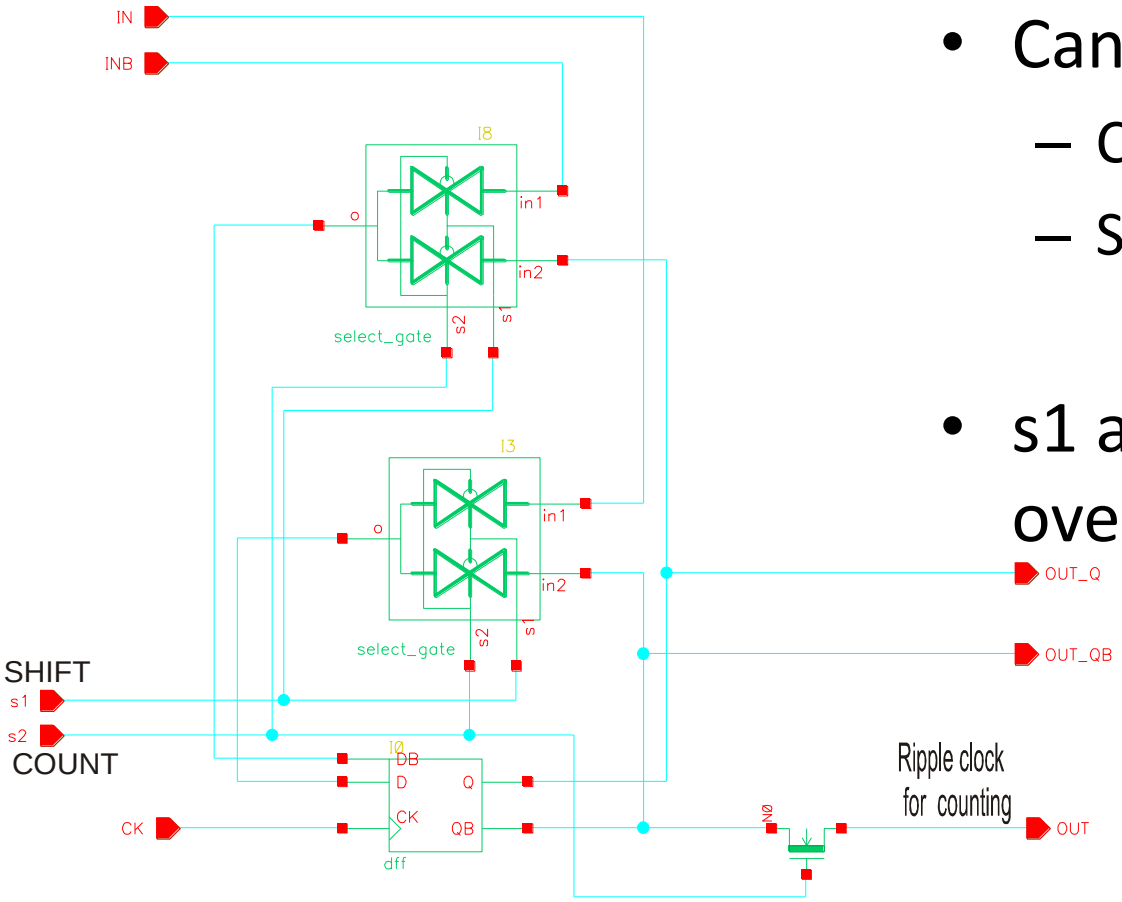
Configuration Register

- Serial In Parallel Load
- (4b x 2) for DAC settings
- 3 bit test setup
- Test Control block used as decoder to control switches for test

	Setup
000	Normal Operation
001	Analogue Output for test calibration
010	Test Input, counter connected
011	Calibrate DAC L
100	Calibrate DAC H
101	xx
110	xx
111	Pixel Disabled



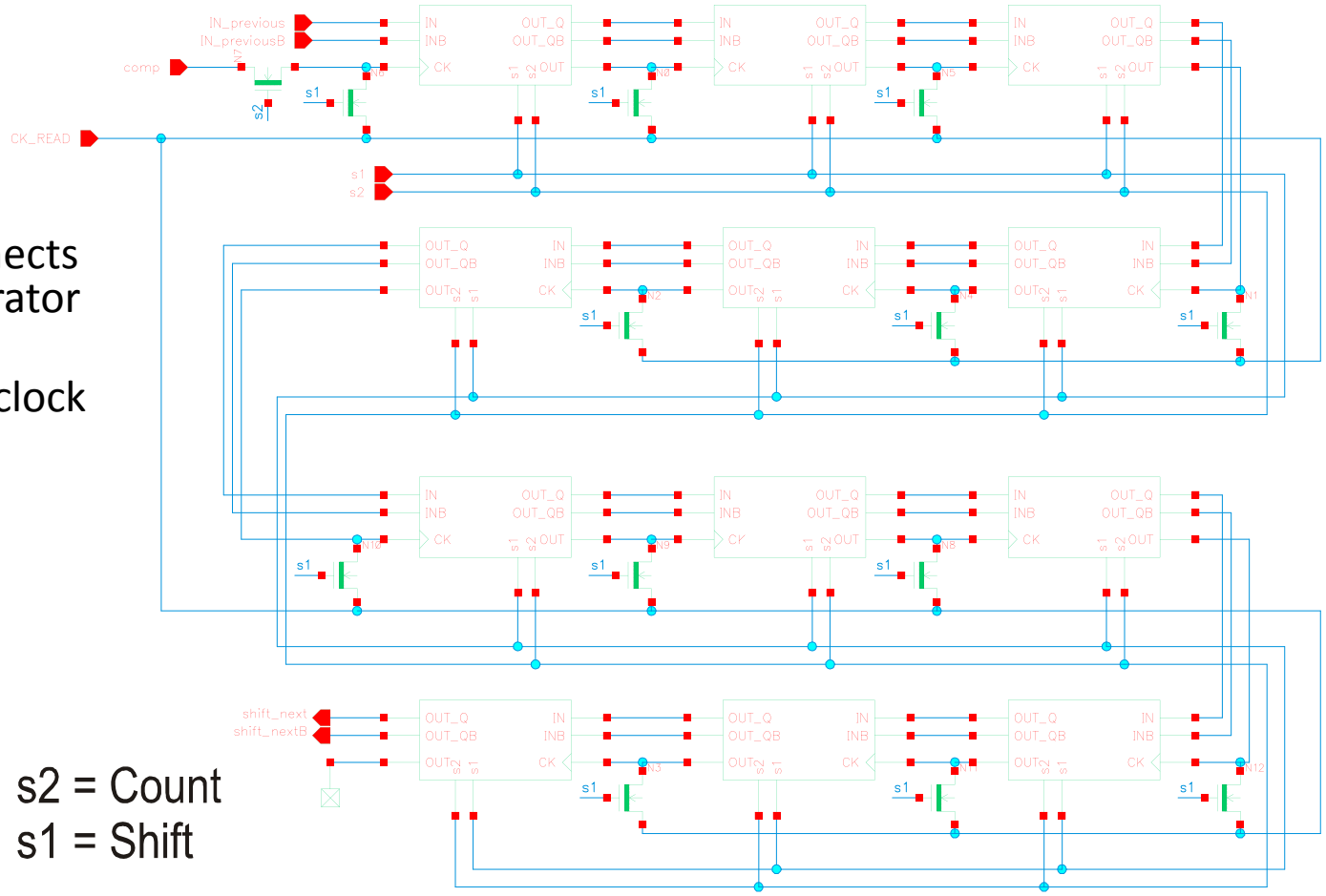
1bit Counter



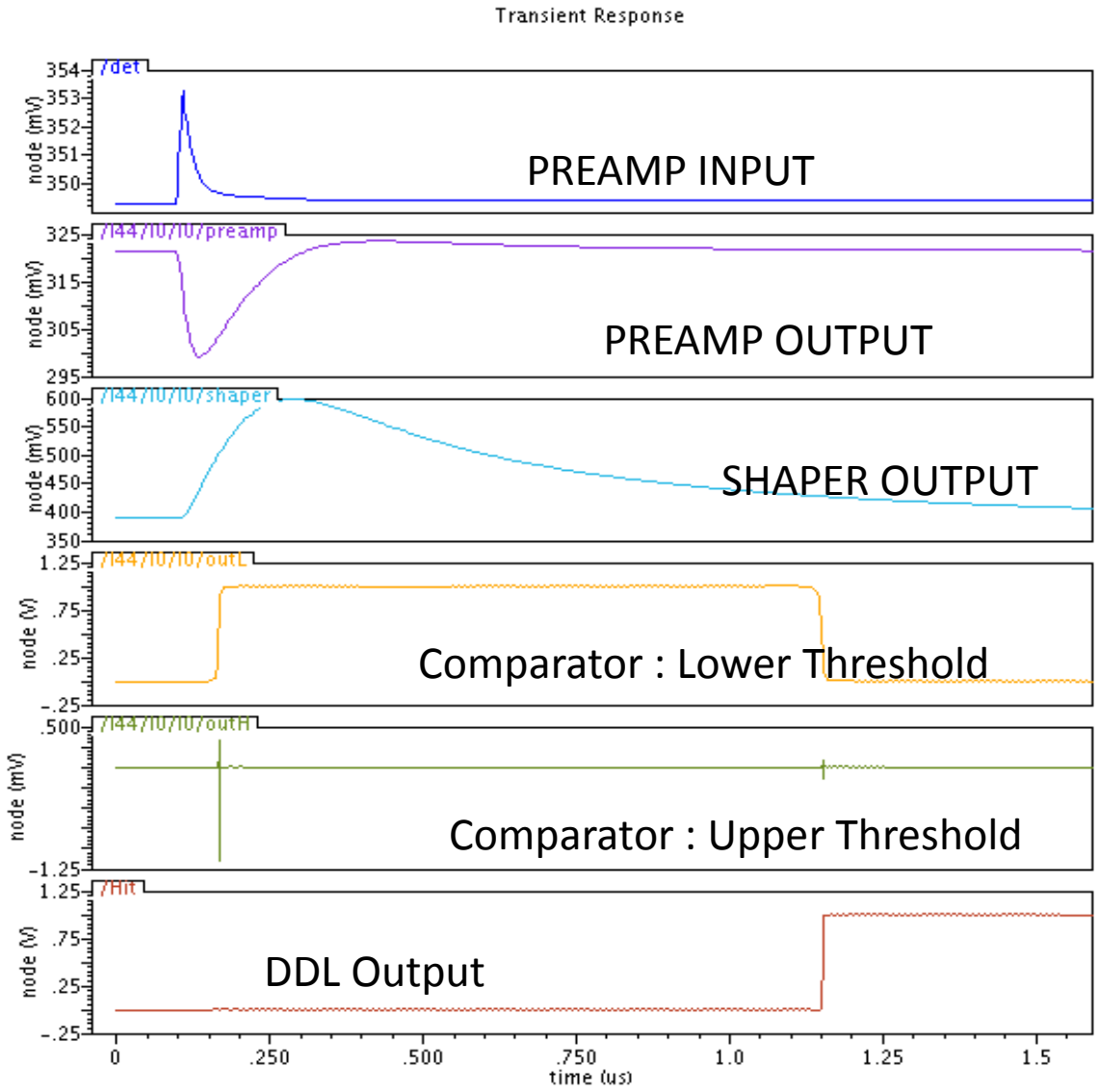
- Can be configured as:
  - Counter (s1 is ON)
  - Shift Register (s2 is ON)
- s1 and s2 are non-overlapping clocks

Counter /Shift Register

- 12 bit ripple counter
- Count switch disconnects counter from comparator while shifting
- CK_READ is external clock used for shifting data



Simulation result



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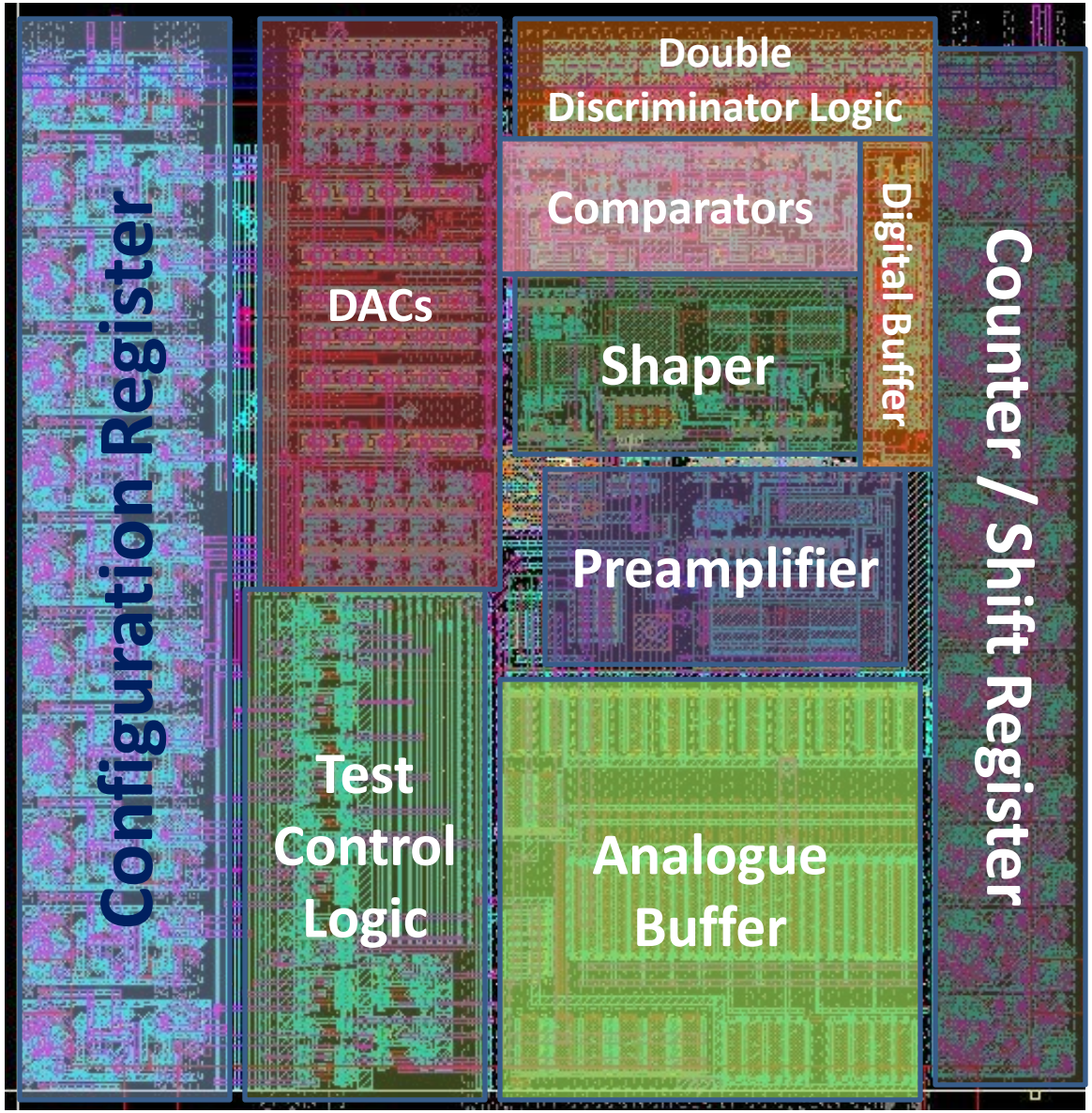
LAYOUT

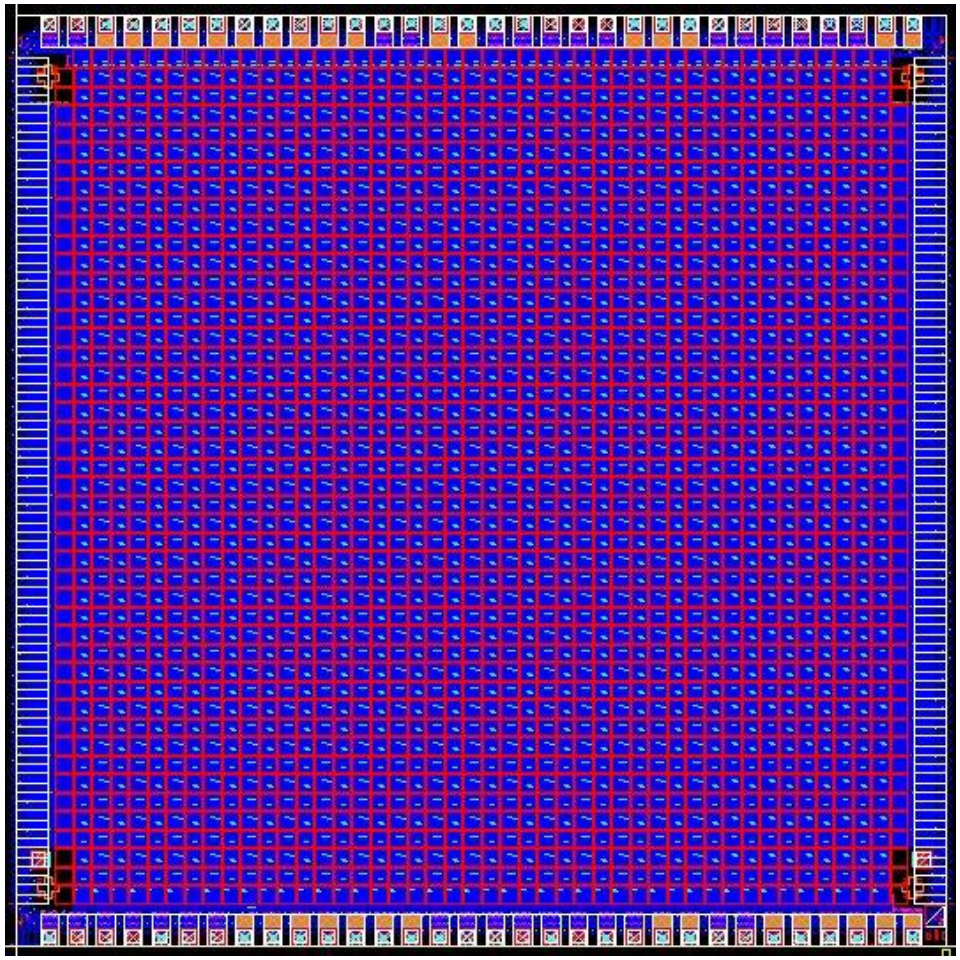
MAMBO3: top pixel

- 100µ x 100µm
- Transistor count ~ 950

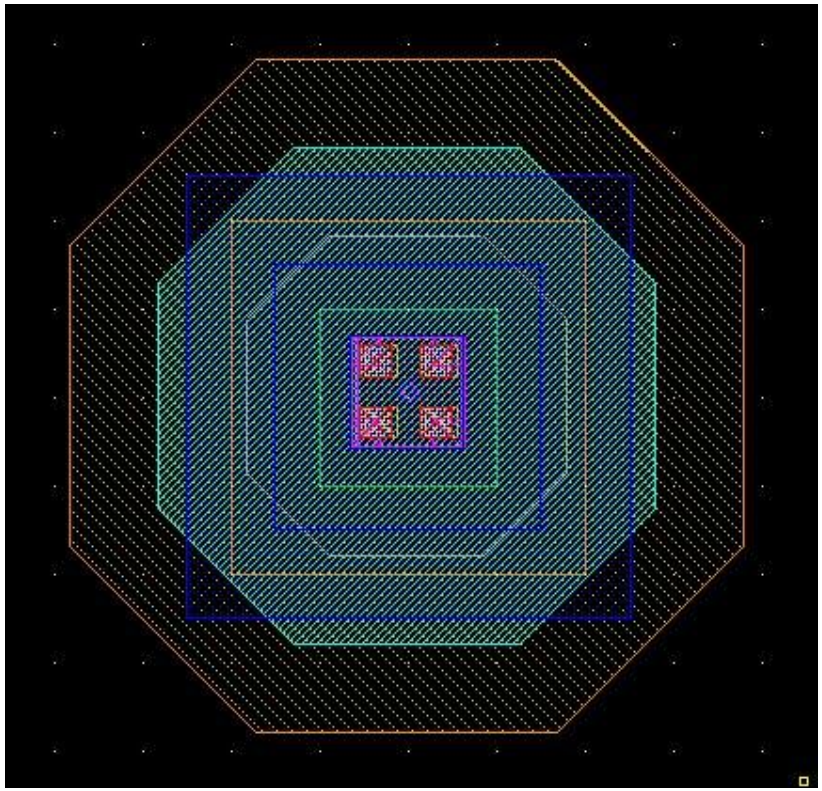


Upper Chip

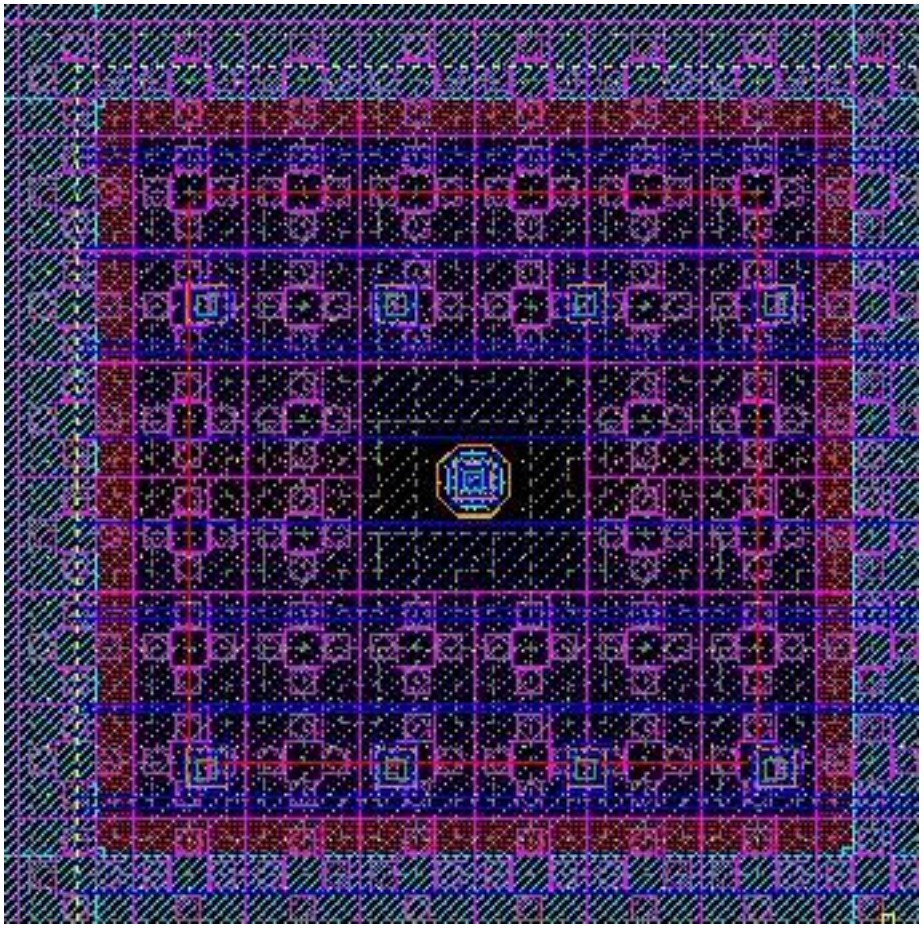
- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- Each column has additional buffering of analog and digital signals
- Pads with back metal opening
- Alignment markers on all 4 corners



Lower chip: Diode Pixel

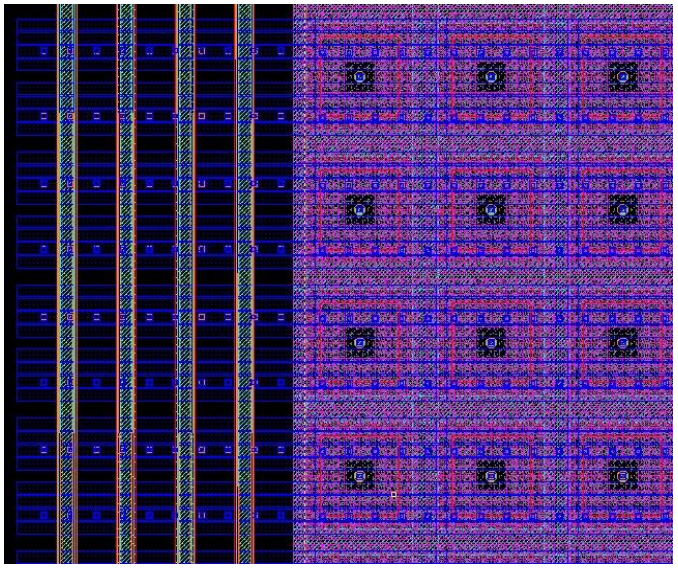


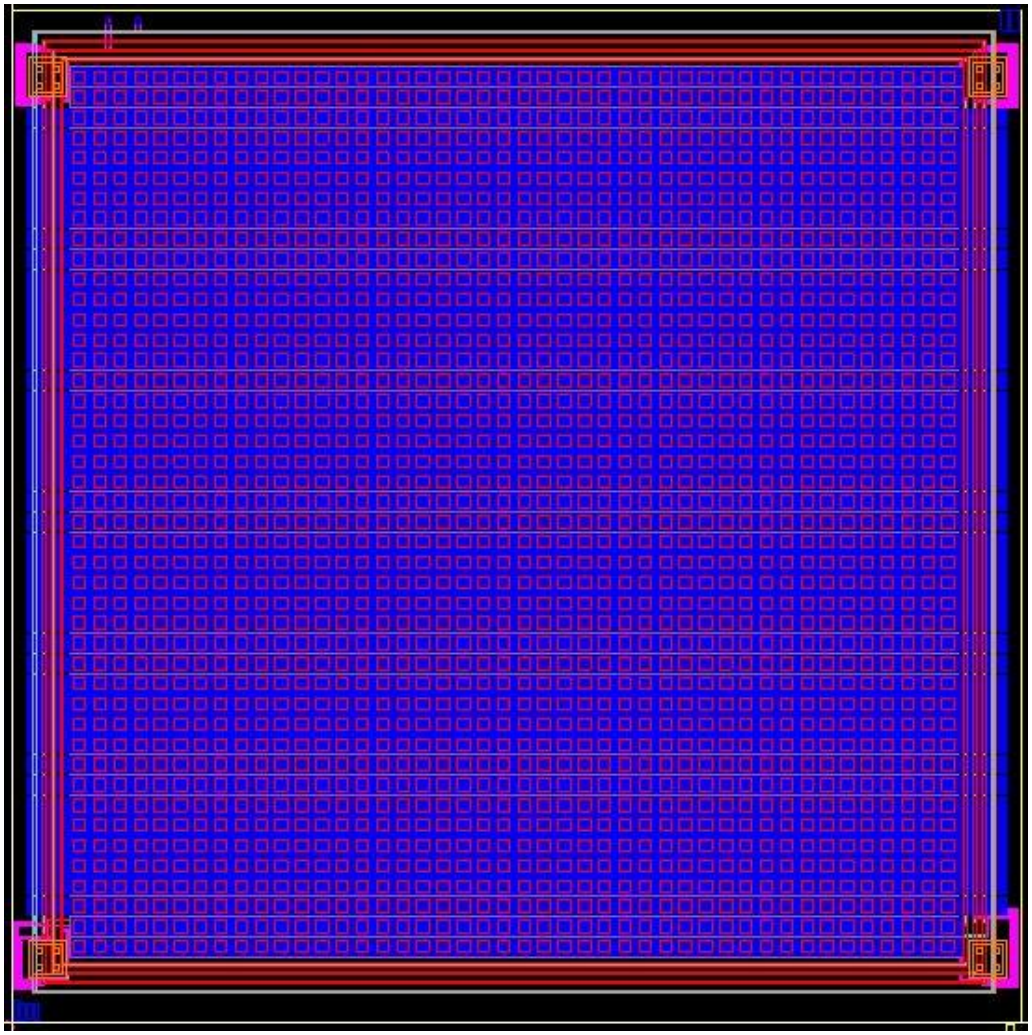
DIODE



100µ x 100µ

Lower Chip

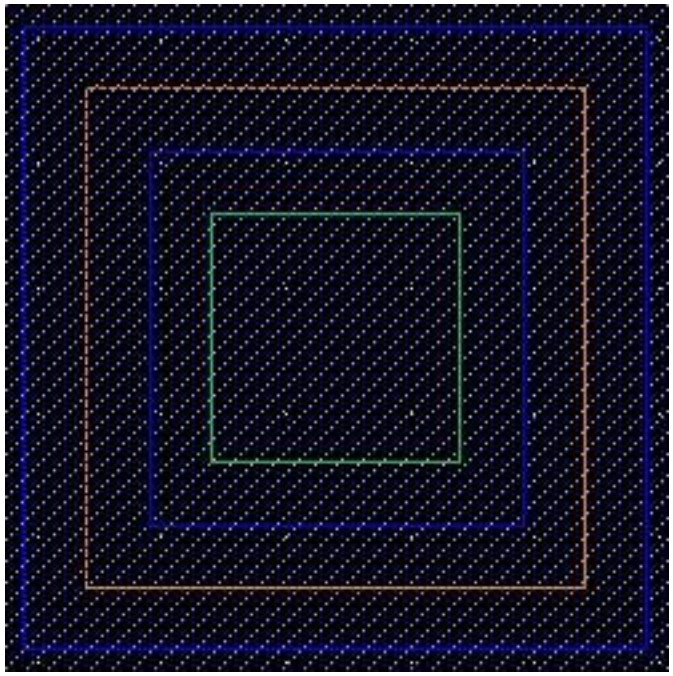




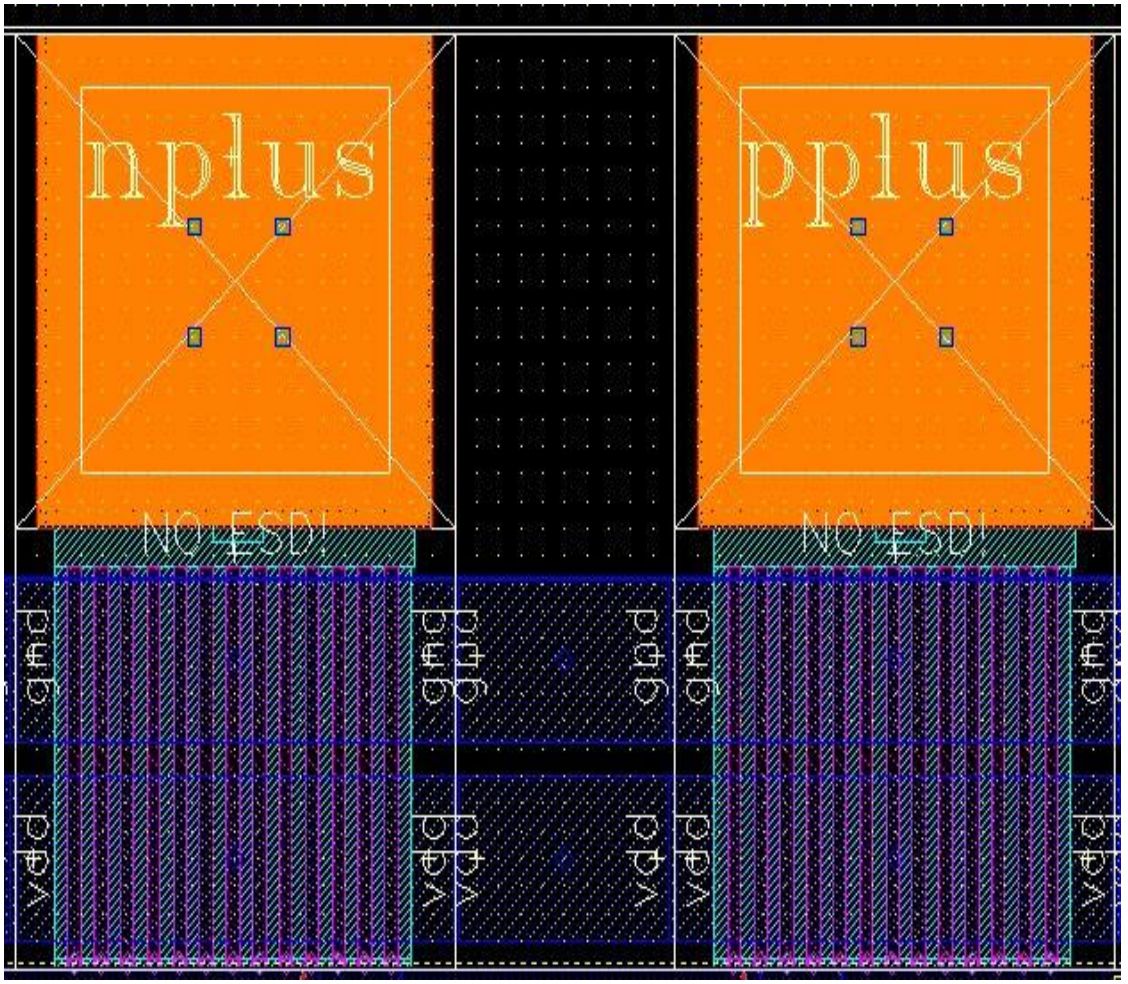
- 5mm x 5mm
- 1936 pixel matrix (44 x44)
- 4 guard rings around the matrix
- No bond Pads contains only micro bump pads, aligned with the top chip.
- Alignment markers on all 4 corners

Chip connection

MICROBUMP (5µmx5µm)



-Diode connection per pixel
-Dummy connections
-guard rings
-diode shielding (gnd!)
-gate control

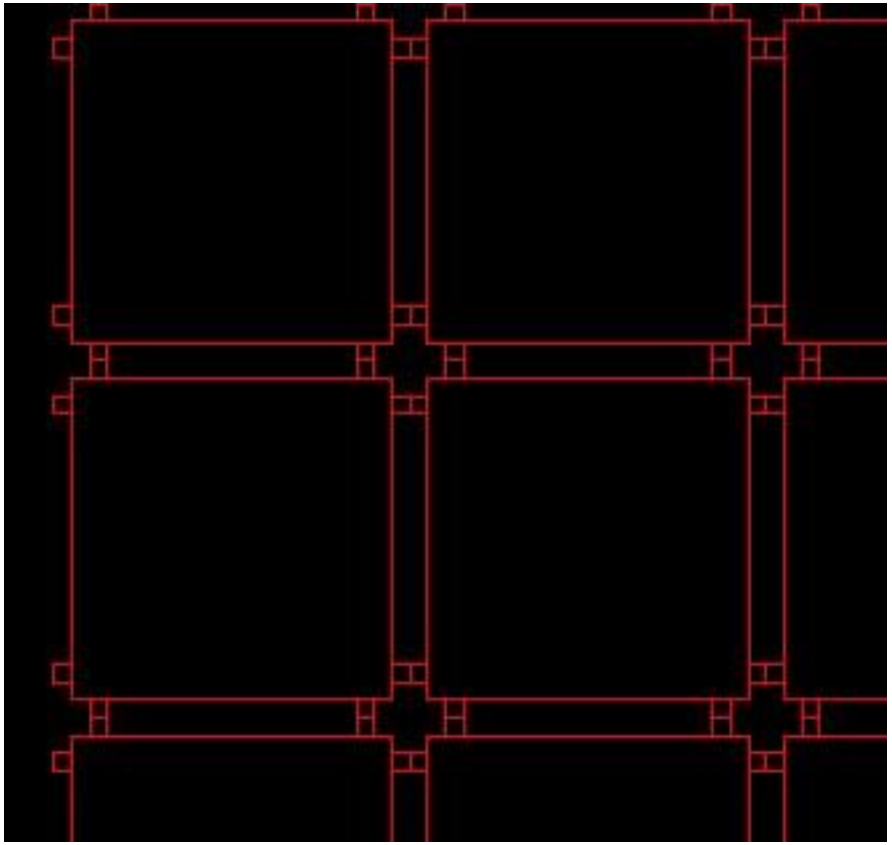


Protection

- Protect transistors from external environment

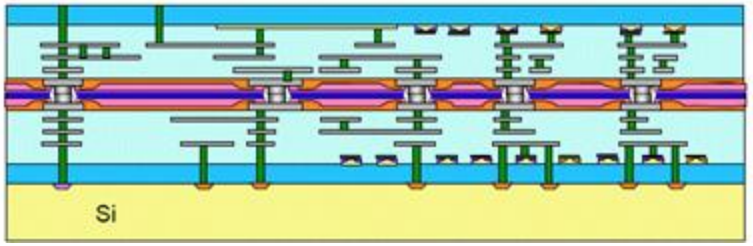
- Backplane connected to Analogue Ground per pixel

- Peripheral digital logic connected to Digital ground plane



Shielding per pixel using back metal

exposed transistor



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INTEGRATION

Zycube 3D Integration process

(1) Stack Process Flow (after finishing wafer process)