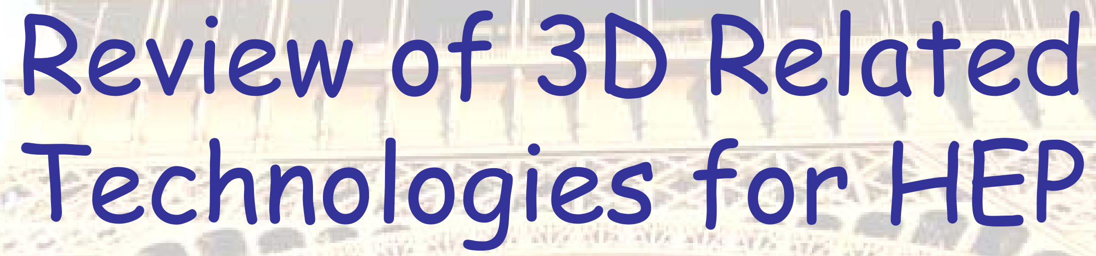


Review of 3D Related Technologies for HEP

Ray Yarema

For the Fermilab ILC Pixel Detector Group

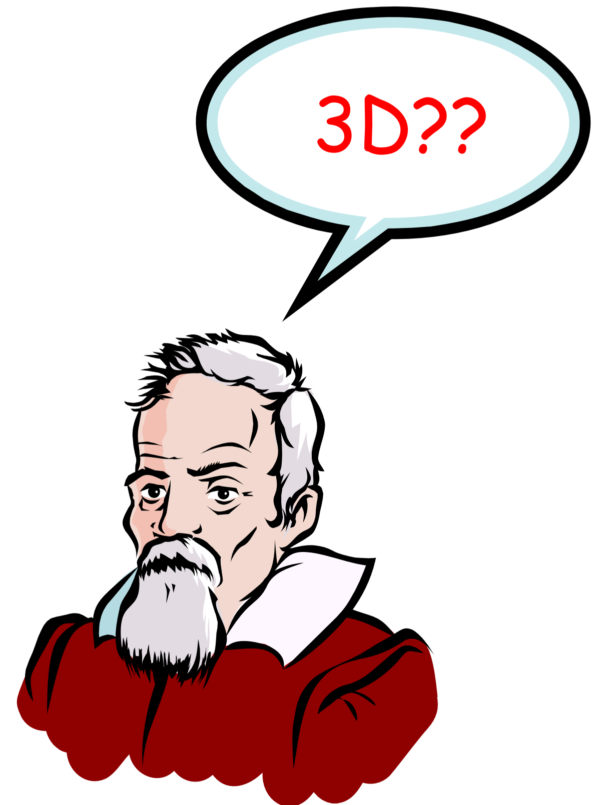
Fermi National Accelerator Laboratory

November 29, 2007

Paris, France

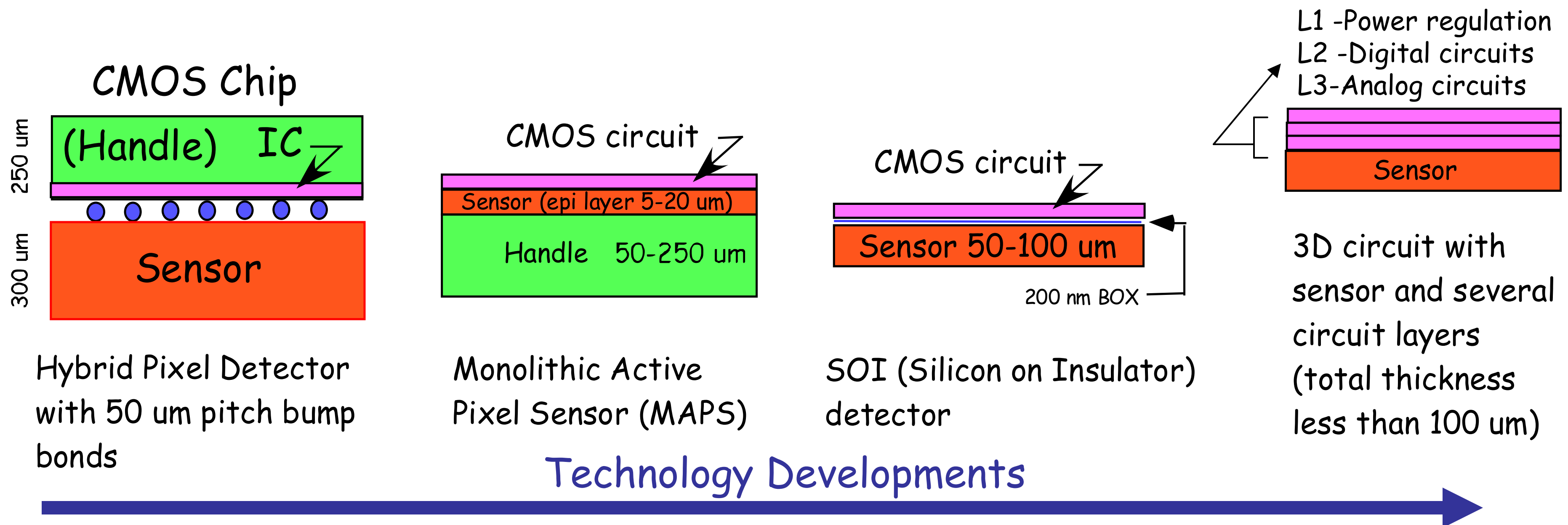
Outline

- Introduction –
  - The Dream
  - World wide interest in 3D
- Applications
  - Industrial applications
  - HEP applications
- 3D for the ILC and SLHC
  - Key 3D Technologies
- SOI Detectors
- 3D circuits of interest to HEP
  - Industry
  - Fermilab
- Cost considerations
- Summary



Physicist's Dream

- Physicists have long dreamed of integrating sensors and readout electronics.
- Pixel designs have progressed from hybrid designs to MAPS.
- There is now an opportunity to provide further improvements with newer technologies (SOI detectors[1], and 3D).



3D Movement in Industry

- Movement driven by several factors
  - 1) form factor,
  - 2) higher performance,
  - 3) heterogeneous integration,
  - 4) eventually lower cost.
- Numerous conferences and meetings are being devoted to 3D technologies.
  - 3D integration for Semiconductor Integration and Packaging, Oct. 22-23, 2007, 26 talks, 3rd annual meeting.
  - Technology Roadshow for 3D, MEMS, and Advanced Packaging, October 26- Nov. 7 in 5 Asian cities, 9 talks.
  - 3D IC Technology Symposium (EMC-3D), Netherlands, Oct. 4th 2007, 10 talks.
  - ISSCC'06 Tutorial, "Introduction to 3D Integration" by K Bernstein from IBM.

3-D Architectures for Semiconductor Integration and Packaging

Going Mainstream—Defining the Technology and Market Opportunities

22–24 OCT 2007

Hyatt Regency San Francisco Airport Hotel
Burlingame, California

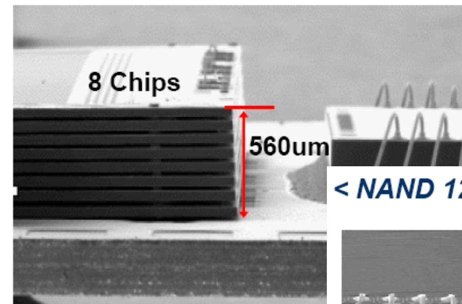
Technology Venture Fall 2007 Forum

Headline Sponsors: EVG, Lam Research
Exclusive Media Sponsor: Semiconductor International
Coordinated by: RTI International

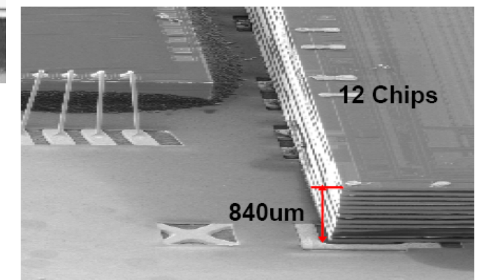
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

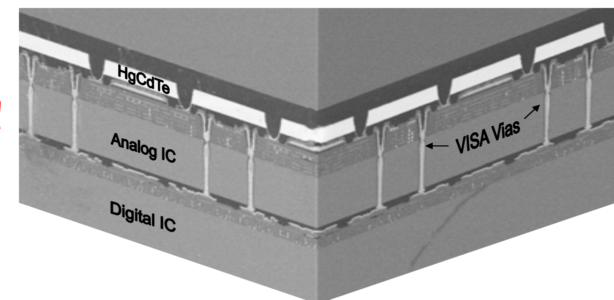


< NAND 12 Stacked Memory Card >



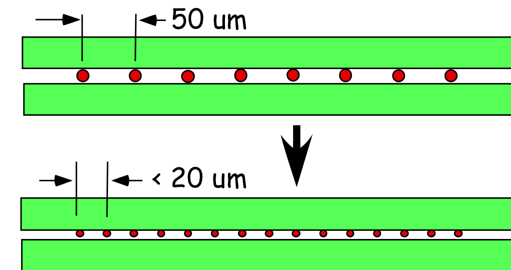
Samsung - 30 um laser drilled vias in 70um chips

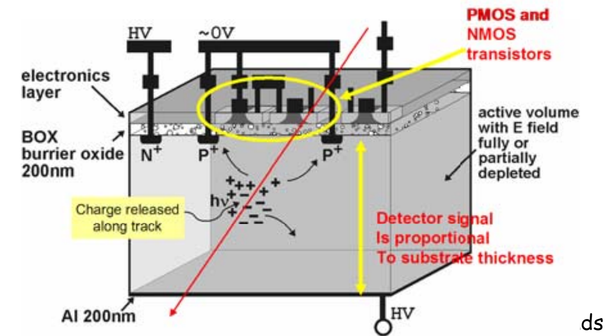
RTI Infrared Imager

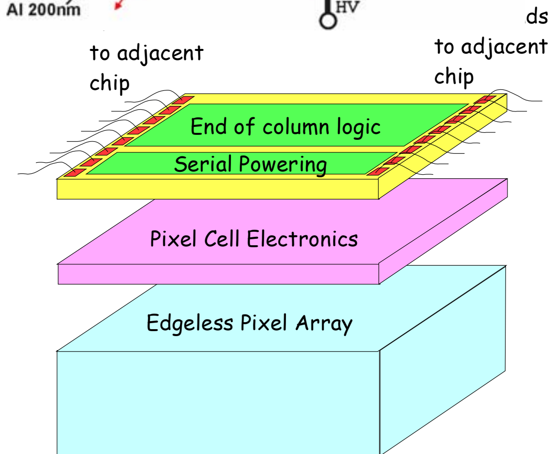


Possible Applications for 3D Technologies in HEP

- Replacement for pixel bump bonding
  - Finer pitch bonding
  - Lower cost bonding?
- SOI Detectors
- Higher performance pixel detectors
  - More functionality/ pixel
  - Smaller pixels
  - Mixed technologies

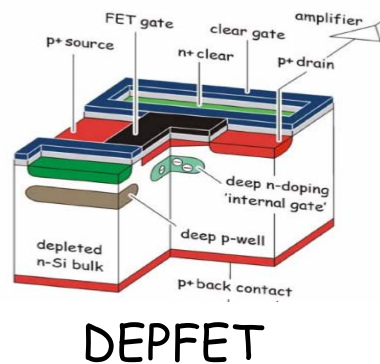




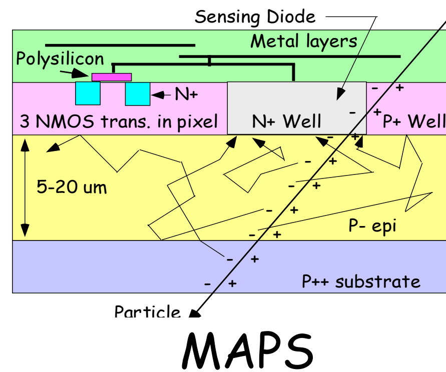


Mixed Technology HEP Applications

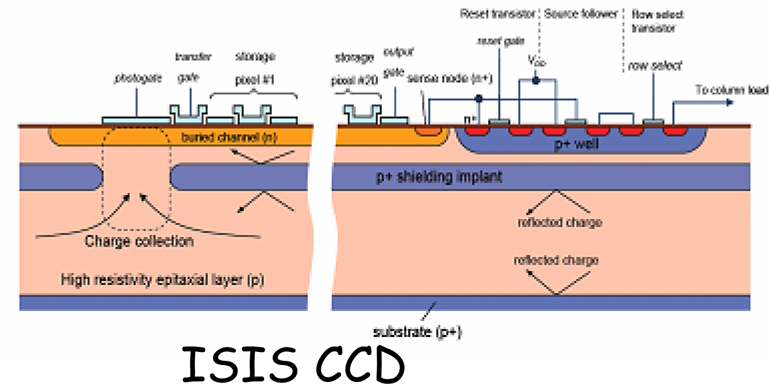
3D processing can be used to integrate parts fabricated in different technologies (DEPFET,CMOS, CCD, SOI)



DEPFET



MAPS



ISIS CCD

Advantages of 3D for mixed technologies in HEP

* DEPFET – Place peripheral CMOS electronics above DEPFETs
* MAPS – Reduce PMOS devices in MAPS. Place CMOS above.
* CCD – Place amplifier above each CCD (ISIS) pixel cell.

Mixed technology circuits can use either CMOS or SOI for upper levels. Most people not familiar with SOI.

1) SOI mostly used for high speed and low power applications.
2) No latchup and more immune to SEU (radiation tolerant).
3) SOI very promising for Monolithic Active Pixel detectors and 3D assembly.

SOI Wafer Fabrication

- SOI has a thin silicon layer for fabrication of CMOS circuits on top of a thin buried oxide (BOX) layer which is supported on a handle wafer.
- SOI wafers are very useful in 3D circuit integration and fabrication of SOI detectors
  - The handle wafer can be high resistivity silicon in which diodes are formed by implantation through the BOX.
  - Vias are formed through the BOX to connect the diodes in the substrate to the CMOS circuitry in the top layer
- SOITEC, France is a major producer of SOI wafers
  - Wafer diameter 100 mm -300 mm
  - SOI thickness 50 nm – 1 um (Smart Cut)
  - BOX thickness 100 nm – 3 um
- Discussion of how to best use SOI will follow later.

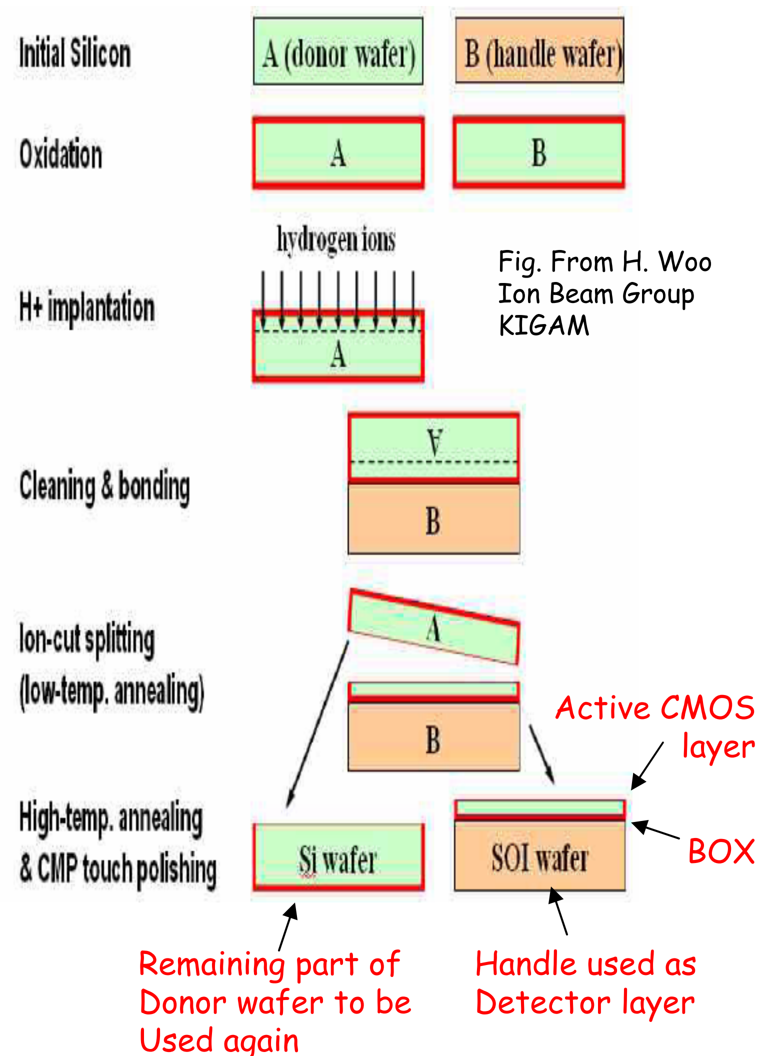


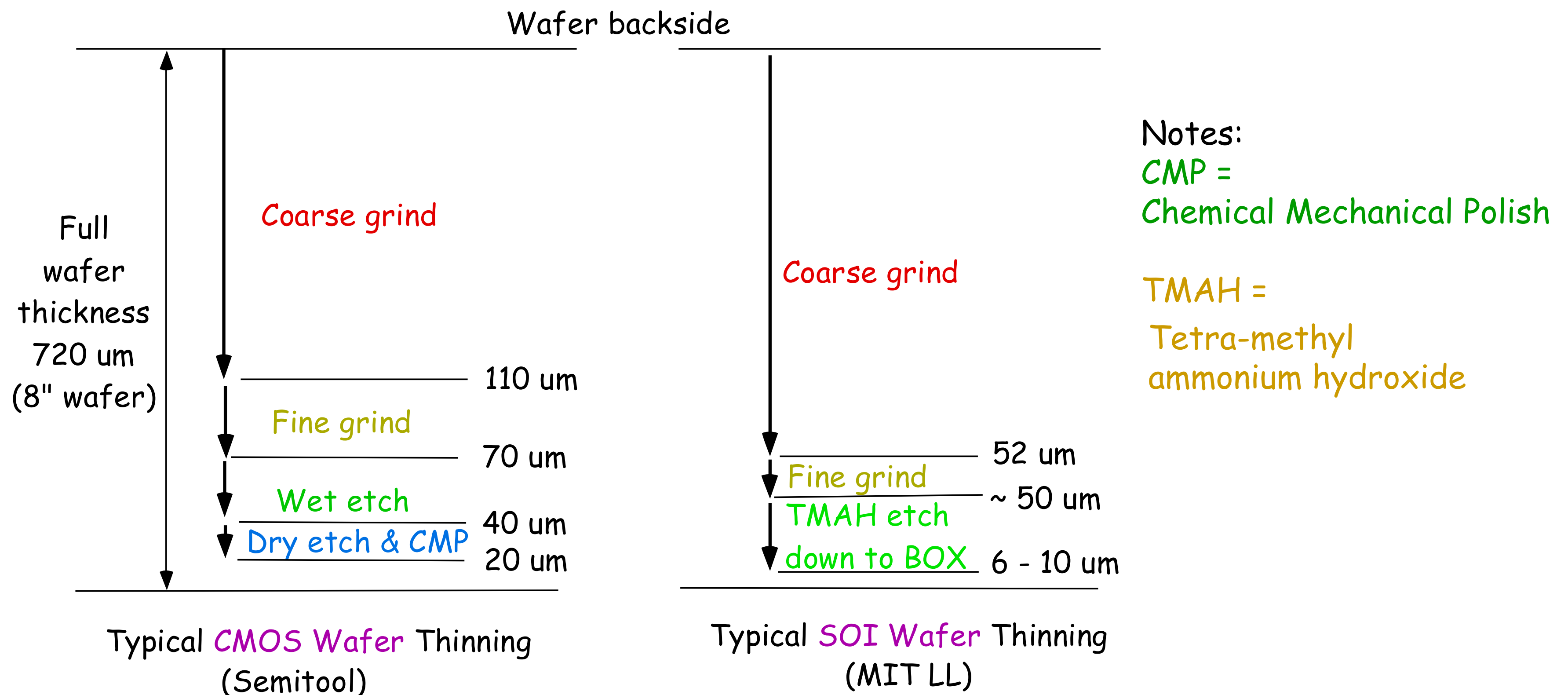
Fig. From H. Woo
Ion Beam Group
KIGAM

Consider Pixels for ILC and SLHC

- The needs for future pixel applications are somewhat different.
- ILC
  - Lowest mass possible, X_0 = 0.1%/layer
  - Very small pixels, approx 20 um x 20 um
  - Moderate radiation levels ~ 1.0 Mrads
  - Very low power
- SLHC
  - Lowest mass possible given cooling constraints
  - Moderately large pixels, 50 um x 250 um (ATLAS)
  - Very High radiation levels ~ 100 Mrads
  - Relatively high power dissipation due to continuous readout
- Look at the four key 3D technologies applied to ILC and SLHC
  - 1) Wafer thinning
  - 2) Interconnections, via formation and metallization
  - 3) Bonding, wafer to wafer or die to wafer
  - 4) Alignment

Wafer Thinning

Both CMOS and SOI wafers can be thinned to a point where they represent an insignificant fraction of a radiation length (X_0) for HEP experiments.

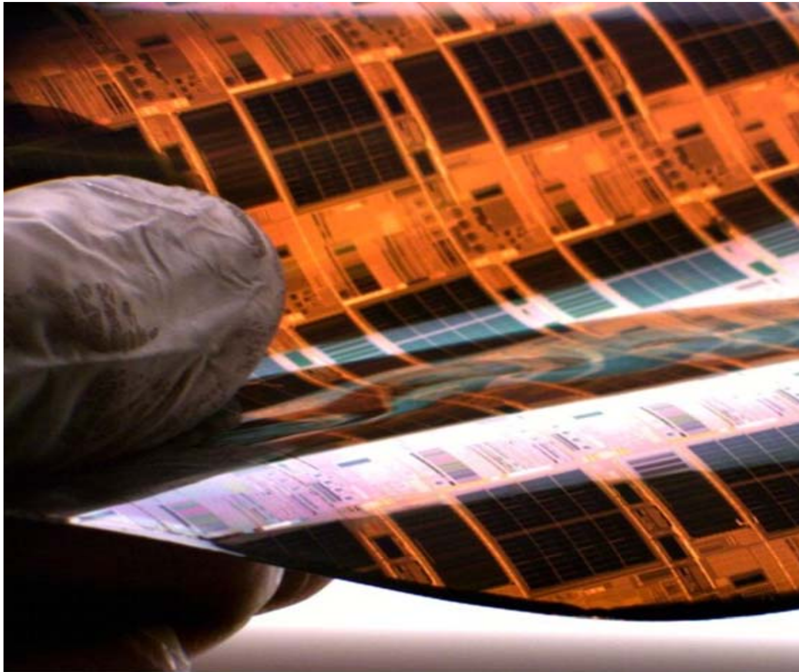


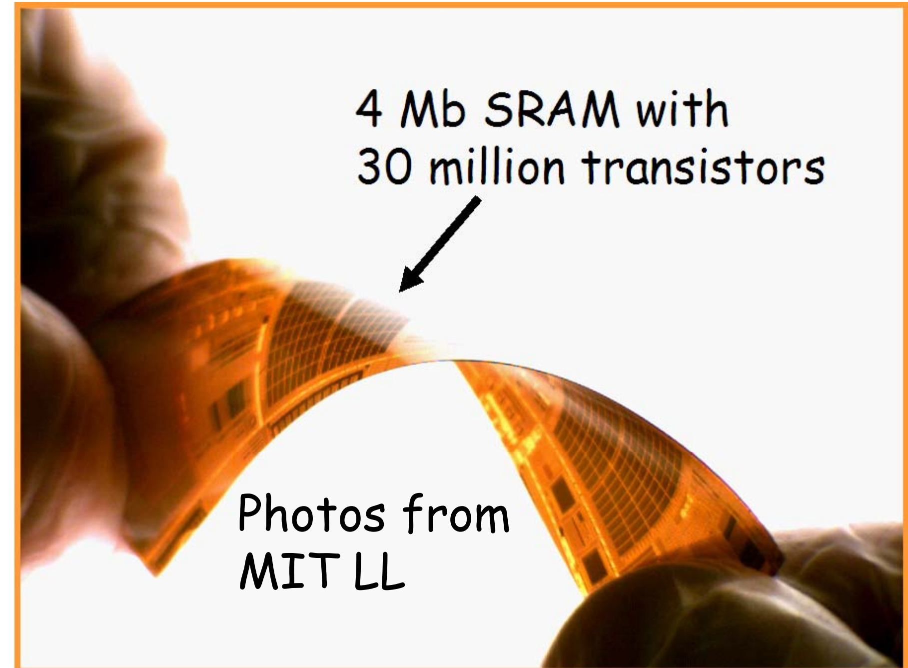
The thinner SOI wafers, however, can represent significant advantages for 3D circuit layout in some designs.

Wafer Thinning

Through wafer vias typically have an 8 to 1 aspect ratio for etched vias. Thus, in order to keep the area associated with the vias as small as possible, the wafers should be as thin as possible. This is critical for small pixel designs.

Thinned SOI wafer from MIT Lincoln Laboratory

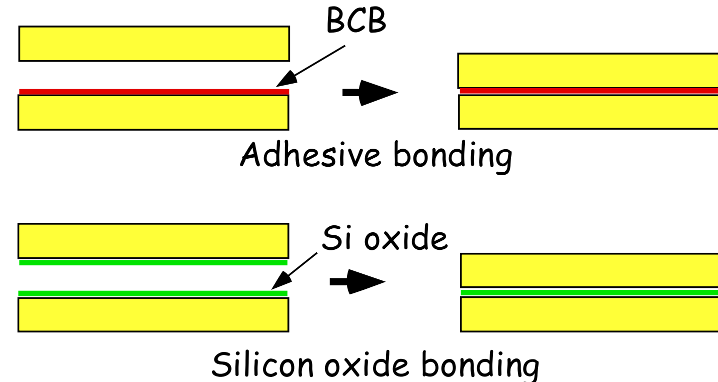




Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

Wafer to Wafer Bonding With Mechanical Bond Only

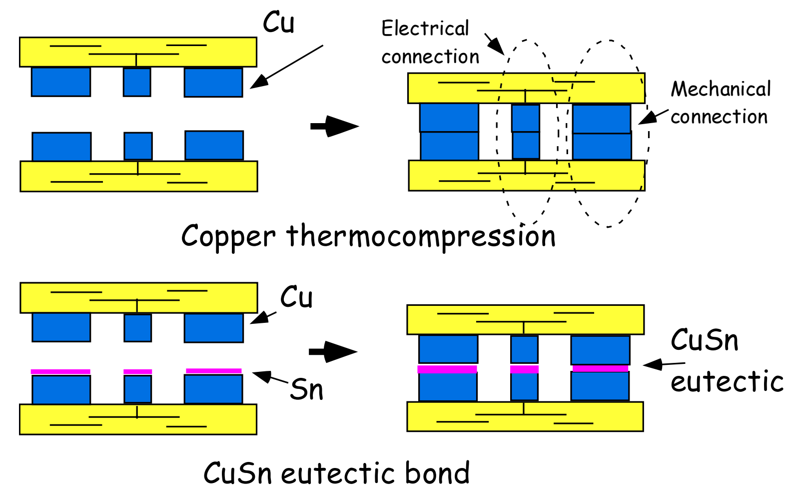
- Two processes available
  - Adhesive bond (has temperature limits)
  - Oxide bond (SiO to SiO)
- Excellent mechanical bond good for handling and further processing
- SiO bond is fast (better) compared to adhesives
- Cannot be used as a bump bond replacement - No electrical connections
- Electrical connections with filled vias are formed after bonding



- Could use capacitive or inductive coupling for transmitting signals between parts.
  - OK for very small signals (test inputs)
  - Normally either large areas or signal amplifiers are needed that require extra space – not good for high density circuit designs in HEP.
  - Vias may be needed for power anyway
- Used by IBM, MIT LL and others for 3D circuits with inter wafer vias.

Die/Wafer to Wafer Bonding by Means of Electrical & Mechanical Bonds

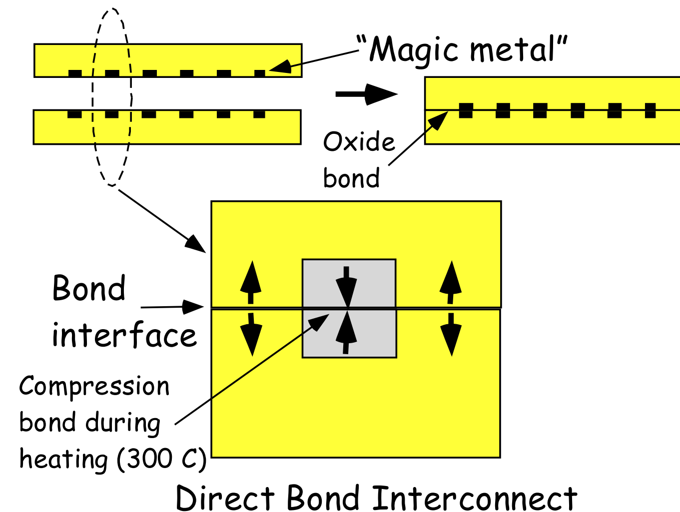
- Processes using metallic pillars
  - CuSn Eutectic
  - Cu thermocompression
- Can be used to replace bump bonding for face to face bond between parts
- Mechanical bond strength is dependent on percent of surface area used for bonding
  - Most applications to date have had large coverage (~75%)
- Good alignment is more difficult since parts have to be held in place during heating process
- Used by IZM, RTI, and others



- Pillars on each part to be bonded are typically 5 um tall
  - 10 um of copper covering 75% of bond surface represents 0.075 Xo
    - Unacceptable for ILC
    - Large coverage can create unwanted paracitics
    - Could be acceptable for SLHC
  - Need to reduce copper to ~10% coverage for ILC
    - 10% may not provide sufficient mechanical strength
    - 10% coverage may result in very uneven surface for thin parts
    - Under fill with BCB may be necessary for strength and support

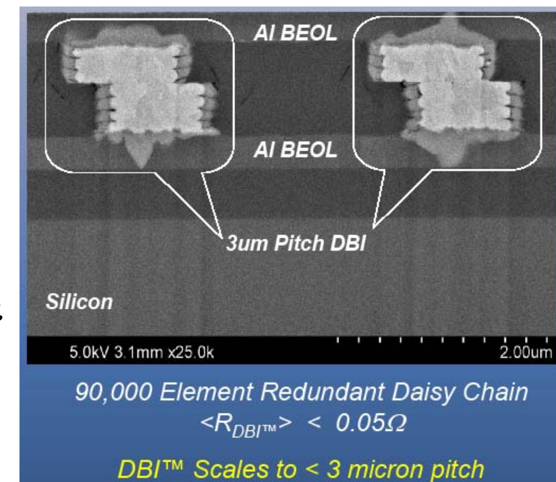
Die/Wafer to Wafer Bonding by Means of Electrical & Mechanical Bonds

- Direct Bond Interconnect (DBI)
  - Oxide bond between devices forms immediate bond
  - After oxide bond reaches sufficient strength, devices are heated and the metallic compression bonds are formed.
  - Provides minimal metal needed to form electrical connections.
    - Provides extremely low Xo and is excellent choice for ILC
    - Metal bond ~ 1 um x 1 um
    - May not be necessary for other less critical applications (SLHC)
  - No surface warping when using thin parts
- Can replace bump bonds in a face to face connection.
- Is used for 3D integration in a back to face connection or face to face connection.
- Process is currently only offered by one vendor – Ziptronix, in North Carolina.



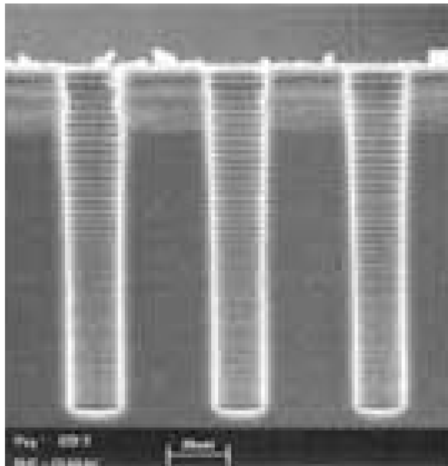
Direct Bond Interconnect

3 um pitch DBI bond (Ziptronix, 3D Conference Oct, 2007)[2]

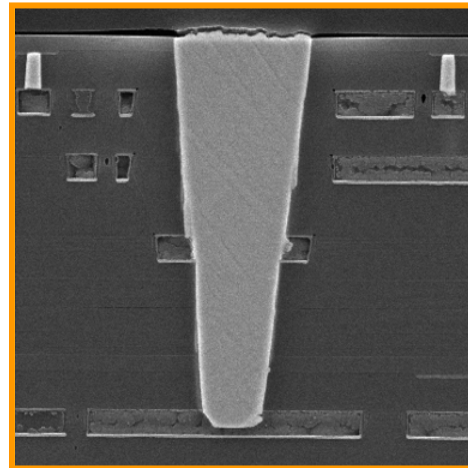


Through Wafer Vias and Metallization

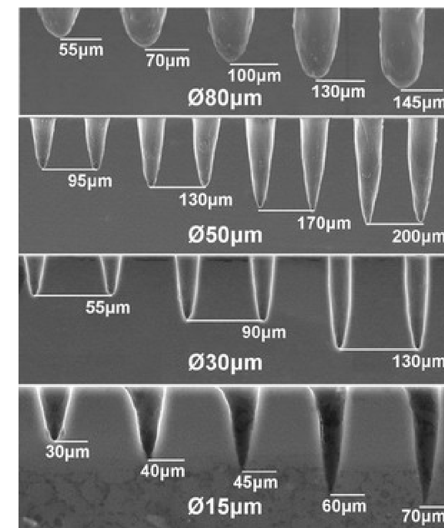
- Small diameter vias are critical for high circuit density circuits like ILC. (Smallest vias (< 5 um) use DIRE or oxide etch)
- SOI lends itself to smaller vias since layers can be thinner.
- Passsivation
  - Vias in CMOS must have via holes passivated (extra step) to prevent short circuits.
  - Vias in SOI require no passivation before metallization.



SEM of 3 vias In CMOS using Bosch Process[3]



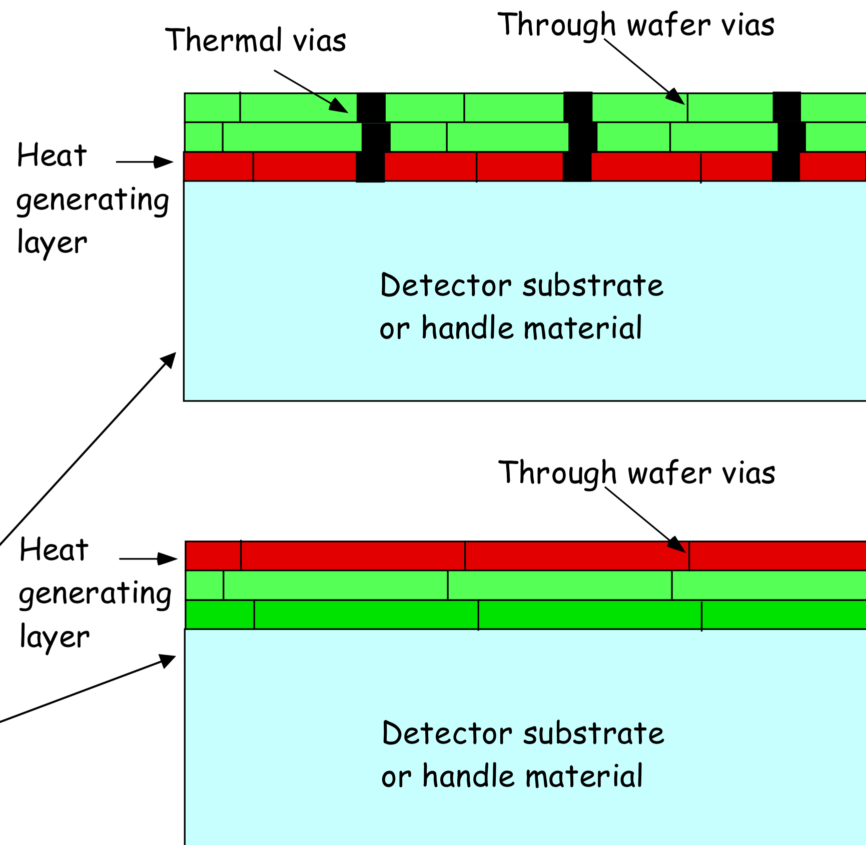
Filled via using oxide etch process in SOI (Lincoln Labs)



Laser drilled vias down to 15 um dia by Xsil

Heating Considerations

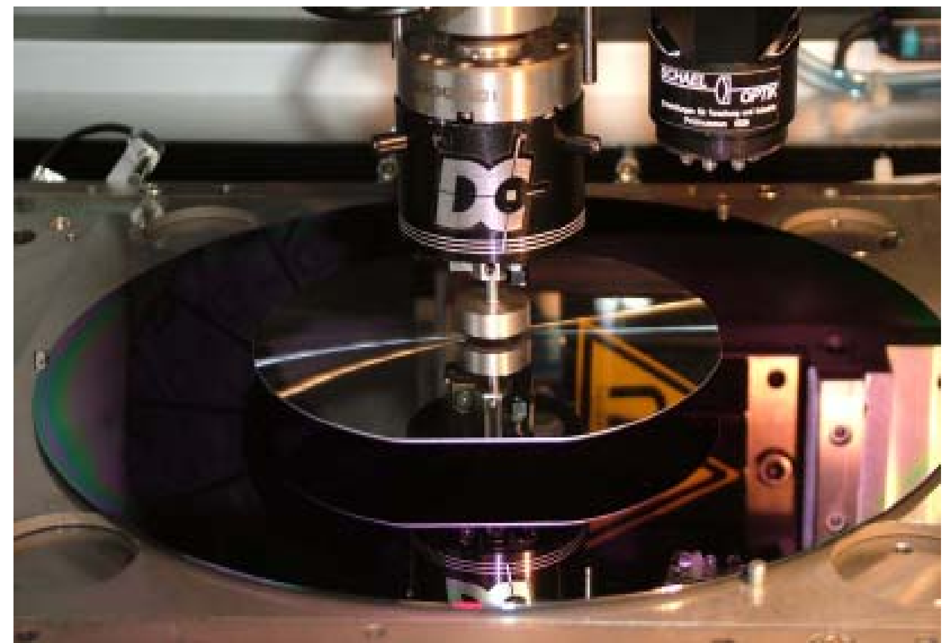
- Separate thermal vias may be needed when stacking many layers.
  - Thickness and number of layers (SOI layers are thinnest)
  - Location of heat producing components
- ILC must have minimal power – No thermal vias needed due to extremely low power density
- SLHC projects have higher power due to continuous operation.
  - May need thermal vias
  - Place heat producing components (analog) on top layer or nearest to a heatsink



Last Key Element - Alignment

- 1 micron alignment (3 sigma) has been achieved for both wafer to wafer and die to wafer bonding (MIT, Ziptronix, IBM, others)
- Die to wafer will provide best yield for HEP and is better suited to layouts with different arrangements of die on a wafer.

1 Mpixel, 8 um pitch die being mounted to 200 mm "ROIC" wafer



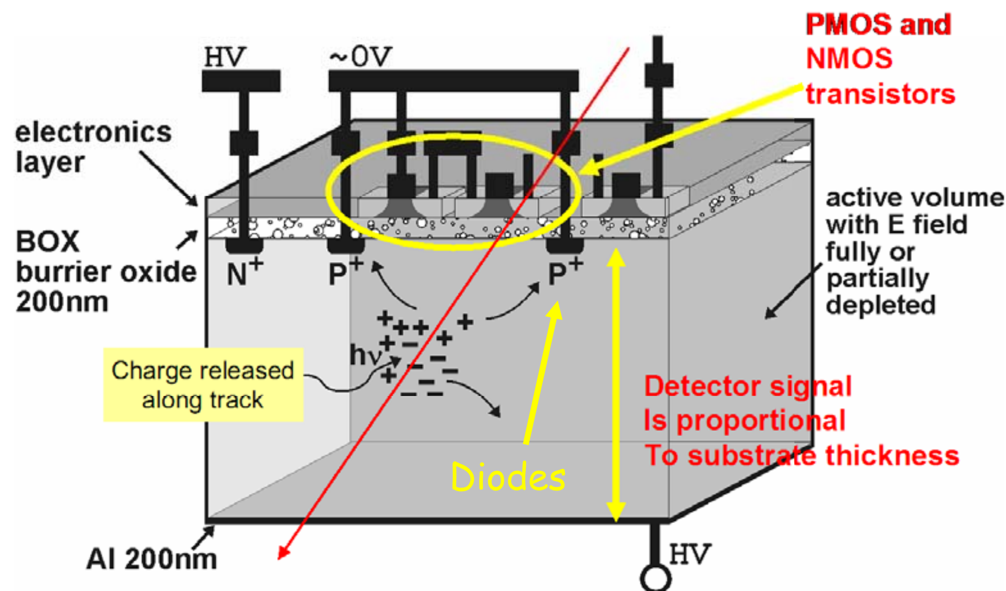
Wafer to wafer alignment and Placement (Photos by Ziptronix)

Active Pixel Sensor in SOI

SOI detectors are a first step toward 3D integration since it uses many of the same processes as 3D integration. (oxide bonding, wafer thinning, via formation)

- Thin top layer with silicon islands in which PMOS and NMOS transistors are built.
- A buried oxide layer (BOX) which separates the top layer from the substrate.
- High resistivity substrate which forms the detector volume.
- Diode implants are formed beneath the BOX and connected by vias.

The raw SOI wafers which have the CMOS layer bonded to the substrate layer are procured from commercial vendors such as SOITEC in France.



Advantages:
* 100% fill factor in pixel
* NMOS + PMOS transistors
* Large signal
* Faster charge collection
* Less charge spreading
* SOI features:
  - No latch up
  - Low power

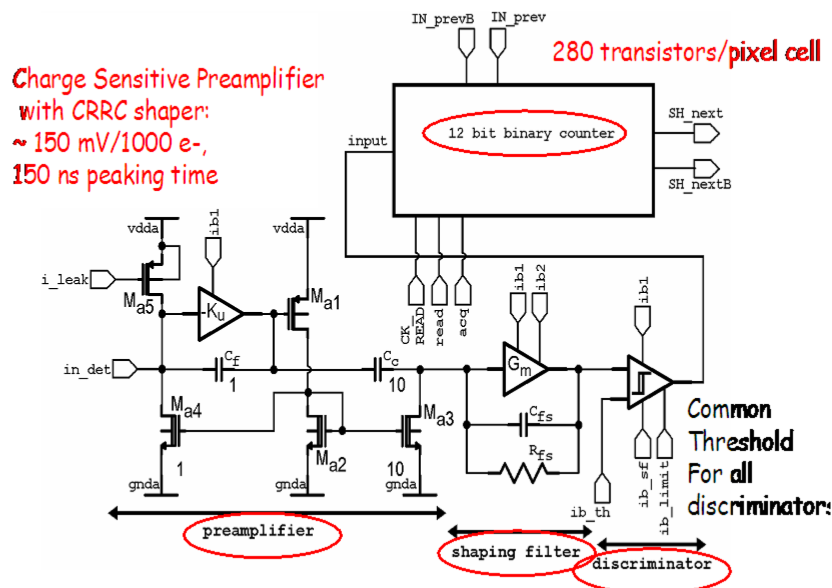
SOI Detector Multiproject Run

- Two multiproject runs to OKI have been coordinated by Yasuo Arai at KEK.
- Recent meeting in Hawaii during NSS brought all designers together to discuss their results and prepare for the next multi-project run.
  - KEK – photon counting array
  - University of Hawaii – pixel array for Belle upgrade
  - LBNL – study of simple pixel arrays
  - ISAS – A/D converter design
  - Fermilab – photon counting array (MAMBO)

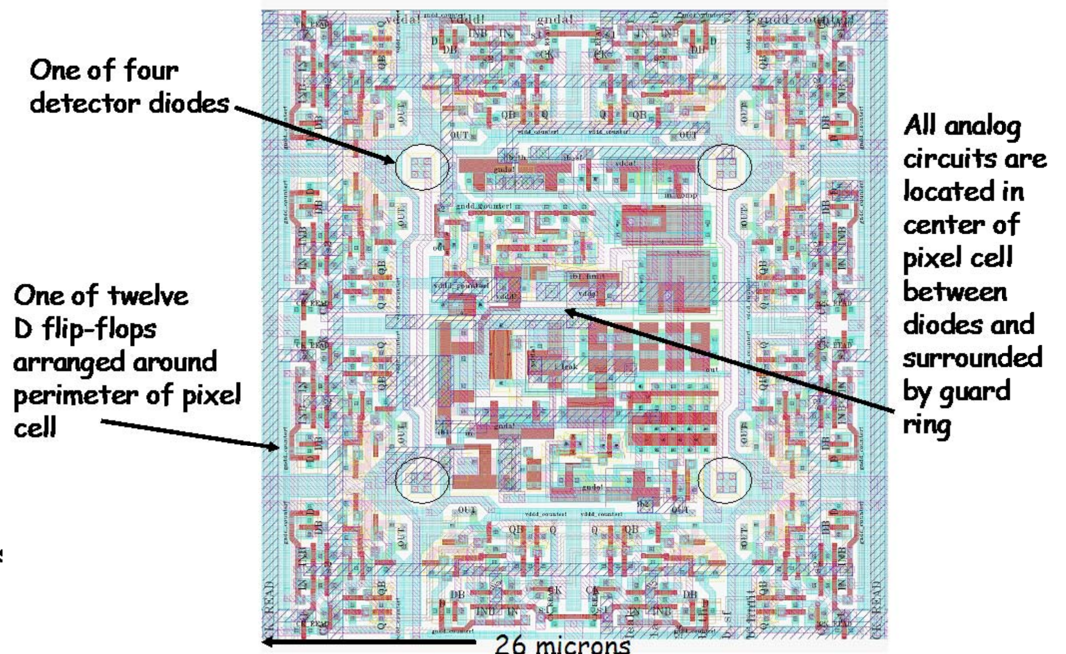
Fermilab Pixel Sensor in SOI Process

Design done in OKI 0.15 um multi-project run coordinated by Y. Arai at KEK. [4]
MAMBO – Monolithic Active pixel Matrix with Binary Output. [5]
Imaging detector for direct detection in electron microscopy (TEM), and soft X-rays.
Designed for counting applications

- 64 x 64 pixel array, 26 µm pitch, 4 parallel diodes/pixel (spaced 13 µm apart).
- Each pixel has CSA, CR-RC2 shaper, discriminator + 12 bit binary counter.
- The counter is reconfigurable as a shift register for serial readout of all pixels.



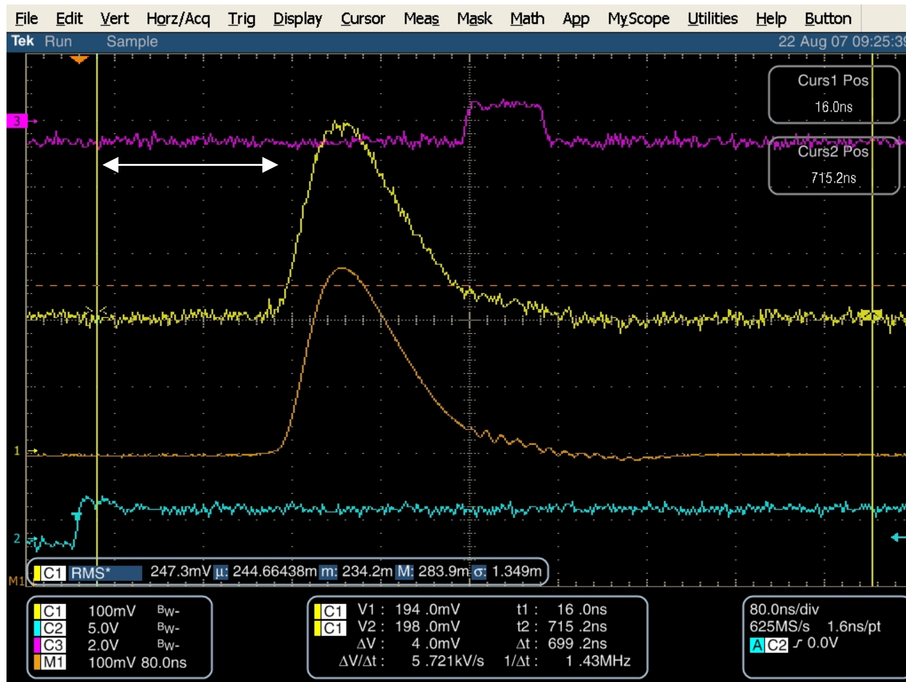
Single pixel schematic

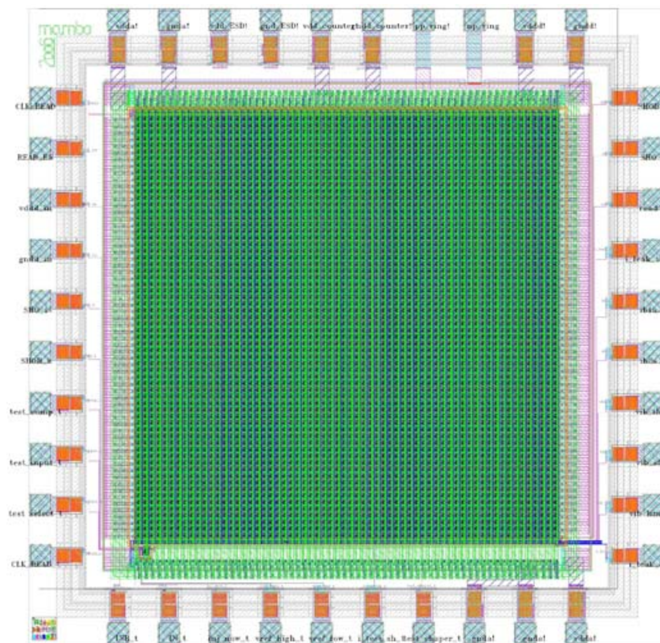


Single Pixel Layout

Test results

Analog section working with charge injection circuit
Gain lower and shaping faster than expected
Counter/shift register working (needs back gate voltage for proper operation)
Discriminator working
Backgate voltage problems have prevented simultaneous operation of the front end and back end electronics.

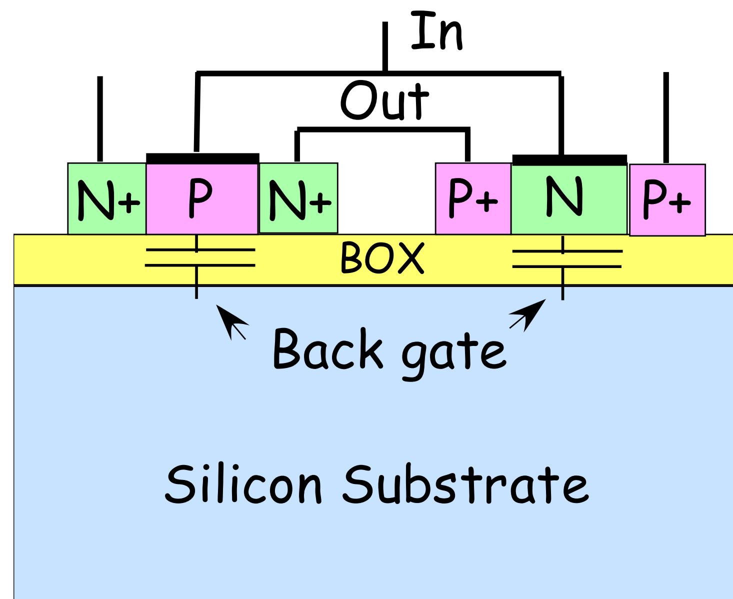




64 x 64 array in pad frame

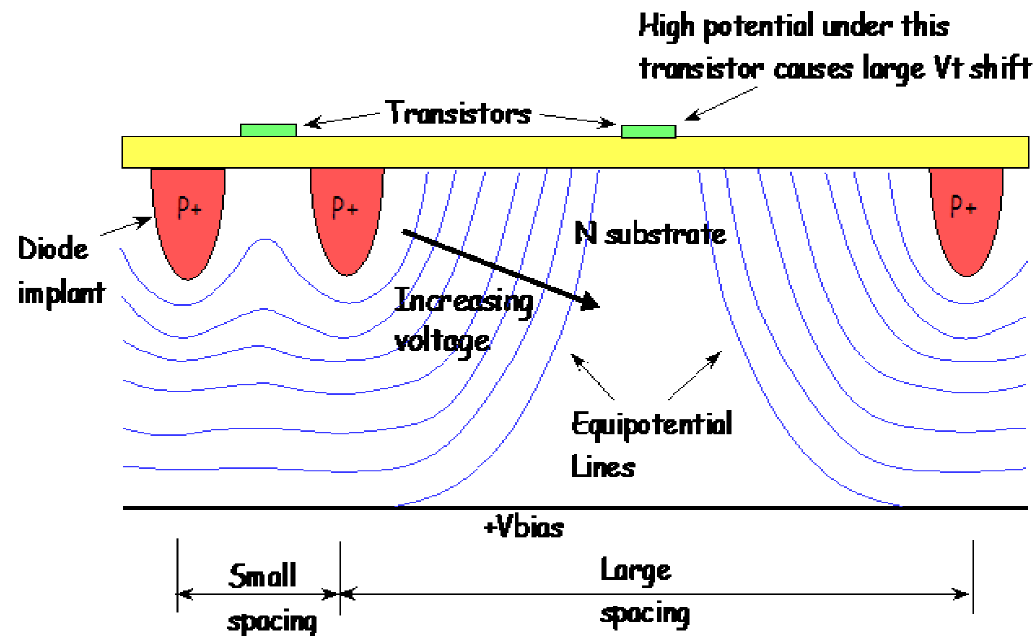
Potential Problems for SOI Detectors

1) The BOX (Buried Oxide) acts as a back gate for the NMOS and PMOS transistors. The BOX is thick enough (200 nm) to trap charge from ionizing radiation and cause Vth shifts. (The Vth shifts can be fully corrected by adjusting the substrate/back gate potential). [3]



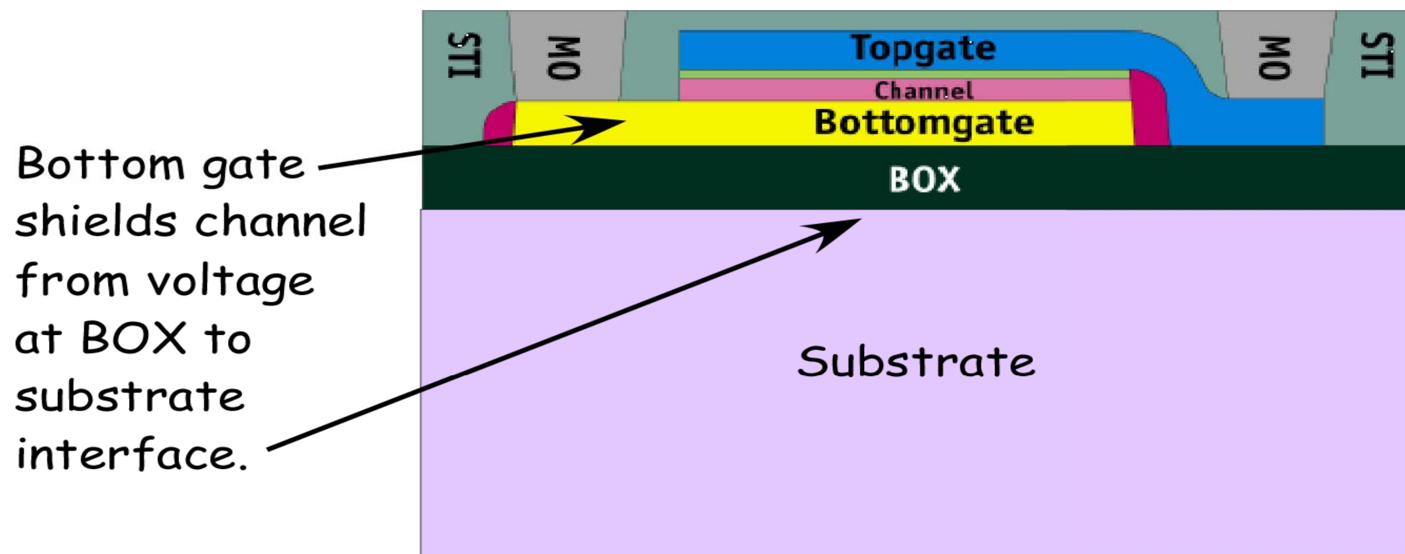
Although Vth shift due to radiation has been corrected at the 1 Mrad level, operation at 100 Mrad and may be a serious problem for SLHC applications. More measurements are needed for these HEP applications.

2) The back gate voltage affects the transistor threshold voltage in a manner similar to the top gate. The voltage on the back gate of transistors and hence Vth is affected by the distribution of the diode contacts which affects back gate potential.

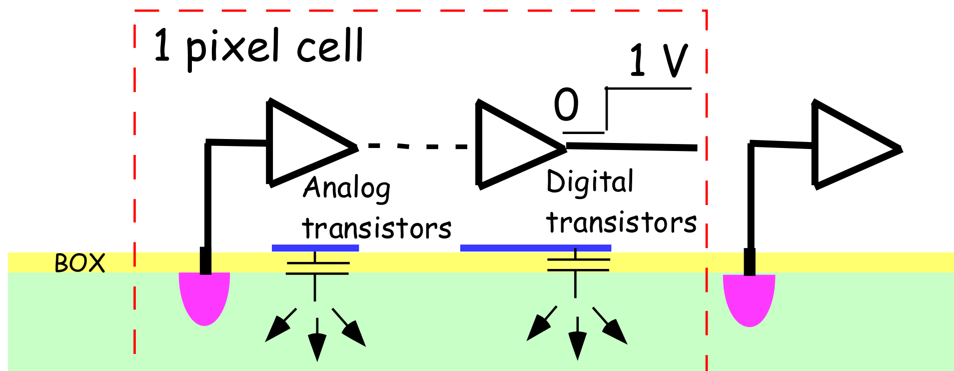


This problem can be solved by placing p+ implants relatively close together or by use of Flexfet transistors as shown on the next slide.

- ASI (American Semiconductor Inc.) has a process based on dual gate transistor called a Flexfet.[6]
  - Flexfet has a top and bottom gate.
  - Bottom gate shields the transistor channel from voltage on the substrate and thus removes the back gate voltage problem.
  - Bottom gate also shields the transistor channel from charge build up in the BOX caused by radiation.



3) The Box is relatively thin, permitting the circuit to capacitively inject charge into the substrate which is collected by the sensing diodes.



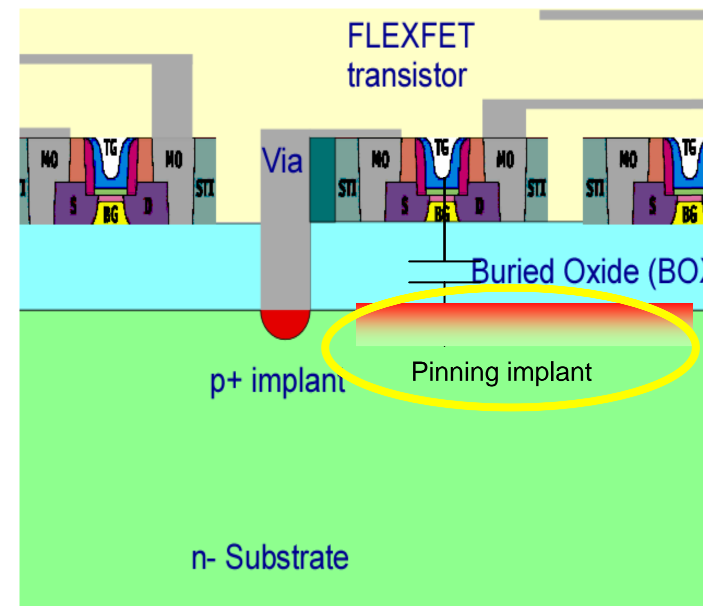
Charge is injected through the BOX by transistors or metal traces on or near the top of the BOX. The charge is collected by the offending pixel, neighbor pixels, and the backside contact. 1 um x 1 um of material on top of a 200 nm BOX with a 1 v swing injects 1035 electrons into the substrate. The amount collected by a P+ implant is dependent on the location of the injection point.

Note: capacitive coupling should be considered whenever layers are very close to the detector. (Bump bond spacing is helpful.)

Problem can be mitigated by
a) Using thicker BOX
b) Using differential signals
c) Dividing circuit design into two tiers such that there is no electrical activity above the BOX during the signal acquisition period.
d) Add a pinning layer as shown on the next slide.

Pinning Layer

- SOI detectors are sensitive to capacitive coupling of CMOS signals to the pixel diode.
  * Adding a “pinning” layer at the surface of the substrate, between pixels, tied to a fixed potential can reduce the problem.
- 2D / 3D Silvaco device simulations confirm effectiveness of pinning layer.
- However, pinning layer can also increase capacitance, make depletion harder, and trap charge. More study needed.
- Available in ASI, MIT-LL Process



3D Examples

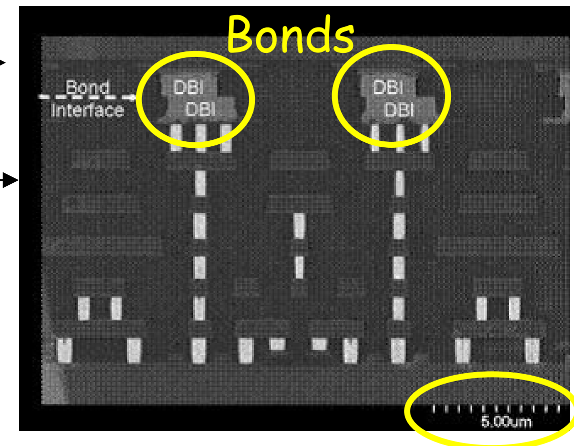
- There are many articles on 3D technologies and their future
- There are far few descriptions of actual circuits.
- Circuits examples
  - Industry
    - Raytheon
    - RTI
    - MIT Lincoln Laboratories
    - Rensselaer Polytechnic Institute
  - HEP
    - FNAL

Raytheon Megapixel Image Sensor[7]

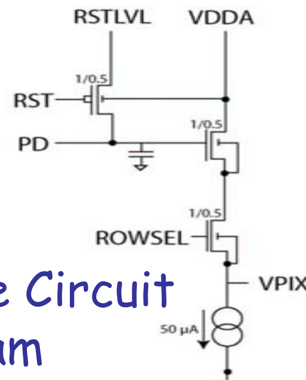
- 1 Megapixel array, 8 μm pixel pitch
- 2 tiers
- Die to wafer stacking
- 100% diode fill factor
- Tier 1 - pin diodes
- Tier 2 – 0.5 um SOI CMOS
- 2 μm diameter face to face bonds
- DBI (Oxide-oxide, and metal bonding)
- 1 million 3D vias
- 100% pixel operability
- Replacement for fine pitch bump bonds and/or minimal mass interconnects

Pin diode layer

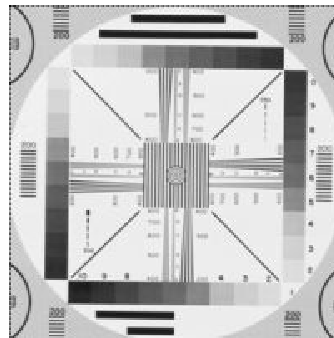
0.5 um CMOS
5 metal layers



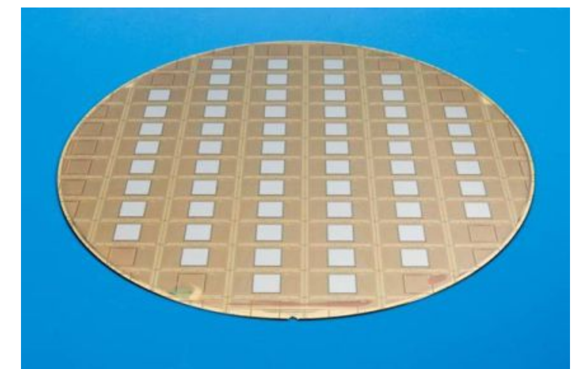
SEM Cross section



Simple Circuit Diagram



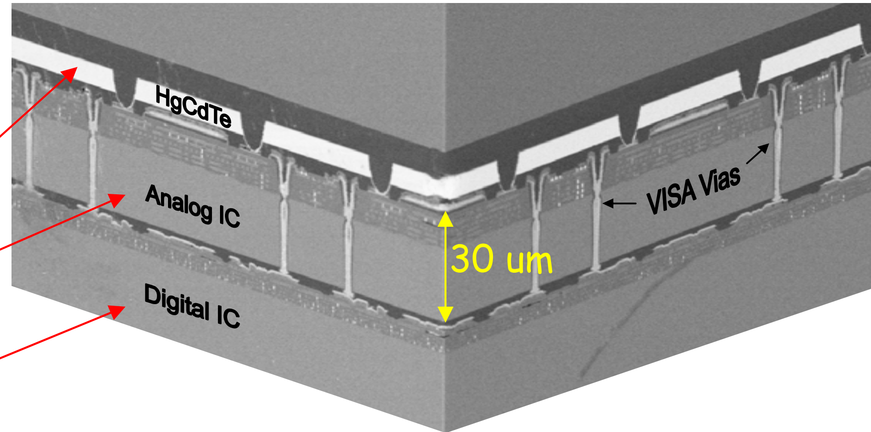
Captured Image



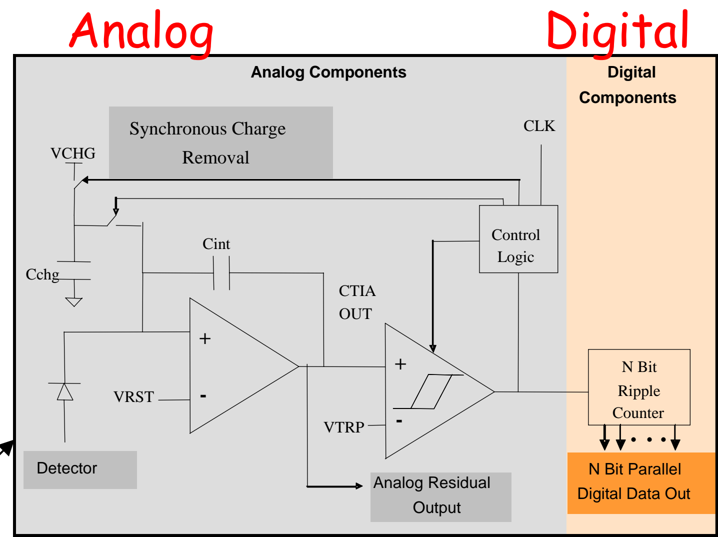
Die placed with 1 um accuracy

RTI 3D Infrared Focal Plane Array[8]

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Analog
Digital



Diode

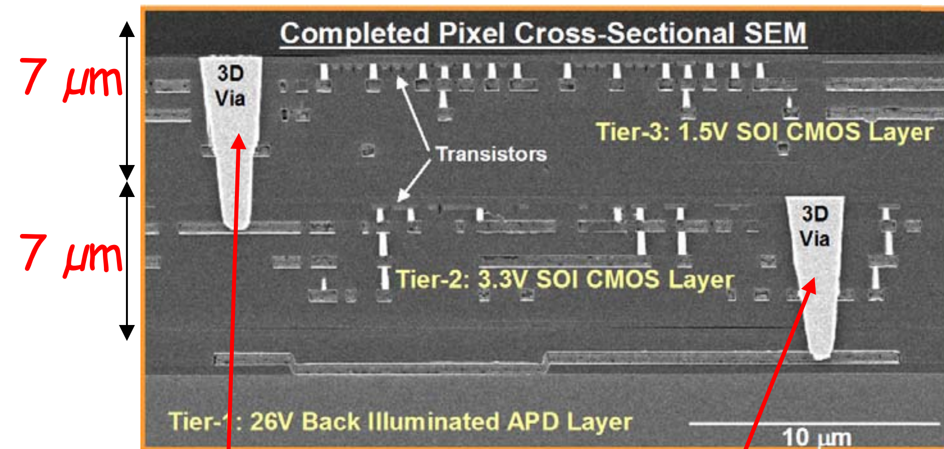
3 Tier circuit diagram

Infrared image

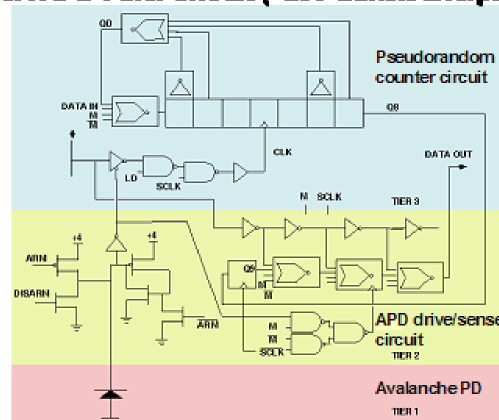
MIT LL 3D Laser Radar Imager[9]

64 x 64 array, 30 μm pixels
3 tiers
- 0.18μm SOI
- 0.35 μm SOI
- APDs in substrate layer

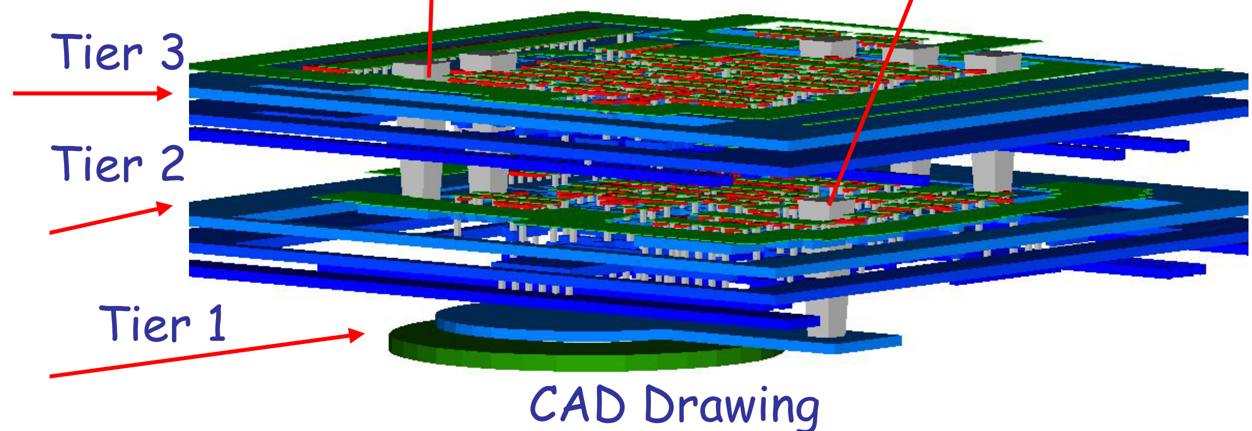
Oxide to oxide wafer bonding
1.5 μm vias, dry etch
Six 3D vias per pixel



SEM Cross section



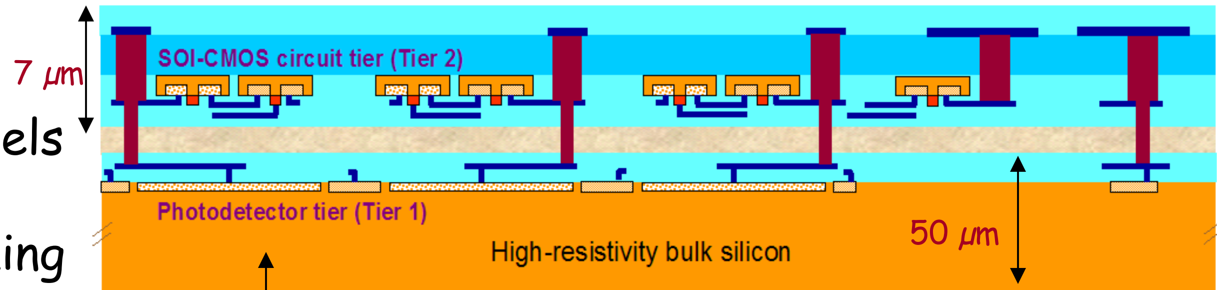
Schematic

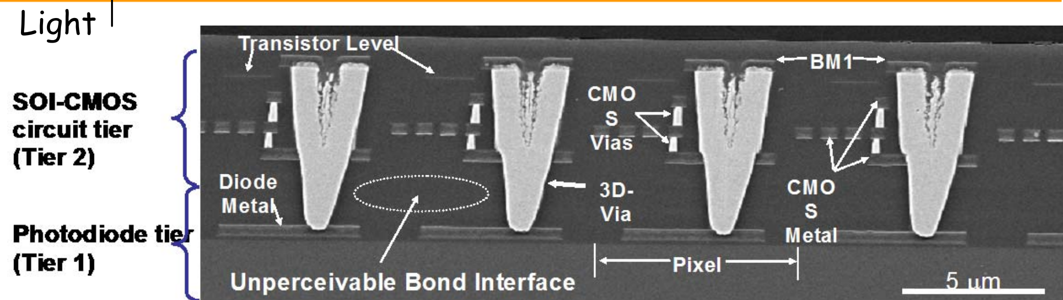


CAD Drawing

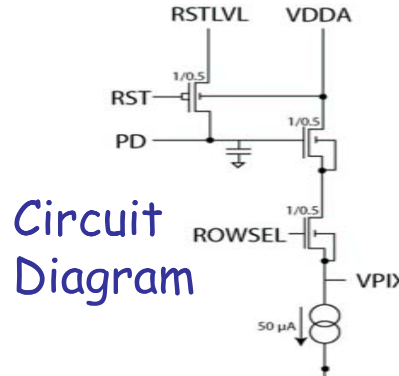
MIT LL3D Megapixel CMOS Image Sensor[10]

- 1024 x 1024, 8 µm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 µm thick
- Tier 2 – 0.35 um SOI CMOS, 7 µm thick
- 2 µm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





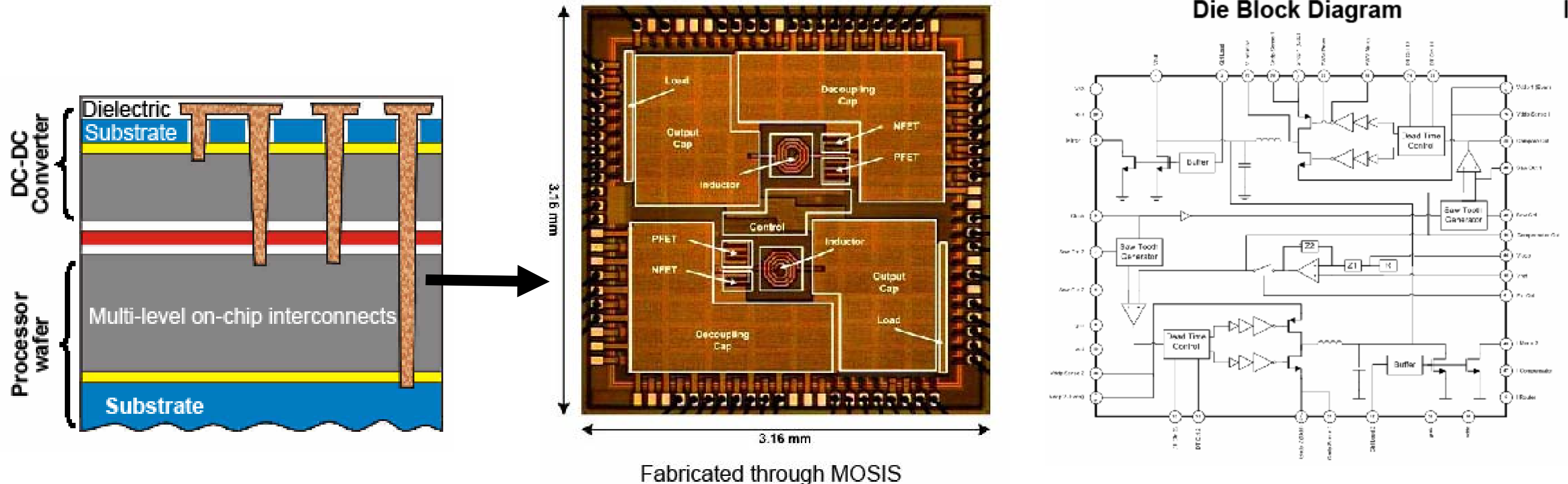
Drawing and SEM Cross section



Circuit Diagram

Image

Monolithic 3D Power Delivery Using DC-DC Converter[11]



Monolithic DC-DC Converter designed at RPI for vertical integration

- Minimizes interconnect parasitic effects
- Easy to supply and distribute multiple supply voltages
- Significantly reduced package pin count
- Uniform, high density power and ground vias to 3D chip

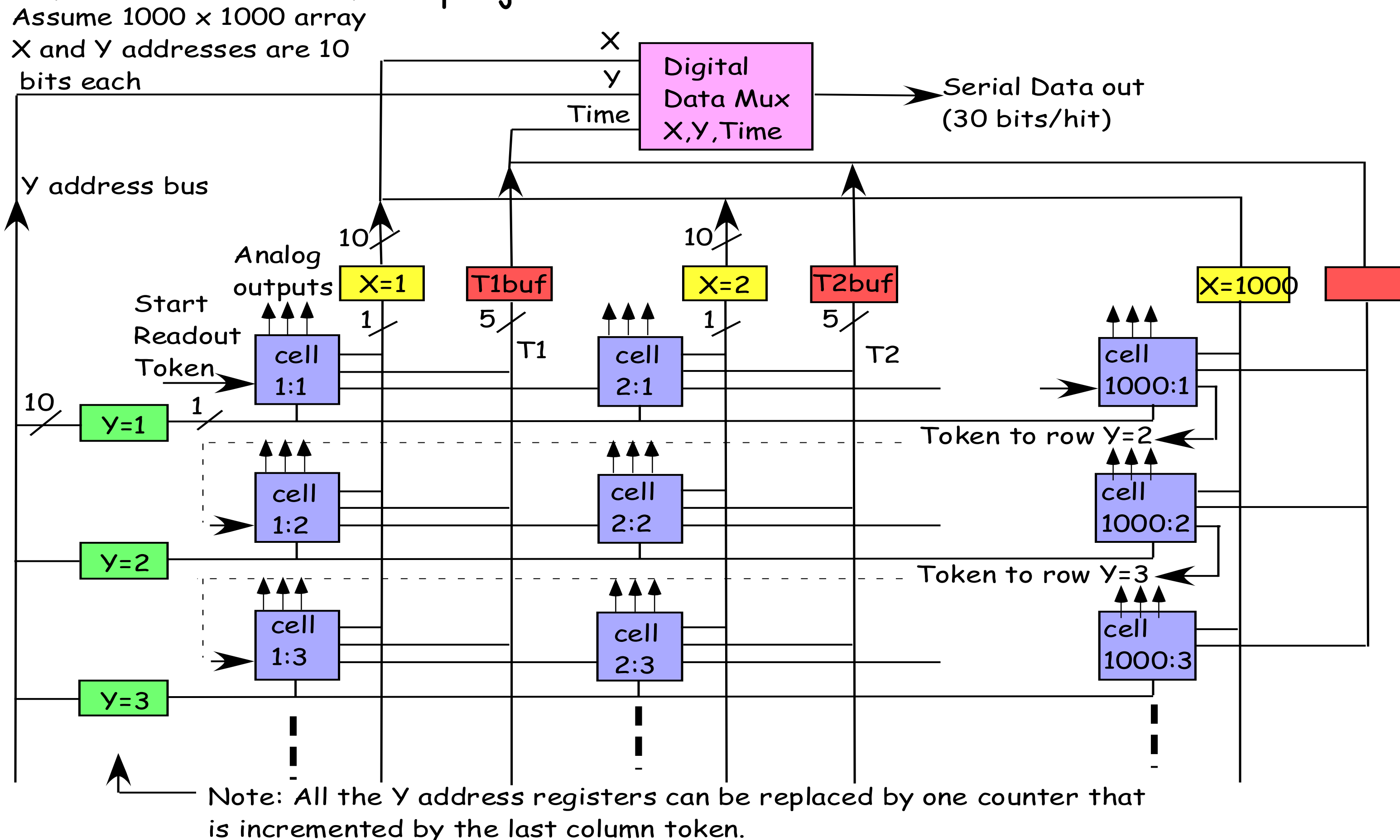
Prototype design shows that monolithic DC-DC converters with power for 3D circuit is possible.

3D Multi-Project Runs

- MIT Lincoln Labs has fabricated several 3D devices.
- MIT LL has also offered two multi-projects runs thus far.
- Fermilab joined the second MPW to explore the possibilities for HEP
- Fermilab will also participate in the next MPW run at MIT LL.

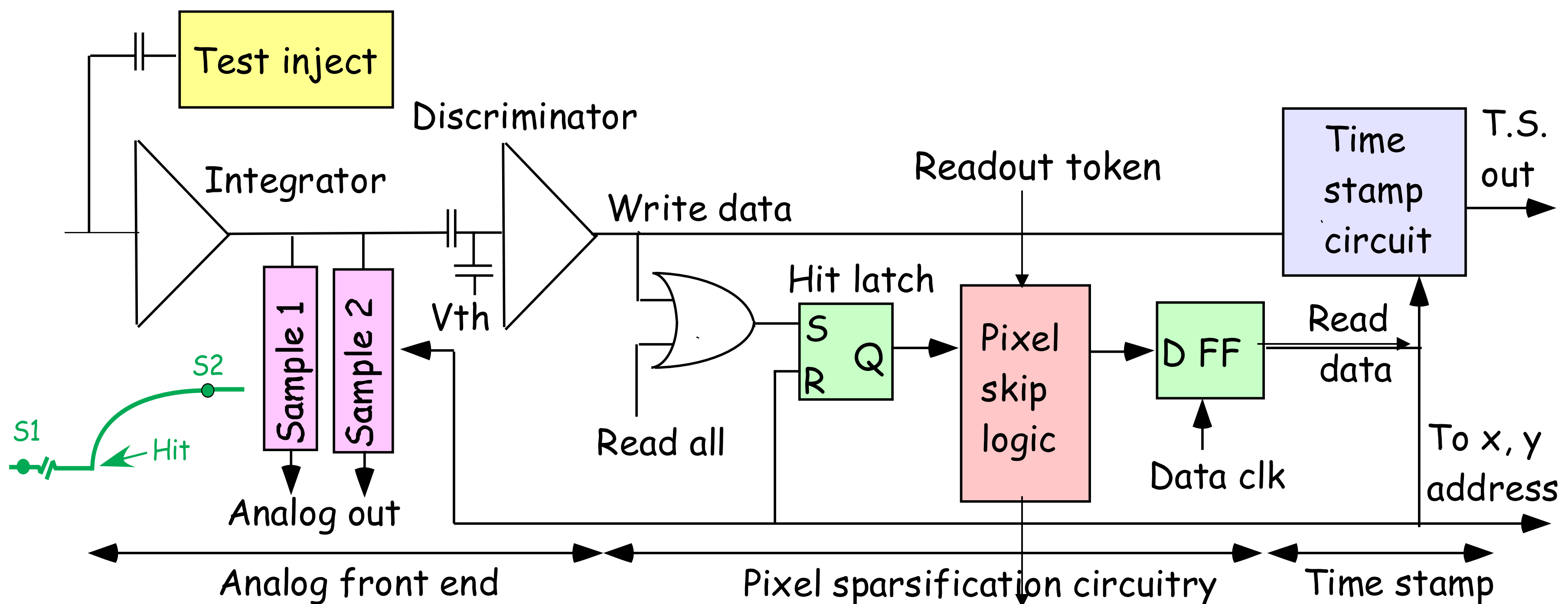
VIP1 - A 3D Pixel Design for ILC Vertex[12]

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
  - Key features: Readout between bunch trains, analog pulse height, sparse readout, high resolution time stamps (~1us), test inputs, 20 um pixels. - Meets all ILC critical requirements.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- 64 x 64 pixel demonstrator version of 1k x 1K array.
- Submitted to 3 tier multi project run. Sensor to be added later.



Simplified Pixel Cell Block Diagram

- When a Hit occurs, the Hit pixel stores Sample 1 & 2 and the Time Stamp, and sets the Hit Latch in sparse readout circuit.
- During readout, when the read out token arrives, the time stamp and analog values are read out, and pixel points to hit address found on perimeter of chip.
- While outputting data from one pixel, the readout token is passed ahead looking for next pixel that has been hit.

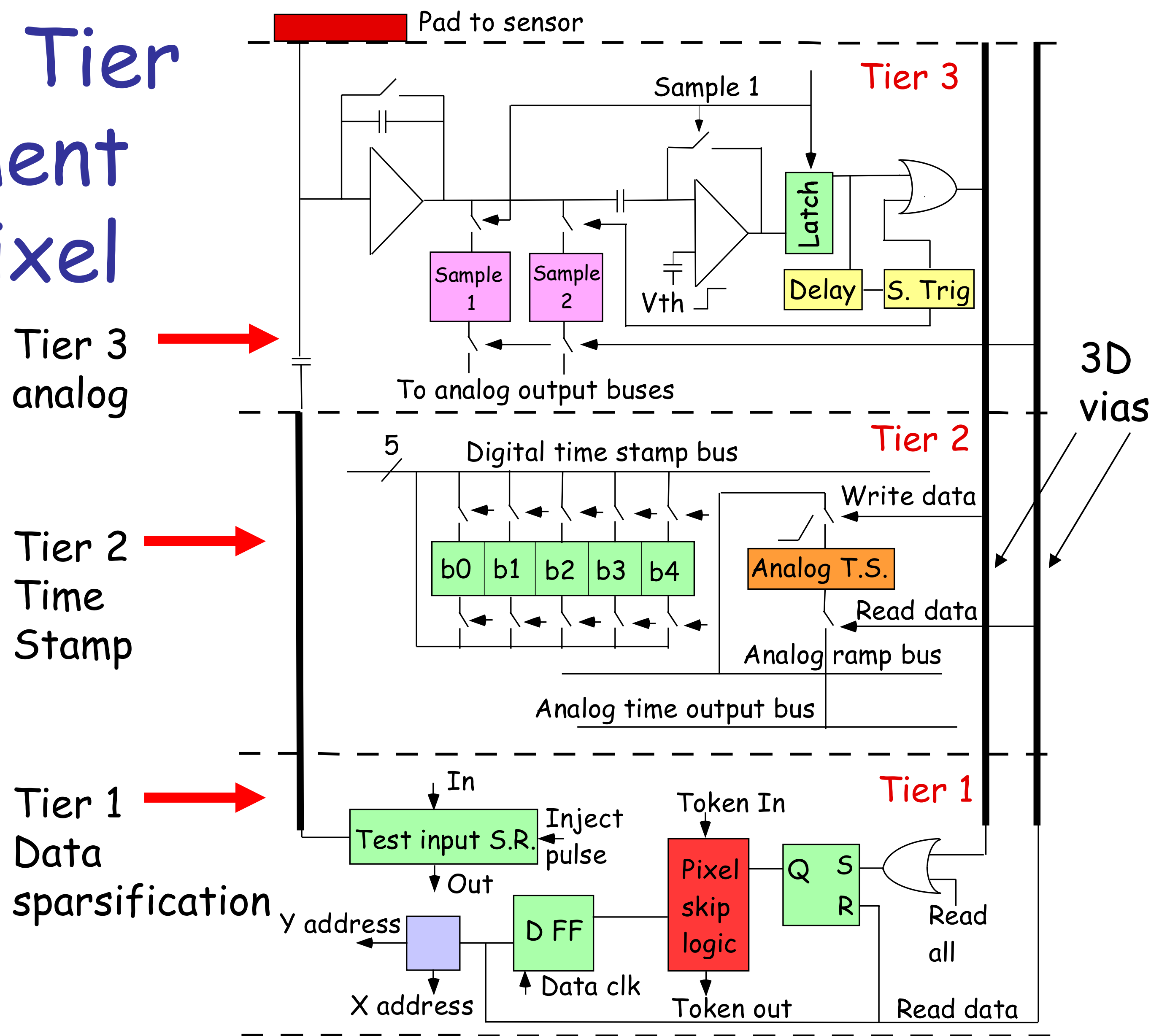


3D Three Tier Arrangement for ILC Pixel

Tier 3 analog

Tier 2 Time Stamp

Tier 1 Data sparsification

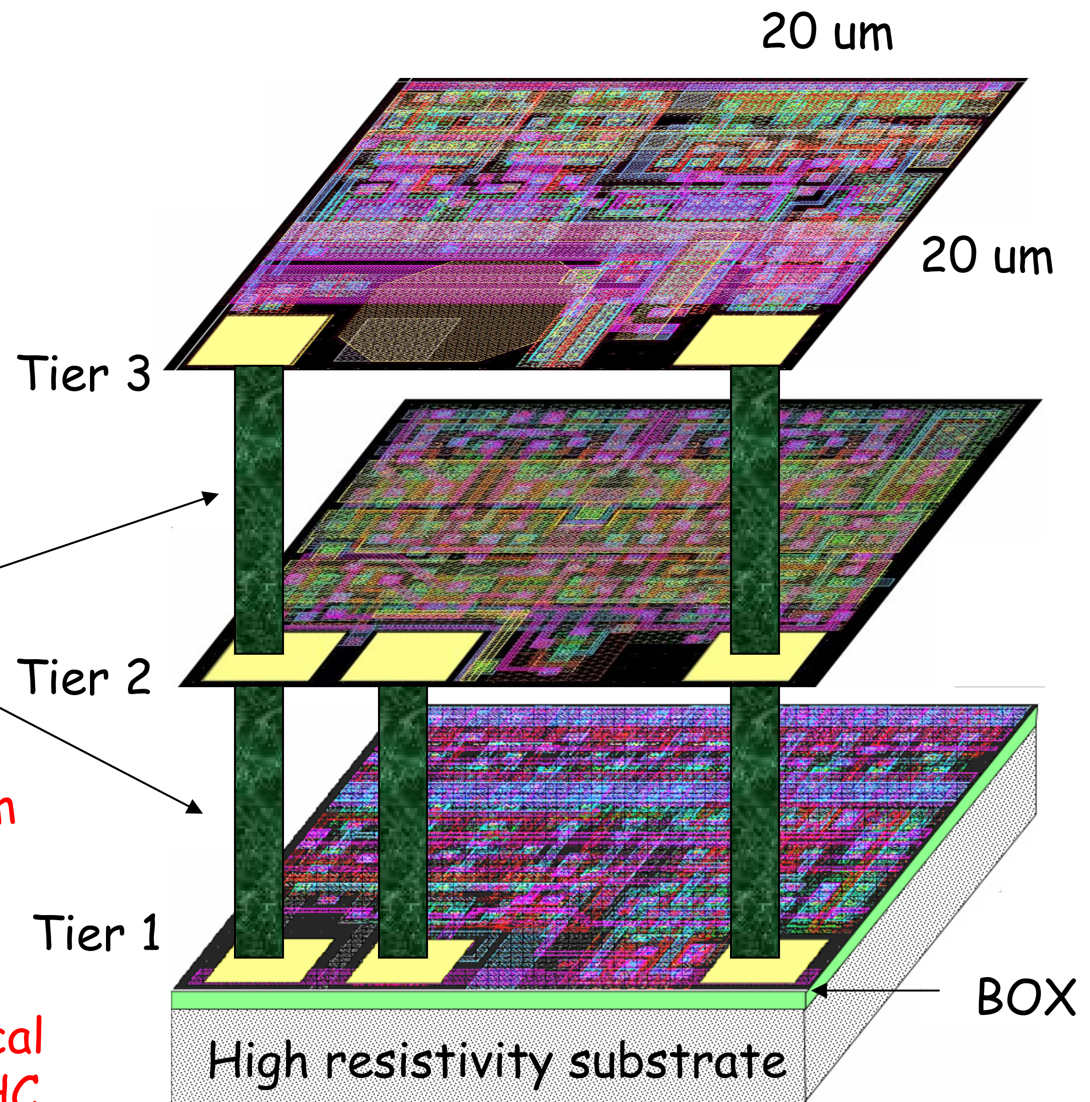


Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff

3D Stack with Vias for One Pixel

Pixel cell:
*175 transistors in 20 μm pixel.
*Unlimited use of PMOS and NMOS.
*Allows 100 % diode fill factor.

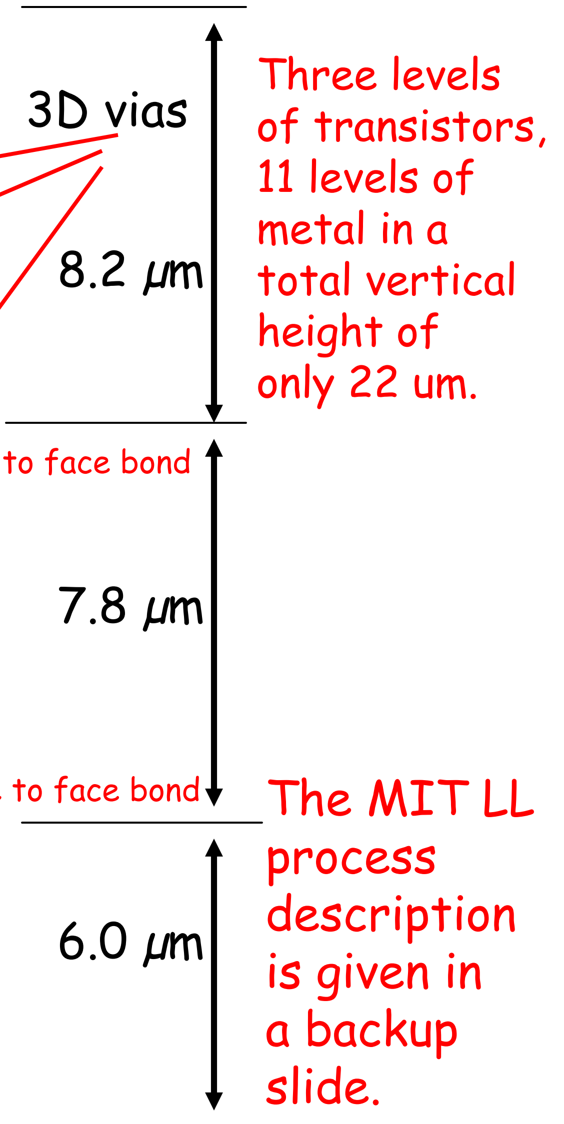
Vias: 1.5 um dia by 7.3 um long



Note these vias are 1.5 um in diameter. Larger vias (~5 um) take up valuable space in small pixel cells and thus may be impractical for ILC but alright for LHC applications.

MIT LL 3D Multiproject Run Chip Cross Section

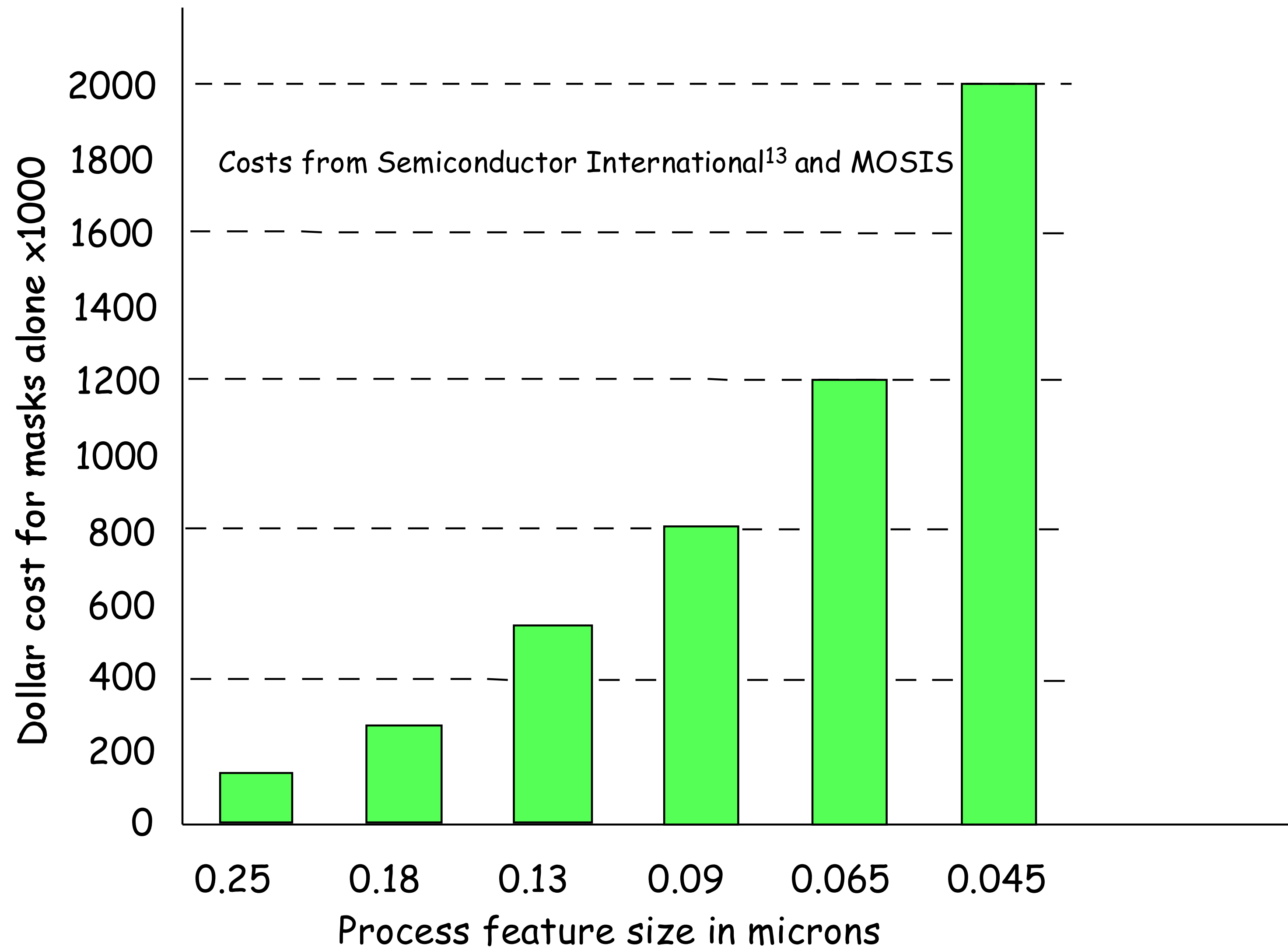
Tier	Layer	Thickness
Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	



Cost Considerations

- 3D integrated circuits are expensive to fabricate.
  - In a 3D integrated circuit, each tier generally comes from a separate dedicated wafer run. Thus the cost is roughly proportional to the number of tiers plus bonding each of the tiers together.
  - If wafer to wafer bonding is used, the yield will be less than if die to wafer bonding is used, and hence cost will be increased.
- In High Energy Physics detectors, the costs need to be justified based on reduced mass, higher functionality in a given area, or by supporting mixed technologies.
- 3D electronics may be the technology that makes certain physics experiments possible.
- Costs of smaller node masks is increasing dramatically, and at some point 3D will be less expensive than going to a smaller node technology, even for HEP applications.

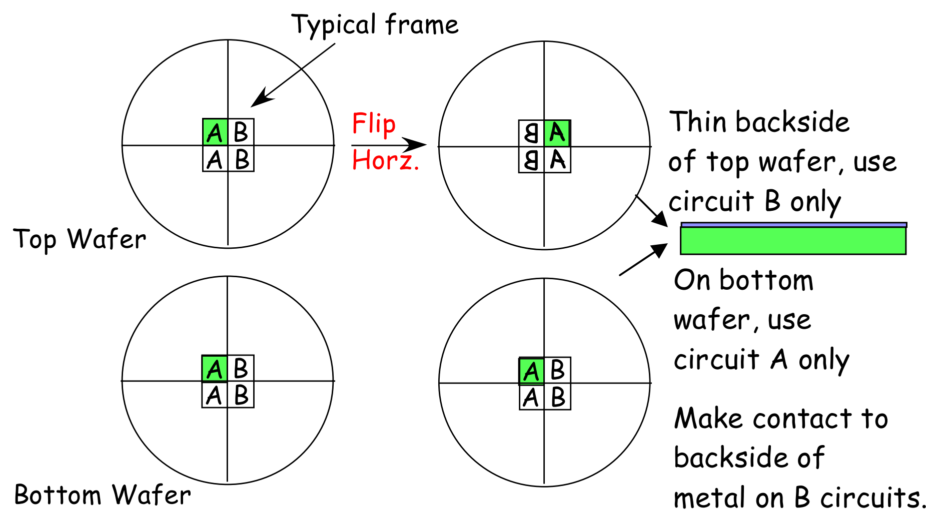
Mask Costs



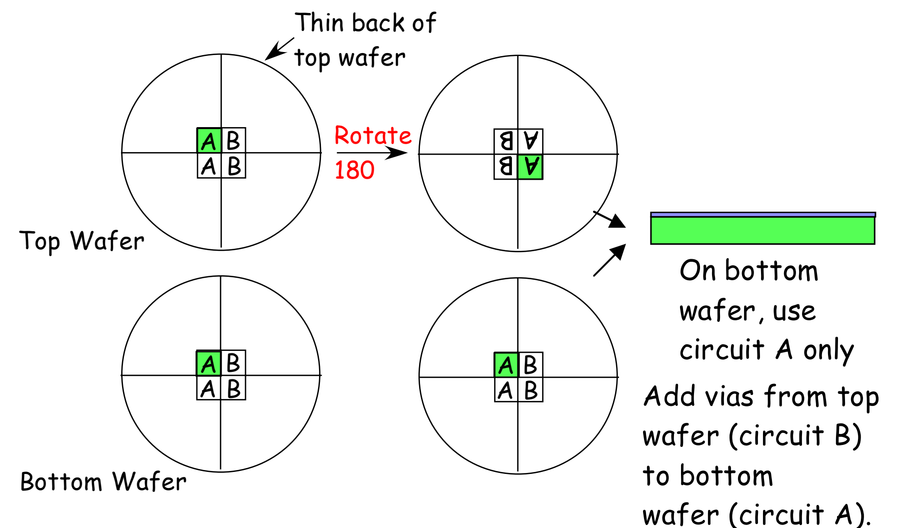
Cost Reduction for Prototyping

A detector tier and two electronics tiers can be fabricated from one set of masks and one wafer run. The three tiers in CMOS or SOI can be assembled with only one 3D bonding step.

As an example consider a frame that has two A circuits (sensing diode plus CMOS, and two B circuits (CMOS only). These circuits can be bonded together either face to face or back to face depending on the type of bonding, via formation, and thinning procedures to be used. Unfortunately, only one half of the silicon results in useful devices.



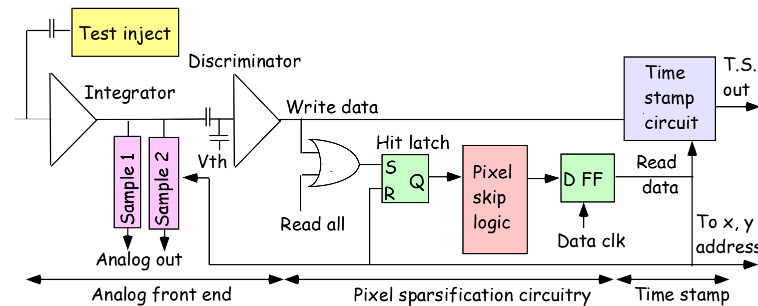
Face to Face Bonding



Back to Face Bonding

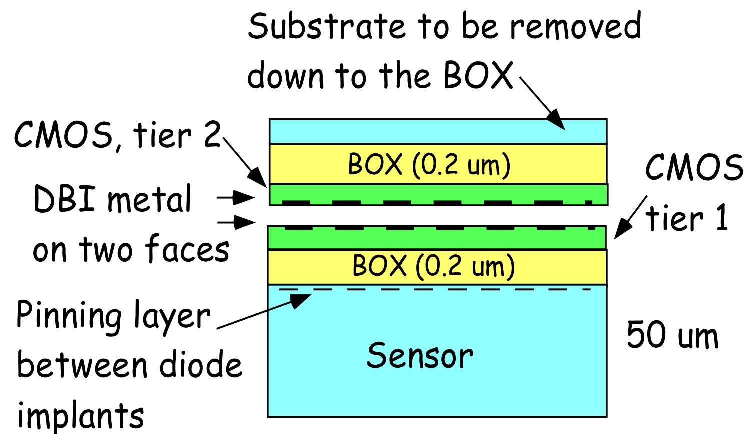
The Single Set of Masks Approach can be Used in Different Technologies

Convert VIP1 design to 2 tiers + sensor in 0.13 um technology with face to face bonds.



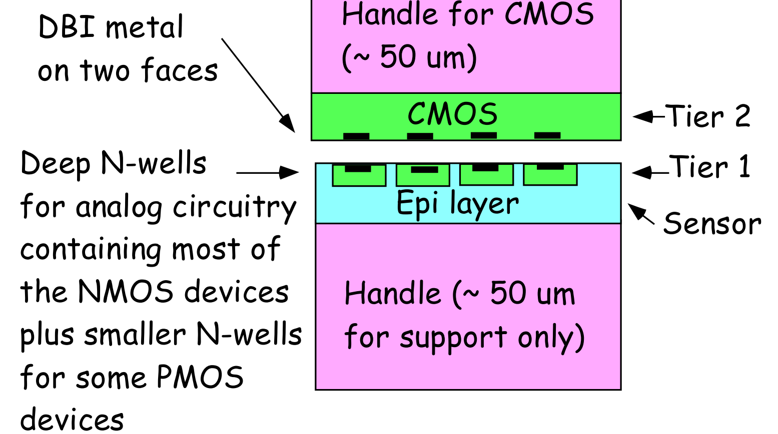
VIP1 Readout chip in 3 tiers

SOI



Each CMOS tier is less than 10 um

CMOS



MAPS in deep N-well process

Pixels < 20 um, Resolution < 5 um

Summary

- Progress is being made to integrate sensors and readout electronics in a monolithic structure for pixel arrays.
- Foundries are starting to develop technologies for SOI detectors and 3D integrated circuits
  - OKI, ASI for SOI detectors,
  - IBM, MIT LL, and others for 3D circuits
  - Radiation limits still need to be studied but they are expected to be sufficient for many applications. In very high radiation environments separate, special detectors may be necessary.
- 3D is being pursued by many commercial organizations[9]
- HEP groups are beginning to look at 3D technologies
  - MPG in Munich is starting an activity to bond pixel sensors to ROICs
  - RAL has expressed interest in 3D with CCDs
  - Bonn has expressed interest in 3D with DEPFETs
  - Fermilab will continue to explore SOI detectors and 3D
- 3D is expensive but offers a great deal of design flexibility.
- These new 3D technologies offer new opportunities for difficult applications that can't be satisfied with other older approaches.

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- 3) A. Chambers, et. al., "Through-Wafer Via Etching", Advanced Packaging, April 2005.
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- 5) G. Deptuch, "Monolithic Active Pixel Matrix with Binary Counters in an SOI Process", 2007 International image Sensor Workshop, Maine, June 7-10, pp. 98-101.
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- 9) B. Aull, et. al., "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing layers," IEEE SSCC 2006, pp. 26-7.
- 10) V. Suntharalingam, et. al., Megapixel CMOS Image Sensor Fabricated in Three-dimensional Integrated Circuit Technology," IEEE SSCC 2005, pp356-7.
- 11) J. Lu, "Monolithic 3D Power Delivery Using Dc-Dc Converter", 3D Architecture Conference, October, 2006, Burlingame, CA.
- 12) R. Yarema, "Development of 3D Integrated Circuits for HEP", 12th LHC Electronics Workshop, Valencia Spain, September 25-29, 2006.
- 13) A. Hand, "Study Examines Changing Face of Next Generation Lithography", Semiconductor International, October 1, 2007

Backup slides

MIT LL process

Ziptronix process

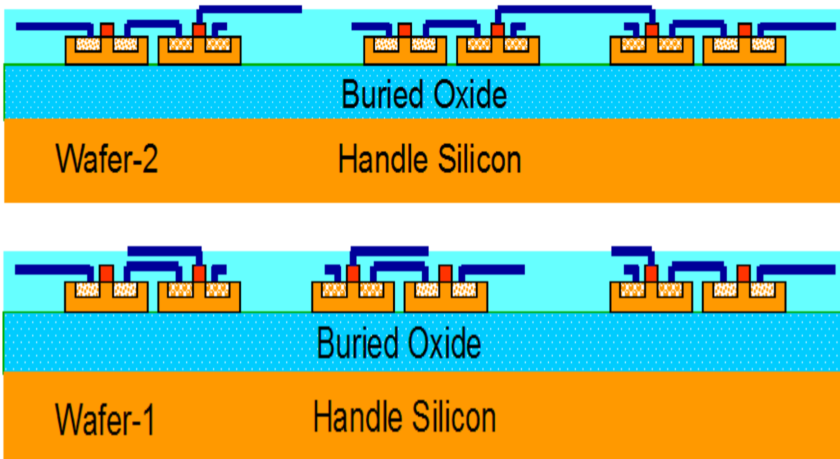
ILC Requirements

VIP 1 Design

Process Flow for MIT LL 3D Chip

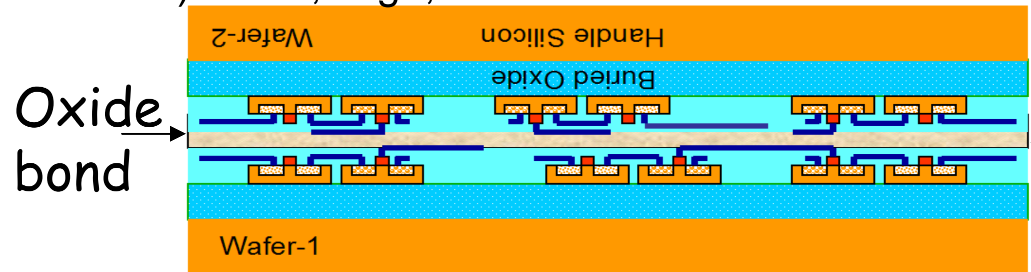
- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers



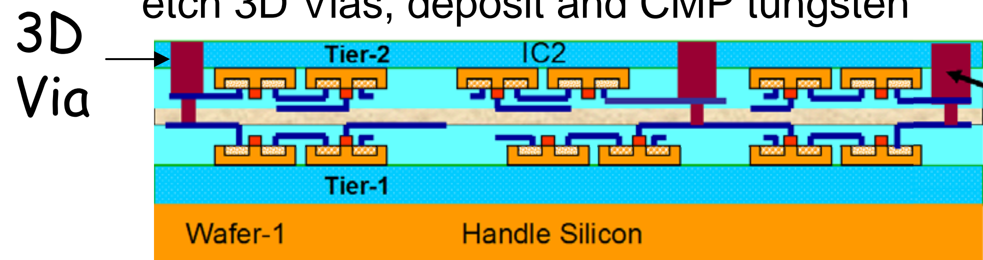
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

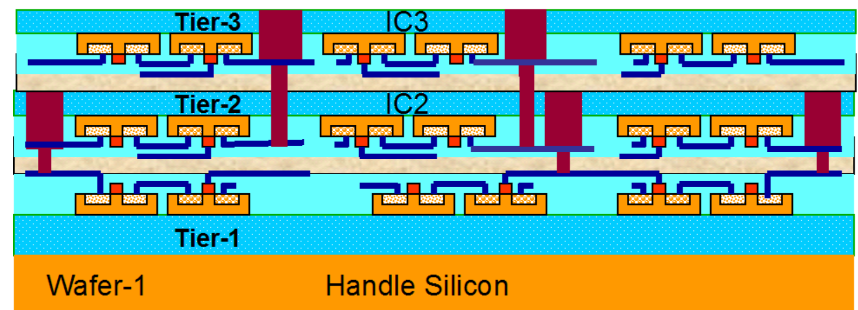


3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via



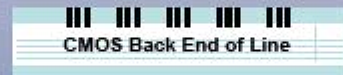
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



ziptronix

DBI™ Process Flow

The 3D IC Company

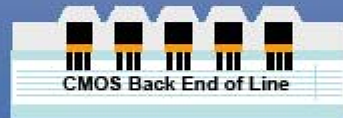


1) **Starting Wafer**
   - Planar Surface
   - Exposed Filled Vias (W or Cu)

2) **Deposit Seed**

3) **Pattern / Plate DBI Metal**

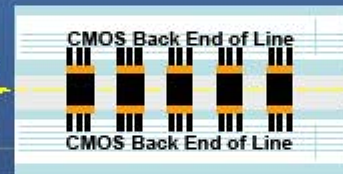
4) **Blanket Etch Seed**
   - Option – Pattern Etch for Lateral Routing



5) **Oxide Deposition**

6) **Planarization**
   - Oxide Bonding Mechanical Spec < 0.5nm

Bond Interface



7) **Place 2 DBI Surfaces into Contact**
   - Conventional Pick-&-Place
   - Room Temperature, Direct Oxide Bonding

10

Paul Enquist, 3D Architecture Conference, October 2007

3D Demonstrator Chip for ILC Pixels

- ILC expected to have beam structure with 2820 crossings in a 1 msec bunch train with 5 bunch trains/sec.
- ILC Maximum hit occupancy
  - Assumed to be 0.03 particles/crossing/mm^2
  - Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)
  - Hit rate = 0.03 part./bco/mm^2 x 3 hits/part. x 2820 bco/train = 252 hits/train/mm^2.
- Study analog and binary read out approach
  - Want better than 5 μm resolution
  - Binary readout
    - 15 um pixel gives $15/\sqrt{12}$ = 4.3 um resolution
    - 20 um pixel gives 5.8 um resolution

Requirements

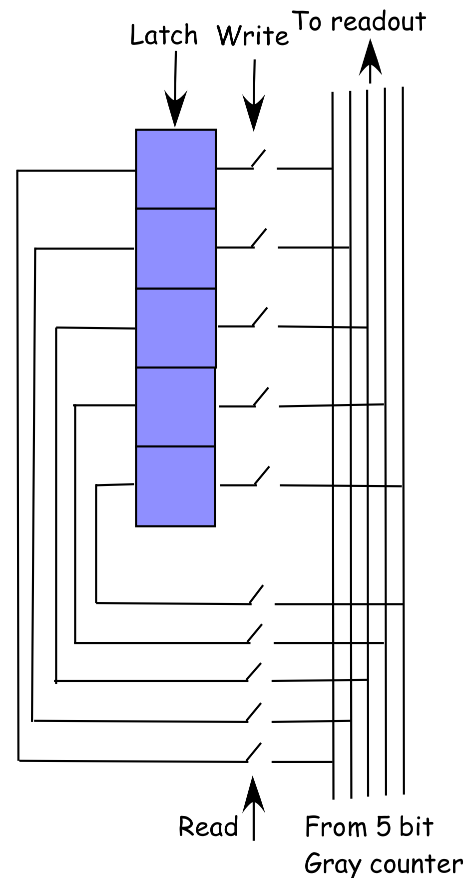
- Occupancy in a pixel for 2820 bco
  - Occupancy in 15 μm pixel = 250 hits/mm2 x (15μm x 15μm) = 0.056 hits/bunch train
    - Chance of a single cell being hit twice in a bunch train = .056 x .056 = .0031 => 0.3%
    - Therefore, with a pipeline depth of only one, 99.7% of hits are recorded unambiguously.
  - Occupancy in a 20 μm pixel = 0.1
    - Chance of a cell being hit twice in a bunch train = 0.1 x 0.1 = 0.01 =>1.0%
    - Therefore, with a pipeline depth of only one, 99% of hits are recorded unambiguously.

Demonstrator Chip Design Choices

- Provide analog and binary readout information
- Divide the bunch train into 32 time slices. Each pixel stores one time stamp equivalent to 5 bits of time information.
- Store the time stamp in the hit pixel cell.
- Use token passing scheme with look ahead feature to sparsify data output.
- Store pixel address at end of row and column.
- Divide chip design into 3 tiers or layers of ROIC
- Make pixel as small as possible but with significant functionality.
- Design for 1000 x 1000 array but layout only for 64 x 64 array.

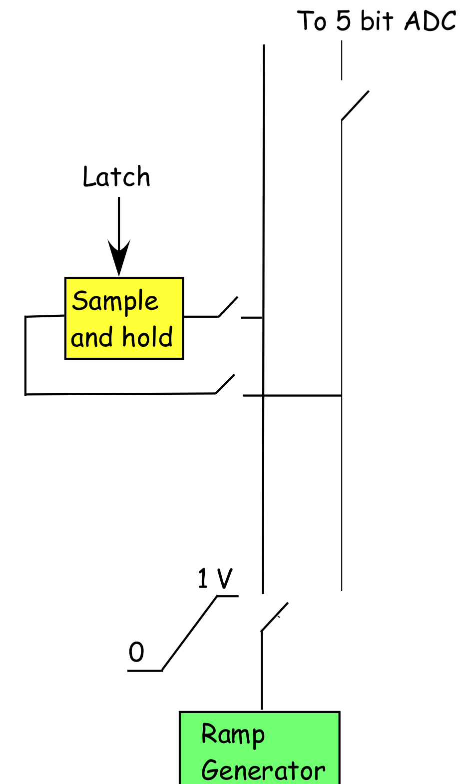
Pixel Time Stamping

- Various MAPS schemes for ILC have suggested 20 time stamps to separate hits in the 2820 bunch train.
- ILC 3D chip has 32 time stamps.
- Time stamp can be either analog or digital.
- ILC demonstrator chip will have both



Counter operates at a slow speed, 32 KHz, (30 usec/step)

All digital - 10 transistors/bit



Ramp operates at low speed for low power.

Analog approach - fewer transistors

Sparsified Readout Operation

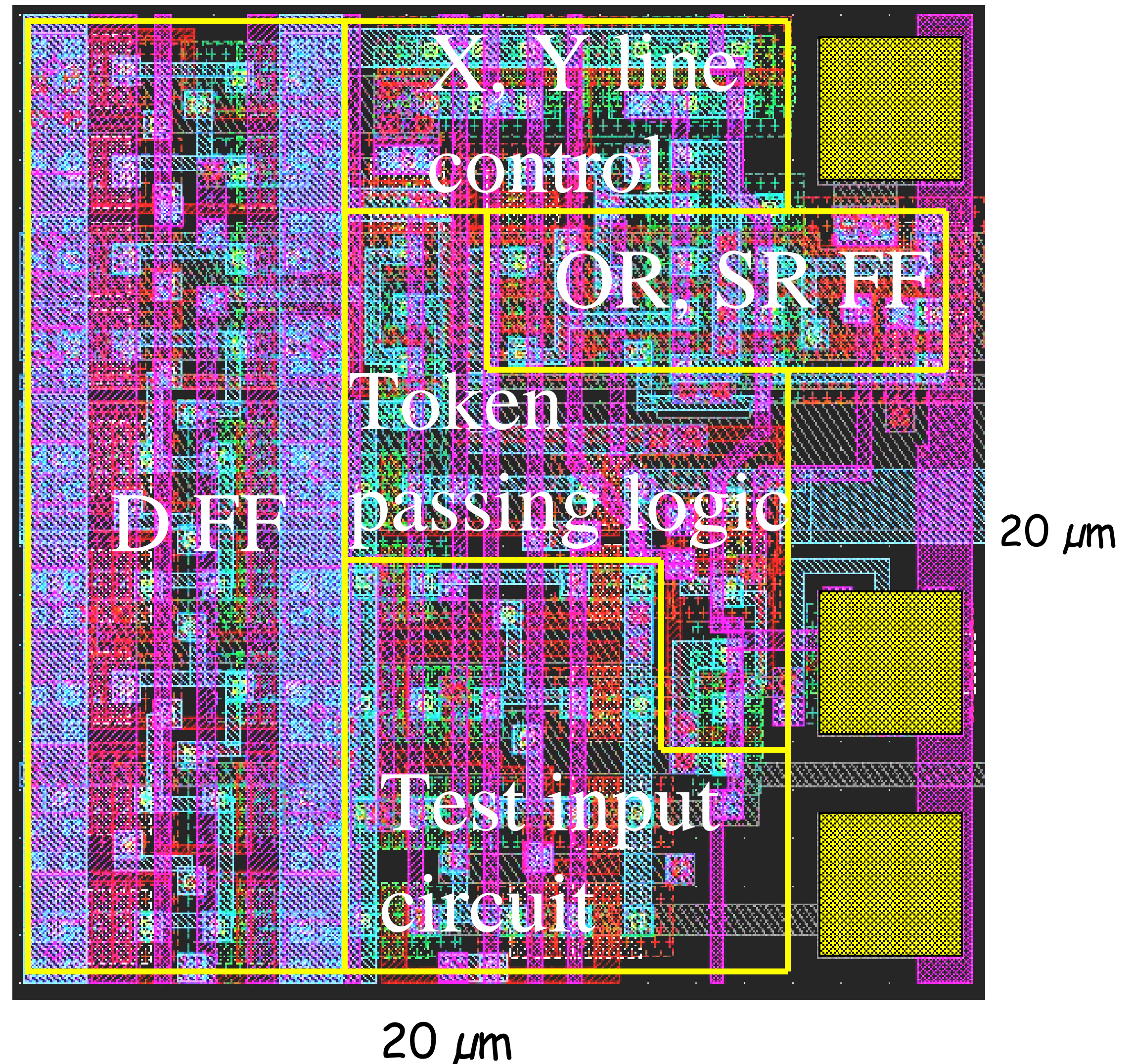
- During data acquisition, a hit sets a latch.
- Sparse readout performed row by row.
- To start readout, all hit pixels are disabled except the first hit pixel in the readout scan.
- The pixel being read points to the X address and Y address stored on the perimeter and at the same time outputs the Time Stamp and analog information from the pixel.
- While reading out a pixel, a token scans ahead looking for next pixel to readout.
- Chip set to always readout at least one pixel per row in the array.
- Assume 1000 x 1000 array (1000 pixels/row)
  - Time to scan 1 row = .200 ns x 1000 = 200 ns (simulated)
  - Time to readout cell = 30 bits x 20 ns/bit = 600 ns
  - Plenty of time to find next hit pixel during readout

Readout Time Example

- Chip size = 1000 x 1000 pixels with 15 um pixels.
- Max hits/chip = 250 hits/mm^2 x 225 mm^2 = 56250 hits/chip.
- If you read all pixels with X=1, add 1000 pixels (small increase in readout data).
- For 50 MHz readout clock and 30 bits/hit, readout time = 57250 hits x 30 bits/hit x 20 ns/bit = 34 msec.
- For a 1000 x 1000 array of 20 um pixels, the readout time is 60 usec.
- Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips.
- Digital outputs are CMOS. The output power is only dependent on the number of bits and not the length of time needed to readout.

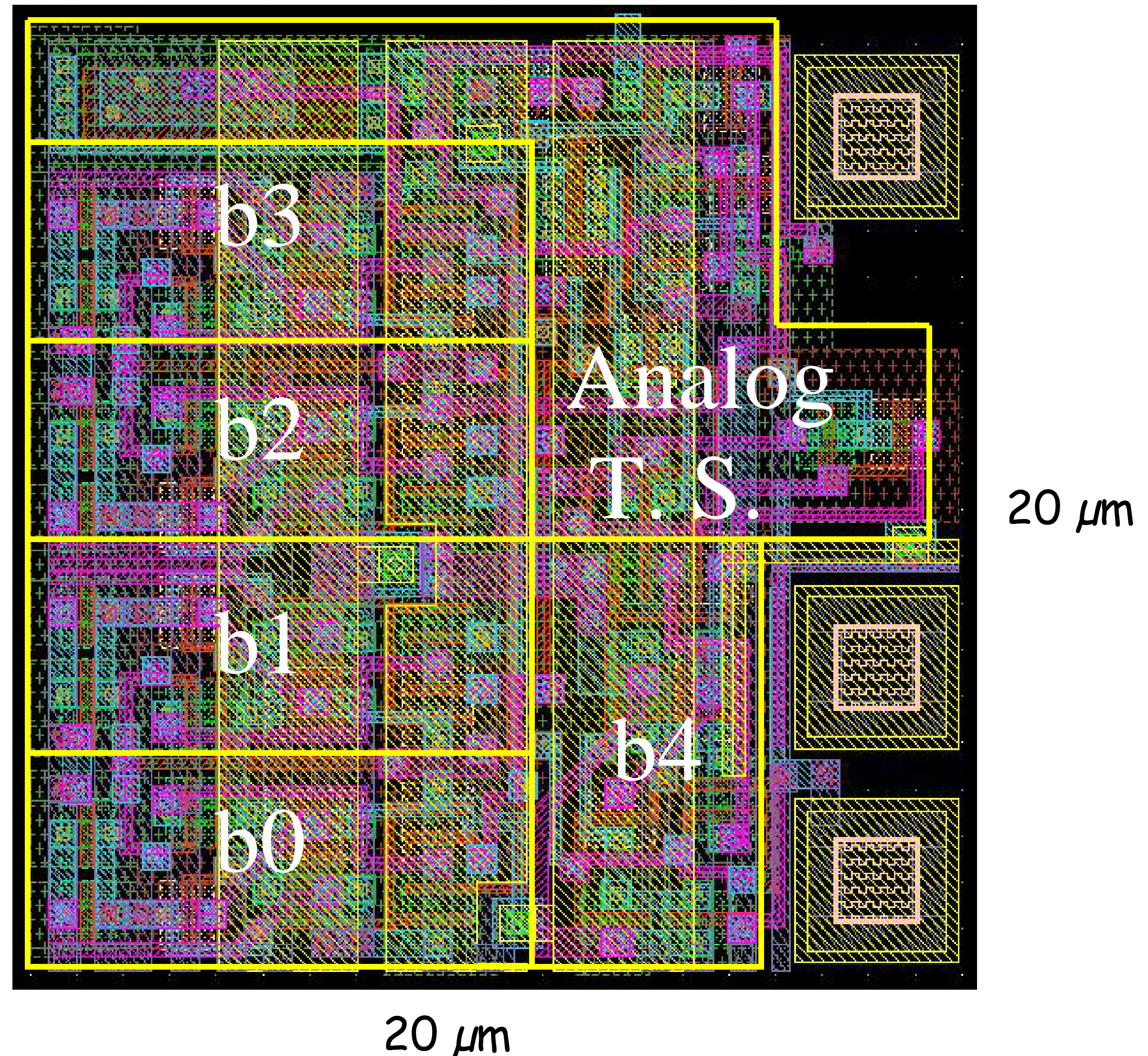
Sparsification Tier 1

- OR for READ ALL cells
- Hit latch (SR FF)
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



Time Stamp - Tier 2

- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Either analog or digital T. S.to be used in final design.
- Gray code counter on periphery
- 72 transistors
- 3 vias

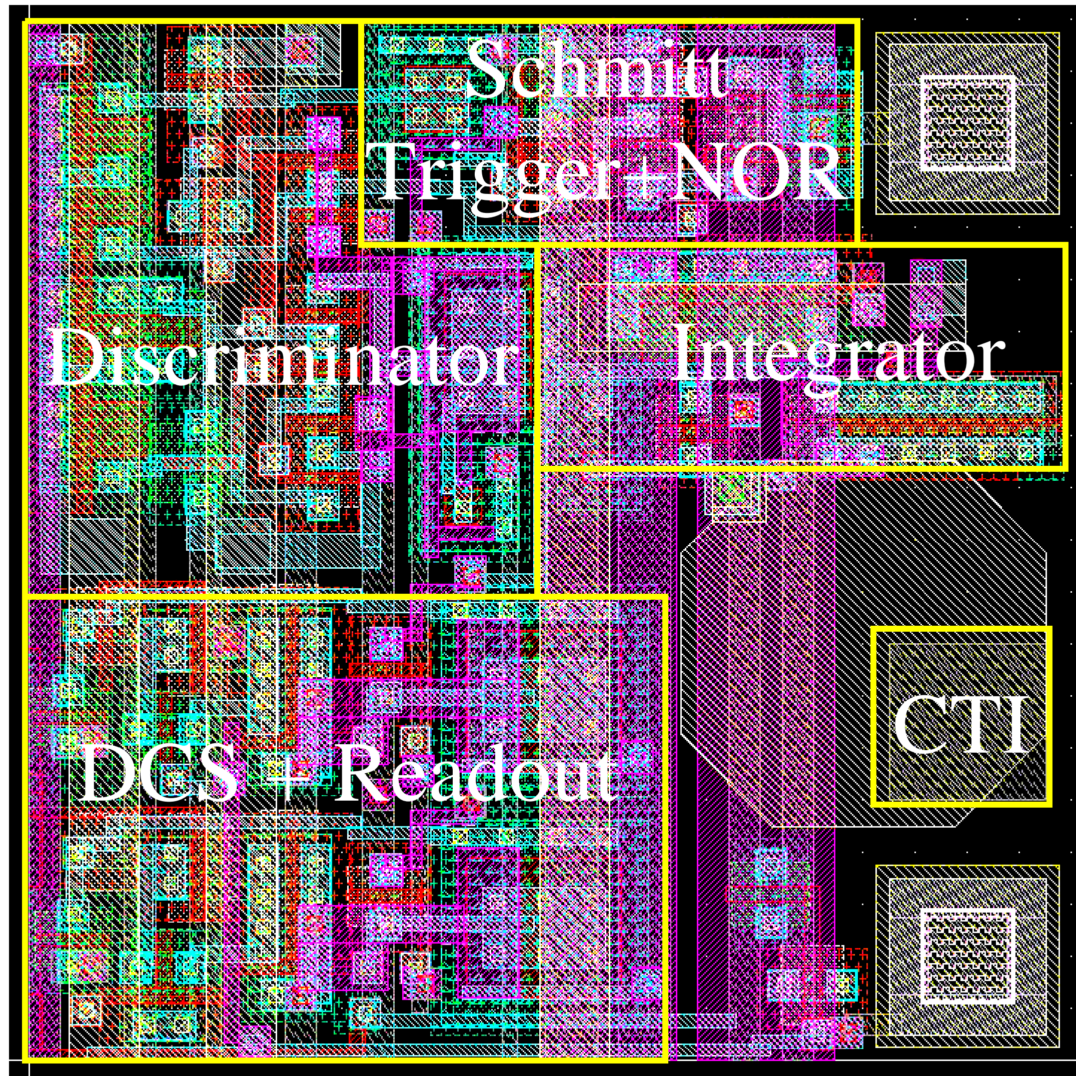


20 μm

20 μm

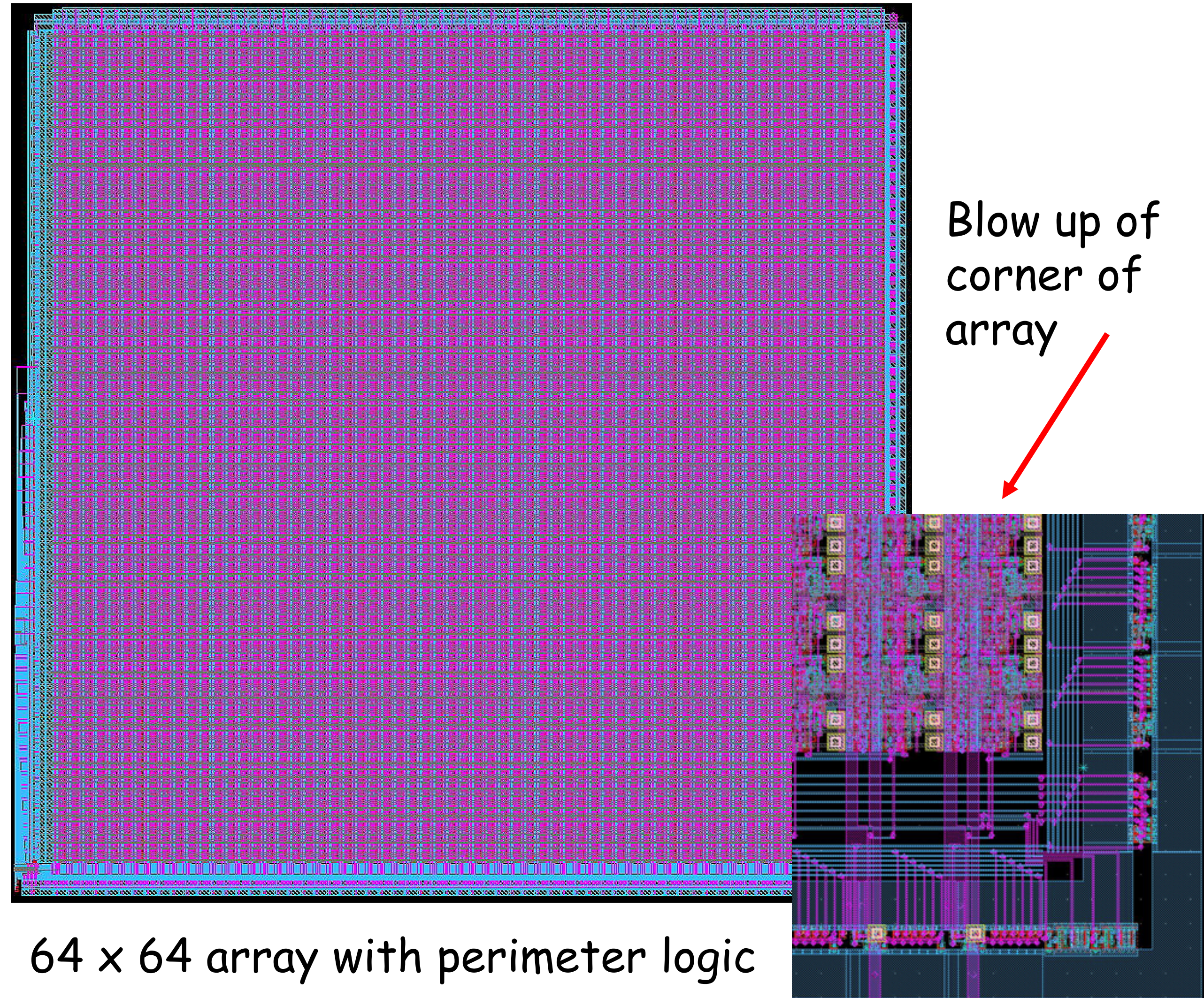
Analog Tier 3

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input (CTI)
- 38 transistors
- 2 vias



Perimeter Logic

- Perimeter circuitry for the ILC Demonstrator chip occupies a small amount of space.
- Area for the perimeter logic could be reduced in future designs.



64 x 64 array with perimeter logic

Demonstrator Chip Summary

- Multi functional device to be used a proof of concept
- 64 x 64 array that can be expanded to 1000 x 1000.
- 175 transistors in 20 micron pixels
- 3 tiers of transistors with an active circuit thickness of 22 microns
- Pulse height information (analog output) may not be required in the final design
- Sparsification with look ahead skip speed of 200 ps/cell for token passing.
- Two types of time stamping (only one chosen for the final application). 32 time stamps available, can be expanded to 64.
- Test input for every cell. Can be expanded to include a disable for every cell with little or no increase in size.

Demonstrator Chip Summary (con't)

- Serial digital output on one line
- Small peripheral circuitry.
- Chip power dissipation set by analog needs
  - Analog power = 0.75 μw/pixel => 1875 μw/mm^2
  - For ILC vertex detector power should not exceed 20 μw/mm^2
  - The vertex detector is expected is expected to acquire data for 1 msec every 200 msec
  - Assuming the analog power is ramped up in 0.5 msec, is held for 1 msec and ramped down in 0.5 msec the analog power for the ILC demonstrator chip would be 18.75 μw/mm^2
- Noise is expected to be in the range of 20-30 e- when connected to the detector.
- Multi-project submission date October 1, 2006