Readout Ideas for Phenix Silicon Endcap

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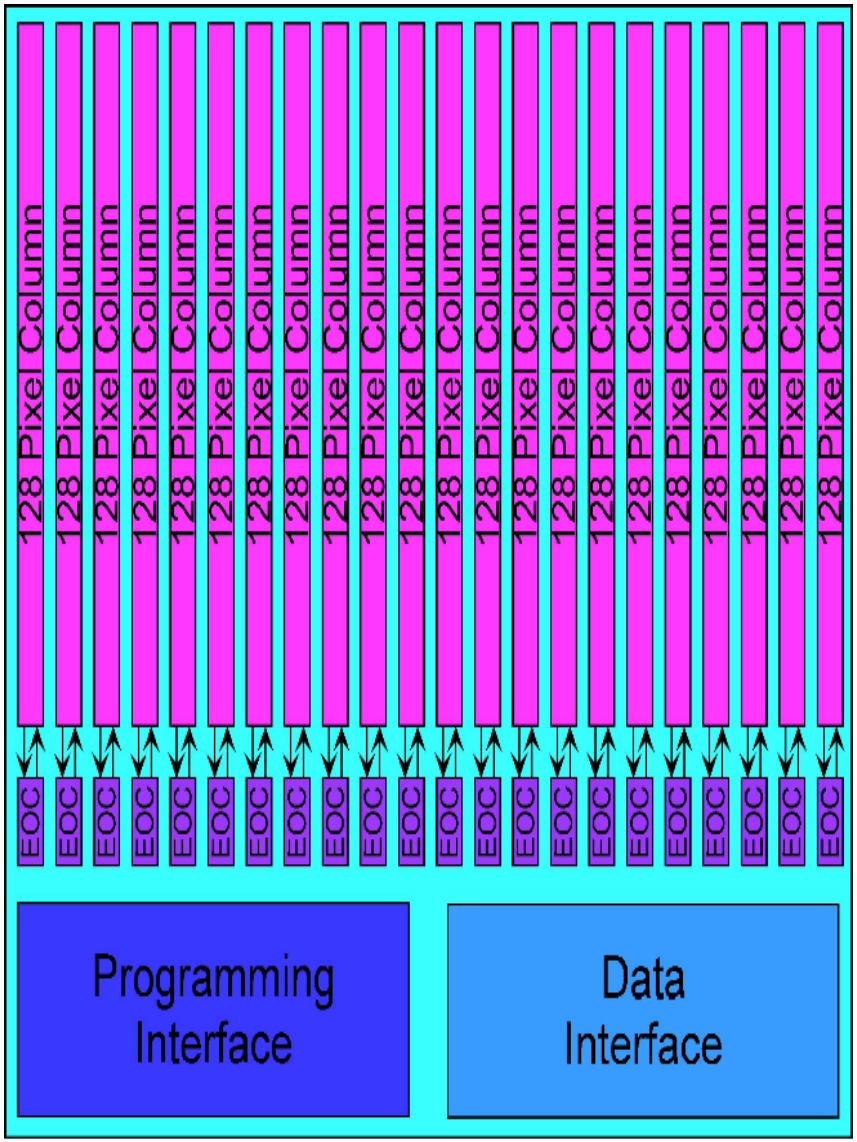
Introduction

- Present brief overview of FPIX2 pixel readout chip for BTEV
  - Architecture
  - Mixed signal performance
- Present possible approach for Phenix endcap readout using some mechanical and electrical features found in pixel readout chip.

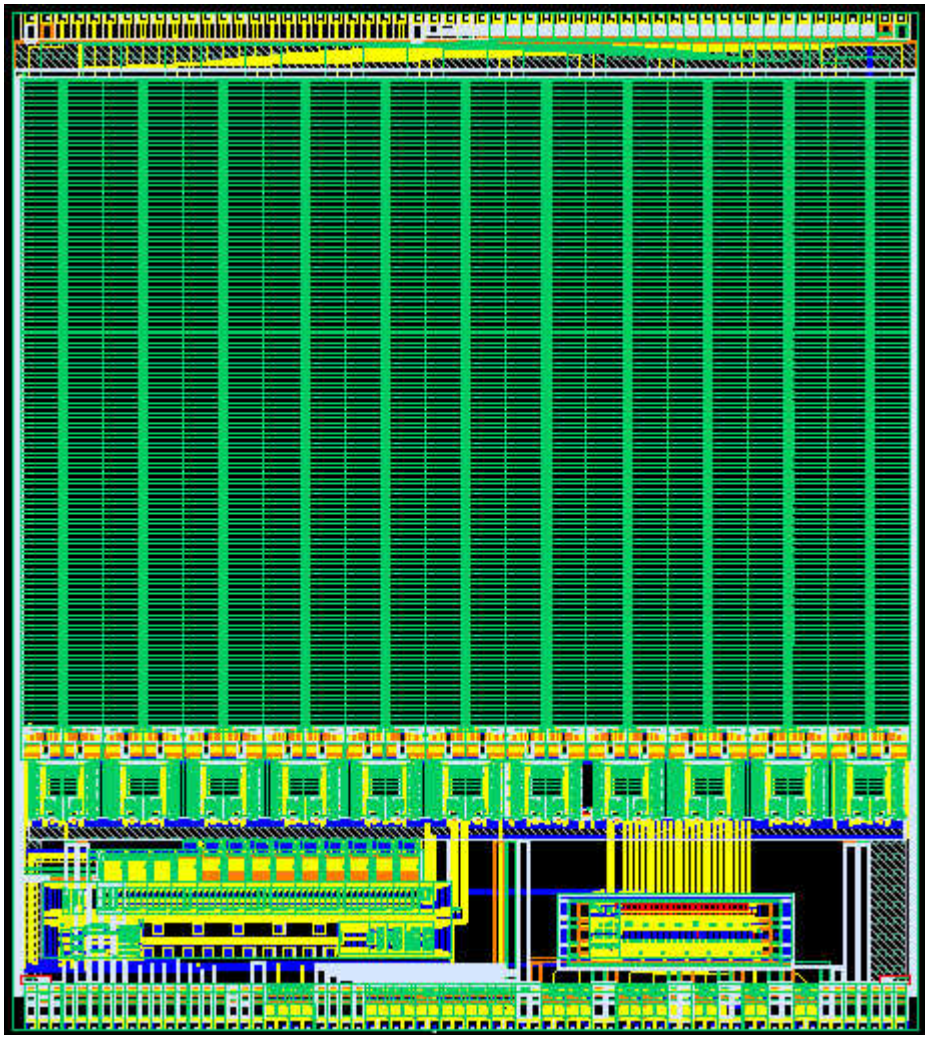
FPIX2 Features

- Advanced mixed analog/digital design
- 128 rows x 22 columns (2816 channels)
- 50 μm x 400 μm pixels
- High speed readout intended for use in Level 1 trigger. Up to 840 Mbits/sec data output.
- Very low noise
- Excellent threshold matching
- DC coupled input
- Fully programmable device
- Output directly drives long cable (10 feet)
- Rad hard to 50 Mrads

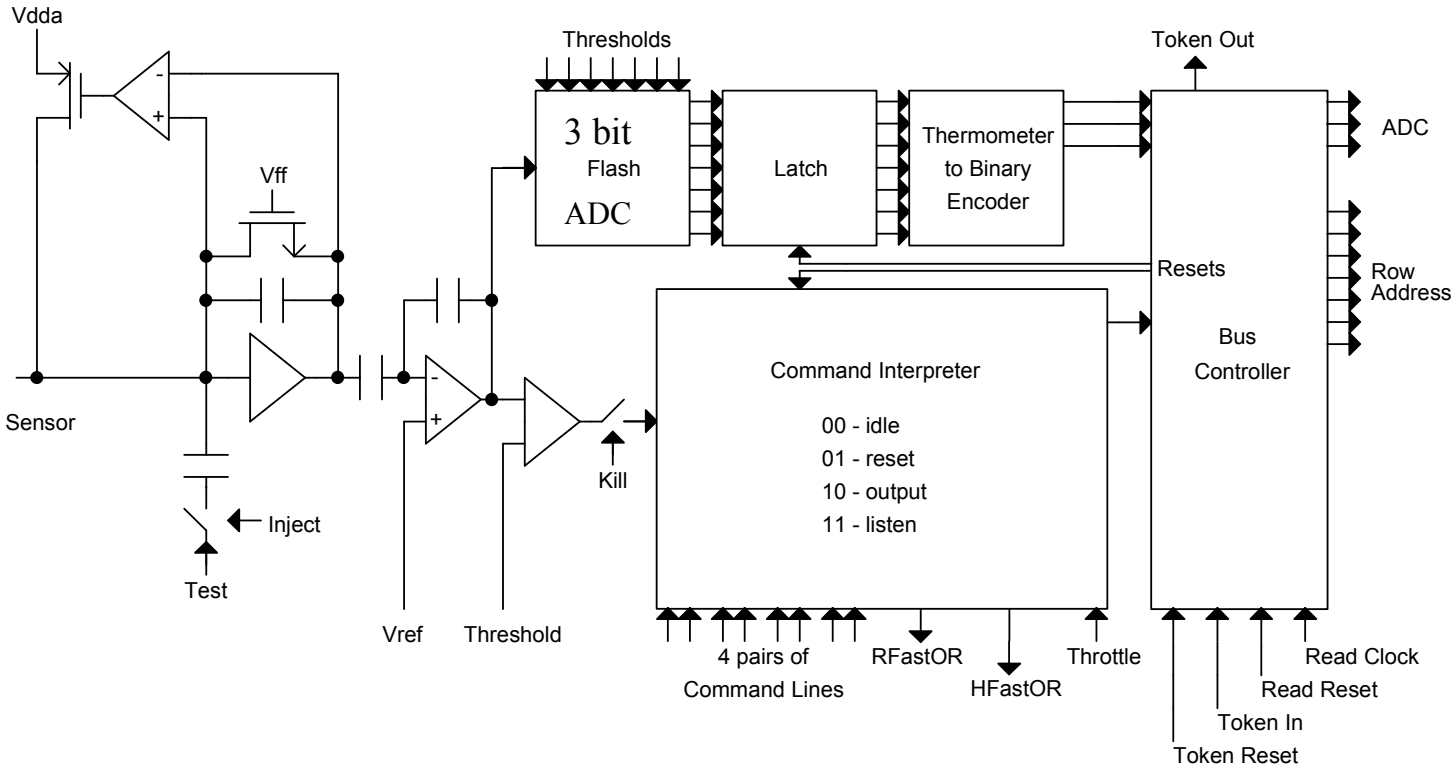

128 Pixel Column
EOC
Programming Interface
Data Interface

FPIX2

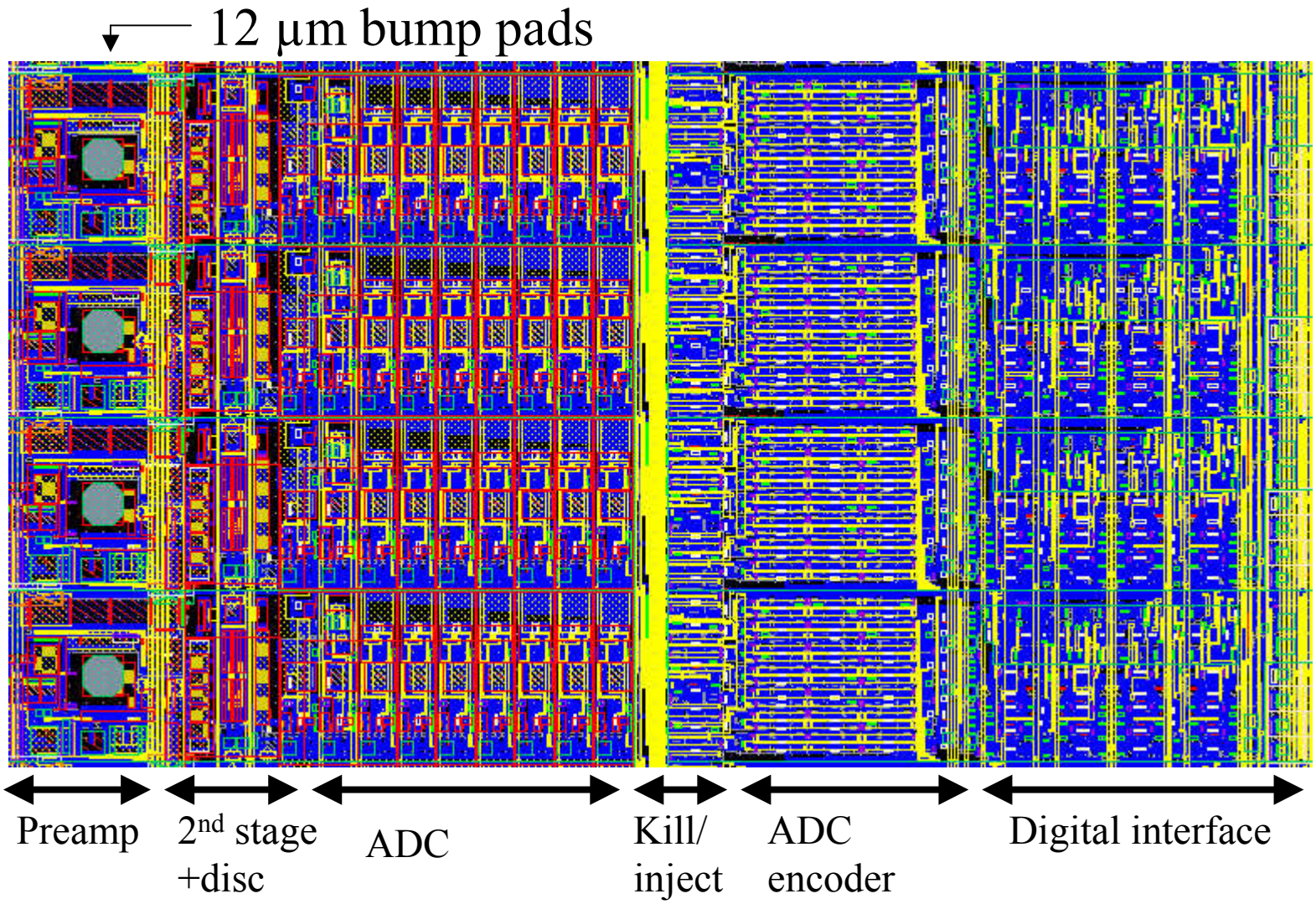
FPIX2 Readout Chip Showing Double Column Architecture



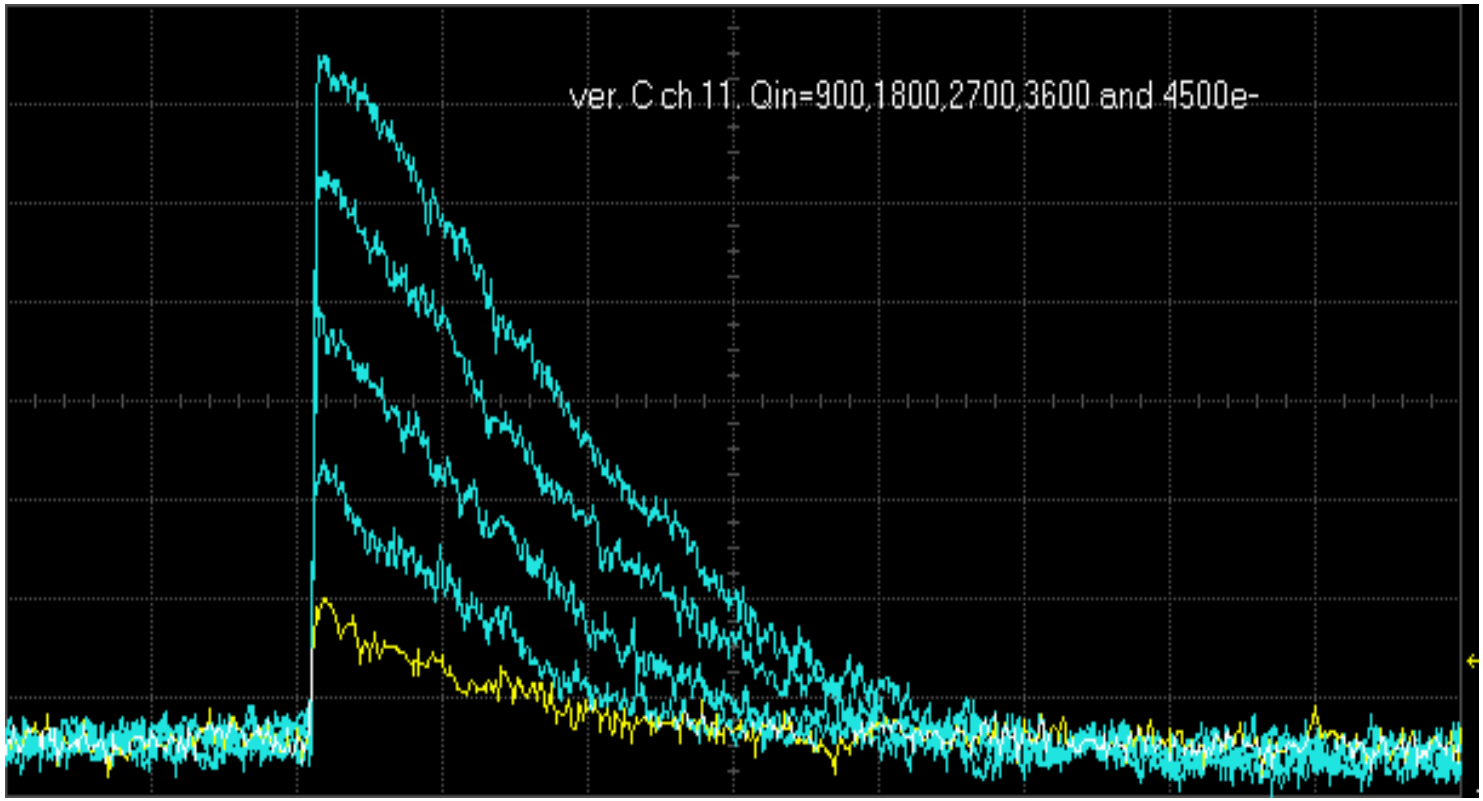
Pixel Circuit (50 x 400 μm)



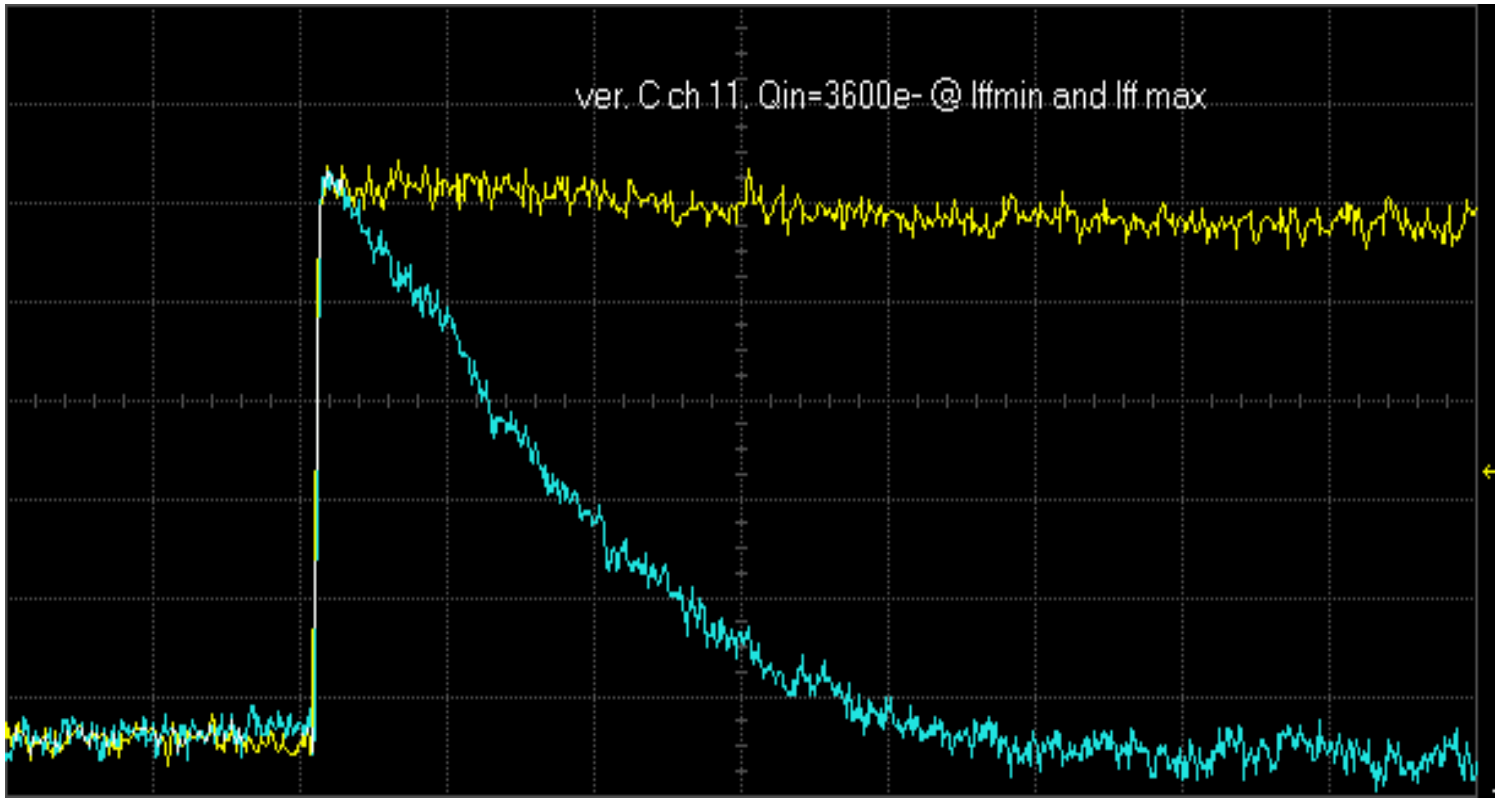
Pixel Cells (four 50 x 400 um cells)



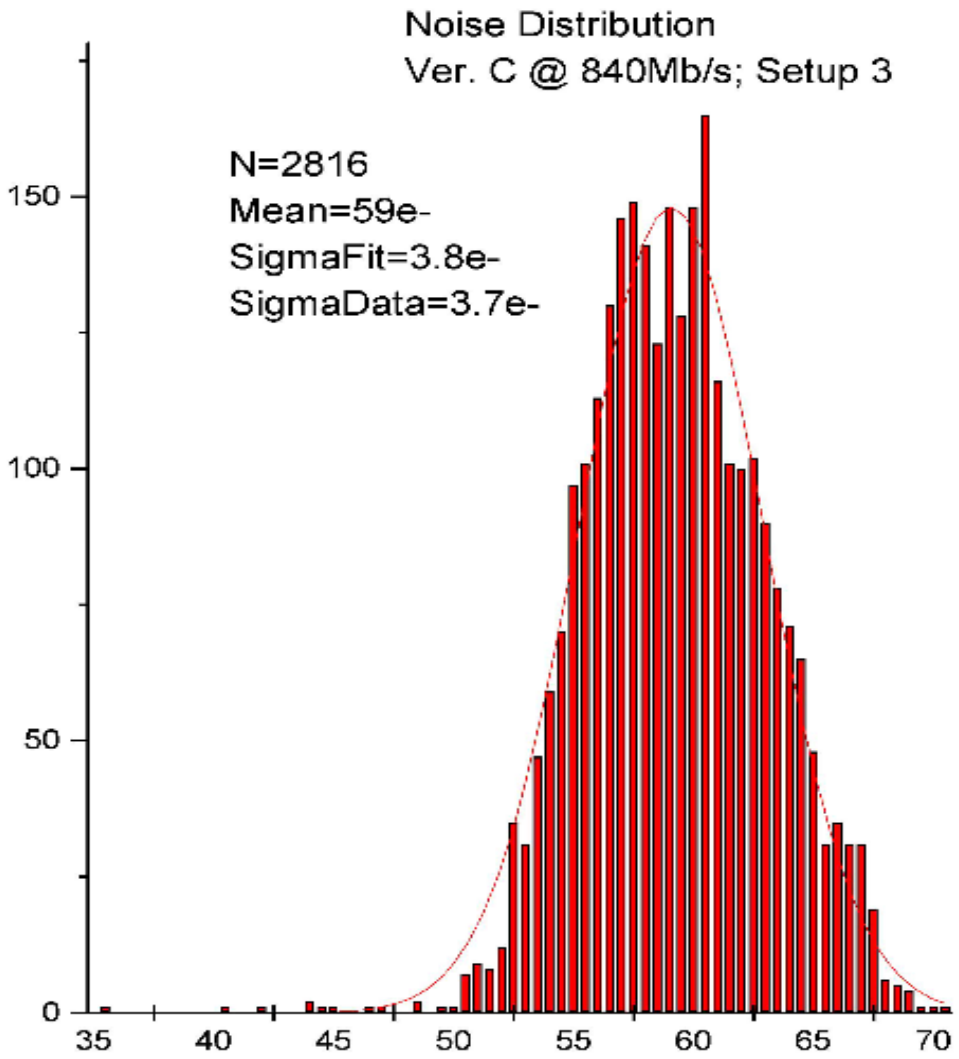
Response to Different Charge Inputs



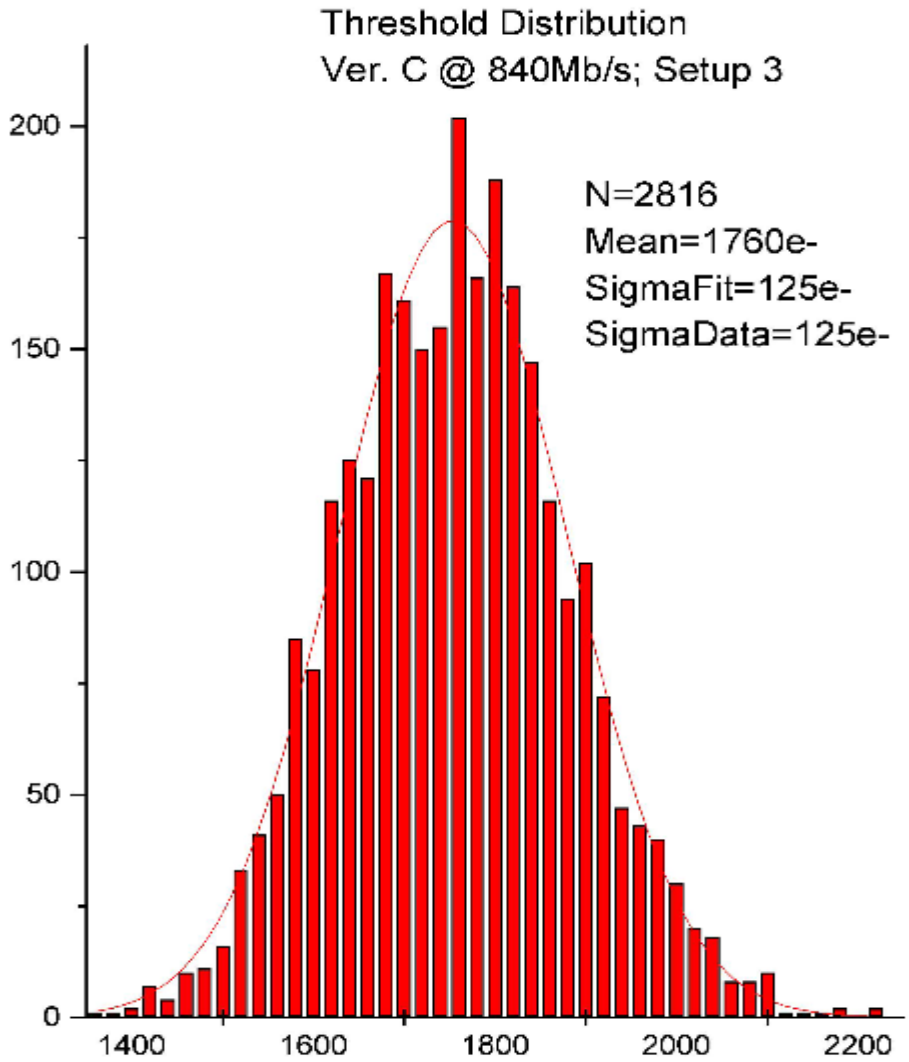
Change in Bias Effect on Response



FPIX2 noise
at C = 0
is about
60 erms



FPIX2 Threshold Distribution @ Cin= 0 pf is 125 erms



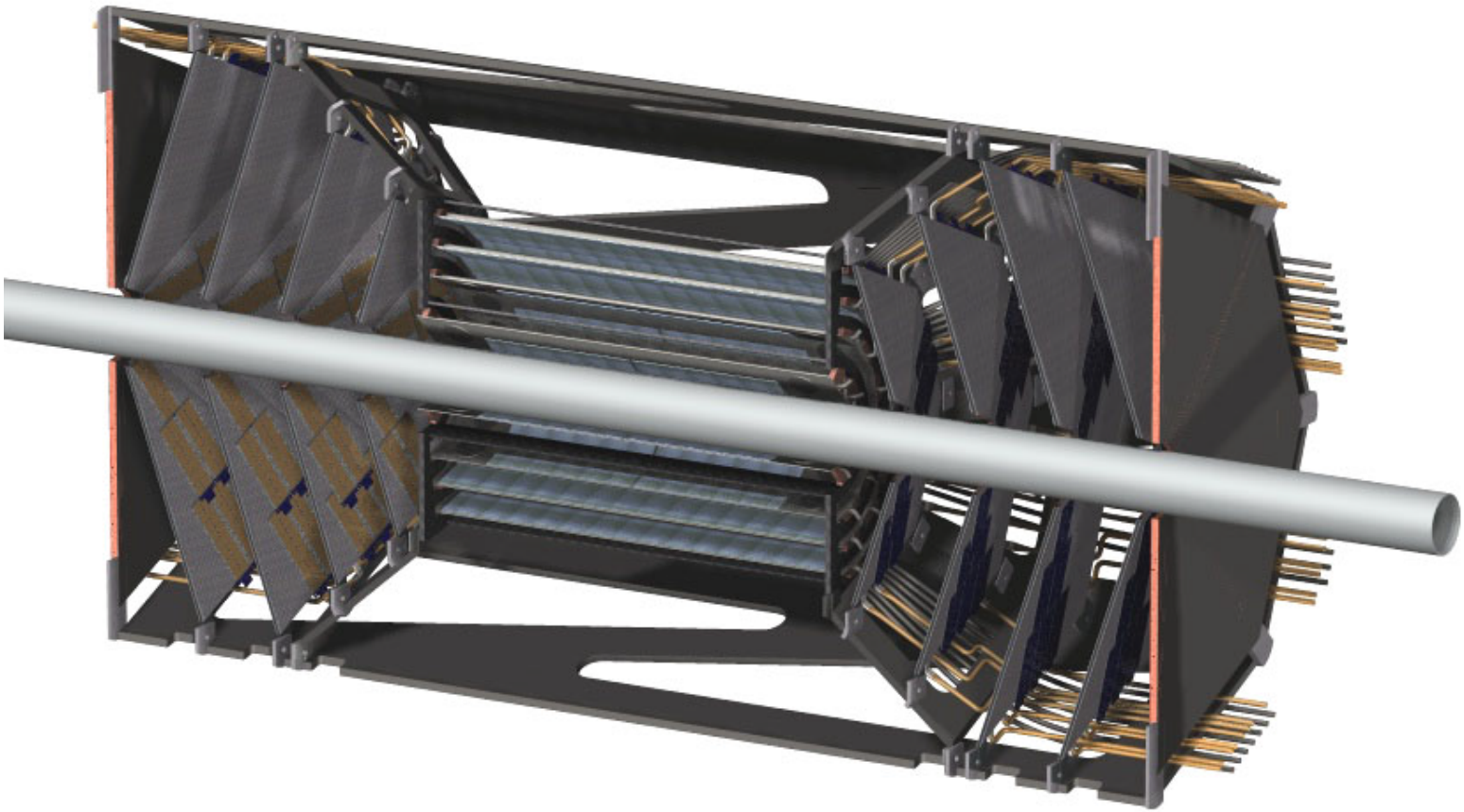
FPIX2 Status

- Produced 3168 chips in engineering run
- Minor tweaking of design needed before production
- Mixed analog/digital design has excellent performance with insignificant interference and cross talk.
- Chip size is 8.96 mm x 10.2 mm (91 mm^2)
- Yield is high
- Chip and readout can be used “as is” in other pixel applications

Phenix Endcap Silicon Readout

- Difficult mechanical constraints for readout chips.
- Power distribution to chips is a major concern.
- Full custom design is almost a certainty.
- Detector fabrication, cooling plan, and chip design need to be all considered at the same time.

Phenix Barrel and End Cap Silicon Cross Section



Pixel/Strip Sizes

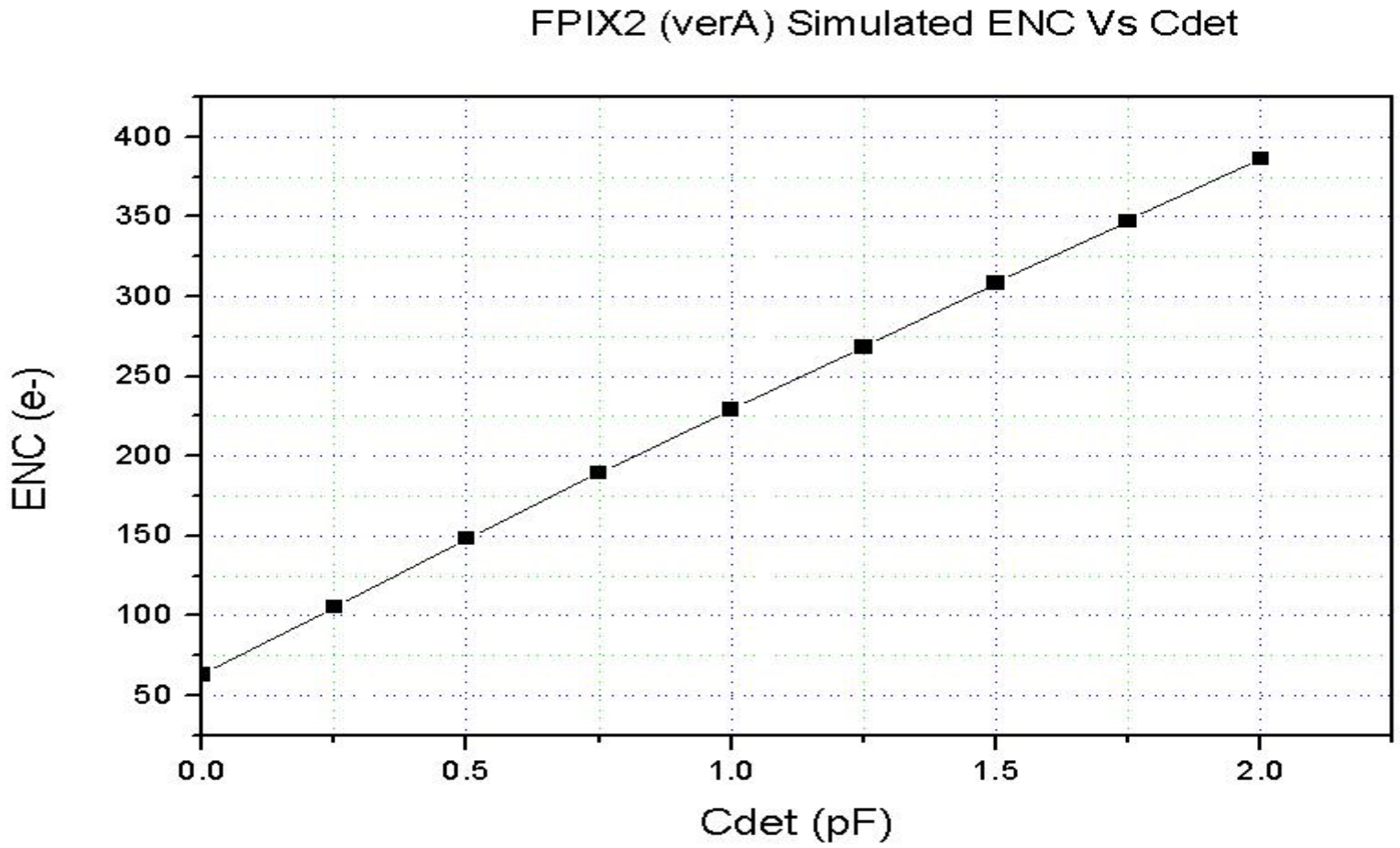
- FPIX 50 x 400 um Cin = .25 pF
- Phenix 50 x 2000 to 9000 um Cin = .2-.9 pF?
- SVX 50 x 10^5 to 3x10^5 um Cin = 10-30 pF

Design for Phenix should be optimized for correct detector capacitance

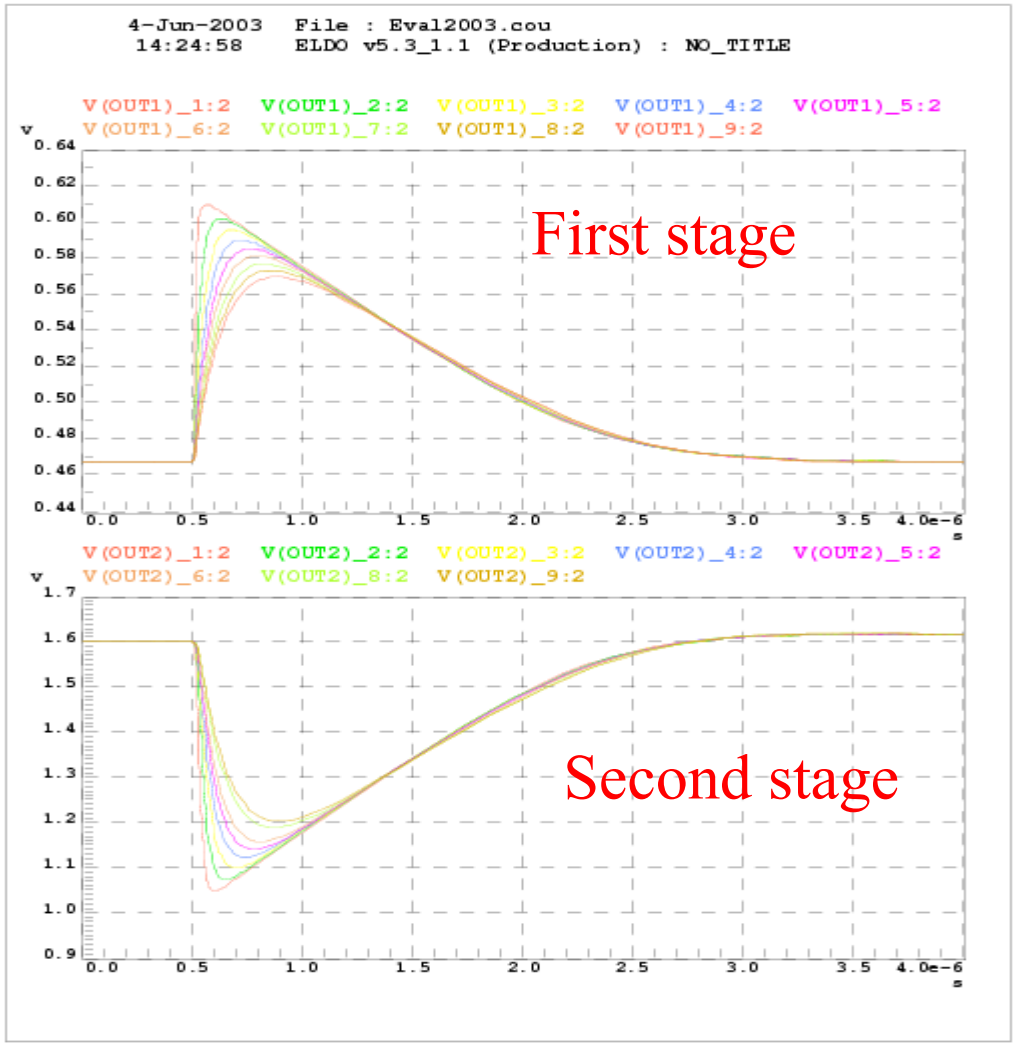
Bits and Pieces for Phenix

- Use modified FPIX2 front end
- Use relaxed bump bonding connections
- Use pipeline and sparcification concepts from SVX4
- Use backside contact for ground return (as done in SVX4)
- Use slow programming control from FPIX2
- May use modified output drivers from FPIX2

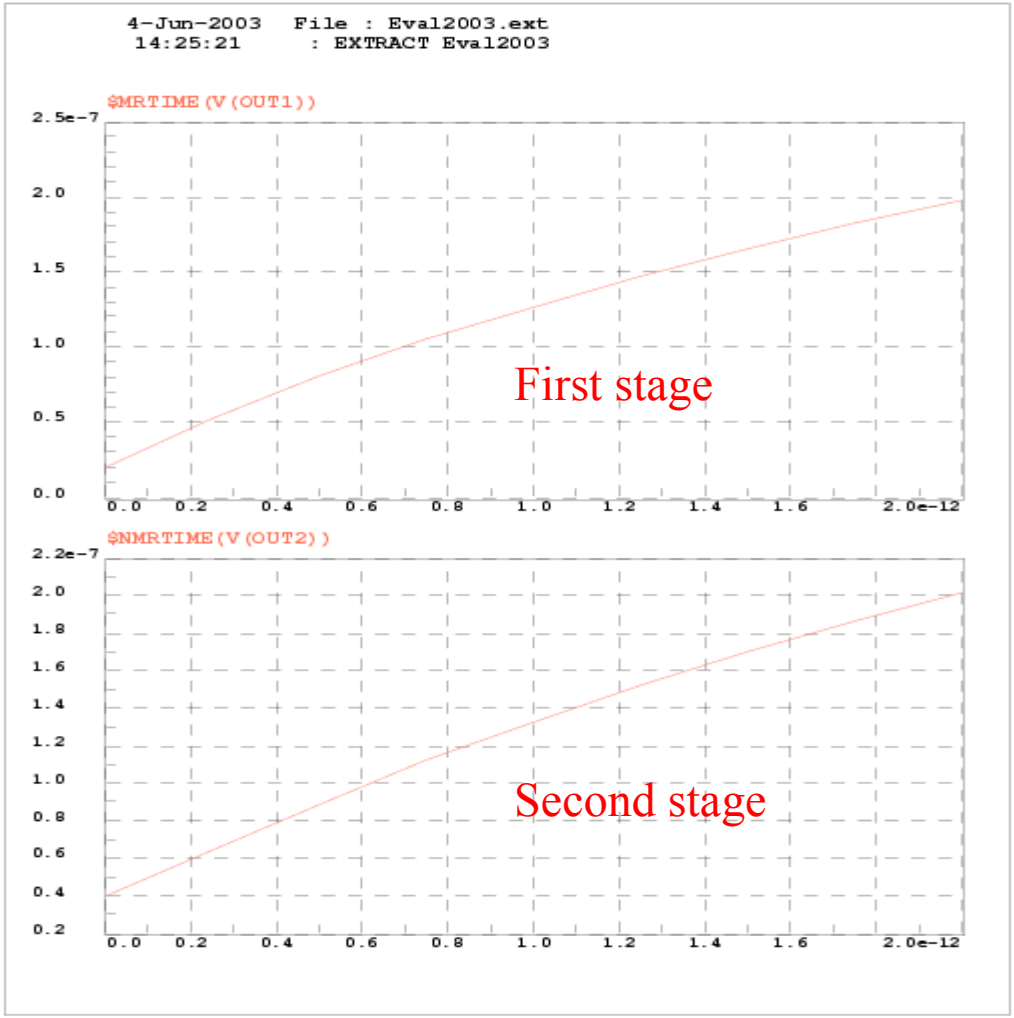
Noise Performance of FPIX2 at Higher Detector Capacitance



Simulated FPIX2 first and second stage response for detector capacitances from 0 to 2 pF in 0.25 pF steps



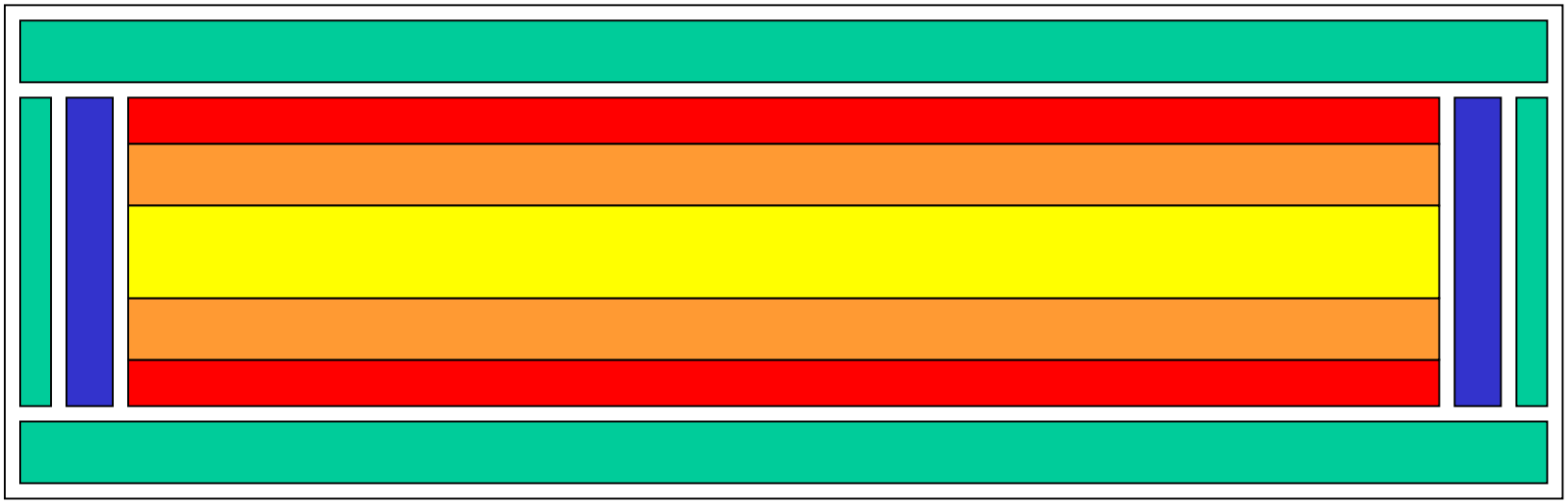
Simulated 1st and 2 nd stage risetime (10-90%) with different detector capacitance



Phenix Chip I/O Ideas

- **Separate analog and digital power buses**
- **Should operate over wide power supply range**
- **Common backside ground**
- **Clocks**
  - **Input clock – 100 ns**
  - **Separate readout clock?**
- **Serial programming interface input**
- **Serial data output**
  - **Chip ID**
  - **Cell number?**
  - **Channel ID**
- **Trigger input**
- **Control line(s)**

Possible Layout Diagram for PHX Chip



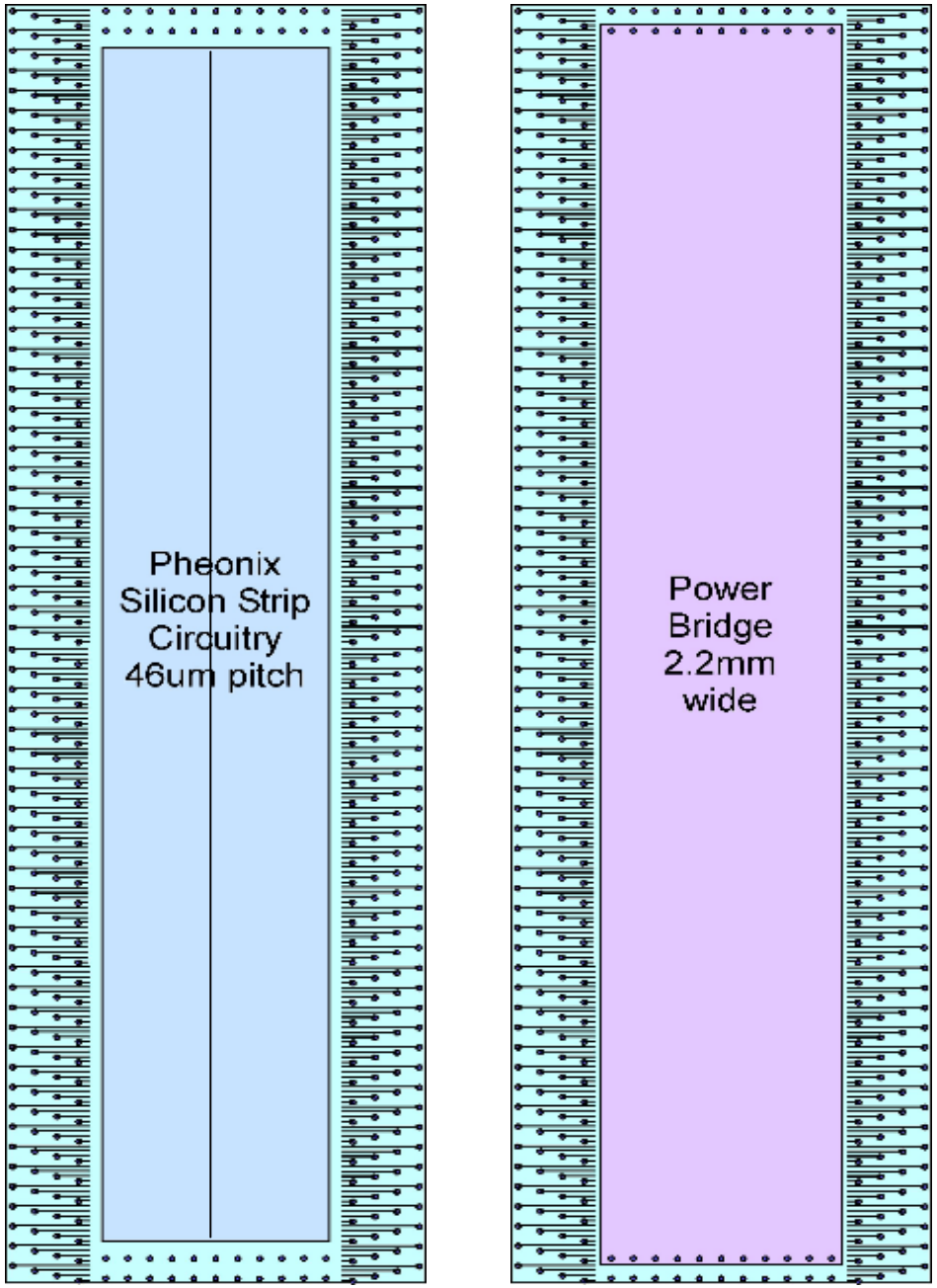
- Bump bonds
- Programming interface
- 1st and 2nd stage and discriminator
- Pipeline
- Digital interface

Phenix Chip Layout:

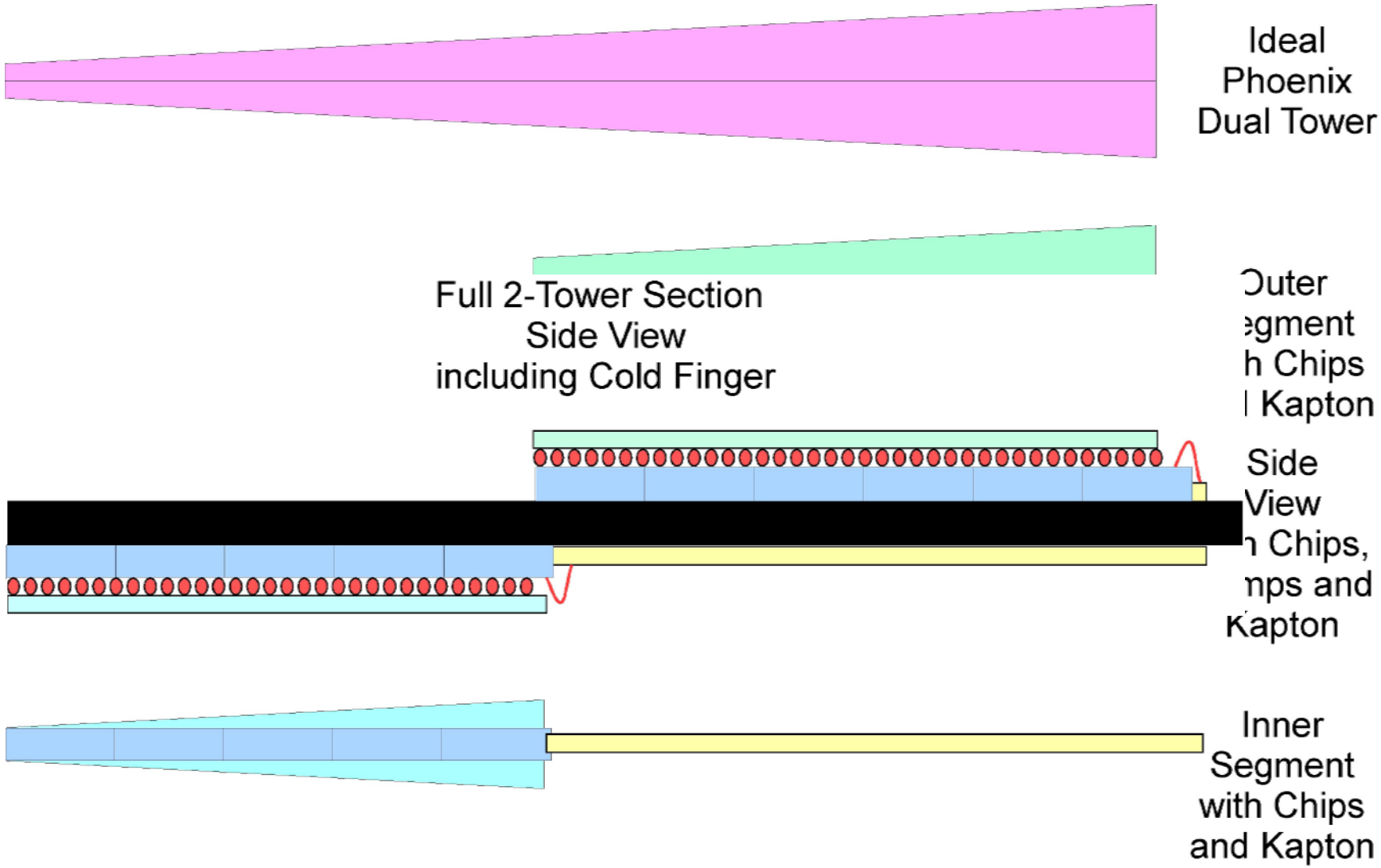
2 columns
256 channels/column
3.8 mm x 13 mm = 49.4 mm^2
Bump bonds on 200 um pitch
50 µm dia bumps
512 bumps plus inter-chip bumps

FPIX2 Layout for comparison:

Chip area = 91 mm^2
Bump bonds on 50 µm pitch
12 µm dia bumps
2816 bumps



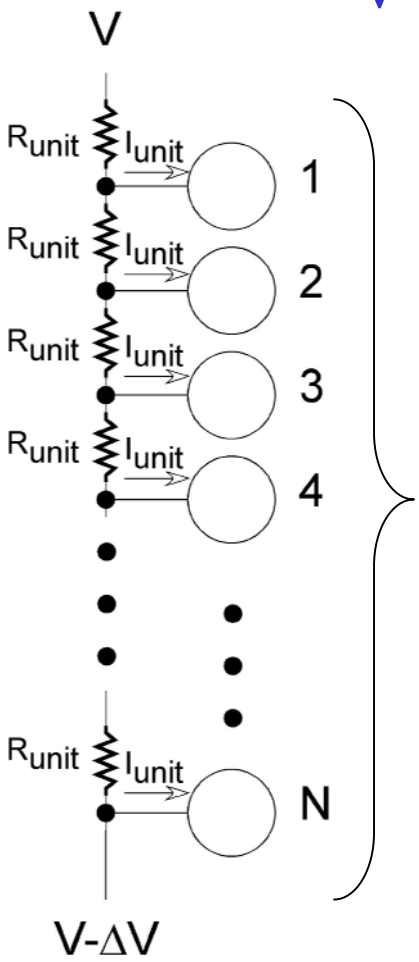
Possible Tower Section



Power Considerations

- Must minimize IR drops
- Reduce number of chips on bus
- Design full custom low power analog and digital sections
- Maximize power bus size on chip
- Use back side contact
- Possibly use cooling structure for ground return

Voltage Drop Estimation



n identical units

- Units are connected as shown
- Each unit consumes current
- What is the IR drop at the output of the last unit?

$$\Delta V = \frac{n \cdot (n-1)}{2} R_{unit} I_{unit}$$

R_{unit} Estimation

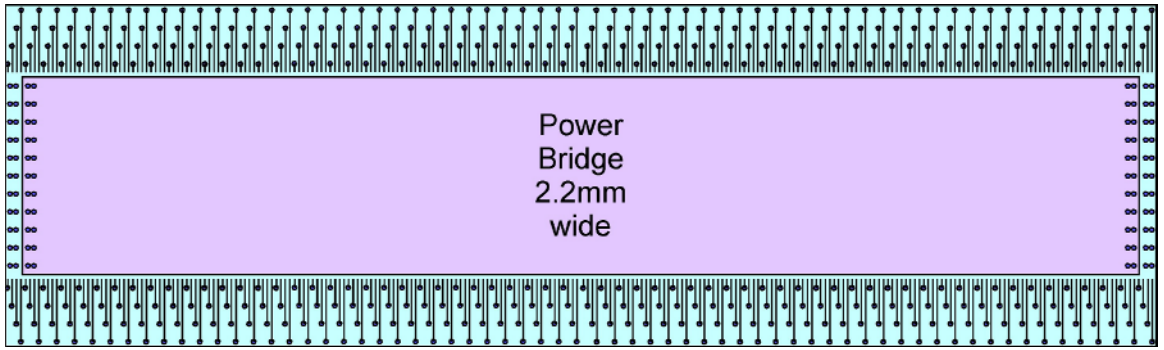
(one chip is a unit)

$$Length = 256 \times 50\mu m = 12.8mm$$

$$Width = 2.2mm$$

$$Squares = \frac{12.8}{2.2} = 5.6 \cong 6$$

$$R_{unit} = 70\frac{m\Omega}{Square} \times 6 = 420m\Omega$$



I_{unit} Estimation

- FPIX2 uses 60mA of Analog Current and 60mA of Digital Current.
- It is fairly accurate to use the FPIX2 Analog Current as an estimation of the Phoenix Mini Strip Analog Current.
- It is conservative to use the FPIX2 Digital Current as an estimation of the Phoenix Mini Strip Digital Current
    - Phoenix Mini Strip will not read out at 840MBits/sec
    - Phoenix Mini Strip will not have as many inputs and outputs

I_{unit} Estimation

$$\text{FPIX2 Analog Current} \longrightarrow \frac{60mA}{2816\,\text{cell}} = 21.3 \cong 25\frac{uA}{\text{cell}}$$

$$\text{"Phoenix" Analog Current} \longrightarrow 25\frac{uA}{\text{cell}} \times 512\ \text{cells} = \underline{\underline{12.8mA}}$$

$$\text{FPIX2 Digital Current} \longrightarrow \frac{60mA}{2816\,\text{cells}} = 21.3 \cong 25\frac{uA}{\text{cell}}$$

$$\text{"Phoenix" Digital Current} \longrightarrow 25uA \times 512\ \text{cells} = \underline{\underline{12.8mA}}$$

$$\text{Total Current} \longrightarrow 12.8\ \text{m}A + 12.8\ \text{m}A = \underline{\underline{25.6\frac{\text{mA}}{\text{Chip}}}}$$

ΔV Estimation

$$\Delta V = \frac{n \cdot (n-1)}{2} R_{unit} I_{unit}$$

Full Tower $\Delta V = \frac{11 \cdot (11-1)}{2} 70m\Omega * 25.6mA = 591.36mV \cong \underline{\underline{600mV}}$

-OR-

Split Tower

Inner Segment $\Delta V = \frac{5 \cdot (5-1)}{2} 420m\Omega * 25.6mA = 107.52mV \cong \underline{\underline{120mV}}$

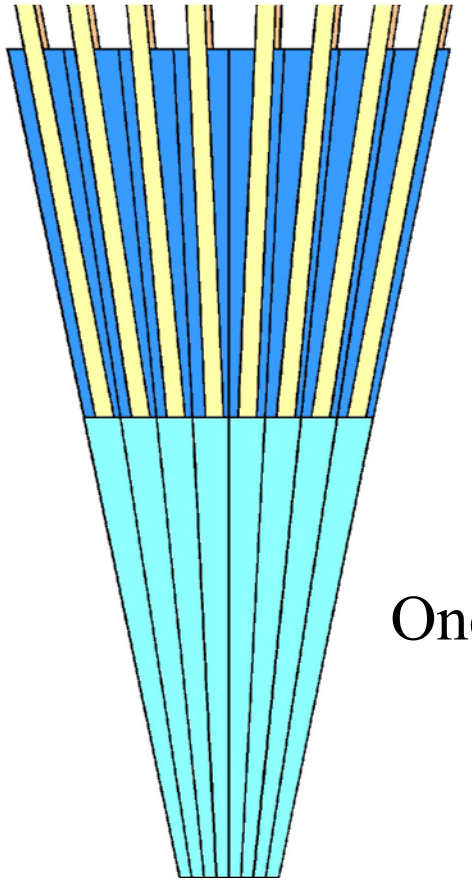
Outer Segment $\Delta V = \frac{6 \cdot (6-1)}{2} 420m\Omega * 25.6mA = 161.28mV \cong \underline{\underline{175mV}}$

Tower Interface Ideas

- No interface, communicate directly with data combiner board located 1 m away.
- Have interface chips similar to those used with SVX4 mounted on cooling surface at top of each tower.
  - Transceivers
  - DAC, Decoders, Regulators

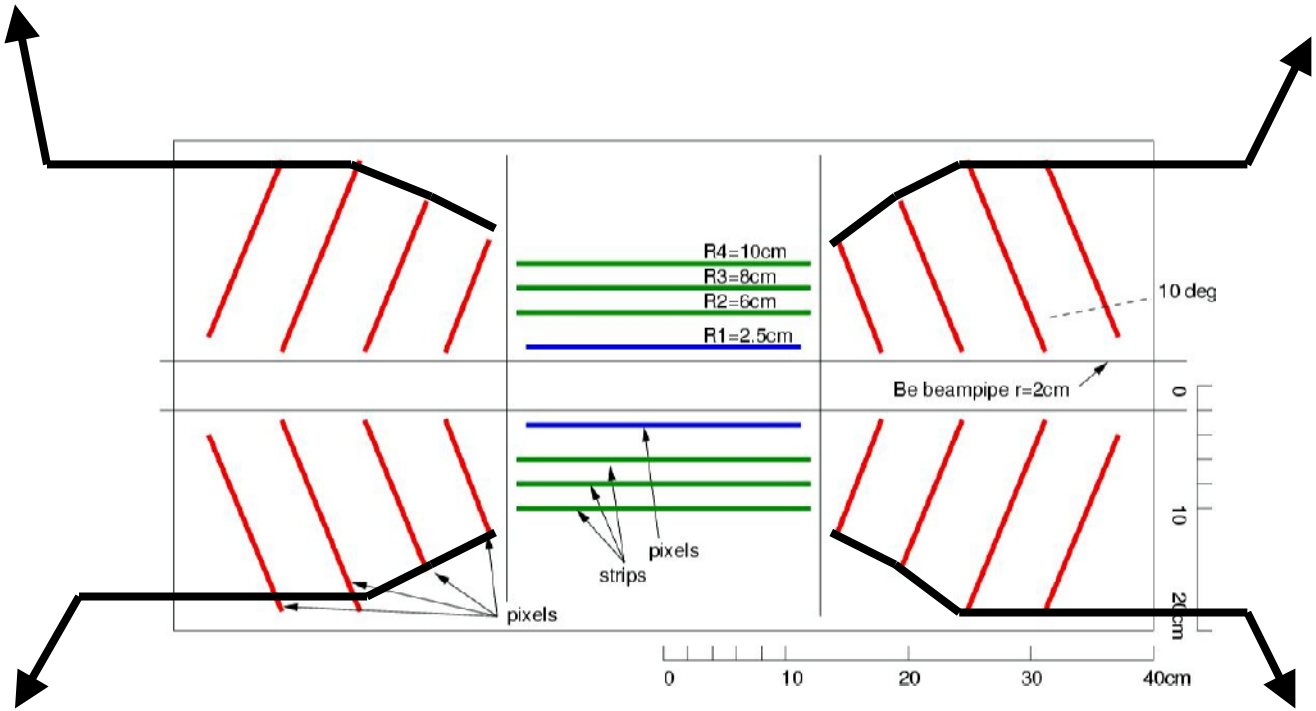
Wedge Assembly Idea

Go to 16 wedges/lampshade to reduce the size of silicon detector pieces and sub assembly size for better yields



One wedge

Cable Routing



Proposed Design Plan

- Build first prototype using multiproject submission (40 chips)
  - Multiple front end designs
  - Use full sparsification and I/O
  - Add numerous test points
  - Chip size = 3.8 mm x 6.5 mm (or full size at higher cost to understand IR drops)
- Fabricate Engineering Run with optimized front end and final digital design (12 wafers)

Production Needs

- 110 towers/lampshade x 8 = 880 towers
- 3000 strips per tower
- 6000 strips per double tower
- 512 channels per readout chip
- 12 readout chips per double tower
- 12 chips x 440 double tower = 5280 chips
- For spares and assembly loss, need 7500 tested good chips.

Production Needs (cont.)

- Useable wafer area = 31,416 x .85 = 26,700 mm^2
- Chip size = 3.8 x 13 = 49.4 mm^2
- 26,700/49.4 = 540 chips per wafer
- Assume 75% yield
- Get 405 good chips per wafers
- Need 7500/405 = 18.5 wafers
- Typical engineering run delivers 10-12 wafers

Schedule Estimate

- Design specifications completed 10/03
- Start design 12/03
- Submit prototype 7/04
- Prototype testing completed 12/04
- Redesign completed for engineering run 1/05
- Engineering run back 3/05

Cost Estimate

- Chip design/testing – 2 man-years - $275K (includes all overhead costs)
- Prototype chip fabrication- $40K (small chip), or $80K (large chip)
- Test board $5K
- Engineering run (10-12 wafers) $200K
- 9 Extra wafers using same masks - $45K
- Production wafer level testing –engineering, tech time, circuit board, probe card - $60K
- Contingency??

Issues to be Studied Further

- Maximum assembly size for fabrication and good yield: number of chips/subassembly
- Need for support chips
- Readout chip wafer processing: bumping, grinding, plating
- Detector metalization
- Readout chip On-chip bypassing
- Data flow rates