

# 3D Design Activities at Fermilab and Associated Opportunities for Physics



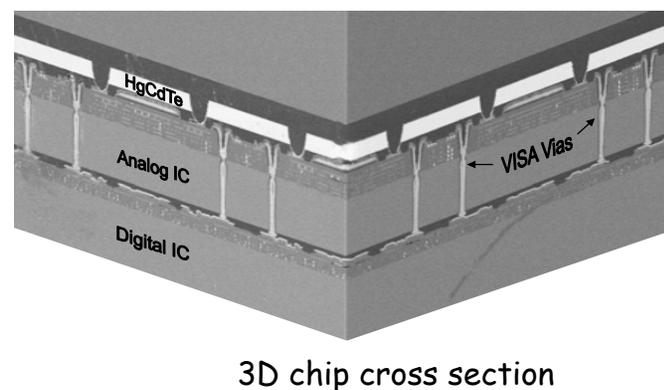
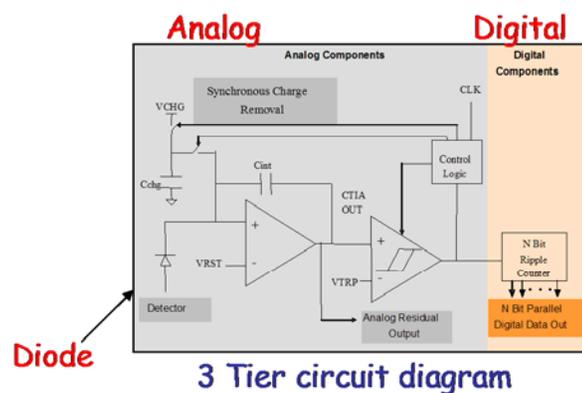
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La Biodola, Isola d'Elba, Italy  
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# Introduction

Fermilab began exploring the technologies for vertically integrated circuits (3D) in 2006. These technologies include through silicon vias, circuit thinning, and bonding techniques to replace conventional bump bonds. Since then, the interest within the HEP community has grown considerably. This talk will provide a brief overview of the activities at Fermilab over the last 3 years.



3D Example - 3 Tier Vertically Integrated 256 x 256 Pixel Array<sup>1</sup>

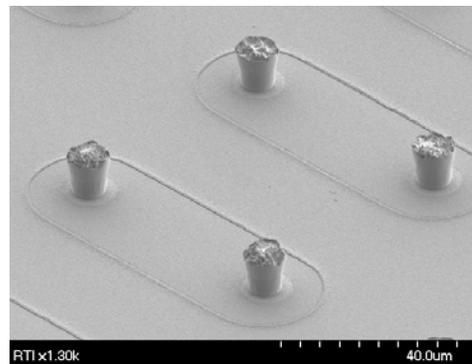
# Outline

- Review processes explored at Fermilab for vertically integrated circuits
  - Chip to wafer bonding
    - RTI
    - Ziptronix
  - 3D Chip fabrication
    - MIT LL 3D process
    - Tezzaron 3D process
- Formation of consortium to produce 3D MPW runs
- Describe 3D designs from Fermilab
  - MIT LL
  - Tezzaron

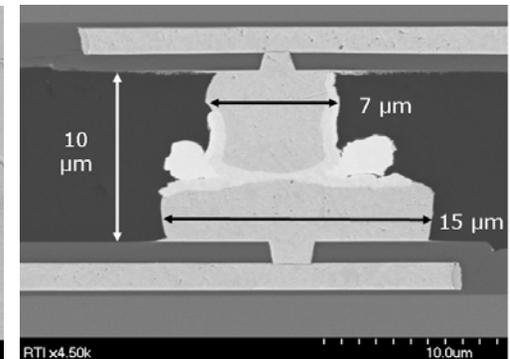
# Bonding

- Bonding along with precision alignment are critical components of 3D integration.
- Bonding approaches
  - Die to wafer, results in highest circuit yield
  - Wafer to wafer bonding, results in lowest cost per mated circuits.
- Fermilab has worked with multiple vendors
  - Bonding techniques to replace bump bonds
    - **RTI** - CuSn eutectic
    - **Ziptronix** - Direct bond interconnect
  - Bonding techniques for 3D circuit fabrication
    - **MIT LL** - Oxide bonding
    - **Tezzaron** - Copper to copper

- **RTI<sup>2</sup>** - CuSn bonding.
  - Bonding at 20 um pitch was demonstrated
  - Higher yields and stronger bonds with CuSn than with PbSn on equivalent test structures
  - Relatively low cost
  - Large area coverage (high mass) needed to reduce warpage if post bond thinning is required



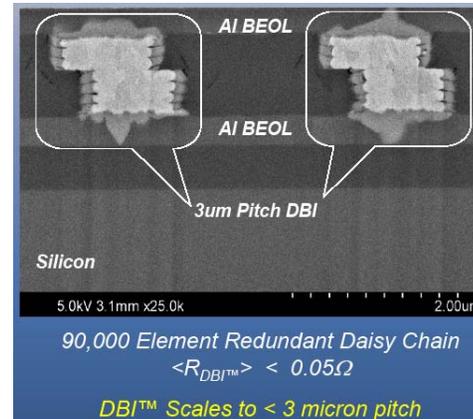
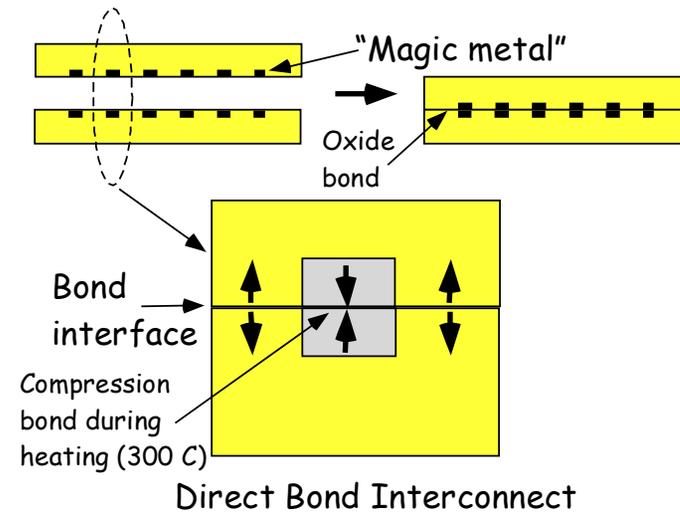
7 um dia CuSn pillars  
Before bonding



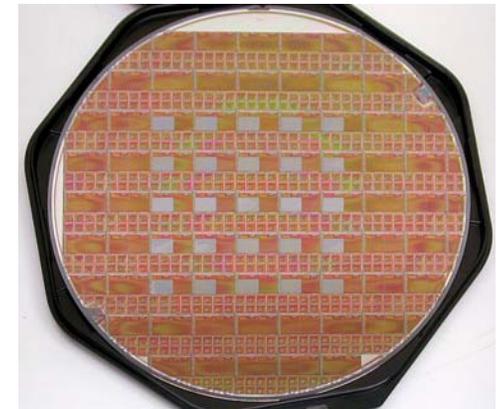
CuSn bond Cross section

# Bonding

- **Ziptronix** - Direct Bond Interconnect (DBI)
  - Begin with metal contacts imbedded in smooth oxide surface
  - Bring oxide surfaces together to form an immediate oxide bond.
  - After oxide bond reaches sufficient strength, devices are heated and the metal contacts expand to form compression bonds.
  - Technique provides minimal metal needed to form electrical connections.
    - Provides extremely low  $X_o$  and is excellent choice for ILC
    - Metal bond  $\sim 1 \mu\text{m} \times 1 \mu\text{m}$
  - No surface warping when mated parts are further thinned ( $\sim 25 \mu\text{m}$ )
- DBI used for die to wafer bonding by Fermilab to mount sensors to ROIC wafer
  - Sensors then thinned to  $100 \mu\text{m}$
  - Yield - reasonable
  - Cost - still relatively high
- Process is currently only offered by one vendor - (Ziptronix, in North Carolina) but licensing is now available.



3 um pitch DBI<sup>3</sup>



25 sensors bonded to ROIC wafer with DBI

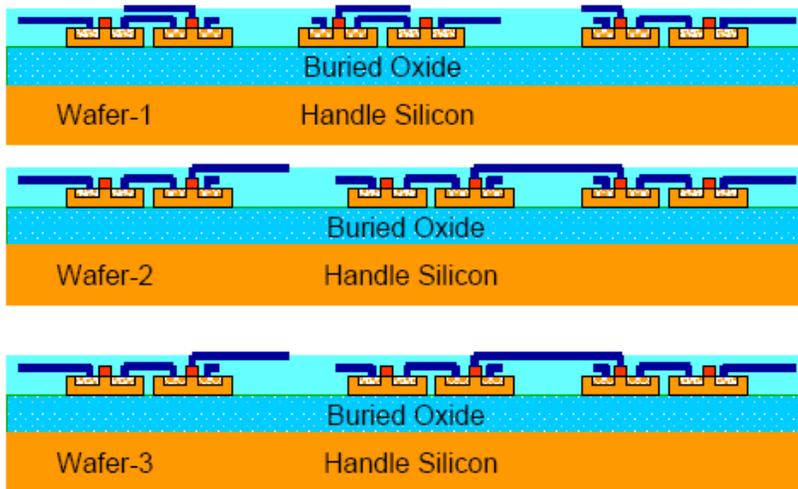
# 3D Chip Fabrication

- Fermilab has worked with 2 different vendors that offer full 3D circuit fabrication.
  - MIT Lincoln Laboratories
    - 0.18 um in house SOI process
    - Oxide bonding between wafers
    - Via last process (vias added to wafers after bonding and thinning)
    - 3 Tier stack of wafers
  - Tezzaron
    - 0.13 um CMOS process from Chartered Semiconductor
    - Copper - copper bonding between wafers
    - Vias first process (vias imbedded in wafers during wafer fabrication)
    - 2 Tier stack of wafers
- Examine bonding and via formation more closely

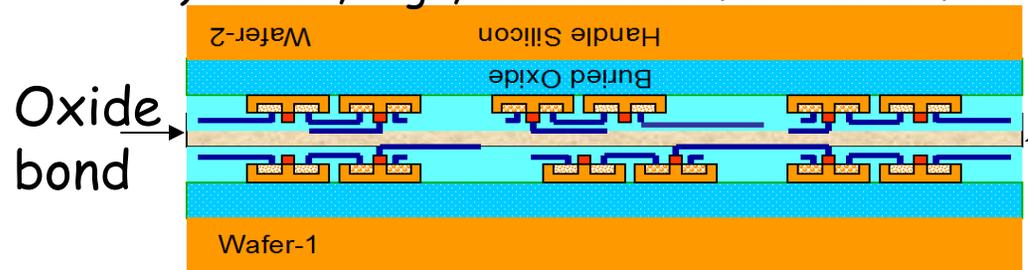
# Process Flow for MIT LL 3D Chip

- 3 tier chip (tier 1 may be CMOS)
- Vias formed after FEOL and BEOL processing is completed

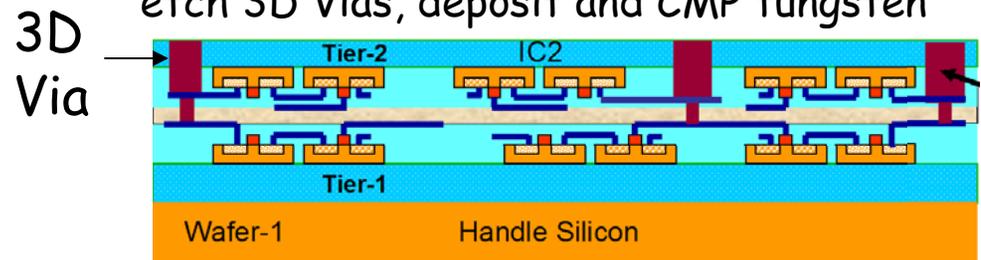
1) - fabricate individual wafers



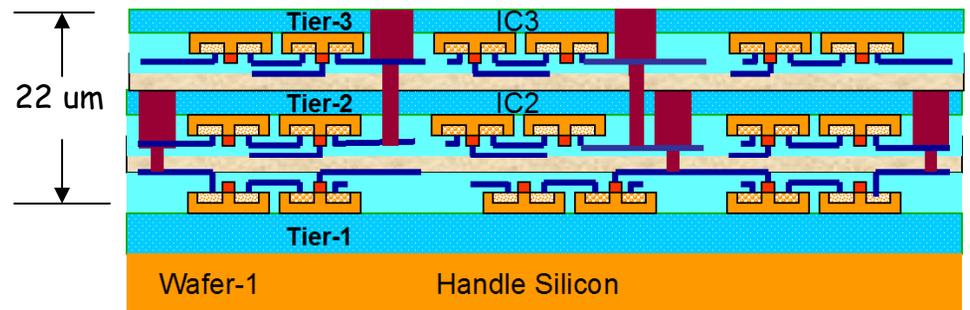
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



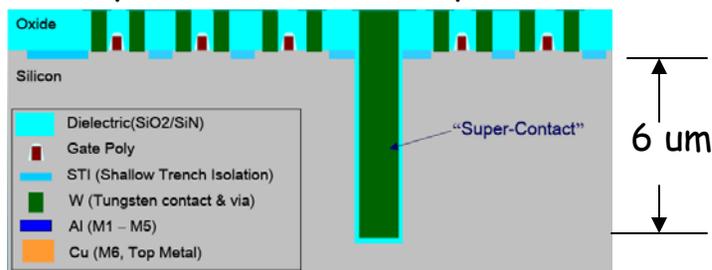
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



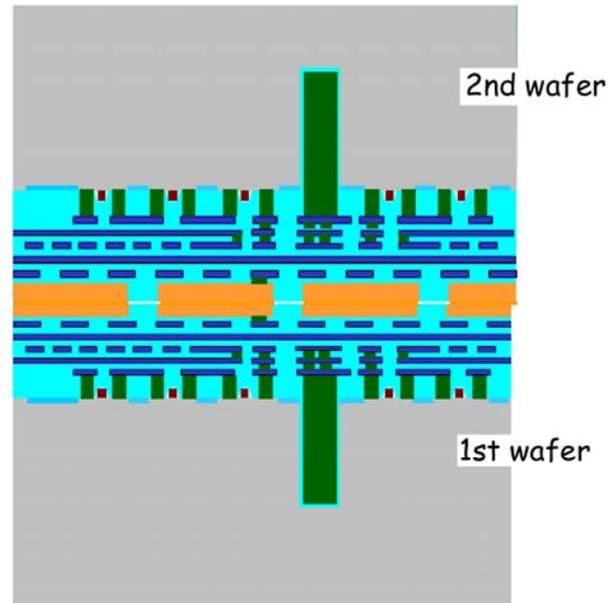
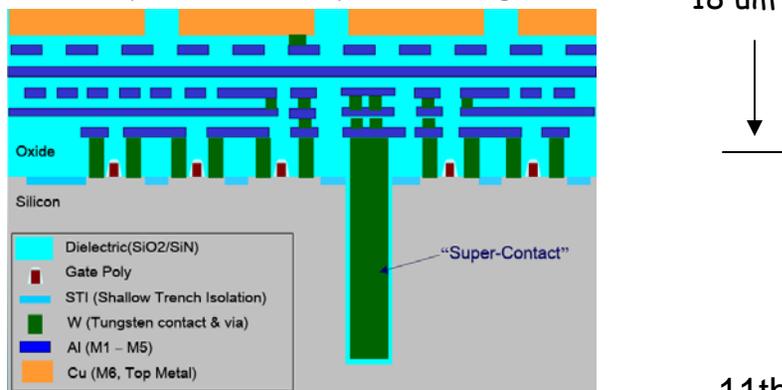
# Process Flow for Tezzaron 3D Chip

- Two tier chip (additional tiers can be added)
- Vias formed just after transistor fabrication

1) Complete transistor fabrication, form, passivate and fill super via

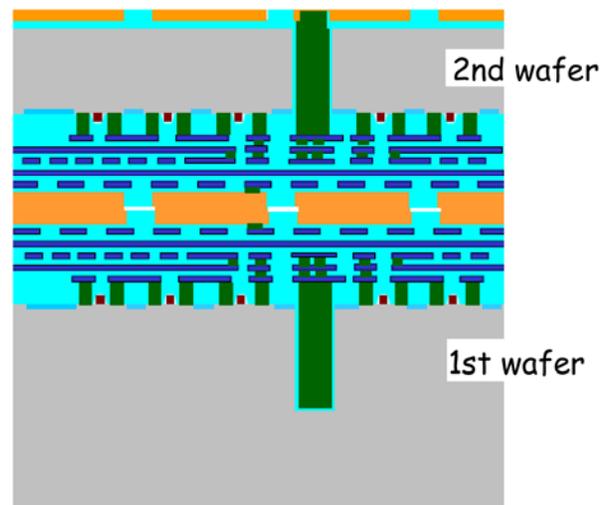


2) Complete BEOL processing



3) Flip 2<sup>nd</sup> wafer on top of first wafer

Bond 2<sup>nd</sup> wafer to 1<sup>st</sup> wafer using Cu-Cu thermo-compression bond



4) Thin 2<sup>nd</sup> wafer to 12 um to expose super Contact.

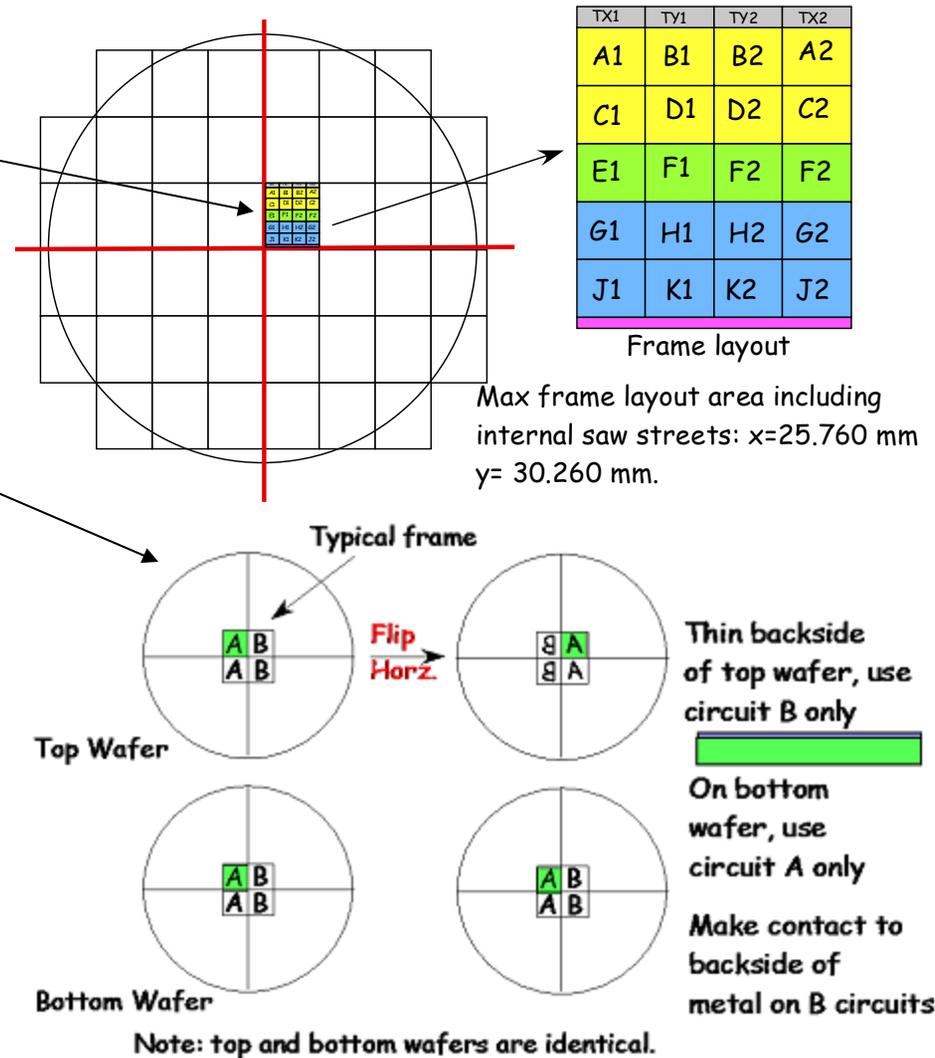
Add metalization to back of 2<sup>nd</sup> wafer for bump or wire bond.

# Consortium Formed for 3D Design

- Organized by Fermilab (late 2008)
- Benefits
  - Sharing of designs
  - Development of special software programs
  - Development of libraries
  - Design reviews
  - Sharing of results
  - Frequent meetings
  - Cost reduction
- Near close of first MPW run with Tezzaron
- Currently 15 members (others joining)
  - Fermilab, Batavia
  - University at Bergamo
  - University at Pavia
  - University at Perugia
  - INFN Bologna
  - INFN at Pisa
  - INFN at Rome
  - CPPM, Marseilles
  - IPHC, Strasbourg
  - IRFU Saclay
  - LAL, Orsay
  - LPNHE, Paris
  - CMP, Grenoble
  - University of Bonn
  - AGH University of Science & Technology, Poland

# First Tezzaron MPW Run

- Wafers fabricated in Chartered 0.13 um CMOS process
- Frame divided into 12 subreticules among consortium members
- One set of masks used for both top and bottom tiers to reduce cost of 2 tier circuit.
  - Identical wafers bonded face to face by Tezzaron.
  - Backside metallization by Tezzaron.
- More than 25 separate designs (circuits and test devices)
  - CMS strips, ATLAS pixels
  - ILC pixels
  - B factory pixels
  - X-ray imaging
  - Test circuits
    - Radiation
    - Cryogenic operation
    - Via and bonding reliability
    - SEU tolerance



# 3D Designs by Fermilab

- Circuits

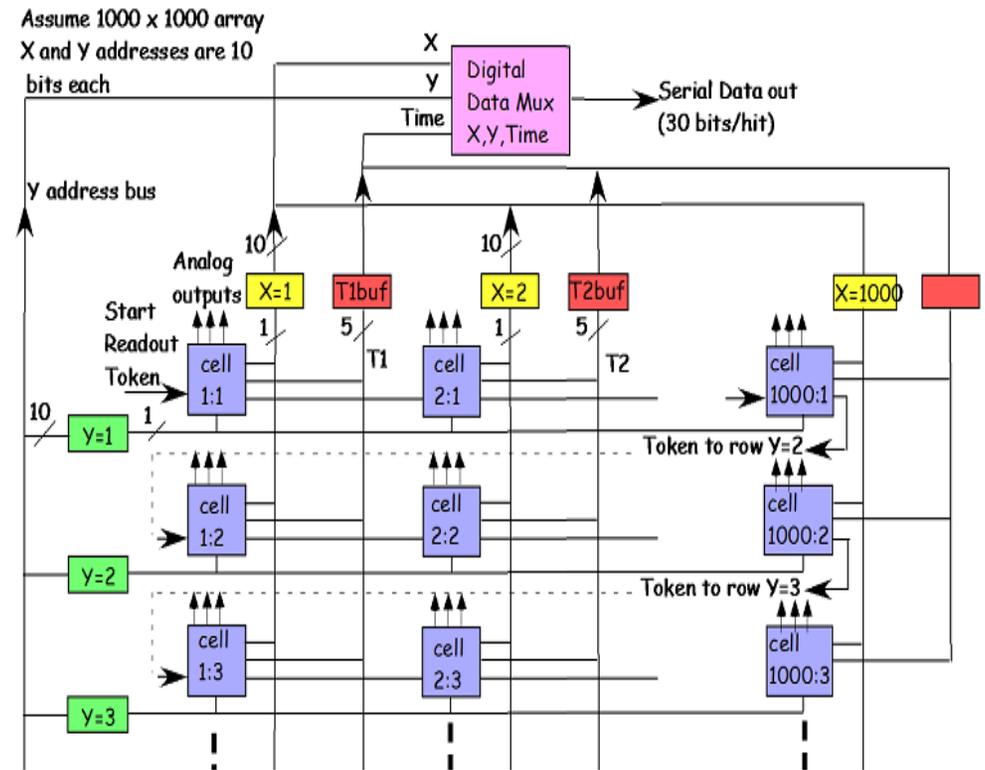
- VIP1 - MIT LL (2.5 x 2.5 mm)
- VIP2a - MIT LL (2.5 x 2.5 mm)
- VIP2b - Tezzaron (6.3 x 5.5 mm)
- VICTR - Tezzaron (6.3 x 5.5 mm)
- VIPIC - Tezzaron (6.3 x 5.5 mm)

- Test Chips

- TX test chip - Tezzaron (6.3 x 2.0 mm)
- TY test chip - Tezzaron (6.3 x 2.0 mm)
  - Test chips TX and TY will not be covered in this talk

# VIP1 and VIP2a

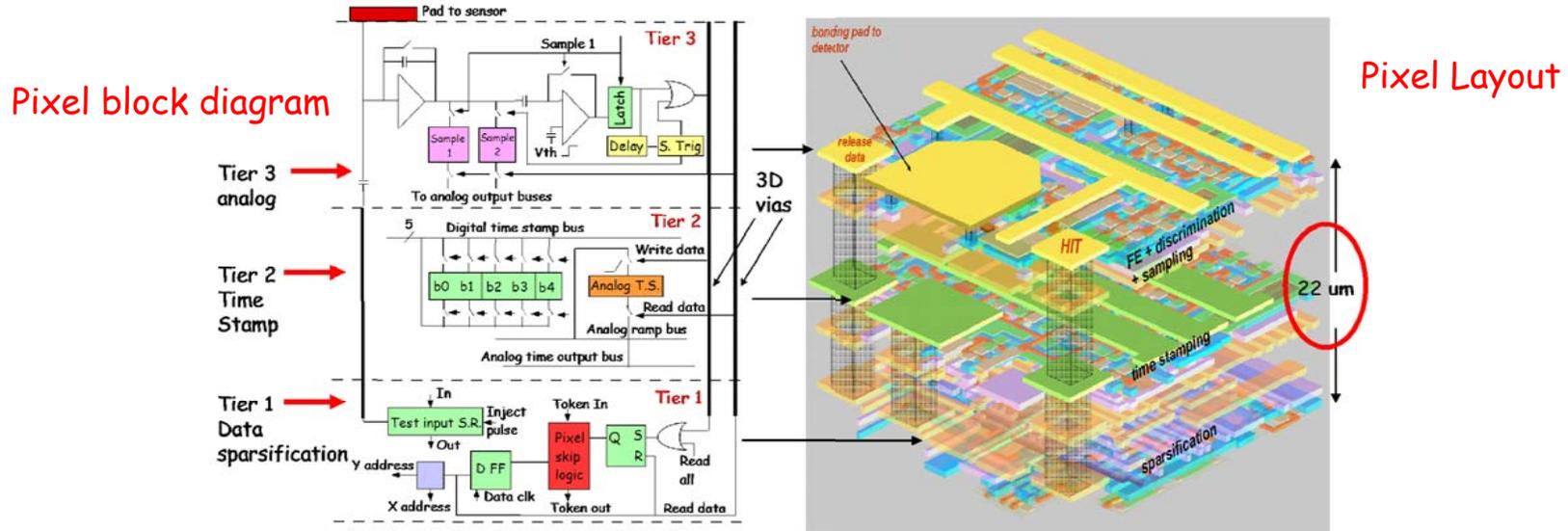
- Demonstrator chips for ILC pixels include most of functionality needed for ILC.
- VIP1 chip<sup>4</sup>
  - Readout between ILC bunch trains
  - High speed data sparsification included
  - Analog output available for improved resolution
  - Digital and analog time stamping options explored
    - Designed for 5-10 bit resolution (30-1 usec resolution)
  - Test input for every pixel
  - 4096 pixel array with 20 um pixels, scaleable to 1 Mpix



VIP1 Functional block Diagram

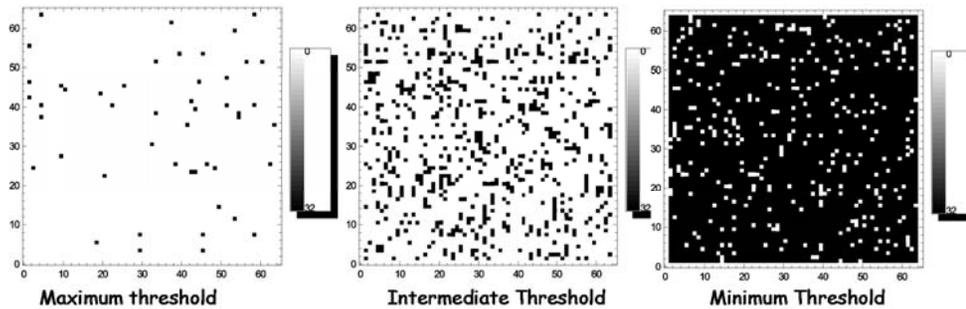
# VIP1 and VIP2a

- VIP1 designed in 3 tier MIT LL 0.18 um SOI process
- Sensor layer not available in MIT LL MPW run



Data readout out using data sparsification scheme.

VIP1  
Test  
Result



Decreasing Threshold



VIP1 found to be functional. Detailed results presented elsewhere<sup>4</sup>.

VIP1 Yield was low.

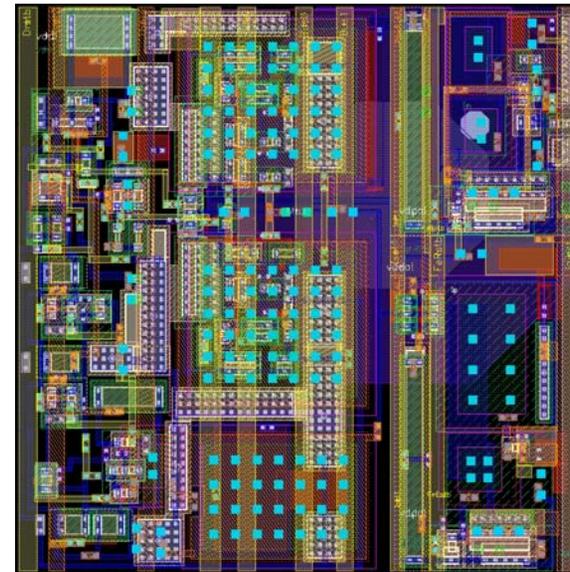
VIP2a designed to improve yield through improved power distribution, wider traces and redundant vias among other things at expense of larger, 30 um, pixel size

VIP2a is in fabrication

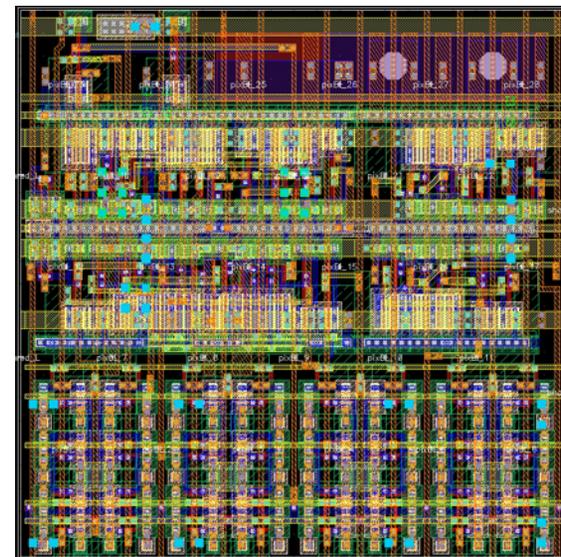
Focus has shifted from working in SOI to CMOS processes

# VIP2b

- Design based on VIP1 and 2a
- Designed in Chartered 0.13 um low power CMOS
- Changes from VIP1 and VIP2a
  - Converted 3 tier design to 2 tiers
  - Removed analog time stamping
  - Increased digital time stamp from 5 bits to 8 bits for 3.9 us time resolution.
  - Larger array 192 x 192
  - Pixel size increased to 24 microns to accommodate larger digital time stamp and maintain analog information through the use of MiM capacitors.
- Expect better yield from commercial CMOS process
- Expect better radiation tolerance
- Submitted for fabrication in May 2009



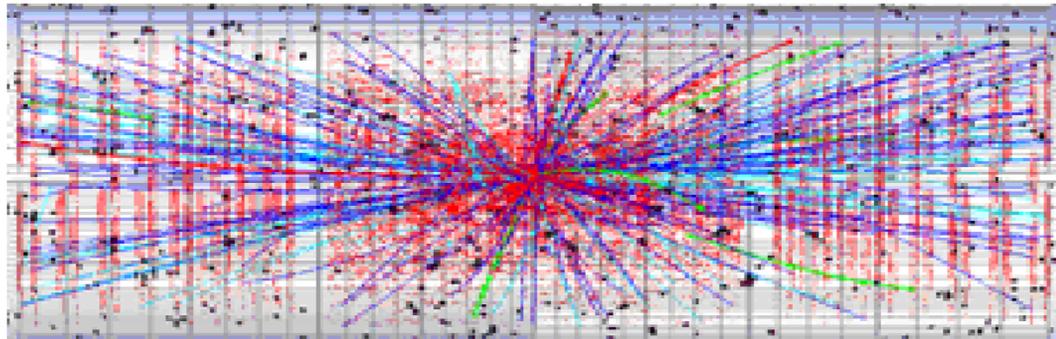
Pixel  
Top Tier  
(analog)



Pixel  
Bottom tier  
(digital)

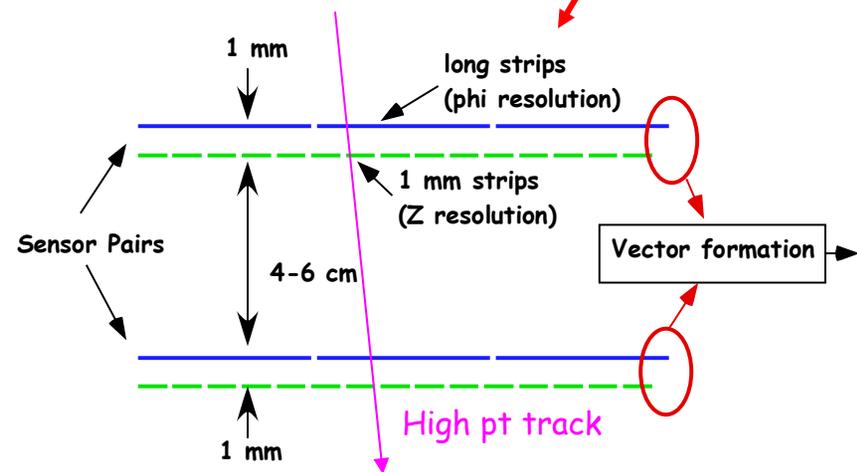
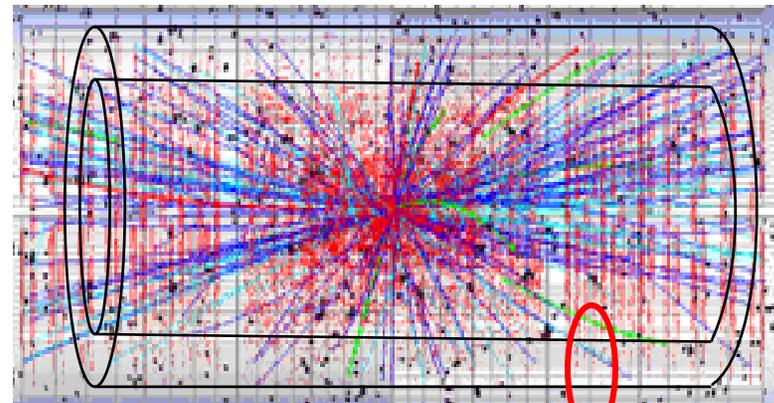
# VICTR-3D Demonstrator Chip for CMS

- SLHC tracker occupancy at  $10^{34}$  and  $10^{35} \text{ cm}^{-2}\text{s}^{-1}$  is extremely high
- An L1 track trigger will be necessary for data reduction since all data cannot be transferred at 40 MHz<sup>5</sup>
  - Must identify hits associated with pt above 2 GeV for data transfer
  - Must rapidly identify high pt tracks with pt above 15-25 GeV
  - Must provide good Z vertex resolution of about 1mm for tracks above 2 GeV
- Need to reduce track hit data by a factor of 100 to 200.

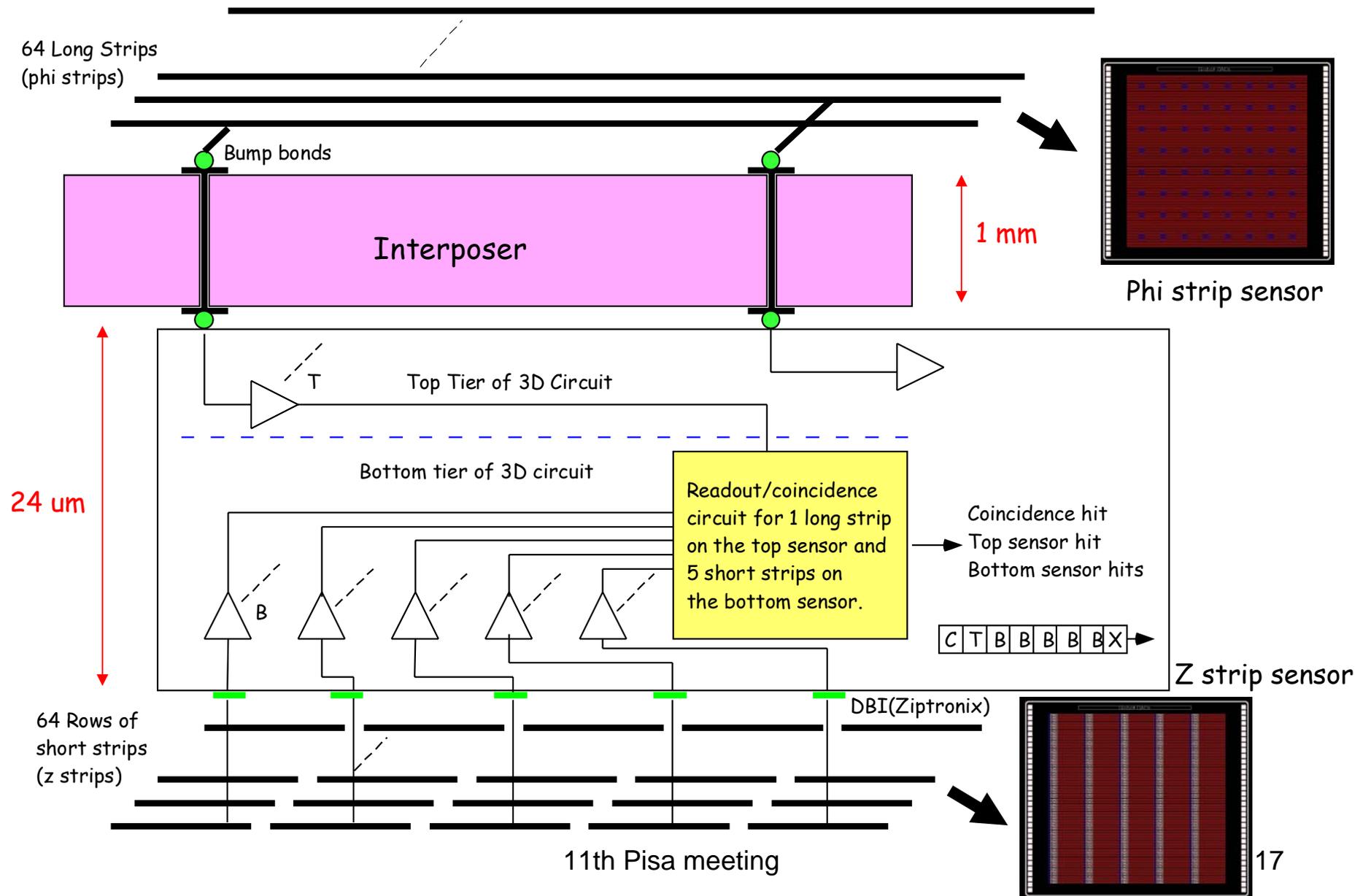


# One Approach to Data Reduction Using Pairs of Sensor Planes

- Detector module: Comprised of a pair of sensor planes with about 1mm separation and VICTR (Vertically Integrated CMS Tracker) chip
  - Locally collect hits from both sensors
  - Finds hit pairs with  $p_t > 2\text{GeV}$
  - Transfers data to vector forming circuit
- Vector forming circuit
  - Locally collect hit pairs  $> 2\text{GeV}$  from two barrels of detector modules
  - Form track vectors for identification of high  $p_t$  tracks
  - Rejects track vectors with low  $p_t$  to further reduce data rate before transferring data off the detector



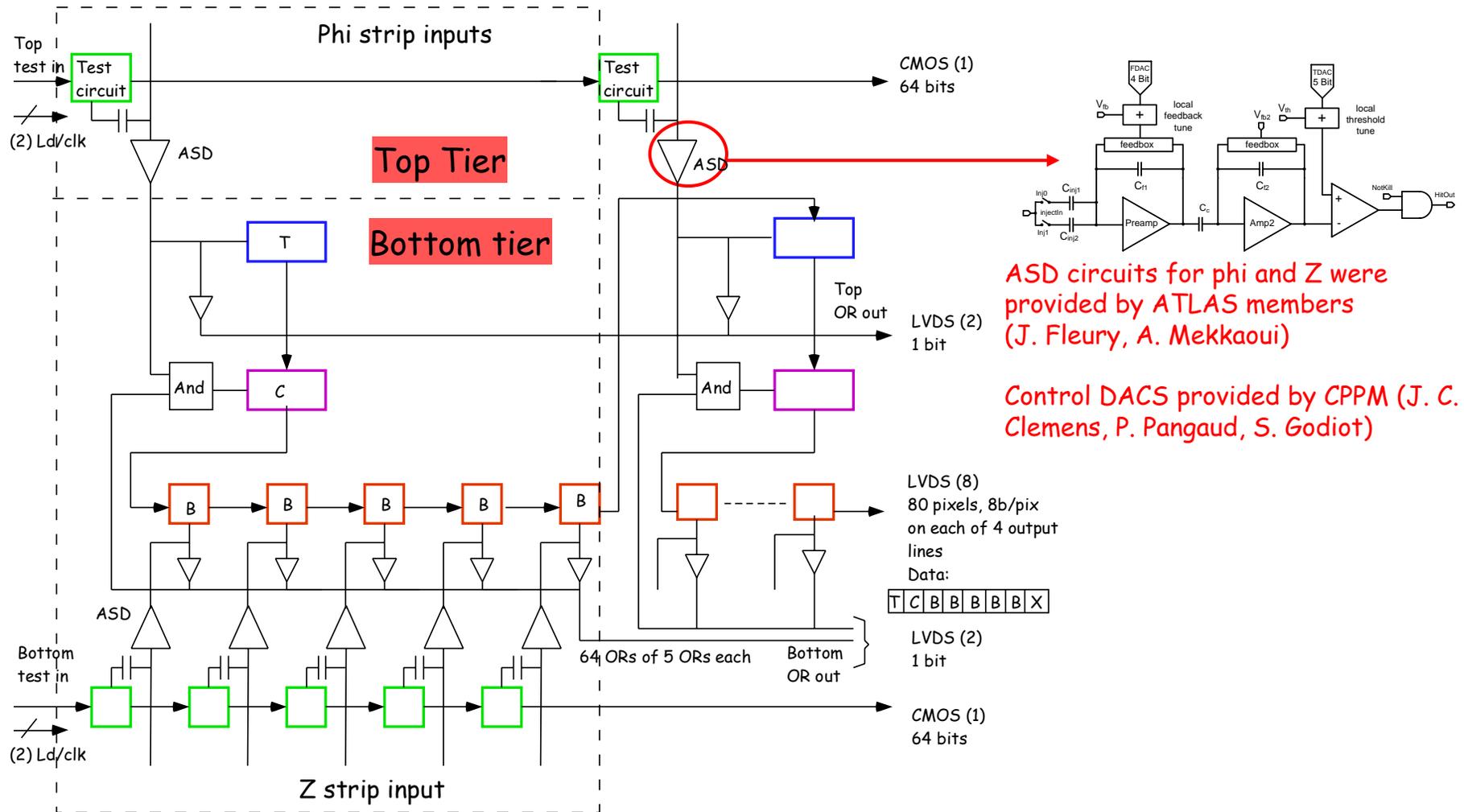
# Simplified Functional View of CMS Demonstrator Chip (VICTR)



# VICTR Demonstrator Chip

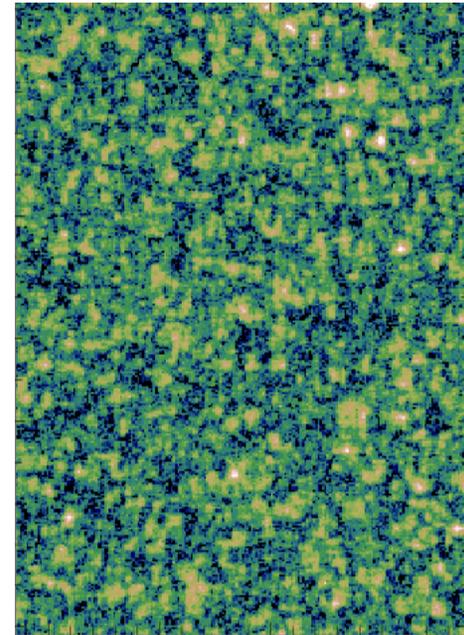
- Demonstrator chip is a two tier 3D chip.
  - The **top tier** processes sensor signals from the top sensor with an ASD and sends the resultant signal to the bottom tier of the ROIC.
  - The **bottom tier** processes signals from the bottom sensor with an ASD and performs additional signal processing
    - The bottom tier looks for a coincidence between 1 long strip from the top sensor and the 5 short strips from the bottom sensor directly underneath
    - The bottom tier reads out all hits on 64 long and 320 short strips along with coincidence hits via 4 output lines.
- Readout from the chip is done serially (T-C-B-B-B-B-X)
- In a final version, the simple coincidence circuit will take into account neighbor strips.
- Other electrical features
  - Fast Or outputs for Top Hits, Bottom Hits, and Coincidence Hits
  - 80 micron pitch for top and bottom sensors
  - Downloadable hit patterns into all preamplifiers for testing.
- Interesting mechanical features
  - The 3D circuit is thinned to 24 microns
  - Through Silicon Vias (TSVs) are used to make electrical connections to both the top and bottom of the 3D chip

# Block diagram of 2 Tier Circuit for 1 Phi Strip and 5 Z Strips For VICTR (Vertically Integrated CMS Tracker) Chip



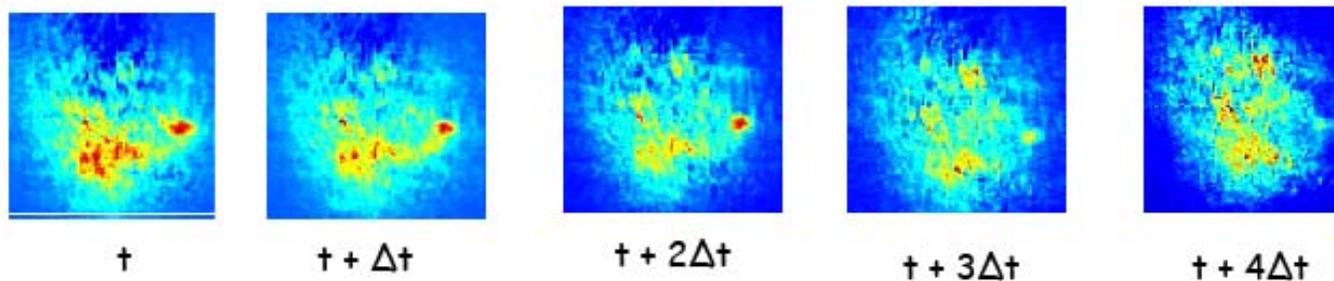
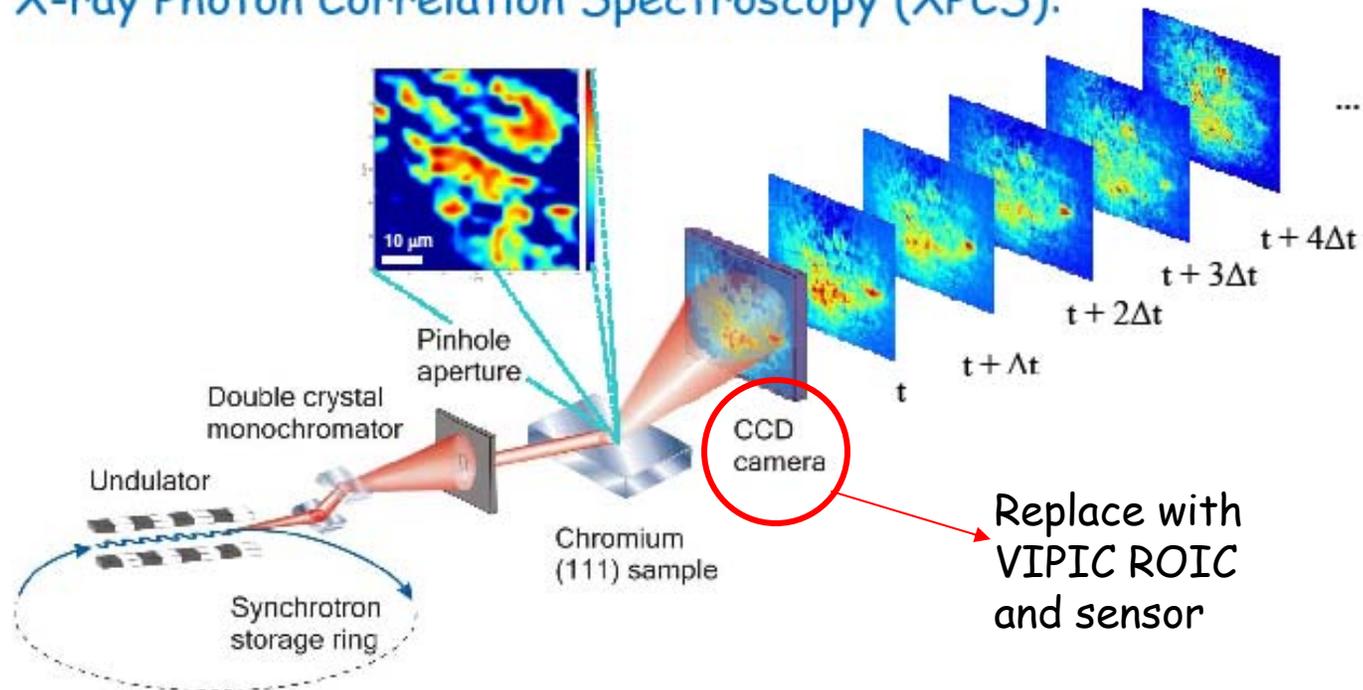
# X-ray Photon Correlation Spectroscopy (XPCS)

- XPCS is a novel technique that studies the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems (e.g. gels, colloids, liquid crystals, bio-materials, membranes, metals, oxides, magnets, etc.)<sup>6</sup>
- XPCS is based on the generation of a speckle pattern by the scattering of coherent X-rays from a material where spatial inhomogeneities are present.
- If the state of disorder of the system changes with time, the speckle pattern will change. Thus by studying the time dependence of the scattered intensity, one can study the dynamics of the materials both in or out of thermodynamic equilibrium (e.g. diffusion constants, magnetic domain relaxation times, phase transformations)
- Advantages
  - Observe smaller features sizes
  - Can be used to observe charge, spin, chemical and atomic structure behavior.
  - Works with non-transparent materials



Speckle pattern

# X-ray Photon Correlation Spectroscopy (XPCS):<sup>7</sup>

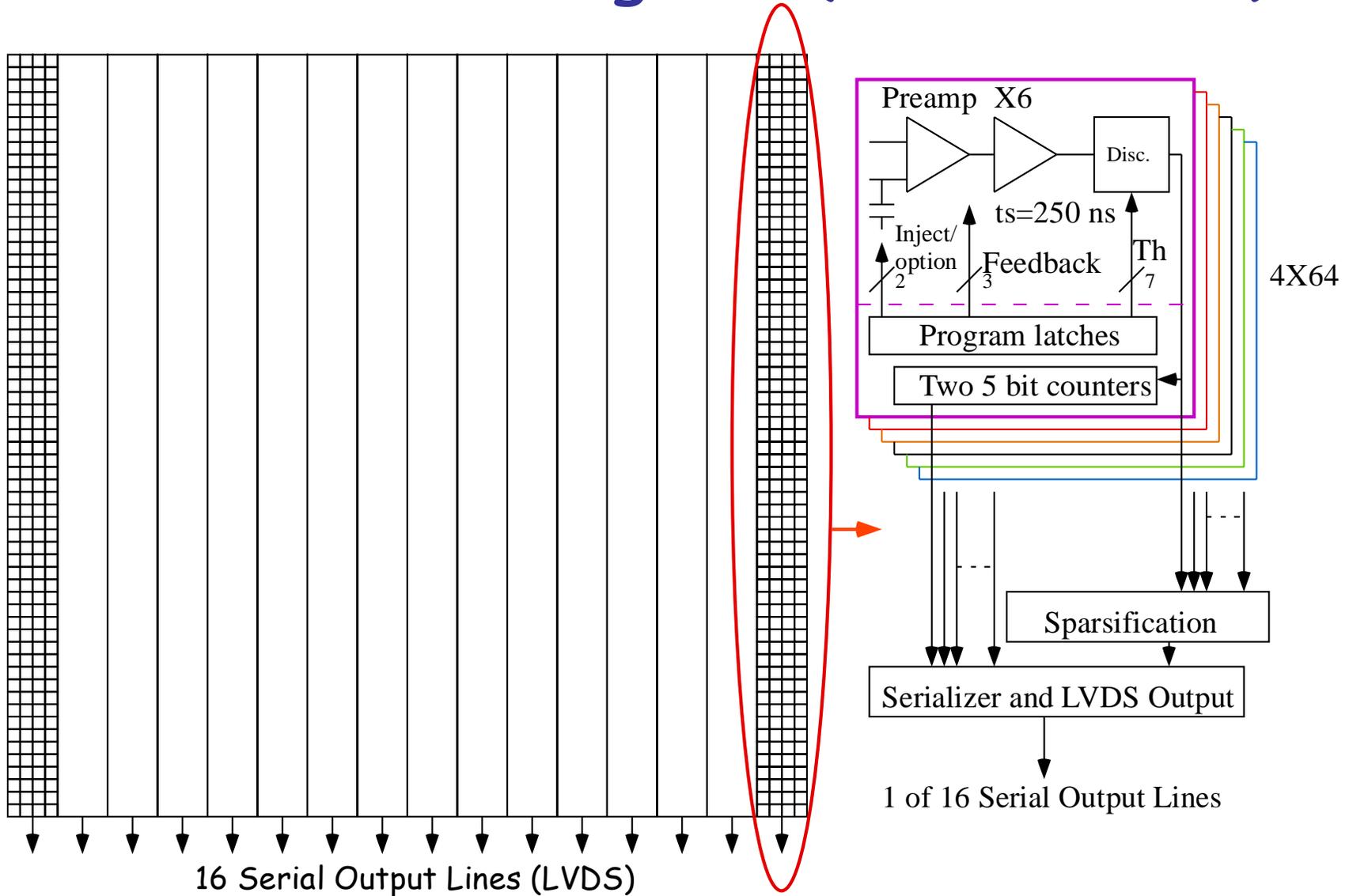


O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

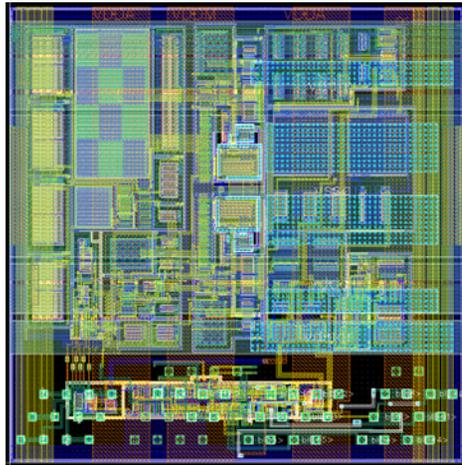
# VIPIC (Vertically Integrated Photon Imaging Chip)

- Specifications
  - 64 x 64 array of 80 micron pixels
  - Dead timeless operation
  - Sparsified data readout
  - Binary readout (no energy information)
  - High speed frame readout time (10 usec for occupancy ~ 100 photons/cm<sup>2</sup>/usec)
  - Optimized for photon energy of 8KeV
  - Triggerless operation
- Features (5.5 x 6.3 mm die size)
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Address generated by circuit without hard coding
  - Constant pixel address readout time (5 ns) regardless of hit pixel location by means of binary tree principle.
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tier readout chip with separate analog and digital sections
  - Adaptable to 4 side buttable X-ray detector arrays

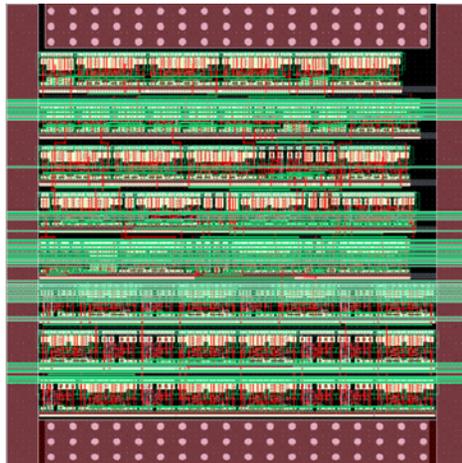
# VIPIC Block Diagram (4096 Pixels)



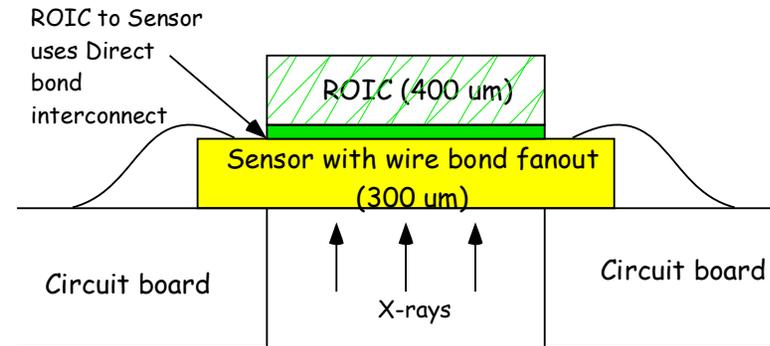
# Pixel Tier Layouts and Sensor Mounting Options



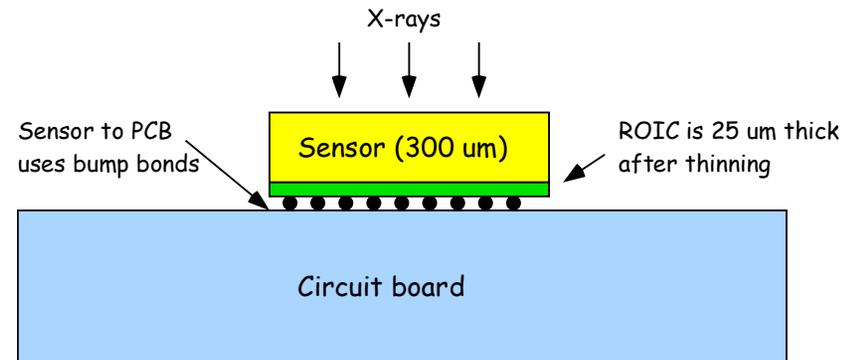
Analog Pixel Tier



Digital Pixel Tier



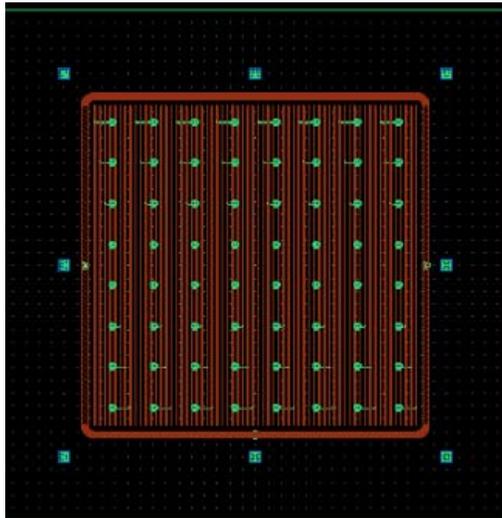
Option 1 - Less Aggressive Mounting



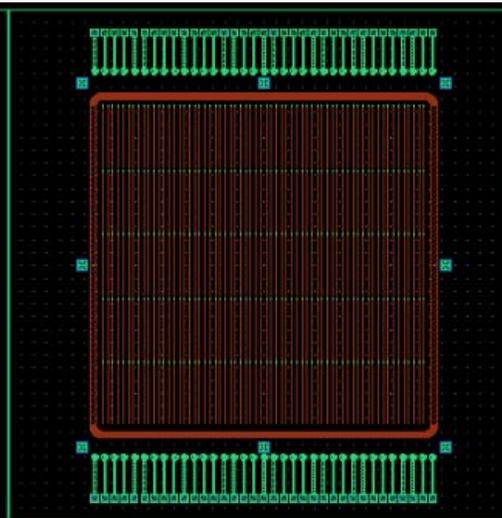
Option 2 - More Aggressive Mounting for four side buttable sensor arrays

# Sensor Floorplan for VIP2b, VICTR, VIPIC with Fanout for Wire bonding

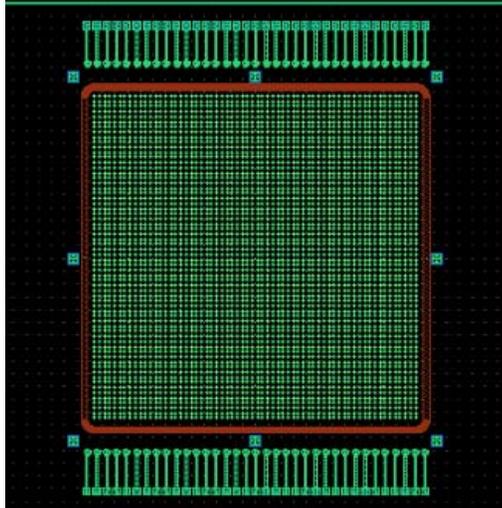
VICTR  
Phi strips



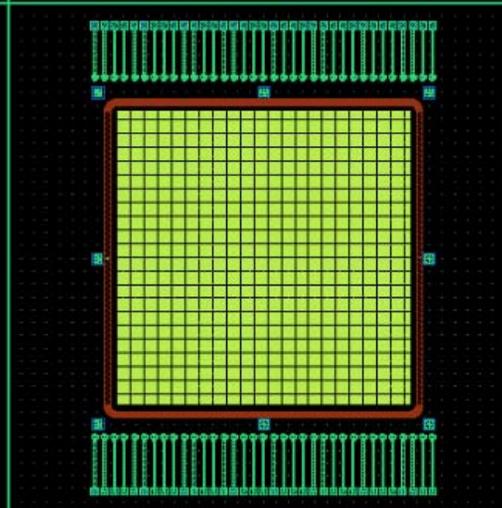
VICTR  
Z strips



VIP2b



VIPIC



# Summary

Fermilab has demonstrated two different processes for replacement of conventional solder bump bonds. The lower cost CuSn technology was shown to work at a pitch of 20  $\mu\text{m}$  and have better yield and strength than PbSn. DBI is a higher cost process but has much lower mass and pitch (3  $\mu\text{m}$ ), and has greater strength for post bond thinning.

Fermilab has been working with two different vendors for 3D chip fabrication. MIT LL uses a via last SOI process with oxide wafer bonding. Tezzaron uses a via first CMOS process with copper-copper wafer bonding.

Fermilab has organized an international consortium of 15 HEP institutions to develop 3D chips. The first MPW run to Tezzaron is nearly ready for fabrication.

Designs from Fermilab for ILC pixels, CMS strips, and X-ray imaging were described showing the range of opportunities in physics for 3D circuits.

# References

- 1) D. Temple, et. Al., *3-D integration Technology Platform for High Performance Detector Arrays*, public release from RTI International and DRS Technologies.
- 2) Allan Huffman, "Fabrication, Assembly, and Evaluation of Cu-Cu Bump bonding Arrays for Ultra-fine Pitch Hybridization and 3D Integration", presented at Pixel 2008, Fermilab, Batavia, Illinois, September 22-26, 2008.
- 3) Paul Enquist, *Direct bond Technology for 3-D IC Applications, 3D Architectures for Semiconductor Integration and Packaging*, Oct, 2007.
- 4) Ray Yarema, "3D IC Pixel Electronics- the Next Challenge", Proceedings of the Topical Workshop on Electronics for Particle Physics (TWEPP-08), Naxos Greece, Sept 15-19, 2008, pp.183-187.
- 5) Marcello Mannelli, *CMS Tracking trigger Straw Men*, CERN ACES Workshop, February 2009
- 6) Eric Dufresne, *What is X-ray Photon Correlation Spectroscopy (XPCS)?*, Argonne National laboratory,  
<http://sector7.xor.aps.anl.gov/~dufresne/UofM/xpcs.html>
- 7) Oleg Shpyrko, *XPCS Studies of Antiferromagnetic Domain Wall Dynamics in Elemental Chromium*, NSLS-II X-ray Photon Correlation Spectroscopy Workshop, Jan 2008.