A New Prototype 10 μ by 340 μ Pixel Cell in a 0.13 μ CMOS Process for Future HEP Applications

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Fermilab Areas of Pixel Interest

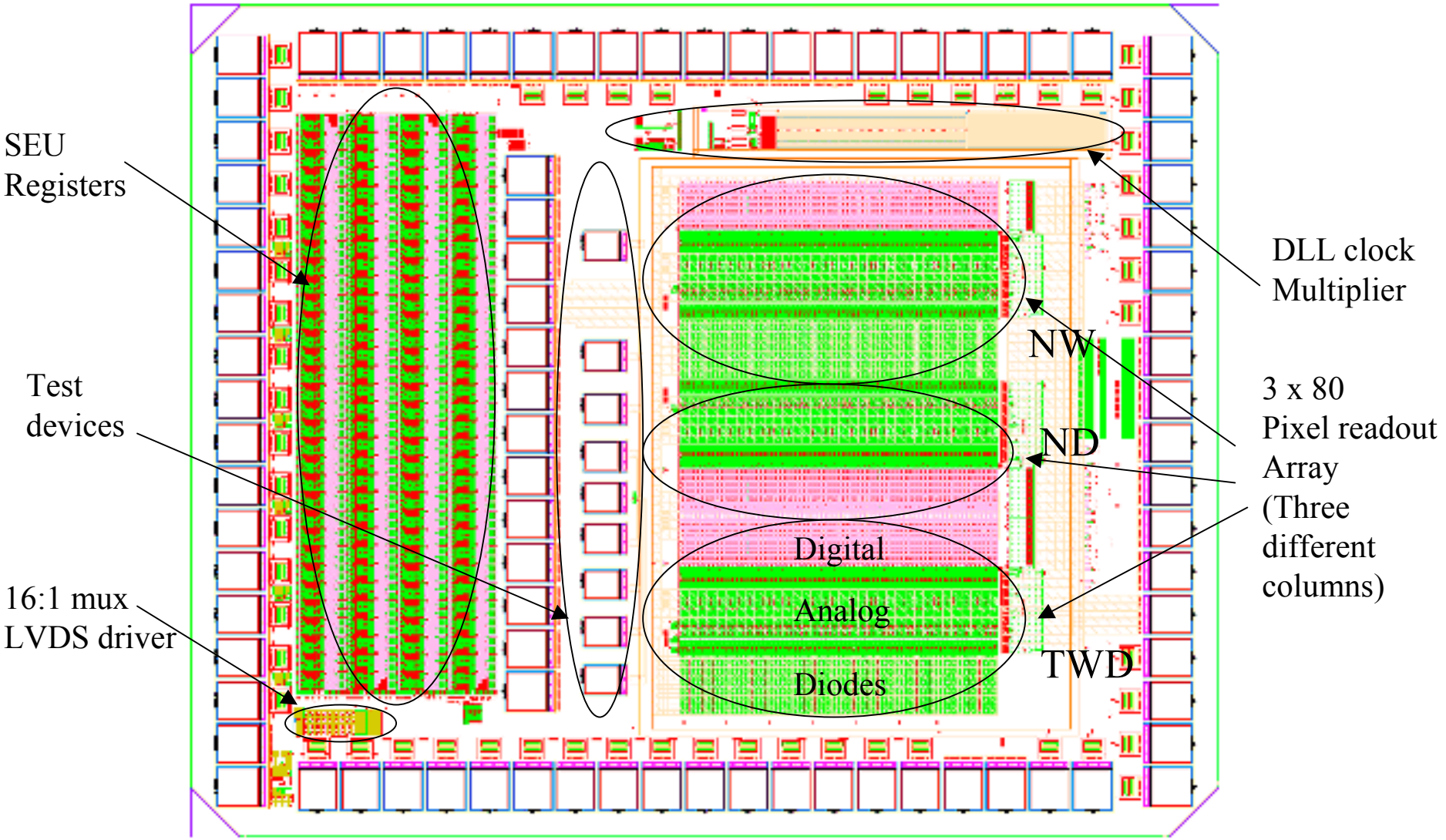
- Readout devices for amorphous silicon pixel detectors at the University of Michigan.
  - Column parallel amplifier arrays
- Pixel readout chip (FPIX) for BTEV experiment.
  - 22 column x 128 row hybrid technology
- New R&D effort to study future pixelated devices for HEP
  - Test chip in IBM 0.13µ CMOS process

0.13 μ IBM Test chip

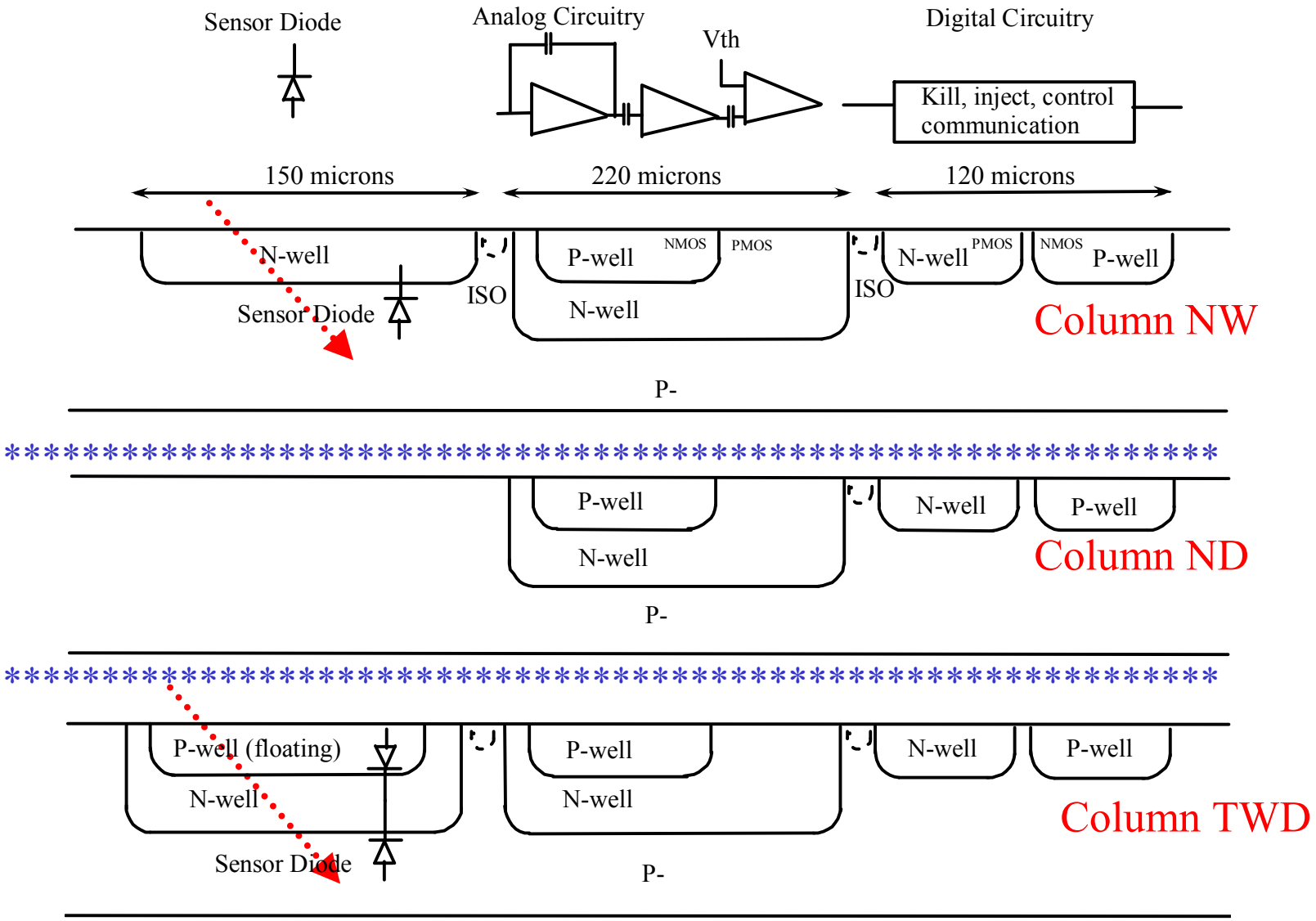
Purpose of the test chip is to explore a 0.13 μ process for possible future HEP designs.

- DLL Clock Multiplier
- Registers for SEU evaluation
- Test Devices
- LVDS drivers
- 80 row x 3 column pixel readout array – each column is different
  - Intended to study fine pitch, higher functionality pixel cell in DSM and diode fabrication on high resistivity substrate
    - Ultra fine pitch readout circuit (10 μ x 340 μ) similar to FPIX
    - Ultra fine pitch diodes (10 μ x 150 μ) connected to readout circuits
  - Not intended for any particular experiment
  - This is a work in progress, only 2 chips tested so far, still many questions.
    - First chip had a short in output buffer that added nonlinear connection from Vdd to substrate. (Analog signals could not be brought out through buffer.)
    - Second chip had successful FIB repair to correct the problem.

0.13 µ Test Chip Layout



Column Pixel Cells



Pixel Cell Operating Conditions

Parameter	Value
VDDA	1.5 V
VDDD	1.5 V
IDDA	12 mA
IDDD	1 mA

Bias	Simulated	Measured
VBP2	1.066 V	1.04 V
VBN2	0.297	0.28
VBN1	0.374	0.364
VBBND	0.318	0.300

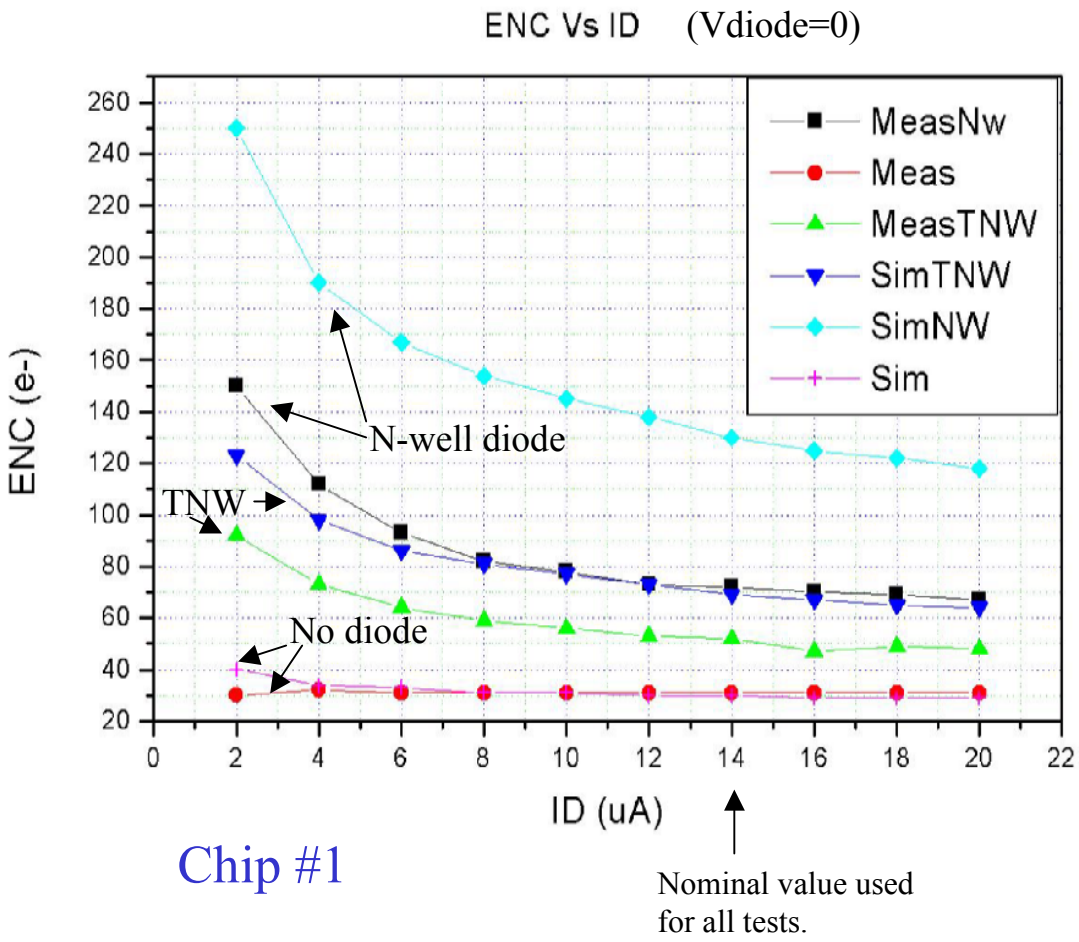
Power dissipation is around 80 uw/pixel cell.

The good correlation between simulated and measured bias voltages suggests that the models used for the pixel cells are good. (Also good noise correlation.)

Look at ENC and threshold characteristics for different columns.

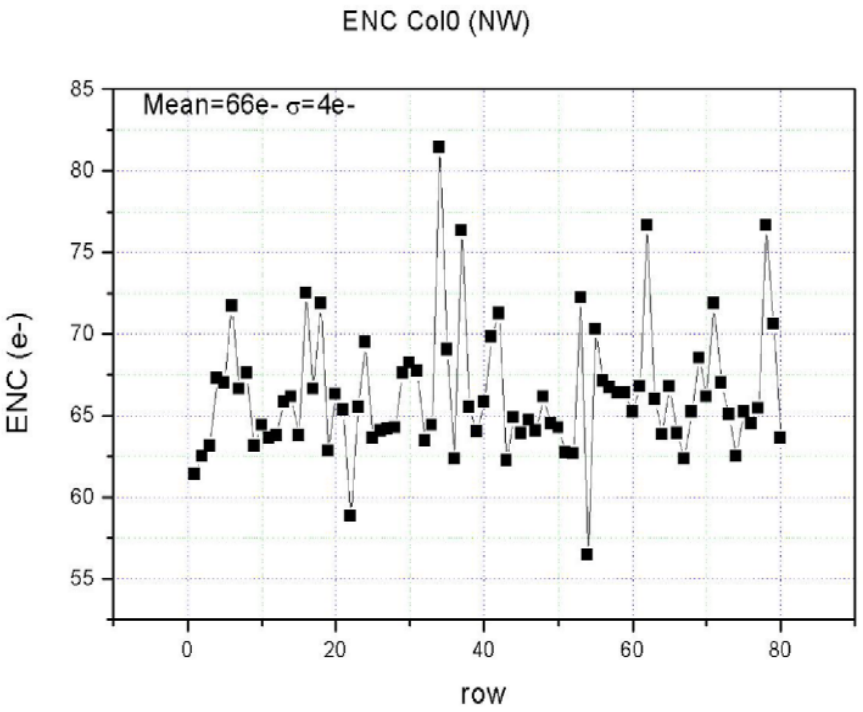
Diode Models and ENC vs Pixel Cell Input Transistor Current

- *Look at diode models*
- Simulation and measurements w/o input diode give similar results.
- Difference for NW and TNW.
- Injection test capacitor value appears close to calculated value.
- ENC is higher with diodes and decreases with increasing Id due to higher gm.



Chip #1

Pixel Cell ENC

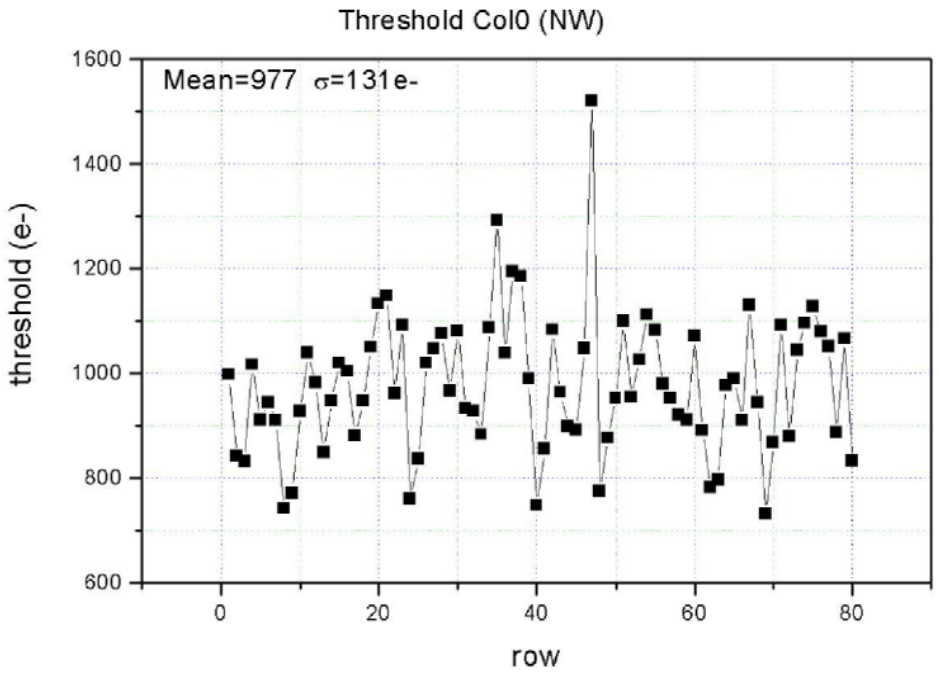


ENC for 80 cells with NW diodes on input.
Chip #1: Vdiode = 0V, Ibias = 14 ua

Input	Mean
N-well diode	66 e-
No diode	33 e-
Triple N-well diode	50 e-

Diode capacitances estimated from simulations to be 0.6 to 1.0 pF

Pixel Cell Threshold Voltage Dispersion

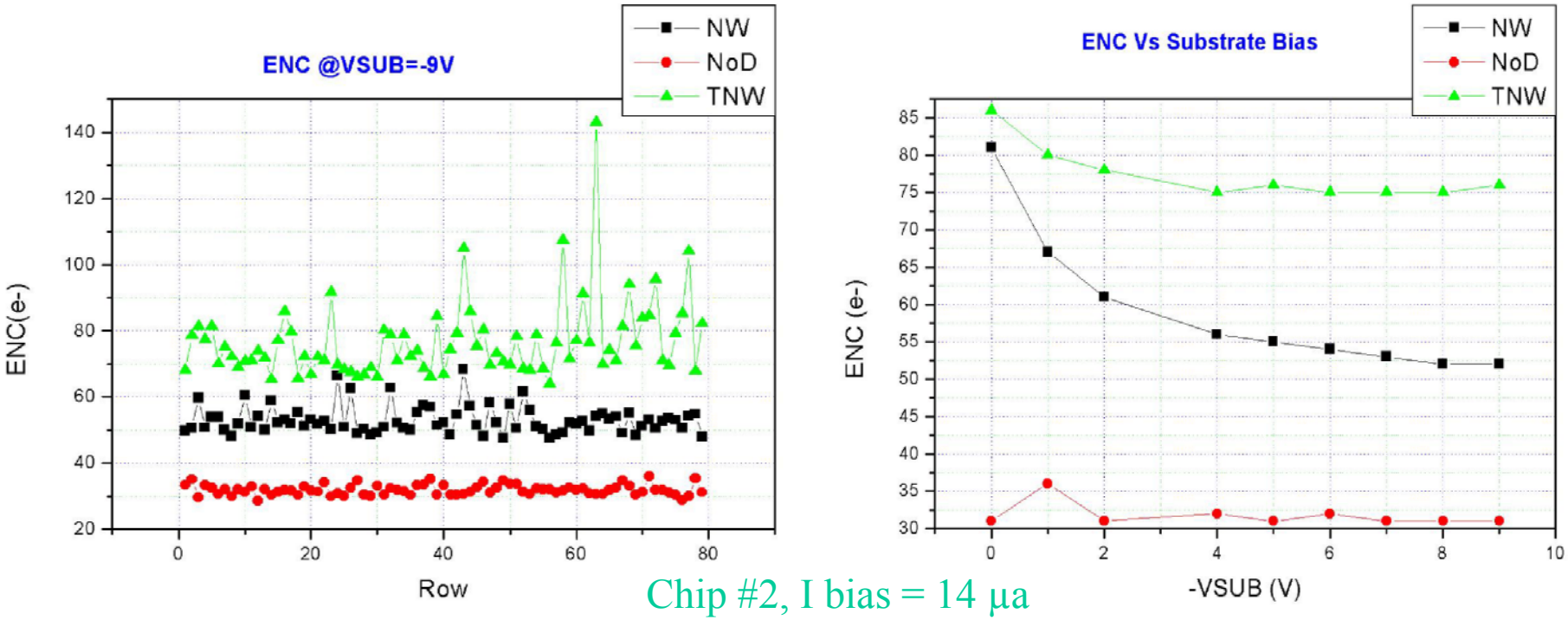


Input	Mean	Sigma
N-well diode	977 e-	131 e-
No diode	1160 e-	170 e-
Triple N-well diode	718 e-	94 e-

Threshold dispersion for 80 cells with NW diodes
Chip #1: Vdiode = 0V, Ibias = 14 ua

No adjustments made to correct for gain changes due to different input conditions.

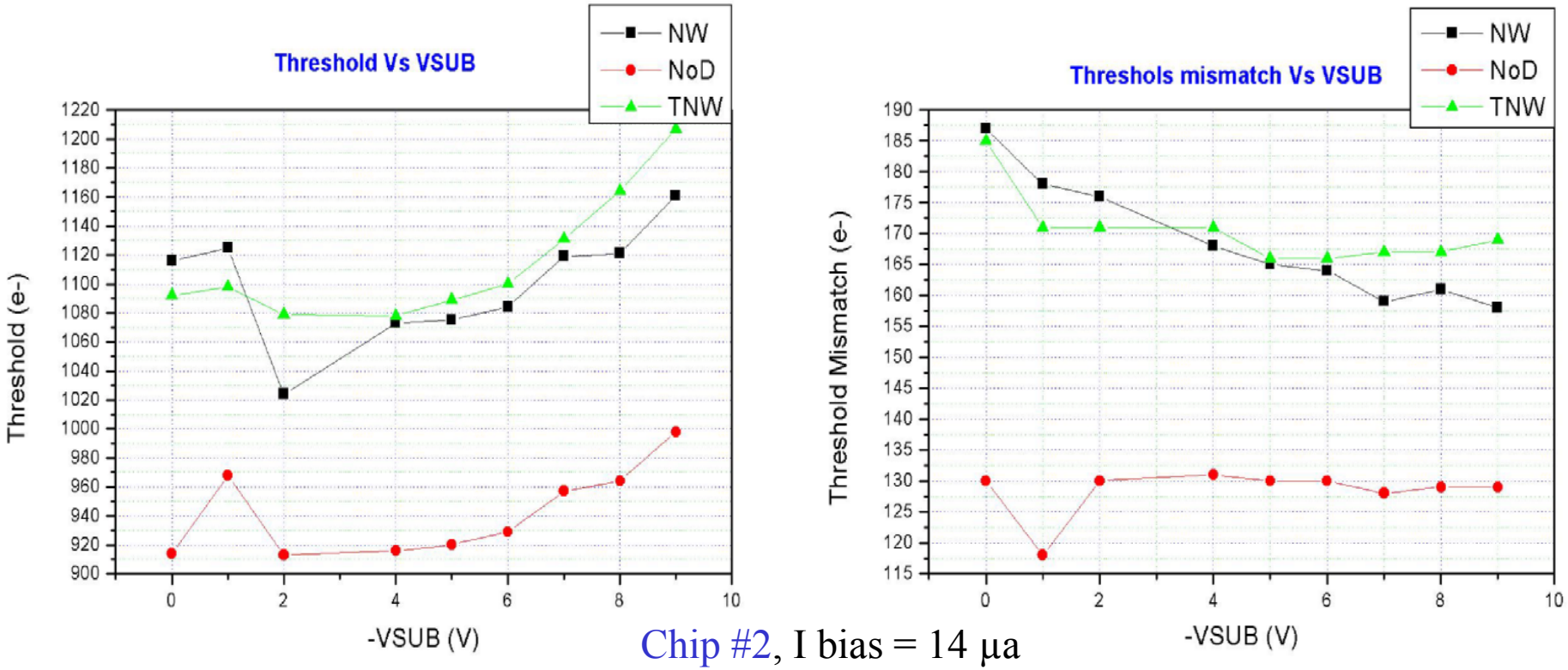
Pixel Cell ENC as a Function of Substrate Bias (Bias on Sensing Diode)



Chip #2, I bias = 14 μa

The mean ENC is found to decrease as the bias is increased. This believed to be due to the decreasing value of the diode capacitance.

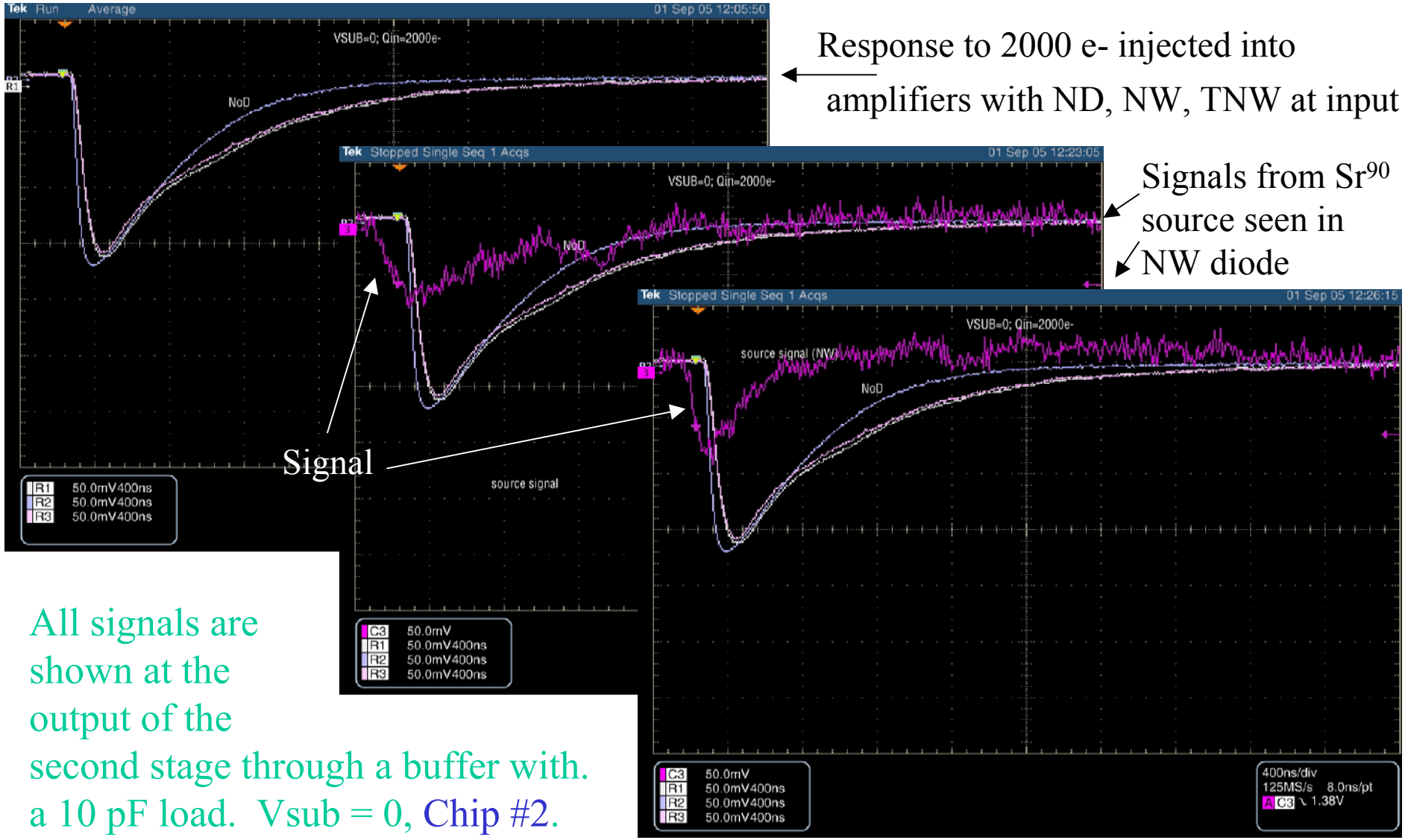
Pixel Cell Threshold Voltage vs. Substrate Voltage



Chip #2, I bias = 14 µa

Beginning at about -5 volts, the average threshold was found to increase for all 3 types of circuits. This is thought to be due to the kill and inject logic failing to pass all hits. Threshold mismatch for diode circuits is found to get smaller with increasing Vsub due to increase in gain as diode capacitance gets smaller.

Sr^{90} Source Test on N-well Diodes



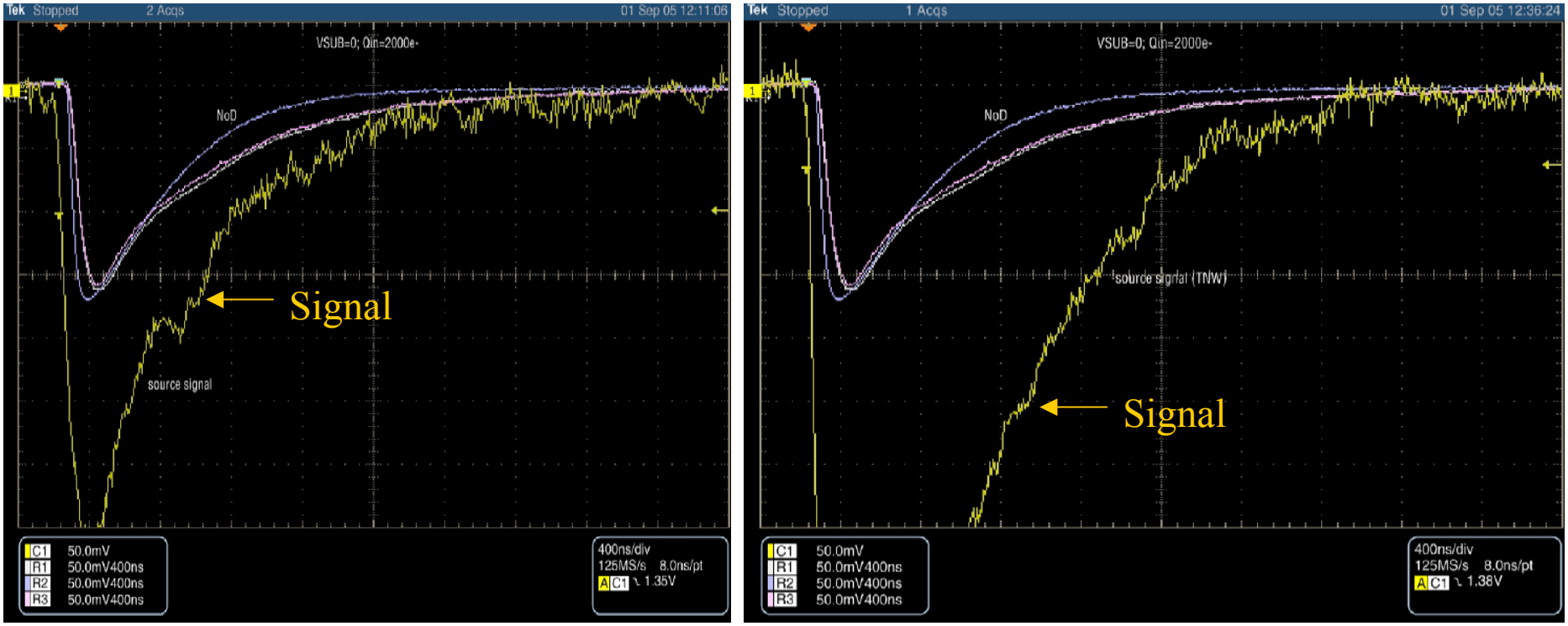
Response to 2000 e- injected into amplifiers with ND, NW, TNW at input

Signals from Sr^{90} source seen in NW diode

Signal

All signals are shown at the output of the second stage through a buffer with. a 10 pF load. Vsub = 0, Chip #2.

Sr^{90} Source Test on Triple N-well Diodes

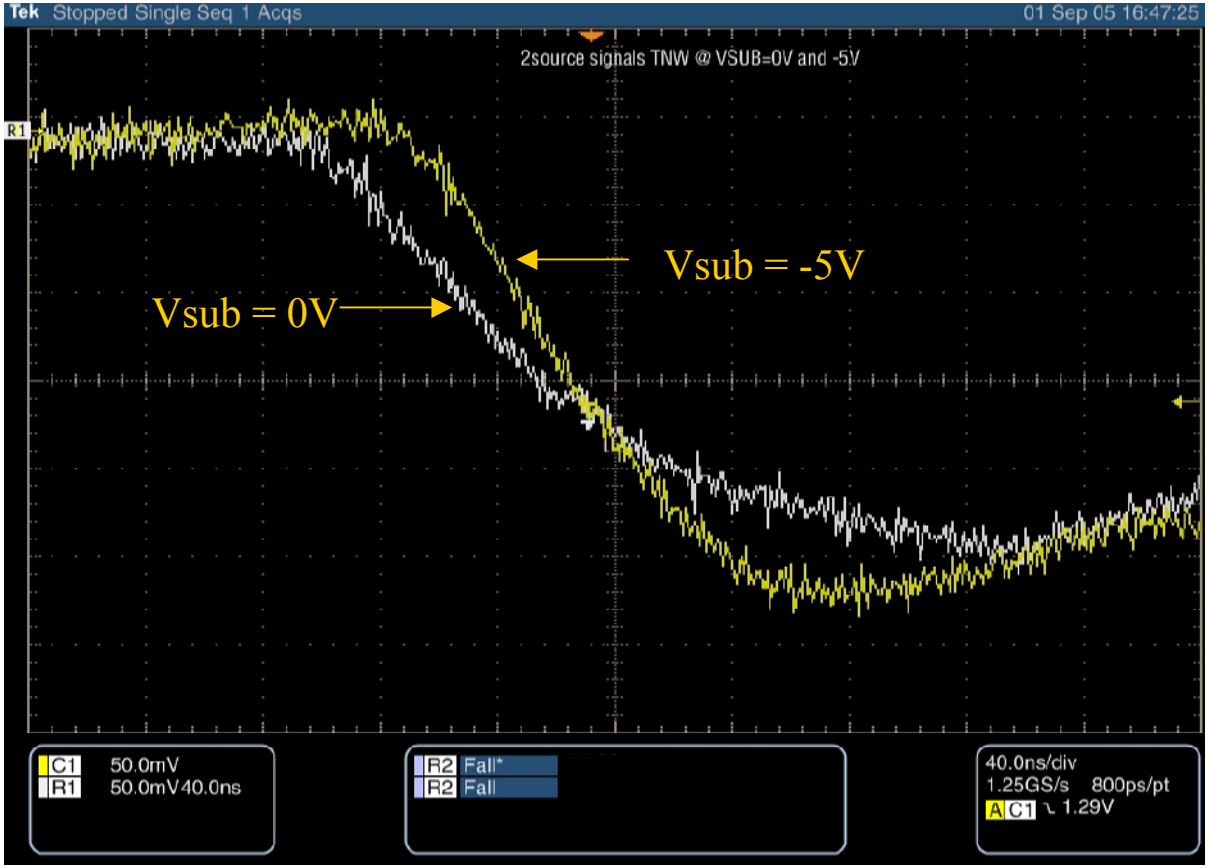


Chip #2, Vsub = 0V

Previous 2000 e- injection signals are superimposed for reference. The signals from the Triple N-well diodes are generally larger than those from the N-well diodes.

Sr^{90} Source Signals vs Substrate Voltage with Triple N-well Diode

Two signals are shown at different substrate voltges. We need to study the dependence of charge collection on substrate bias.



Chip#2

Hit Rate from Sr^{90} Source with and without Bias on Diode

Vbias = 0V

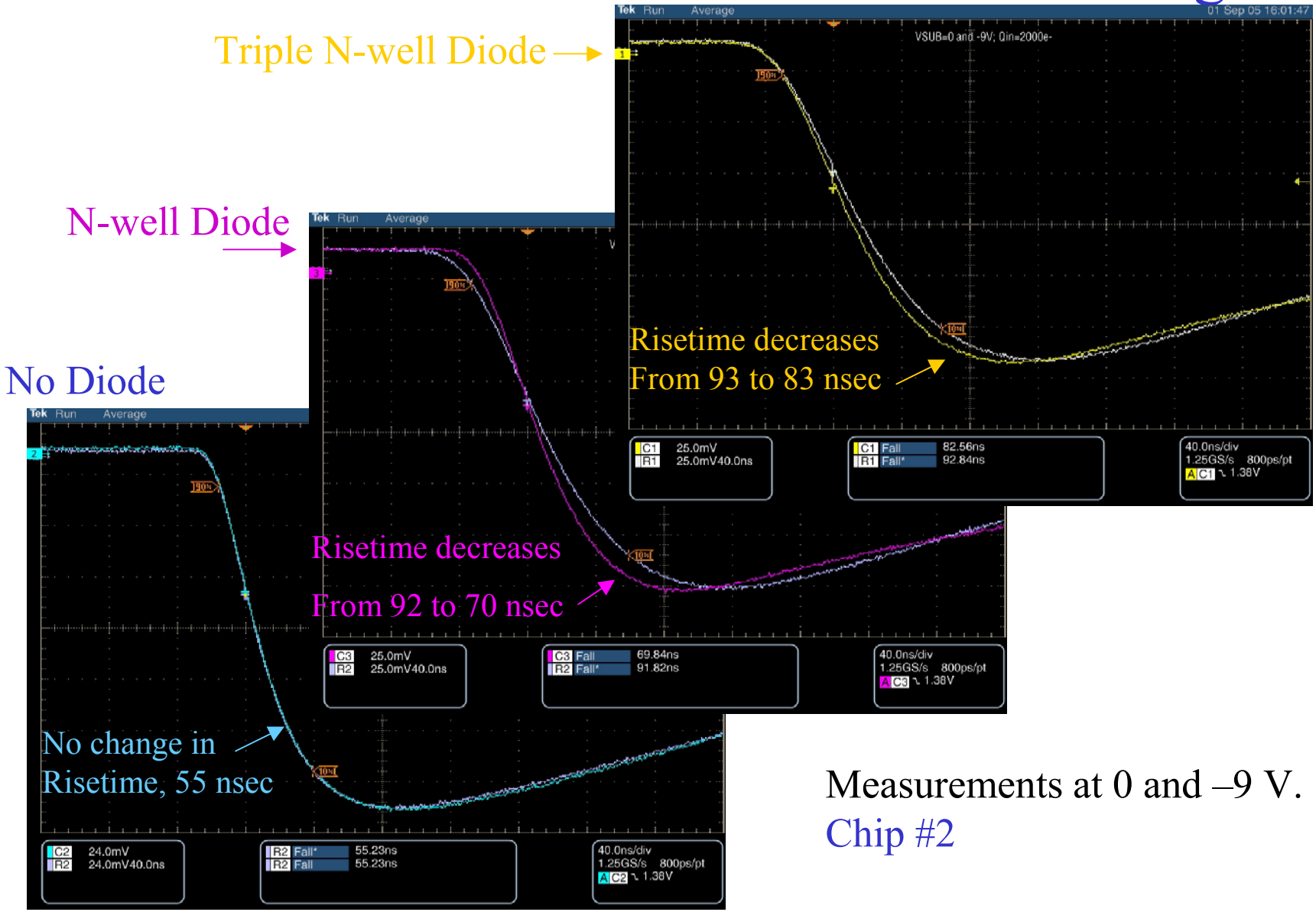
Circuit	Source	Hits
80 NW	On	54
80 TNW	On	350
80 NW +80 TNW	Off	0

Vbias = -5 V

Circuit	Source	Hits
80 NW	On	85
80 TNW	On	492
80 NW +80 TNW	Off	0

Tables show the number of hits recorded in 5 minutes of running with a Sr^{90} source for 2 different bias voltages. Observation on a scope showed that there were no double hits recorded. Threshold was set at 1000 e-.

Risetime with Test Pulse vs Substrate Voltage

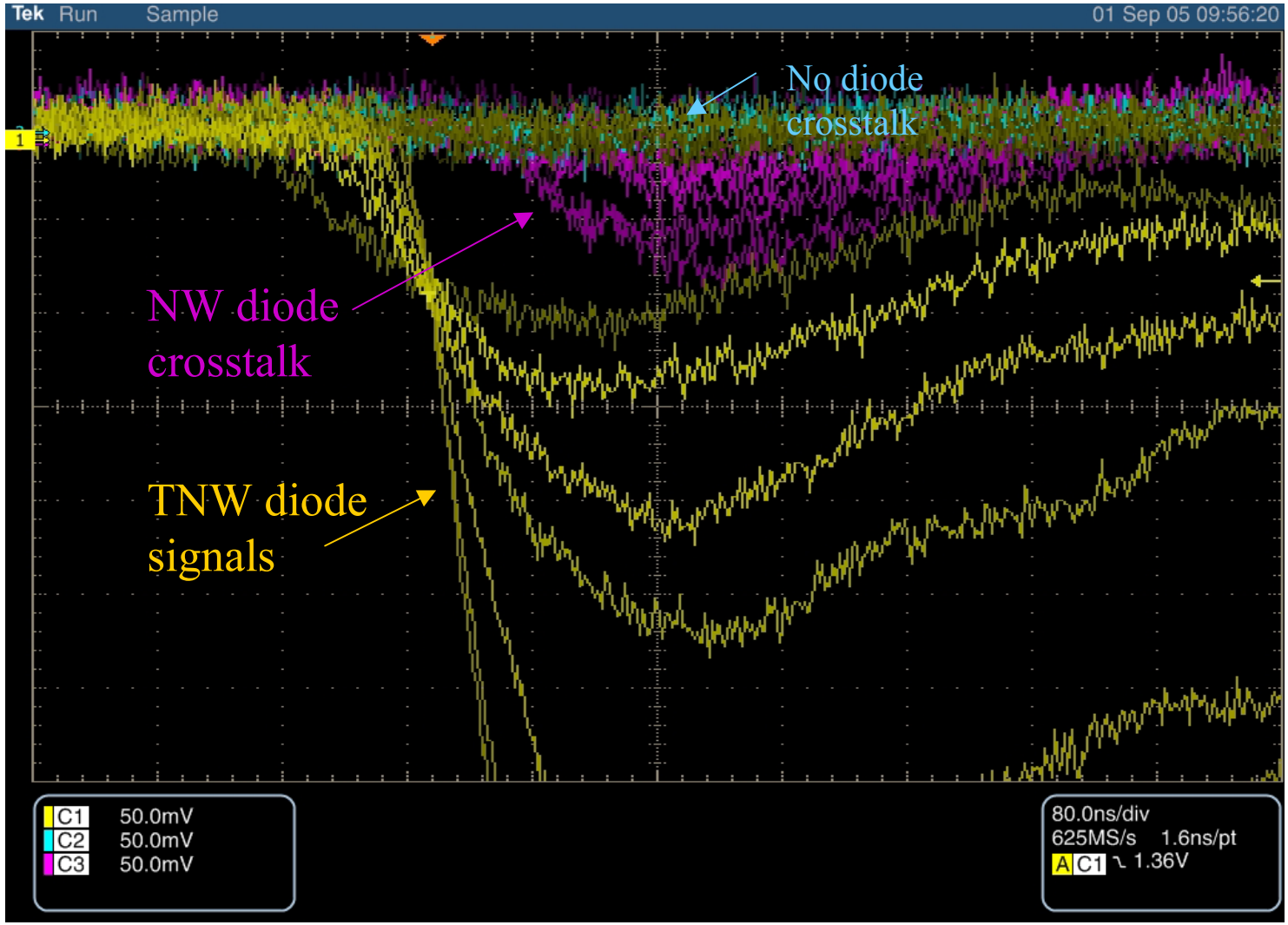


Sr^{90} Source Test with TNW Signals Showing Crosstalk to NW and ND

Blue=ND
Violet=NW
Yellow= TNW

The crosstalk is thought to be due to a combination of factors such as charge injection capacitors, common bias etc.

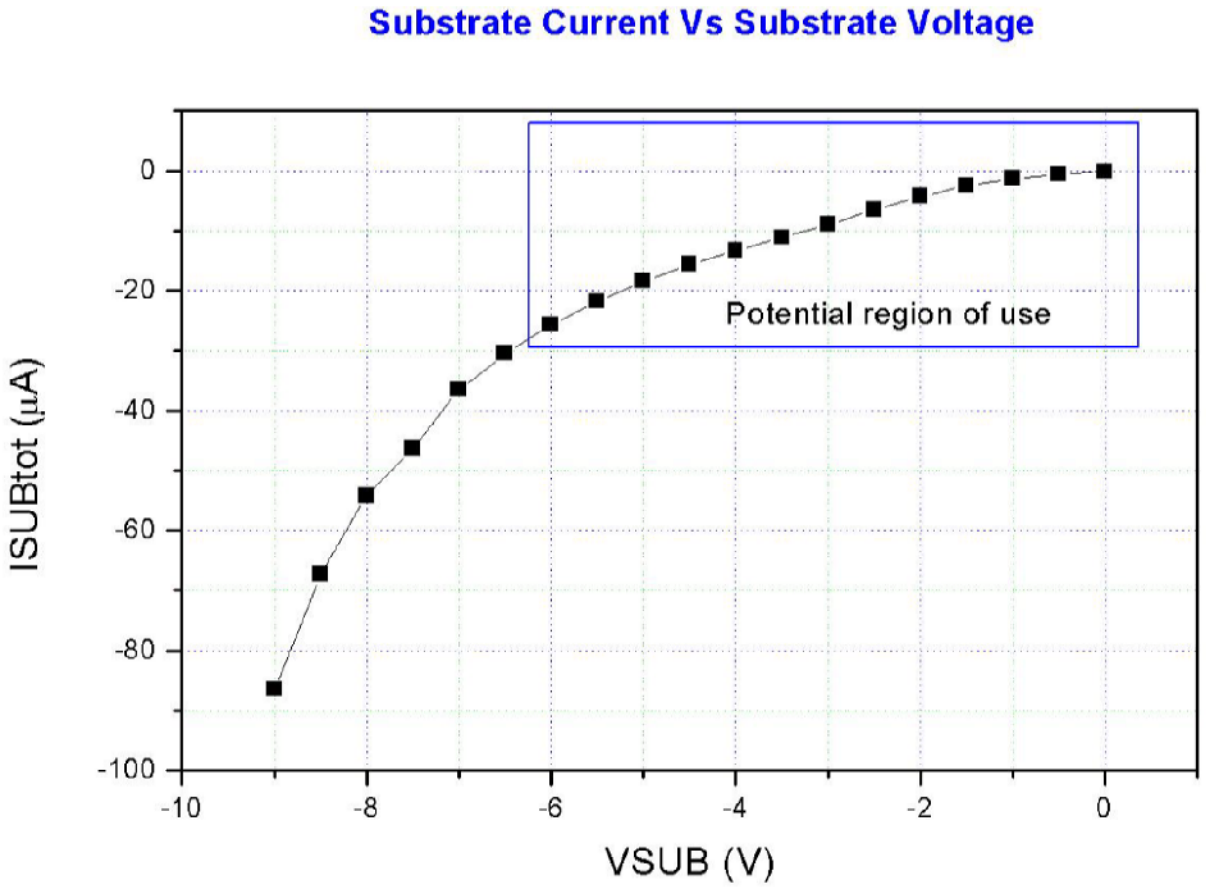
Chip #2



Substrate Current as a Function of Reverse Bias

Substrate current for 160 diodes and 240 pixel cells.

Operating the diodes at a small reverse bias appears possible.



Conclusion

- Very promising results obtained from test chip.
- Properties of deep submicron processes should be studied carefully for new HEP applications.
- The IBM 0.13 micron triple well process offers some interesting features and possibilities.
- Highly functional circuits can be laid out on a very fine pitch in a 0.13 micron process.
- Diodes built on a high resistivity substrate, such as in the IBM RF process, may offer interesting possibilities.
- More studies of charge collection properties of diodes in the 0.13 micron process need to done.