Radiation Test Results of Pixel Circuits Built in Two Different 0.25 μ Processes

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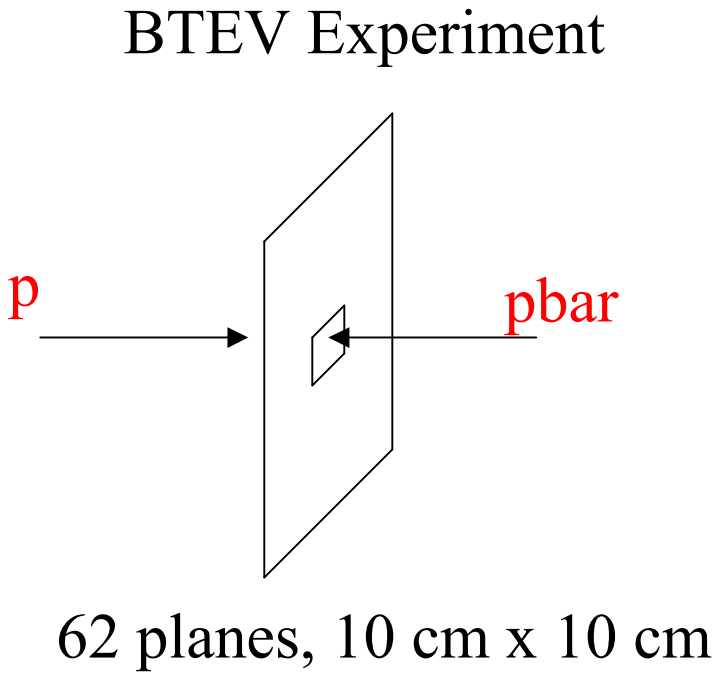
Introduction

- Tests done on pixel circuits for BTEV
- Electronics 6 mm from beam
- Expect 3 Mrads/yr
- Designs in 0.25 μ
- Compatible with TSMC and CERN selected foundry

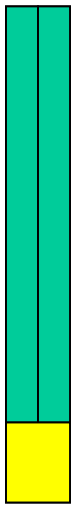


Tests

- Tested two different pixel chips from two different foundries:
  (Process “A”-TSMC, Process “B”-CERN)
- Also tested two different chips with transistors
- ^{60}Co at 325 to 500 krads(SiO_2)/hr
- 200 MeV protons at 2.3×10^{13} p/cm^2/hr
- Looked for changes in noise, threshold, and other characteristics.
- SEU tests to follow

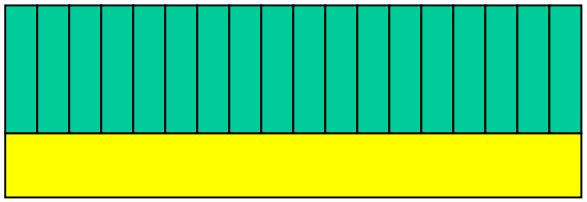
Chips Tested

- TSMC process

(1)  2 columns x 160 rows pixel array – preFPIX2T

(2) Early test chip with transistors and front ends

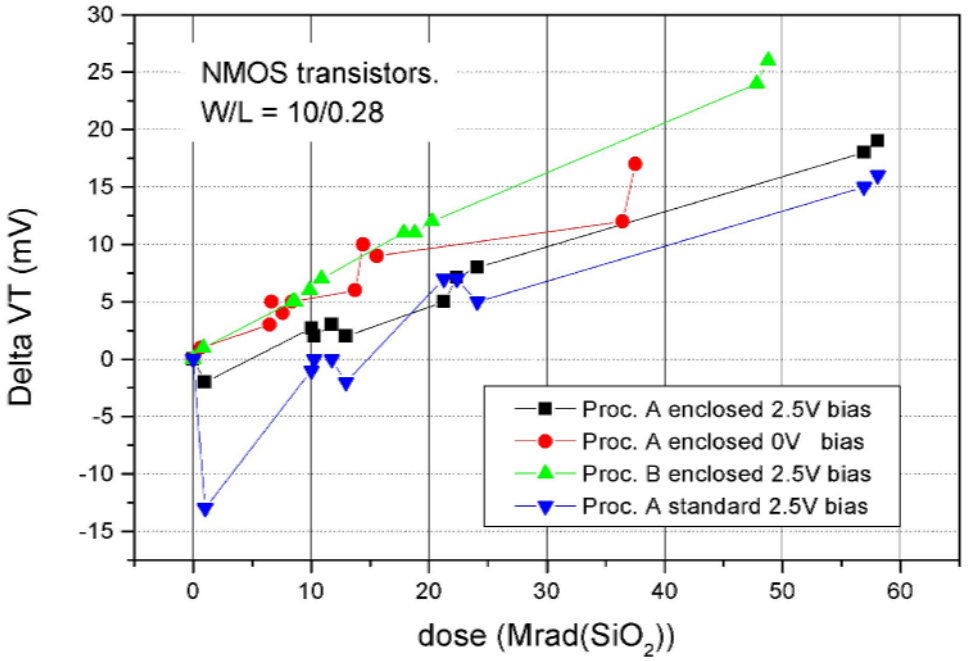
- CERN process

(3) 

18 columns x 32 rows pixel array – preFPIX2I

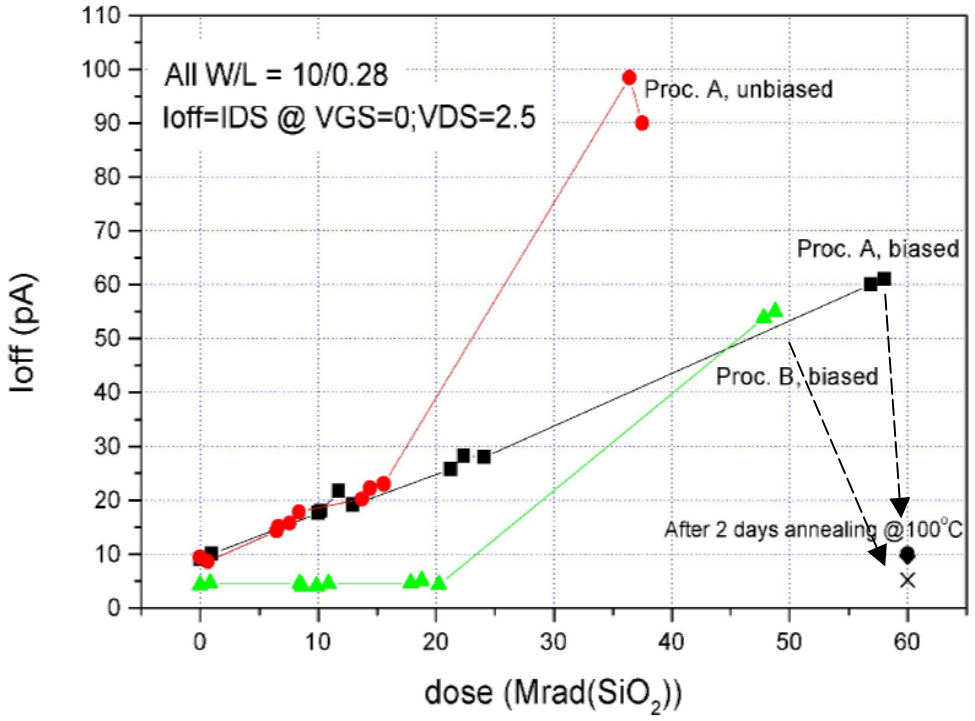
(4) Test transistor chip from CERN

Total Dose Effects on Standard and Enclosed Transistors



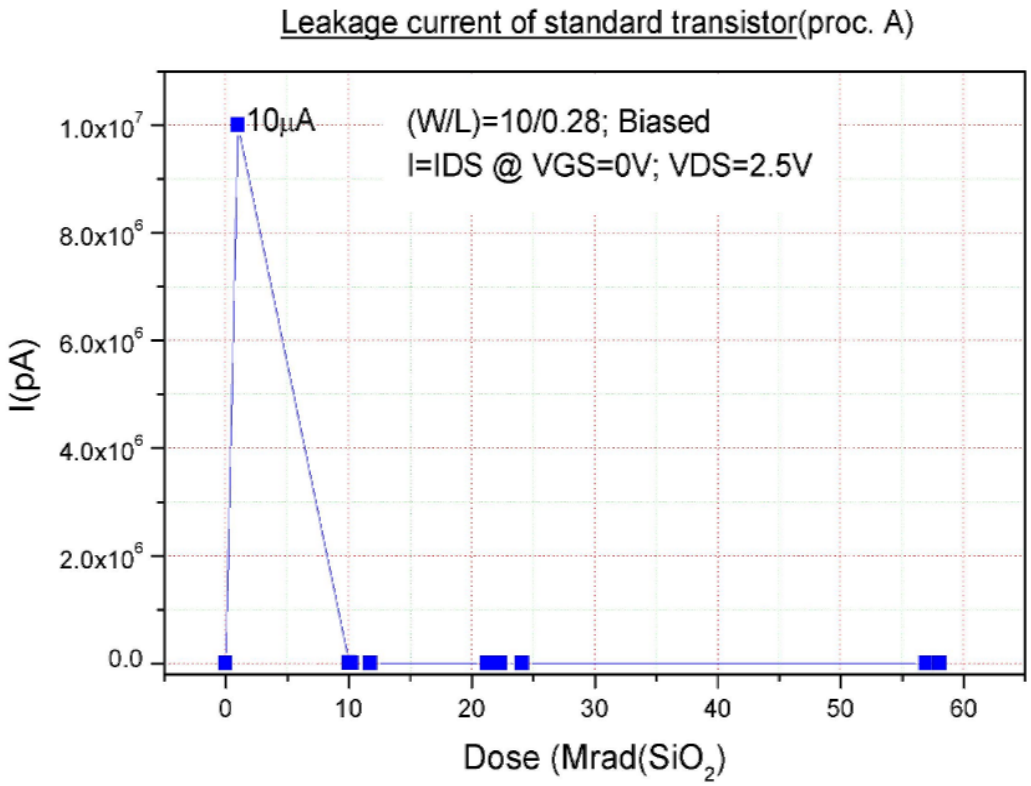
- ^{60}Co radiation
- Process A, 325 and 500 krad/hr
- Process B, 420 krad/hr
- Dosimetry accurate to 20%
- Biased and unbiased transistors
- Source removed during measurements
- Annealing has little effect on Vt shift.

Leakage Current Versus Dose for Enclosed NMOS Transistors



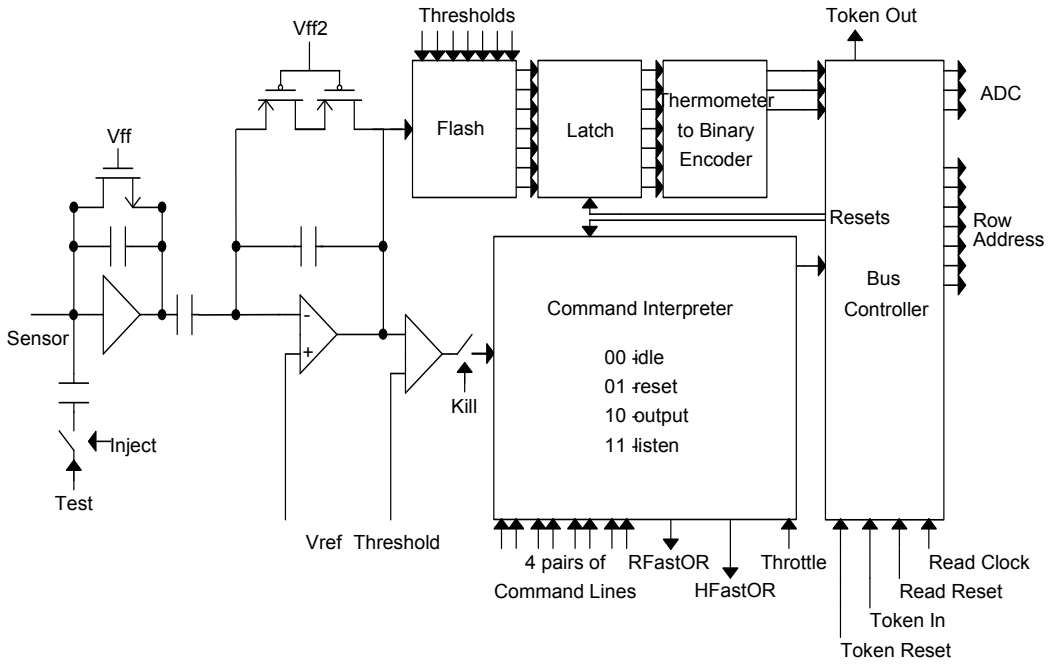
- Enclosed NMOS transistors used to reduce radiation induced leakage currents.
- Enclosed NMOS devices show little increase in leakage and return to initial values after annealing.

Leakage Current Versus Dose for Standard NMOS Transistors



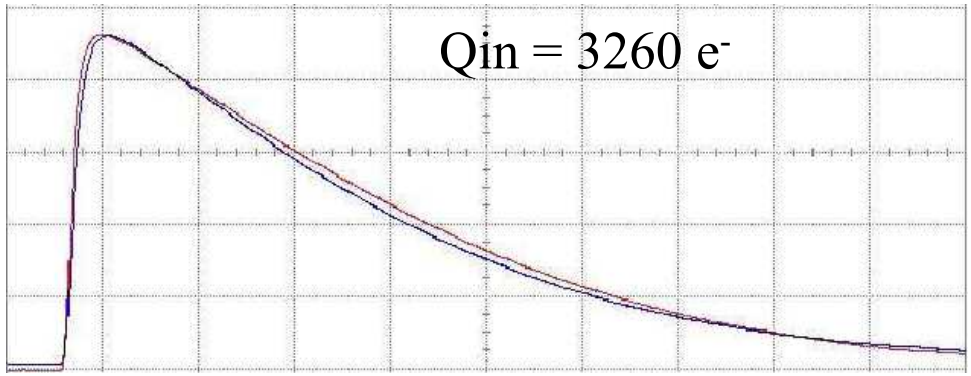
- Standard geometry NMOS transistors in both process A and B show a rapid large increase in leakage current and then a subsequent drop in leakage current over time
- After annealing, transistors from both processes return to pre-radiation levels.

Basic Pixel Cell Used on Chips Fabricated in Processes A and B



- Two stage analog front-end
- 3 bit FADC with all unique threshold settings
- Command control logic
- Kill and inject logic
- Large leakage current compensation (not shown)
- 550 transistors/cell

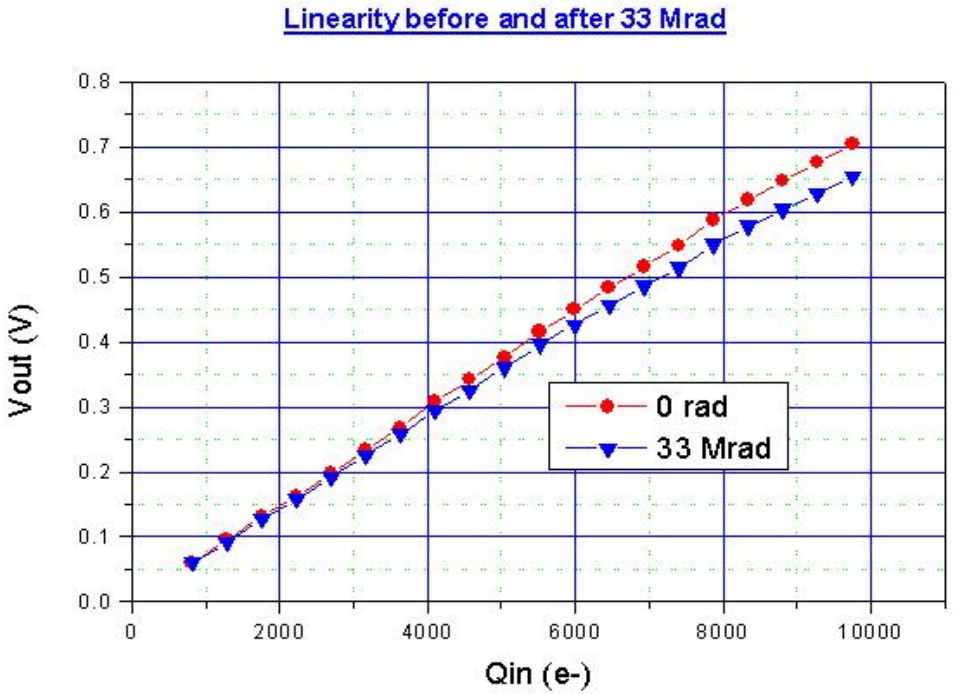
Radiation tests on preFPIX2T Chips (Process A)



Buffered output of second stage before and after 33 Mrads. Exact same bias settings used for both measurements. Observed 3 mv offset change, 5% change in rise and fall times.

- 2 x 160 cell array
- End of column logic is off chip.
- 33 Mrads (SiO_2) ^{60}Co
- 285 krads/hr
- Circuits biased during radiation
- Fully functional after 33 Mrads
- 10% decrease in power
- No change in shift register speed

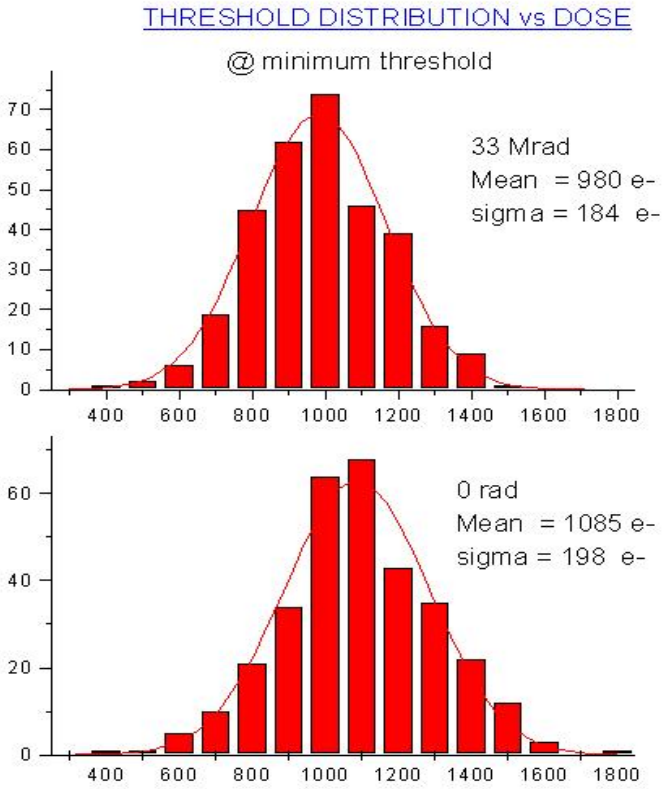
PreFPIX2T Small Signal Radiation Tests



Measurements after buffer at output of 2nd stage

- 33 Mrads (SiO_2) ^{60}Co
- Maximum of 7% degradation in gain
- Gain degradation believed to be primarily due to changes in the buffer (open loop common source stage).

PreFPIX2T Threshold and Noise Radiation Tests

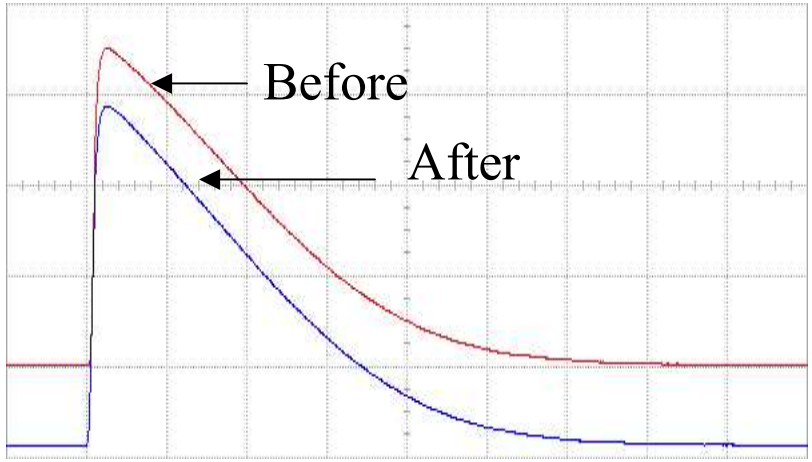


- 33 Mrads (SiO_2)
- Analysis performed on 320 cells
- Threshold: mean threshold voltage decreased by 205 e^-
- Threshold: sigma decreased from 198 to 184 e^-
- Noise: ENC increased from 67 to 70 e^- after 33 Mrads

Radiation Tests on preFPIX2I (Process B)

- 18 by 32 pixel array
- Includes complete end of column logic
- 500,000 transistors per chip
- Four chips on four different boards tested, all under bias
- 200 Mev protons
- 4.4 x10^{14} p/cm^2 (26 Mrads) @ 2.3 x 10^{13} p/cm^2/hr
- All measurements made after storage for about 4 weeks at room temperature
- Tests done to study total dose tolerance and gate damage by protons.
- After irradiation, all boards behave similarly with only minimal changes after irradiation. No change in digital performance.
- From the bias current mirror measurements, the NMOS and PMOS thresholds shifted by –6 and –105 mV respectively (similar results obtained for 8 NMOS and PMOS devices).

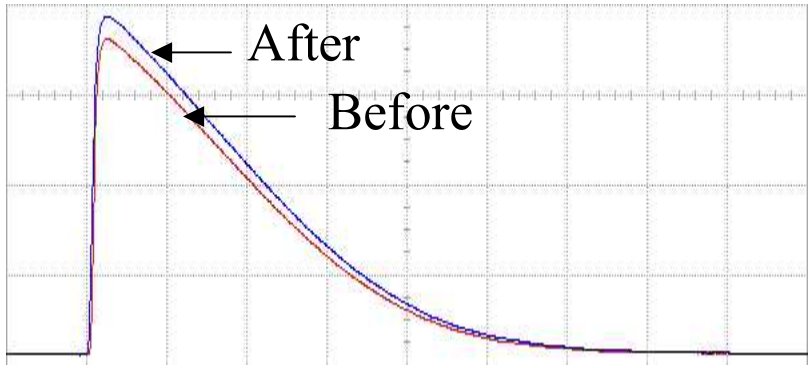
Radiation Tests on preFPIX2I (Process B)



Output of 2nd stage (after buffer) before and after irradiation for input charge of 10 ke-.

- 100 mV shift in 2nd stage
- Shift believed due to shift in PMOS threshold (which increases resistance in the feedback PMOS) and increase in parasitic diode junction leakage
- N-well of 2 PMOS feedback transistors in 2nd stage forms back biased diode with p-substrate. Leakage of the diode through the high resistance PMOS contributes to signal offset voltage

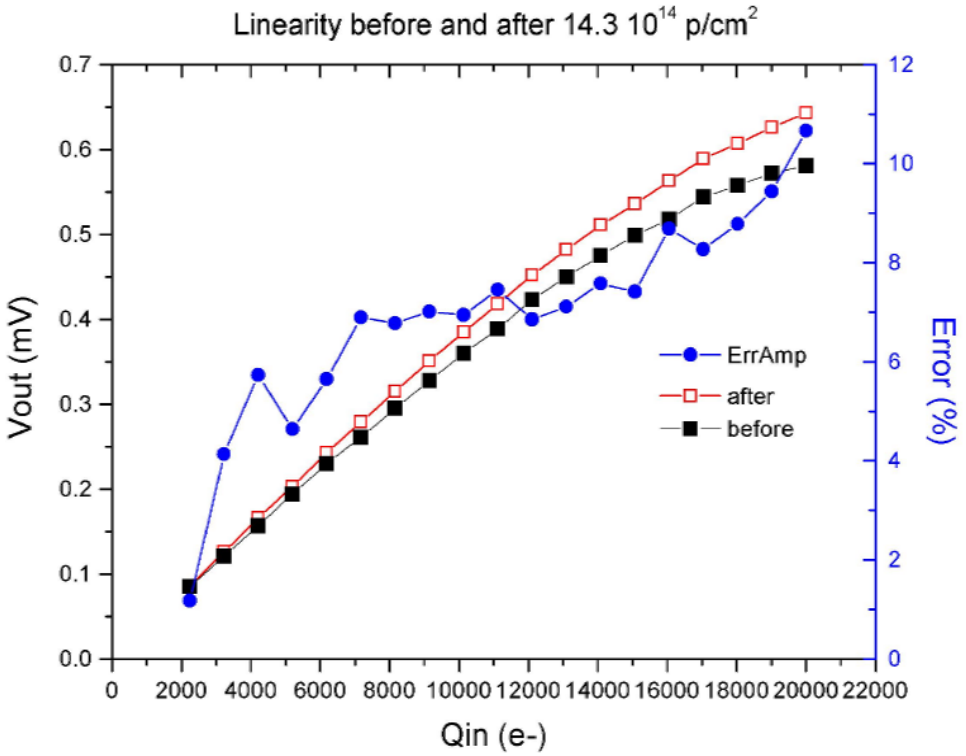
Radiation Tests on preFPIX2I (Process B)



Output of 2nd stage before and after irradiation, with the after signal shifted (on the scope) to correct for 100 mV offset. The same shift can be made by changing Vfb2 which is programmable.

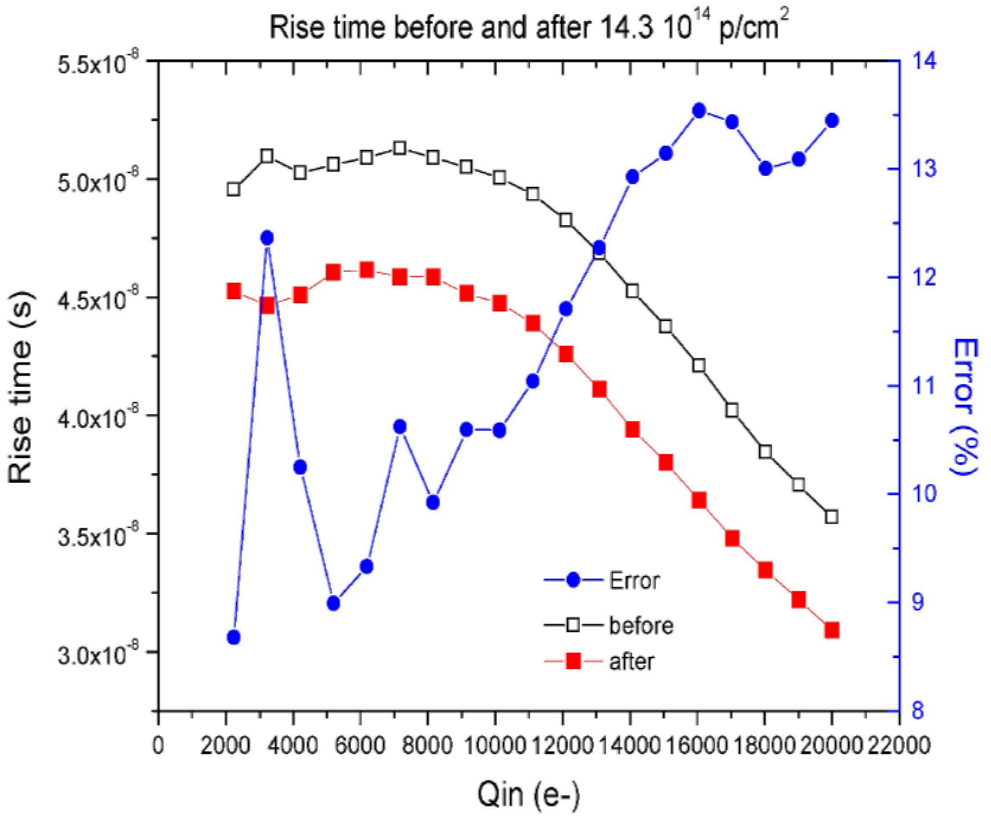
- DC level shift with radiation means that programmable threshold voltage should be changed by 100 mV. Once threshold is shifted by 100 mV (about 2000e^-), chip behavior is similar to pre-irradiation conditions.
- In practice, the shift would occur over a very long period of time.

Linearity Tests on preFPIX2I (Process B)



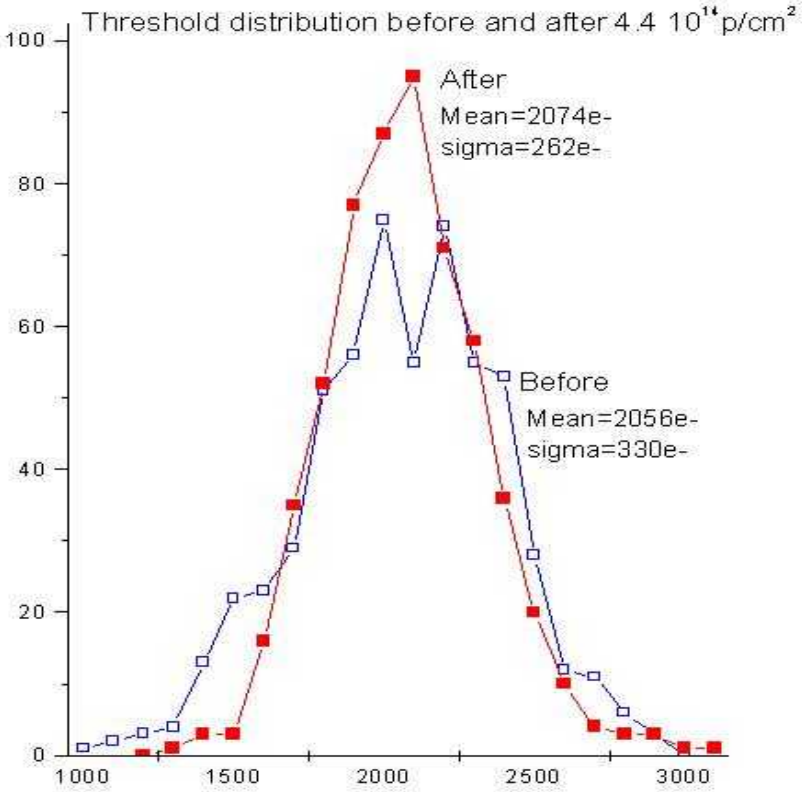
- There is a small increase in gain (5-10%) after irradiation.
- Gain is due to increase in resistance of PMOS feedback transistor in the second stage

Rise time Tests on preFPIX2I (Process B)



- Rise-time of the output decreases about 10% with radiation.
- Fall time is determined by gm and Vt of NMOS transistor in the first stage. The fall-time remains practically unchanged indicating that the NMOS has suffered little or no degradation.

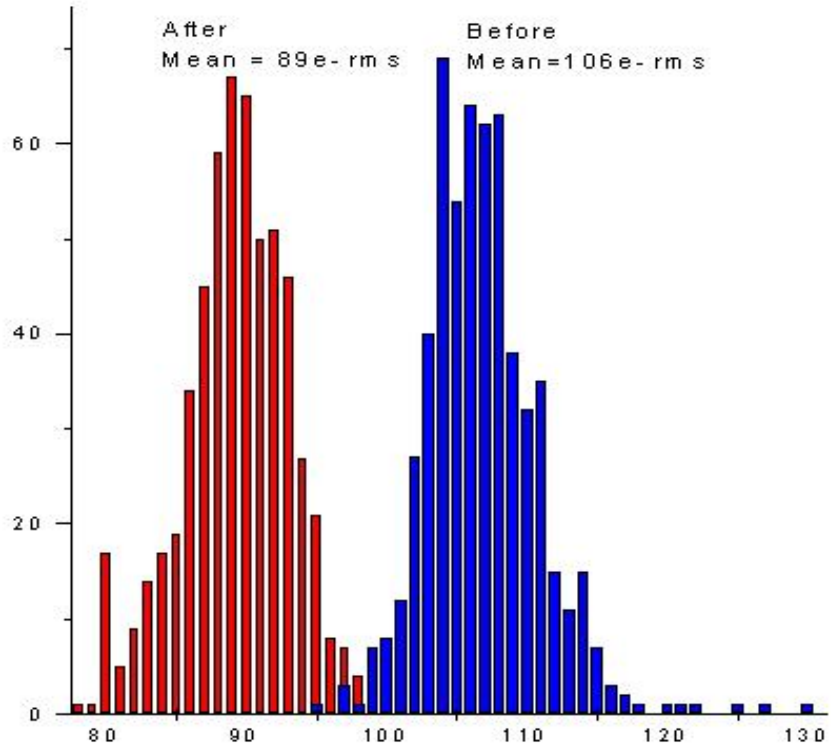
Threshold Distribution Tests on preFPIX2I (Process B)



Input Charge in electrons

- All four chips behave the same before and after irradiation.
- No significant change in threshold distribution. (After irradiation, the 100 mV offset was corrected with Vth setting. If offset is not corrected, the threshold shifts but spread and noise are practically unchanged.)

Noise Distribution Tests on preFPIX2I (Process B)



- There are no high noise channels after radiation in 2304 channels measured.
- Noise decreases with radiation possibly due to increase in the feedback resistance of second stage.

Conclusions

- Transistors from processes A and B have similar radiation characteristics.
- Pixel circuits in both processes A and B perform well in tests up to 30 Mrads.
- No noisy transistors were found after exposure to ^{60}Co and 200 MeV protons.
- No change in logic function observed in chips containing a total of over 2,000,000 transistors.
- Radiation studies must be done to uncover unusual design related phenomena.
- The 100 mV shift observed after proton irradiation can be easily accommodated in present design.
- Use of a common technology file to do designs for process A and process B is a viable option.