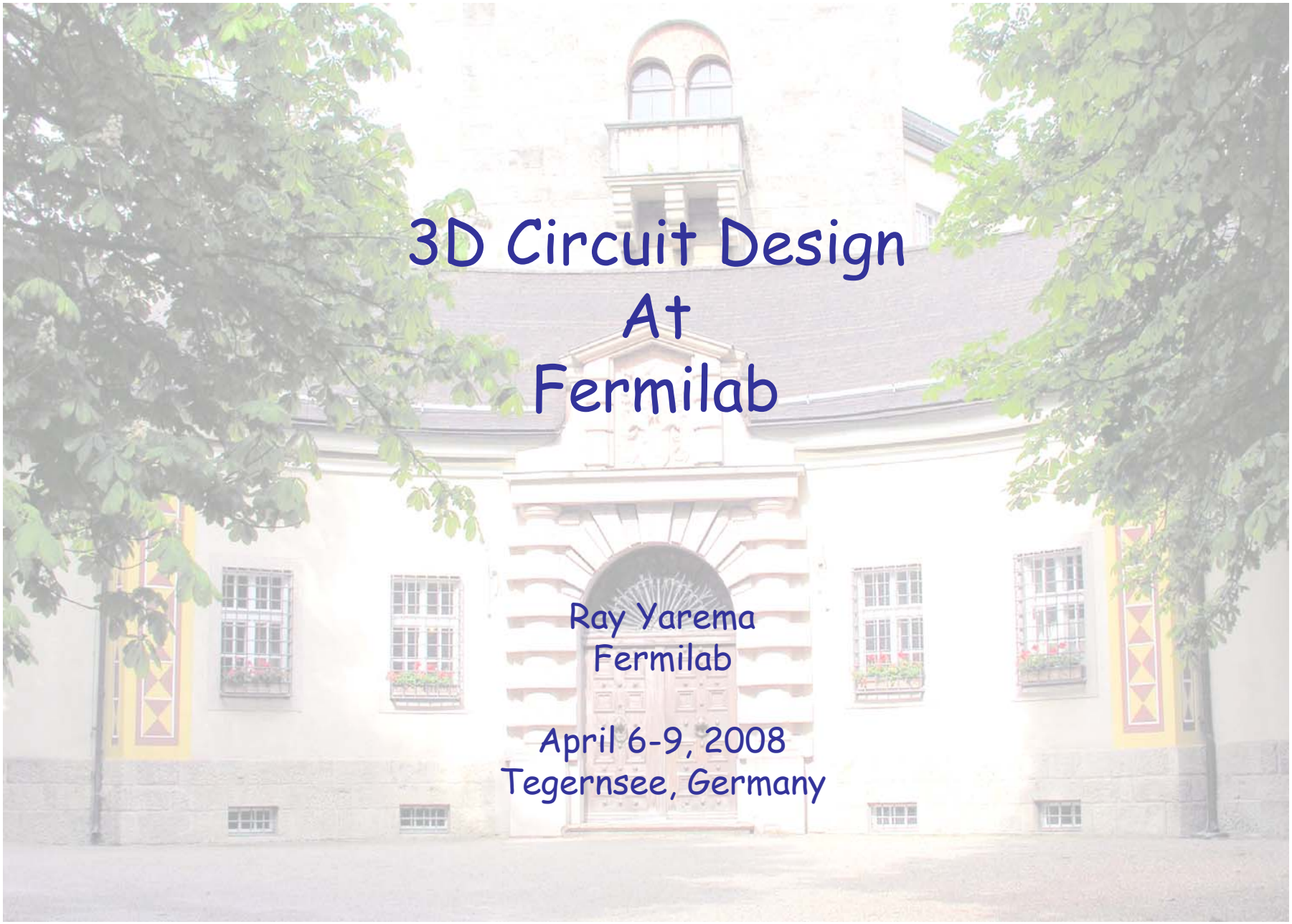


3D Circuit Design At Fermilab

Ray Yarema
Fermilab

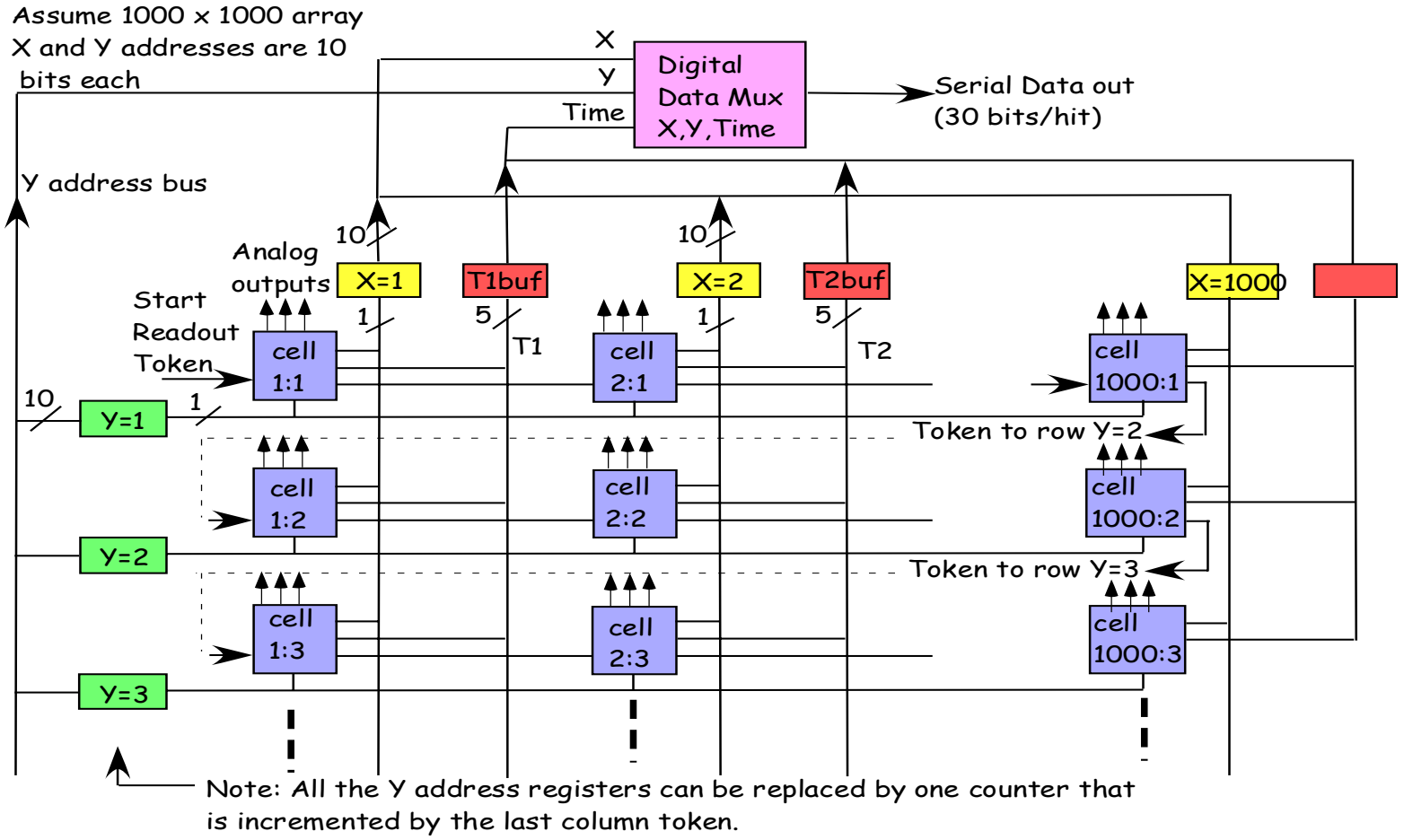
April 6-9, 2008
Tegernsee, Germany

Introduction

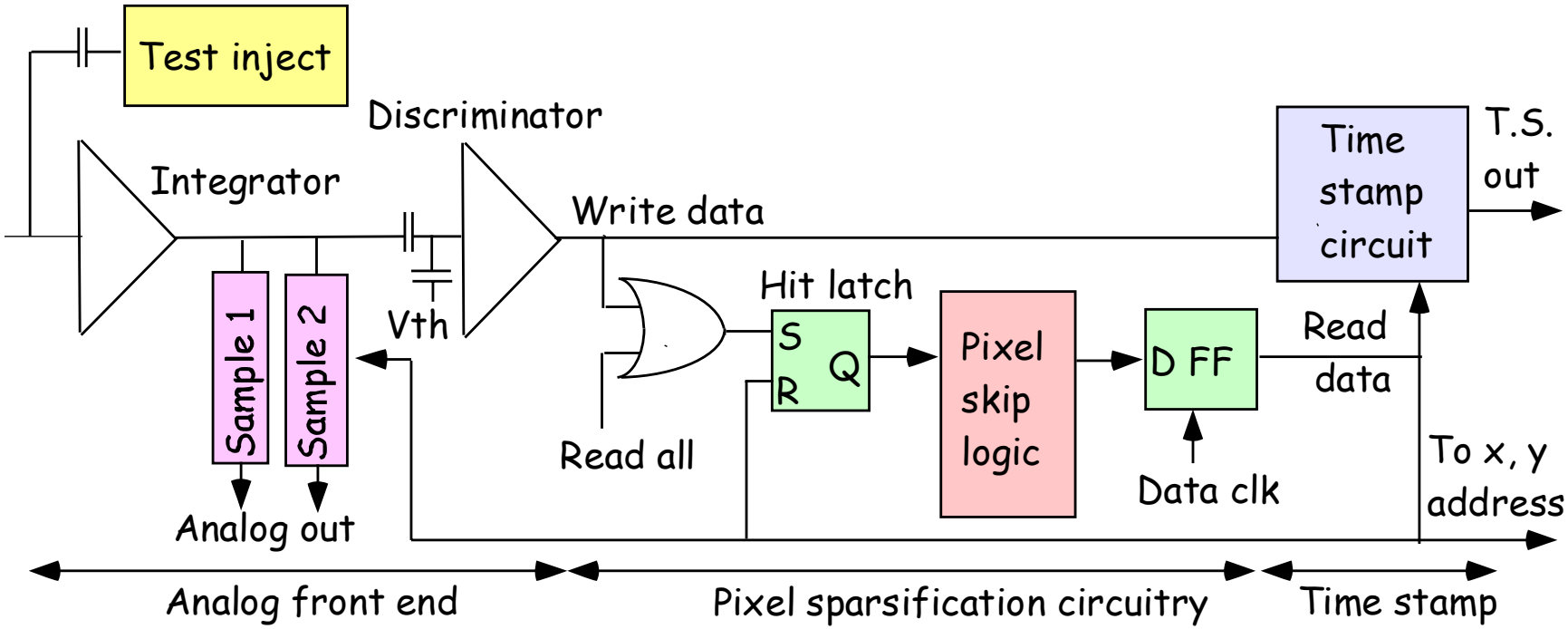
- Fermilab 3D work started in 2006 – first major talk at Ringberg, May 2006[1]
- Previous 3D work at Fermilab
  - MIT LL – 3D circuit design for ILC[2]
  - IZM – wafer thinning studies
  - RTI – chip bonding studies with CuSn pillars
  - OKI – SOI detector/readout design
- New activities in 2008 – (will focus more on industrial vendors)
  - OKI
    - SOI detector design
    - US-Japan program for Development of Advanced Pixel Sensors in SOI Technology
  - MIT LL – new 3D design with on board ADCs
  - Tezzaron – 3D circuit design
  - Ziptronix – low mass bonding
- This talk will focus on subjects in red

MIT LL 3D Chip (VIP) for ILC Vertex

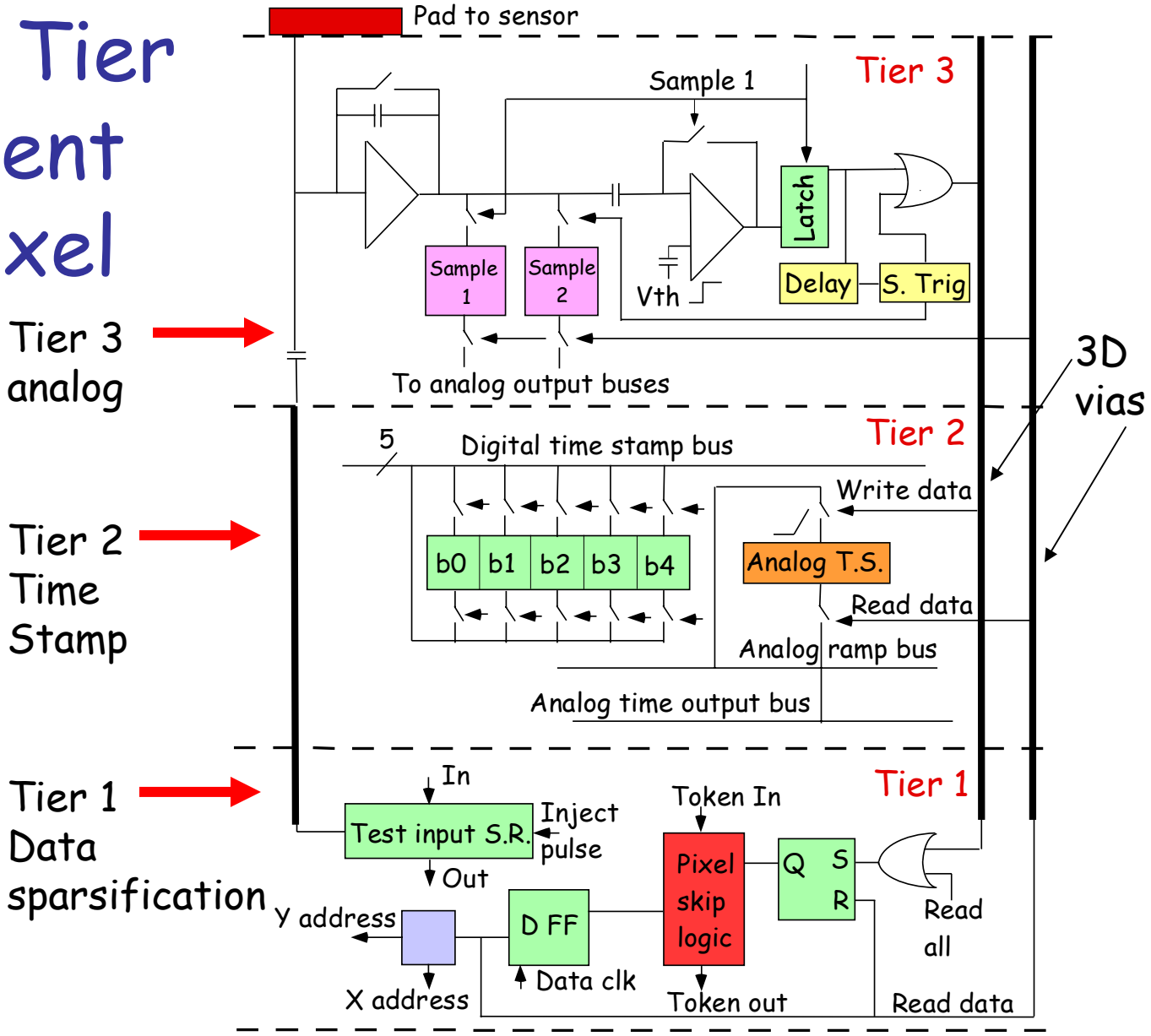
- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out.
- During pixel readout, token scans ahead for the next hit pixel



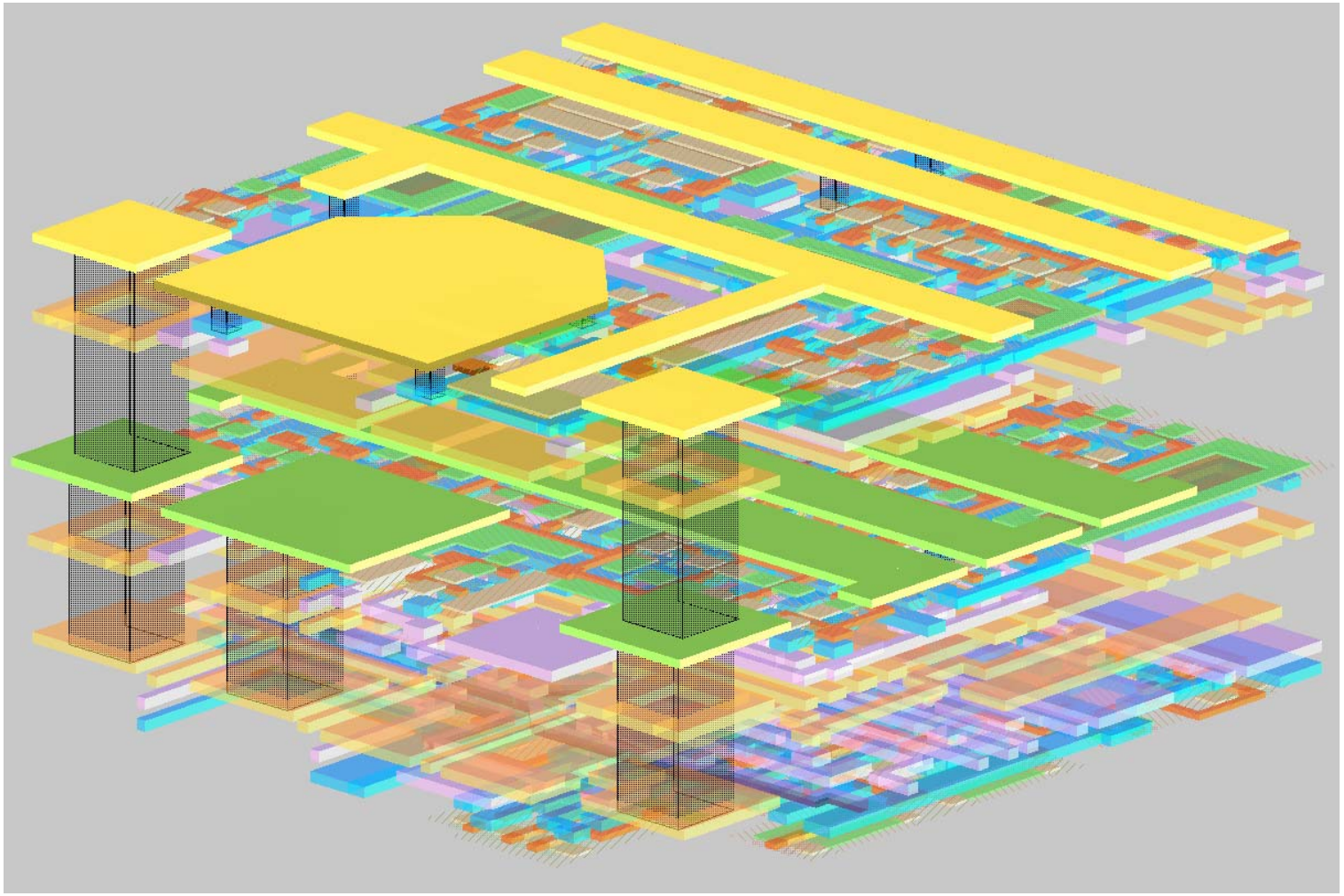
Simplified Pixel Cell Block Diagram



3D Three Tier Arrangement for ILC Pixel



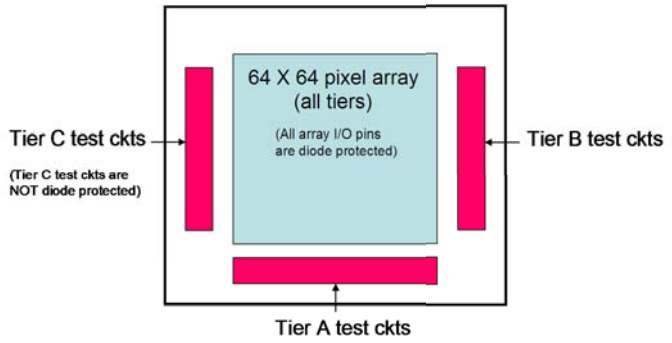
VIP Pixel Stacking with Vias

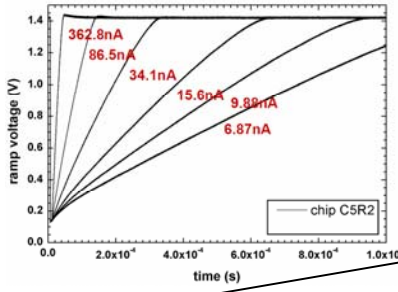


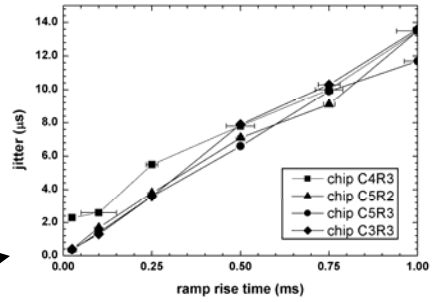
3D-Max Layout View using 3D Design Tool from Micro Magic [4]

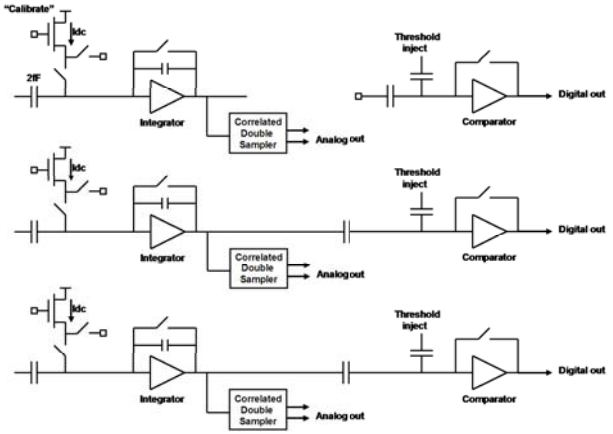
VIP1 Test Results

- Chip is divided into test structures and 64 x 64 array
- Test structure results
  - Bottom tier (tier 1)
    - Simple buffer – performance on one working part is a little faster than simulations
    - Dynamic FF (used for inject in full array) – T_r and T_f should be less than 5 ns for proper operation
  - Middle tier (tier 2)
    - Time stamp ramp test
      - Ramp circuit works but…
        - » Current mirror on different chips gives very different ramp currents
        - » Noise on ramp may be due to protection diodes causing jitter in ramp timing
  - Top tier (tier3) analog ckts
    - Integrators work on some chips
    - Discriminators work on other chips
    - Analog circuits when working are a little faster than simulations.
    - Noise performance appears close to simulations on the few circuits that work



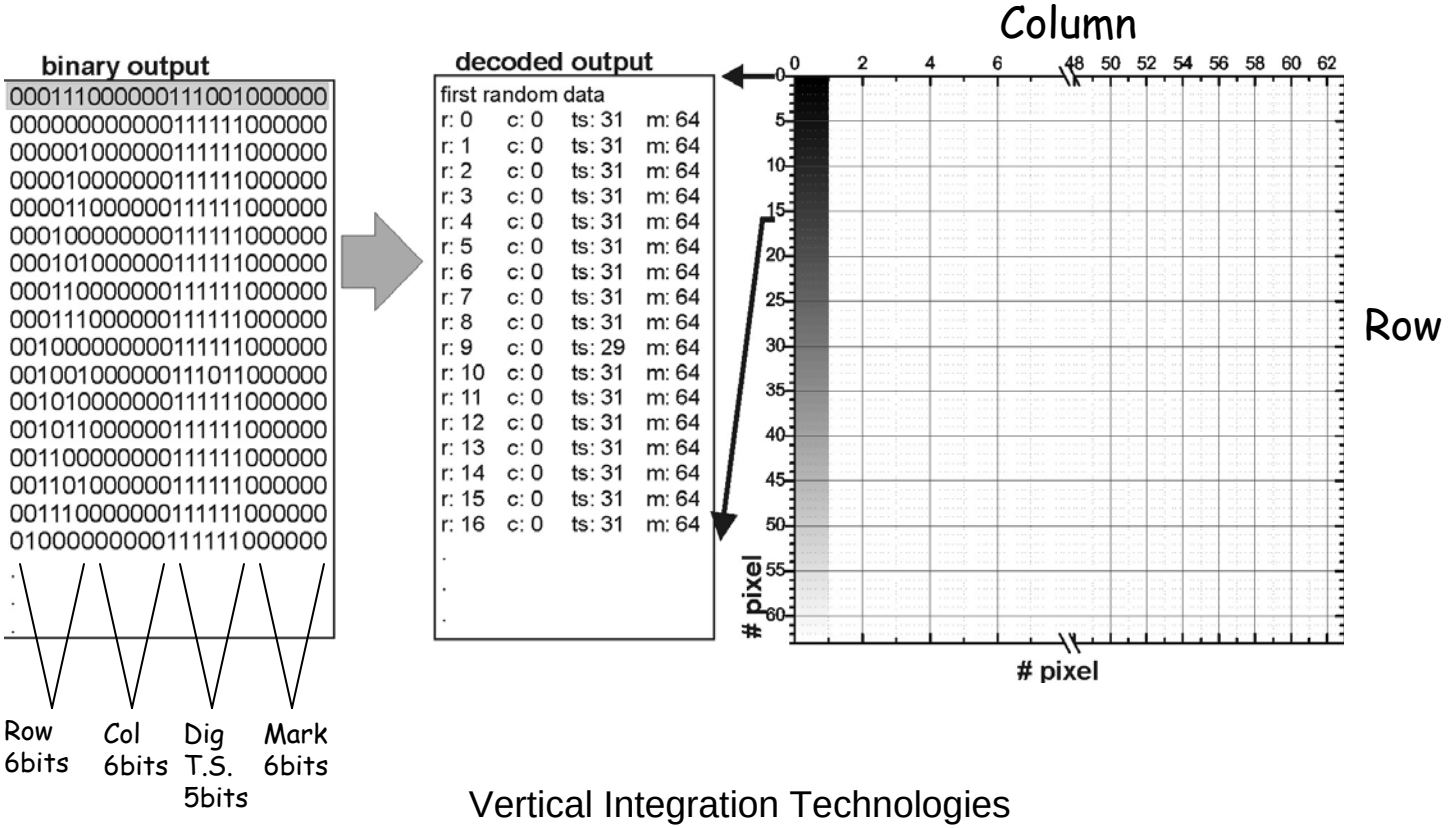






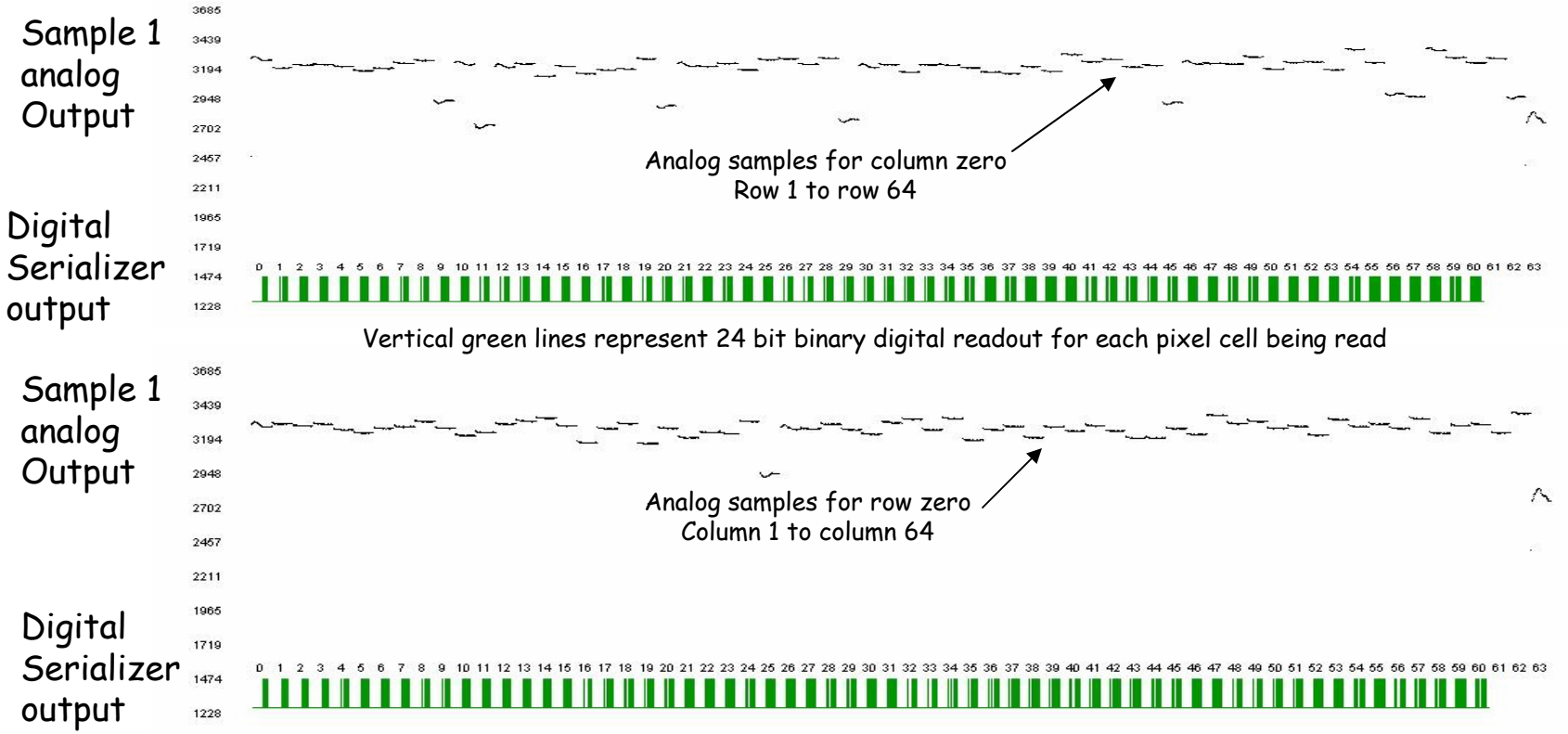
VIP1 Test Results

- Full array results
  - Digital Results
    - Serial readout for address partially working on 3 of 6 chips and only for 0.9<V_{dd}<1.3 V. Circuits do not work at nominal voltage.
    - Serial Shift Register for charge injection works on 3 of 4 chips for 1.0 <V_{dd}<1.2V.
    - Feature needed for large arrays (read all cells in column 1) works as shown below



VIP1 Test Results

- Analog test results
  - Full data acquisition system used to measure analog pedestals on Sample 1 output
    - Results shown below for 64 rows and 64 columns on chip #C3R3
  - The full 64 x 64 array has subarrays with different transistor sizes and input capacitances to help evaluate noise performance.
    - Array noise tests not yet done
  - Additional development of data acquisition system needed for further testing.

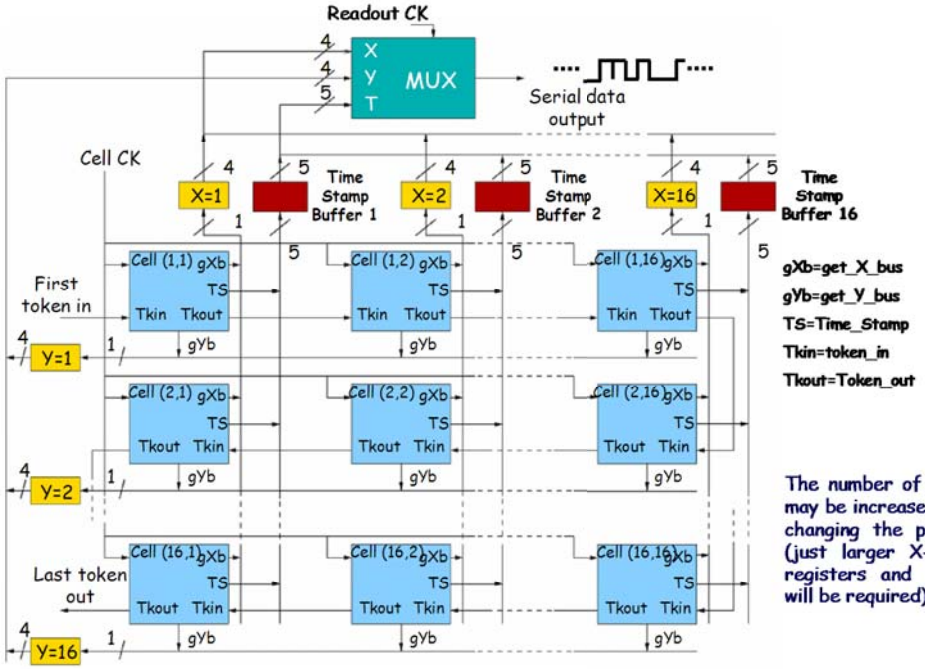


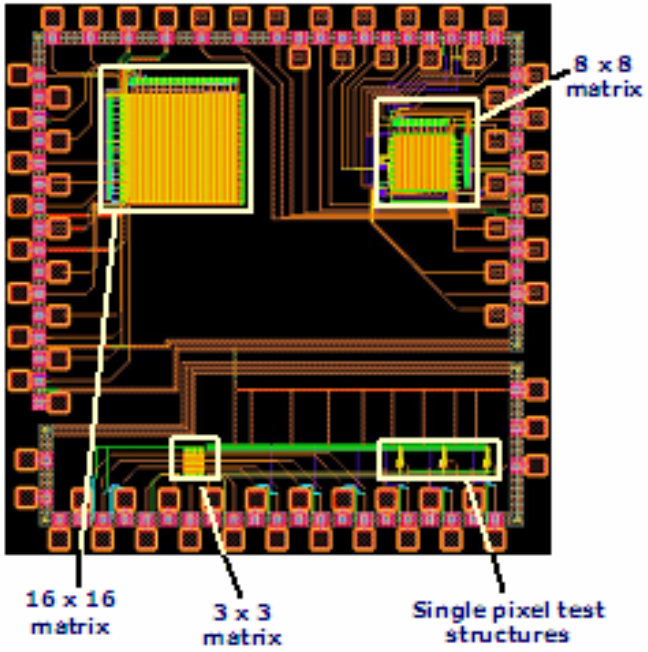
VIP Problems

- Trapped charge between tiers 2 and 3 during fabrication caused NMOS transistor thresholds to shift from 500 mv to 200 mv.
  - Attempts are being made by vendor to correct the problem after the fact with UV radiation
  - Backup lot being processed with different tier2-tier3 bonding conditions to remove threshold shift problem.
- ESD protection diodes are very leaky causing serious problems for circuits with analog inputs.
- Current mirrors used for biasing are not working properly - problem thought to be due to leakage path in the current mirror circuits.
- There are significant variation between chips resulting in low yields - reasons unknown at this time.
  - Testing will continue with parts from a different wafer
  - Discussions are ongoing with other users

MAPS Chip Using VIP Architecture

- Chip developed by Valerio Re in ST 0.13 um CMOS[4]
- Received July 2007
  - Chip only uses digital time stamp
  - No analog output
- Readout architecture is working





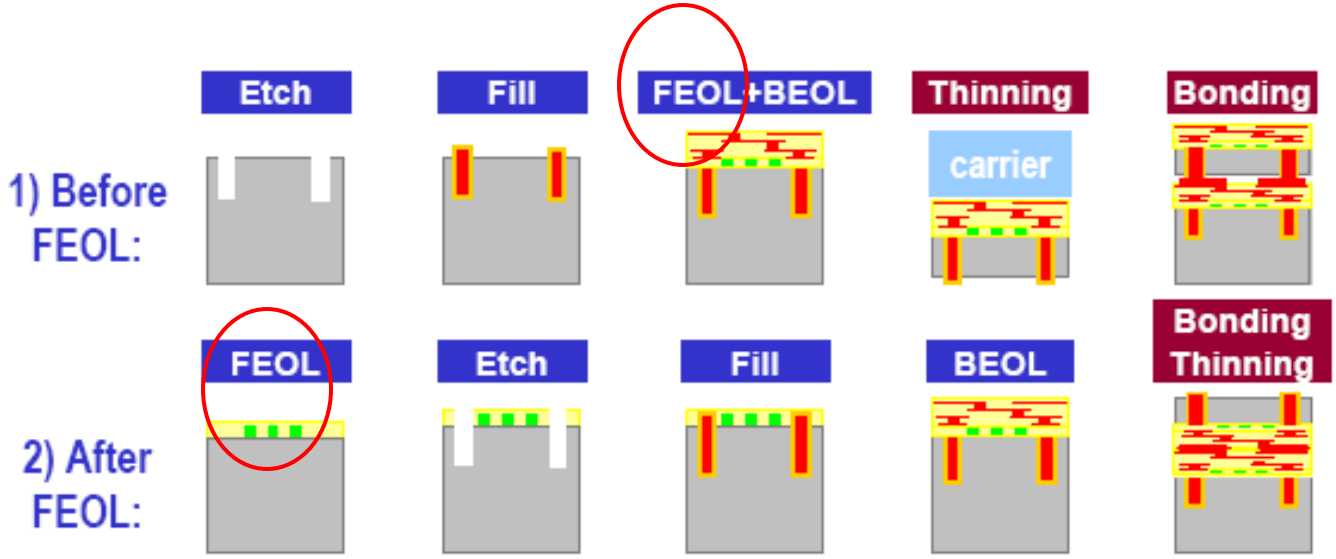
*16 x 16 array appears to work fine
*Tests are continuing
*256 x 256 array to be submitted later this year.

A Move to Commercial 3D Vendors

- There are 3 vendors that have commercially available (external) 3D processes. [5]
  - Tezzaron – uses CuCu thermocompression for bonding
  - Ziptronix- uses Direct Bond Interconnect (oxide bonding)
  - Zycube – uses adhesive and In-Au bumps for bonding
- Fermilab is working with Tezzaron to fabricate 3D integrated circuits using CuCu bonding.
  - Others developing CuCu bonding include IBM, RPI, MIT
- Fermilab is working with Ziptronix to do low mass bonding with DBI to detectors. (FPIX chips to 50 um thick sensors.)
- Commercial 3D processes can be classified as either "via first" or "via last".

Via First Approach

- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing [6]

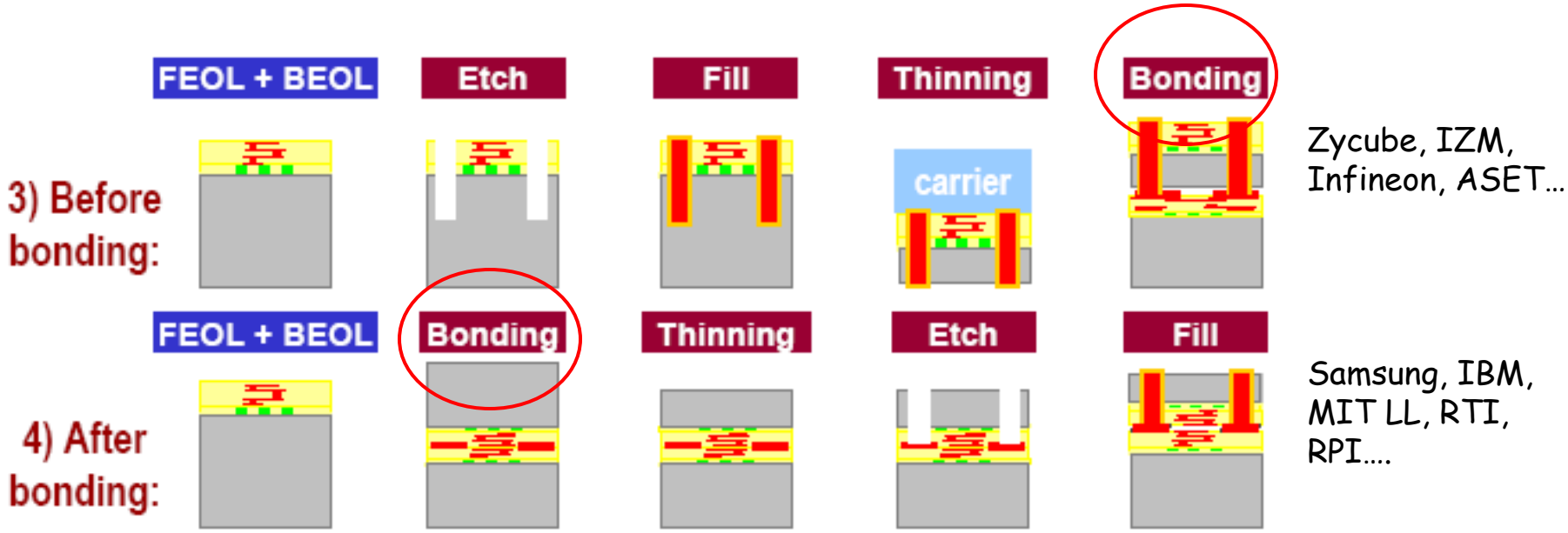


IBM, NEC, Elpida, OKI, Tohoku, DALSA….

Tezzaron, Ziptronix Chartered, TSMC, RPI, IMEC……..

Via Last Approach

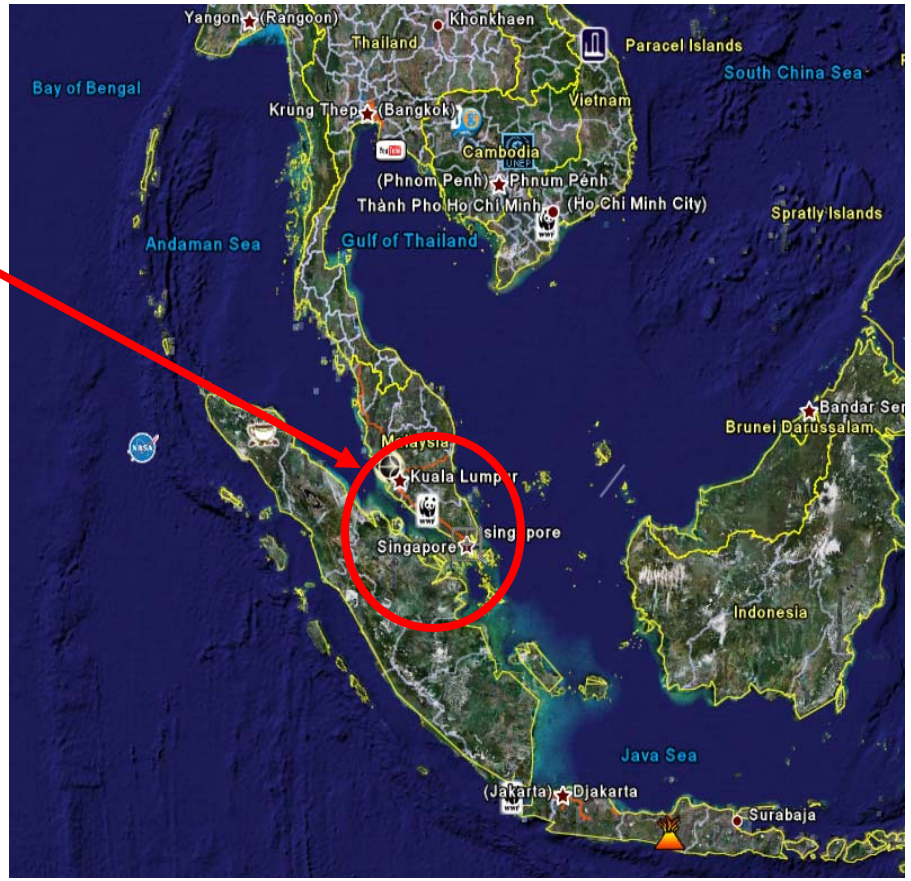
- Via last approach occurs after wafer fabrication and either before or after wafer bonding [6]



Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

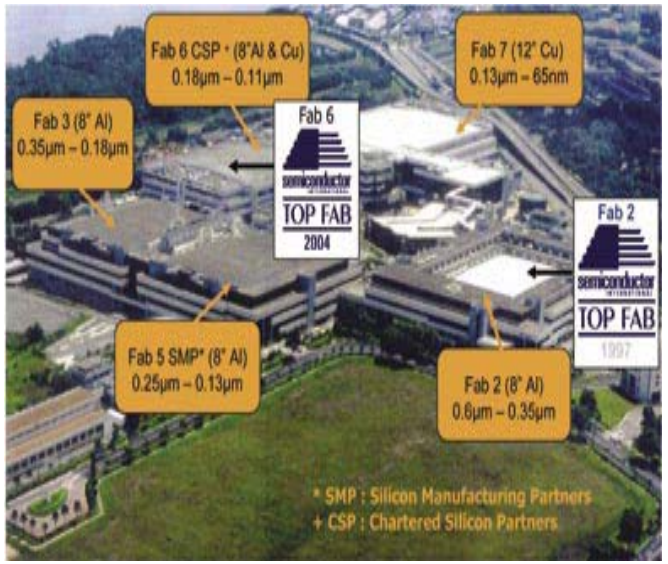
Tezzaron Background

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



Chartered Semiconductor

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Extension to 300mm wafers and 45nm TSVs underway
- Chartered 0.13 um process is similar to the IBM 0.13 um process but has different layer arrangement and transistor thresholds.
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic

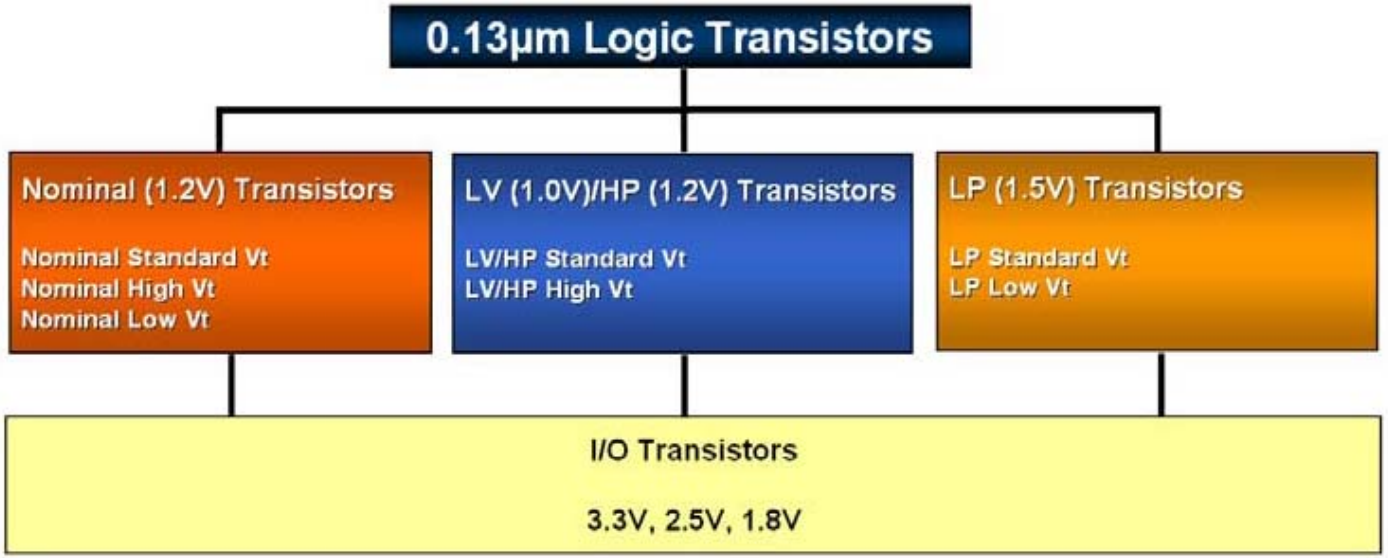


Chartered Campus

Chartered 0.13 um Process

- 8 inch wafers
- Large reticule – 24 mm x 32 mm
- Features
  - Deep N-well
  - MiM capacitors – 1 fF/um^2
  - Reticule size 24 x 32 mm
  - Single poly
  - 8 levels of metal
  - Zero Vt (Native NMOS) available
  - A variety of transistor options with multiple threshold voltages can be used simultaneously
    - Nominal
    - Low voltage
    - High performance
    - Low power

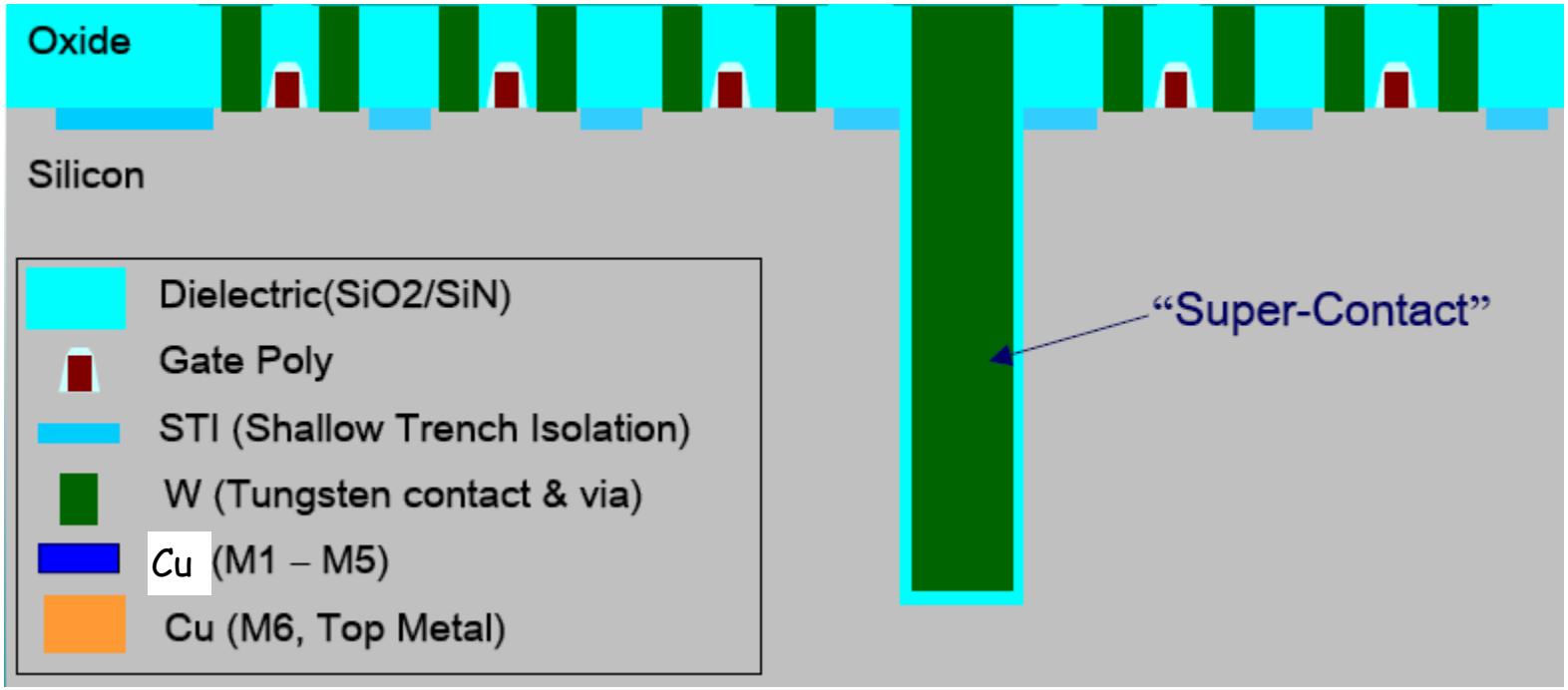
Chartered Transistor Options



Choose one of three processes and one of three I/O transistors types

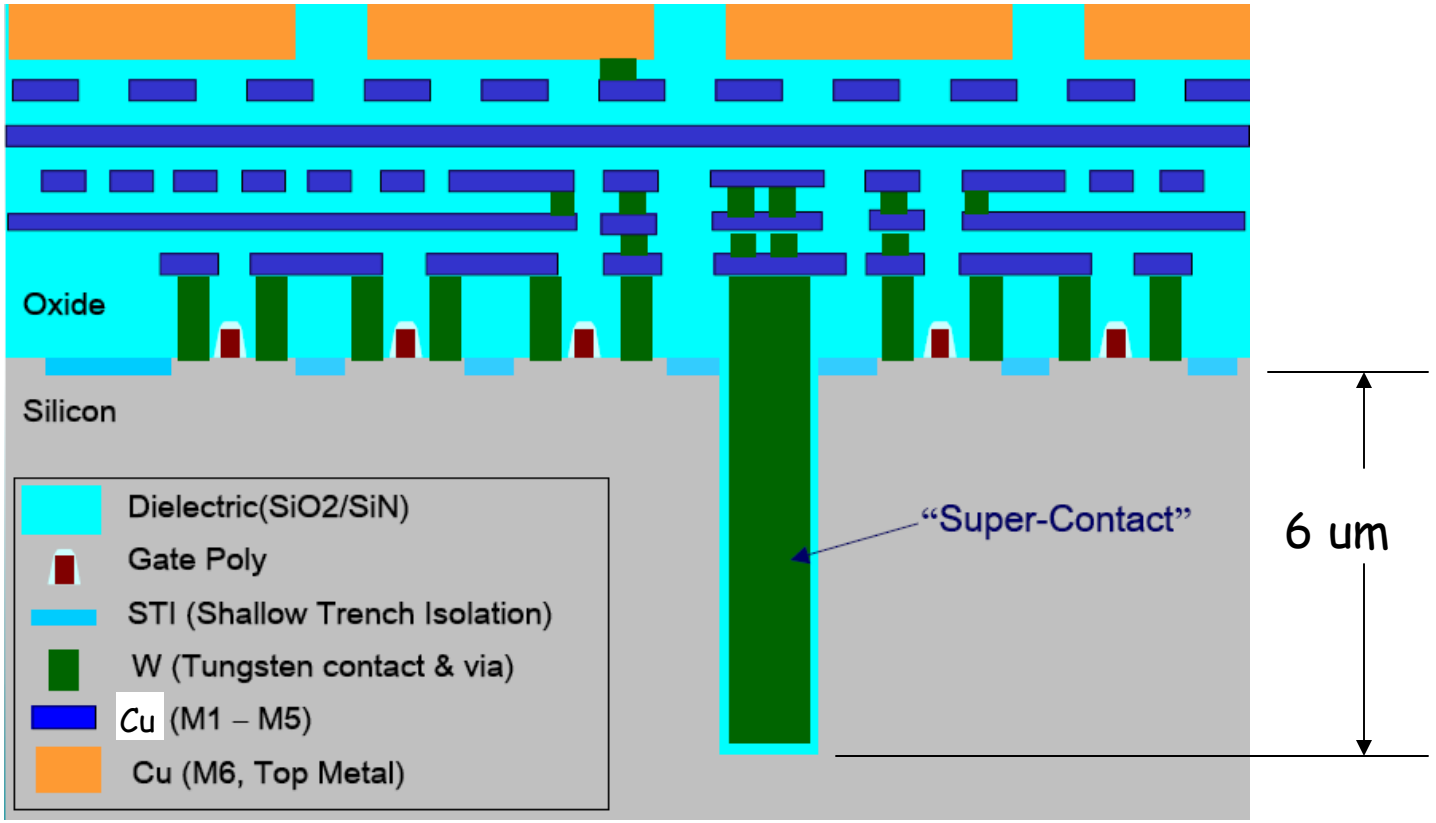
Tezzaron 3D Process[7]

- Complete transistor fabrication on all wafers to be stacked
- Form super via on all wafers to be stacked
- Fill super via at same time connections are made to transistors



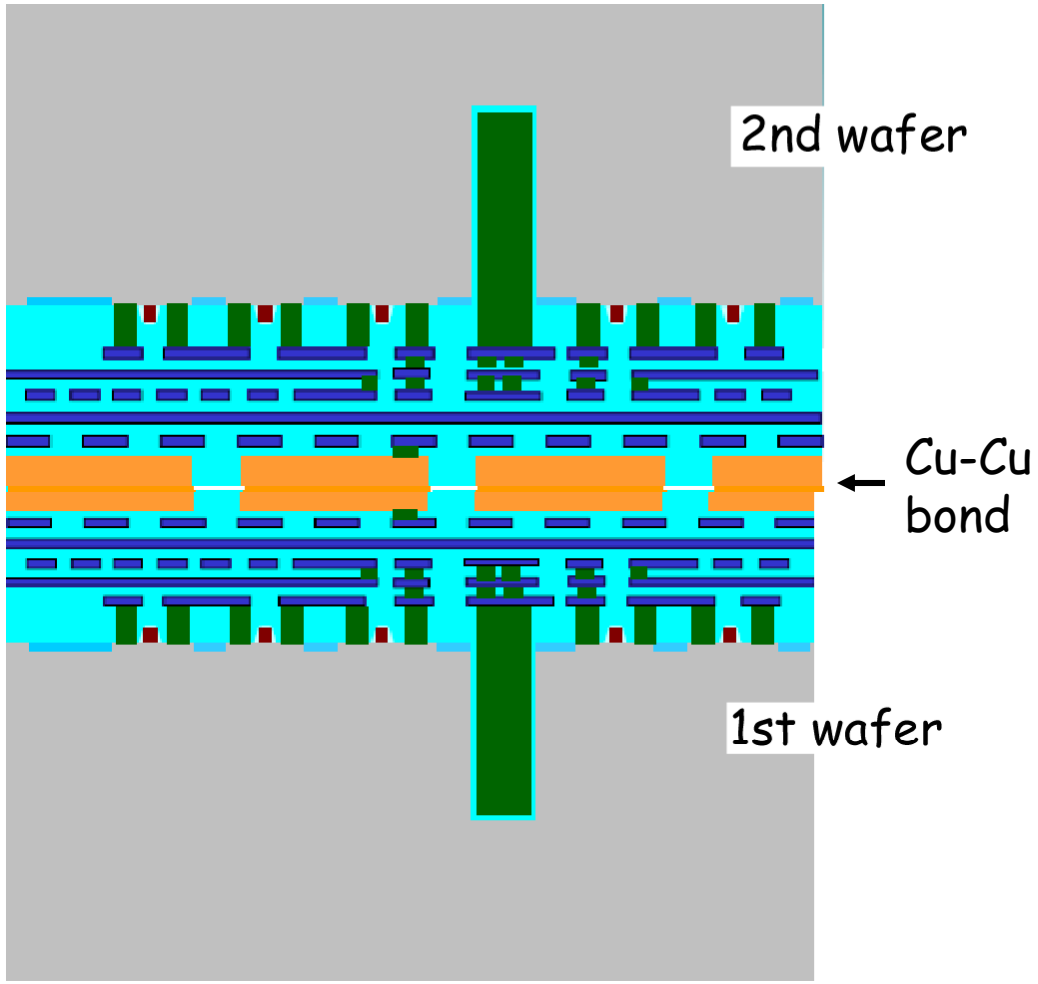
Tezzaron 3D Process

- Complete back end of line (BEOL) processing by adding Al metal layers and top Cu metal (0.8 um)



Tezzaron 3D Process

- Bond second wafer to first wafer using Cu-Cu thermo-compression bond

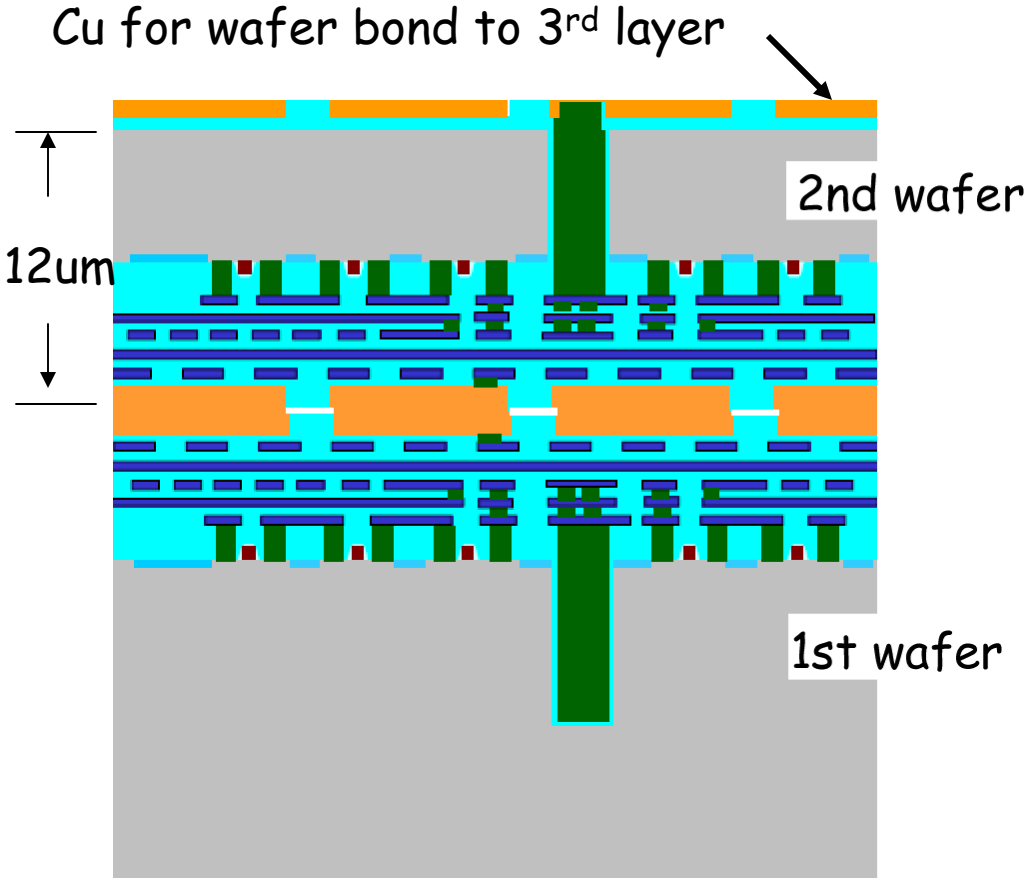


Tezzaron 3D Process

- Thin the second wafer to about 12 um total thickness to expose super via.
- Add Cu to back of 2nd wafer to bond 2nd wafer to 3rd wafer

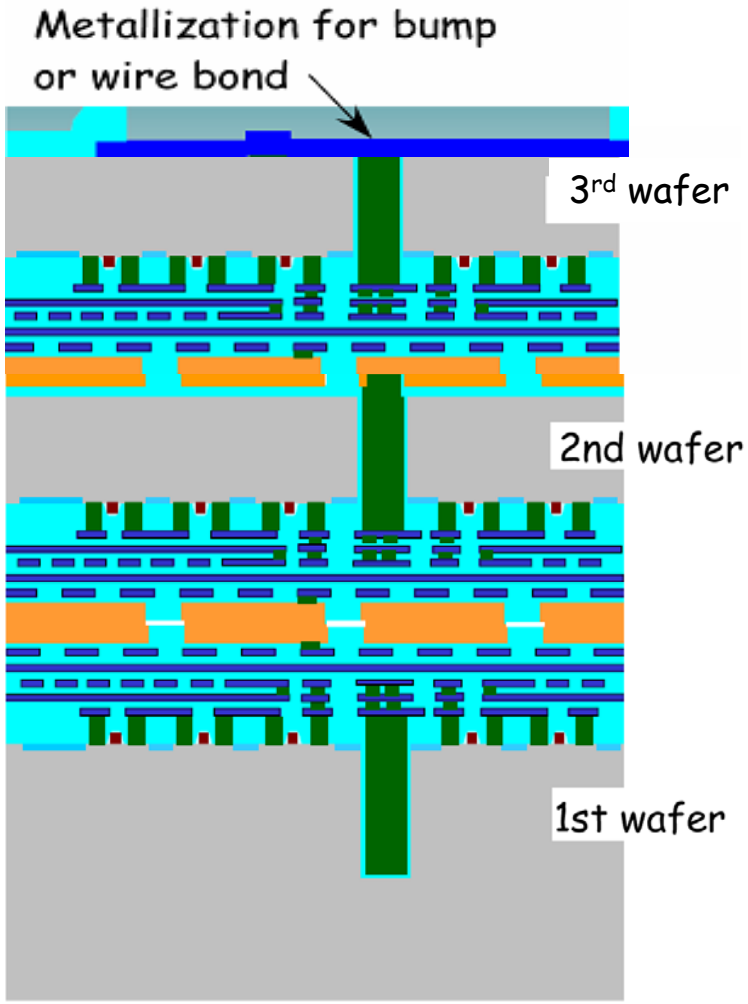
  OR

  add metallization on back of 2nd wafer for bump bond or wire bond.

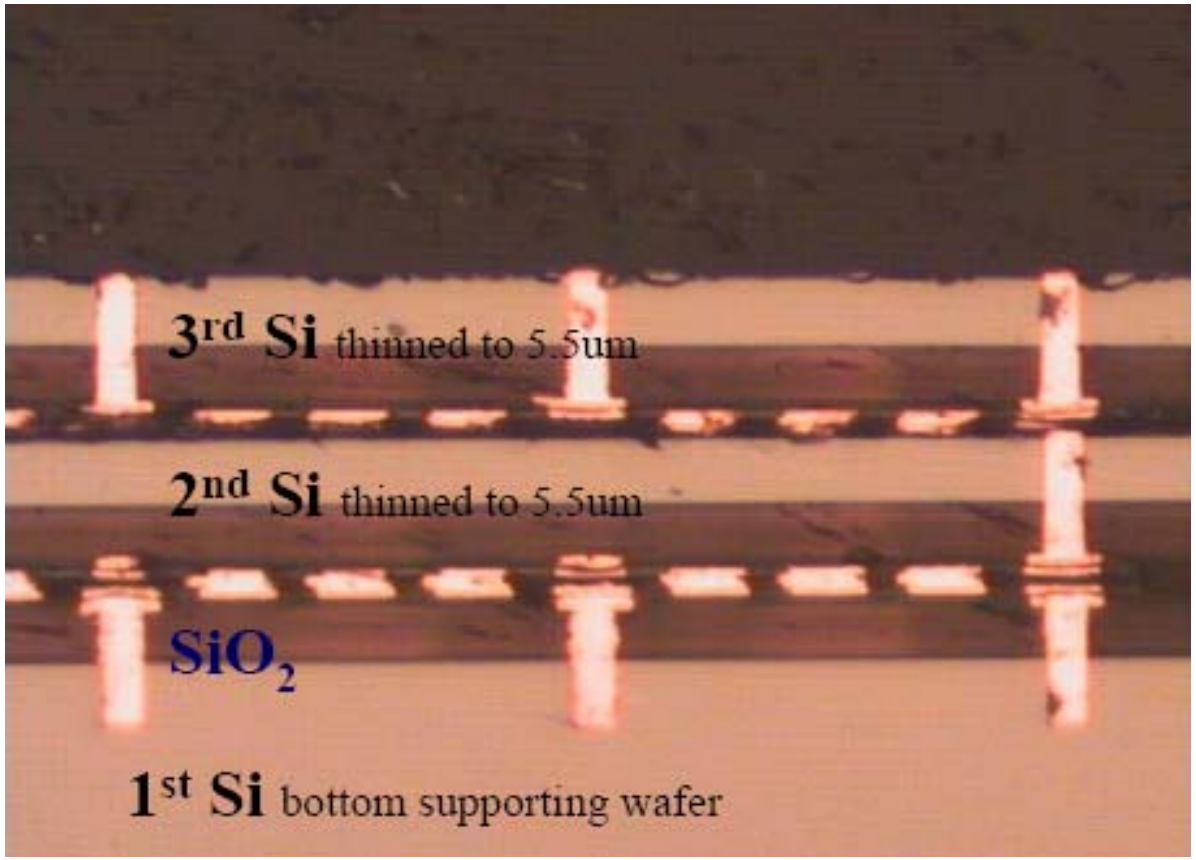


Tezzaron 3D Process

- Stack 3rd wafer
- Thin 3rd wafer (course and fine fine grind to 20 um and finish with CMP to expose W filled vias)
- Add final passivation and metal for bond pads

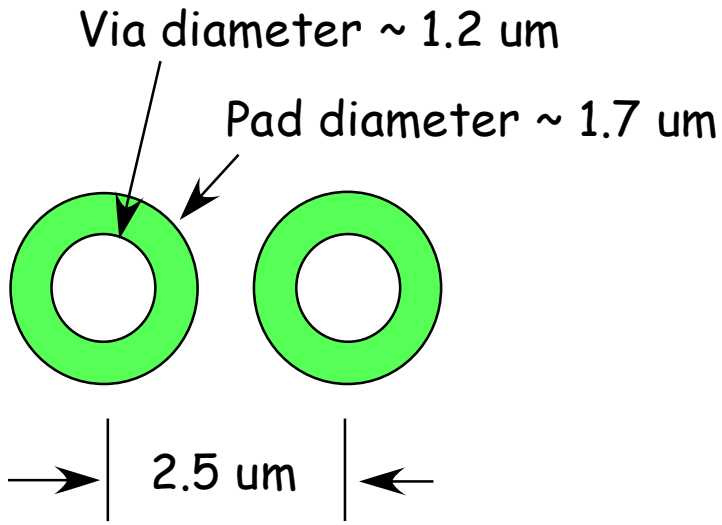


Cross section of Tezzaron 3 layer Stack[7]



Tezzaron vias

- Via size plays an important role in high density pixel arrays
- Tezzaron can place vias very close together

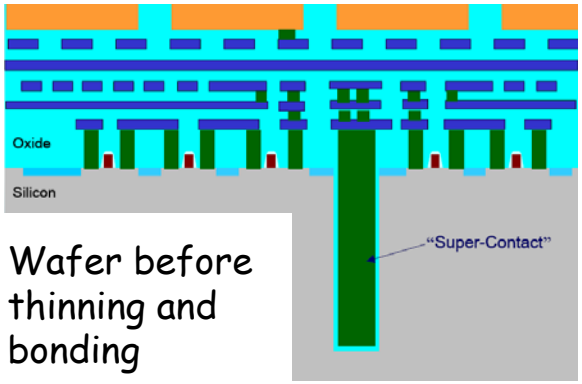


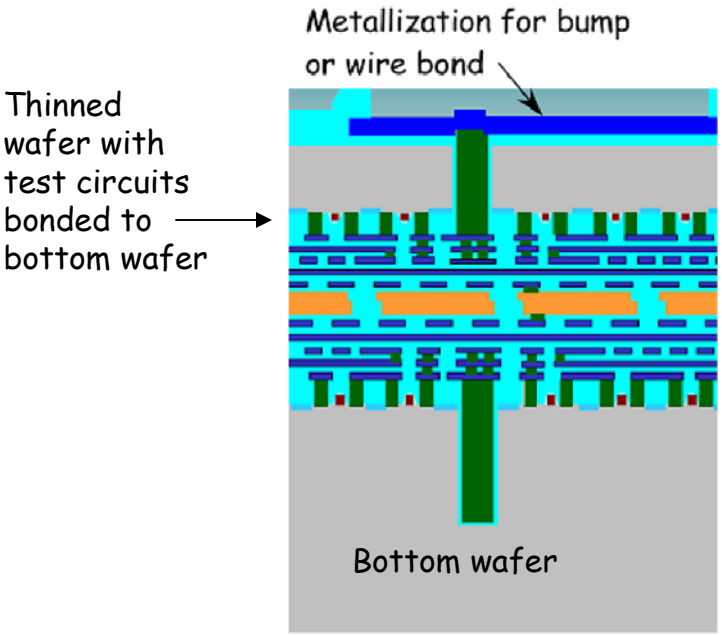
Wafer Bonding

- Bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 um
- Missing bond connections = 0.1 PPM
- Temp cycling of bonds from -65 to + 150 C
  - 100 devices, 1500 cycles, 2 lots, no failures

Circuit Performance

- Circuits tested with full substrate thickness and then after bonding and thinning to 12 um
  - No change in performance between thinned and bonded devices and unthinned/unbonded devices.
    - Bandgap circuit
    - Sense Amplifier
    - Charge pump
  - No change in performance between thinned and bonded devices before and after temperature cycling.
- Transistor measurements on same devices before and after thinning and bonding are shown on the next slide.
  - No noticeable difference in characteristics except small increase in PMOS speed due to strain in silicon as expected





Transistor Performance for Thinned and Bonded Wafers[7]

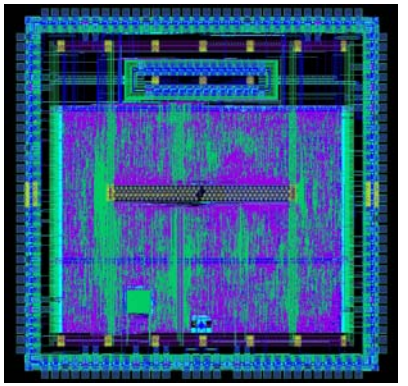
	Threshold Voltage VT0 (V)						Saturation Current Idsat (uA) (Vd= Vg=1.2V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	0.395	0.485	0.479	-0.355	-0.399	-0.398	122.520	5152.000	9696.000	26.940	2061.800	5986.200
Post Ave	0.393	0.484	0.465	-0.357	-0.396	-0.404	121.500	5094.333	9840.333	26.897	1997.333	4473.000

	Breakdown Voltage BVDSS (V) (Ids=2uA)						Leakage Current Ioff (pA) (V=1.4V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	3.380	3.220	3.220	4.100	4.000	2.780	151.820	638.900	3655.000	136.460	1285.120	282050.000
Post Ave	3.377	3.230	3.217	4.147	3.970	3.113	140.433	433.667	3237.667	211.333	910.333	121680.000

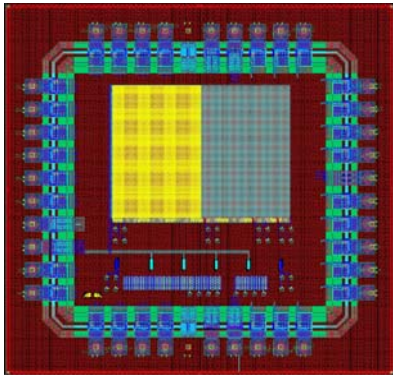
	Subthreshold Slope SUBSLP (mV/dec)						Gate Leakage Current GLEAK (nA)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	75.840	76.820	79.380	-73.040	-76.960	-89.460	1.200	1.172	1.190	0.909	0.883	0.886
Post Ave	74.367	76.100	78.567	-74.733	-76.833	-88.600	1.250	1.287	1.300	1.018	1.011	0.767

Tezzaron Chips

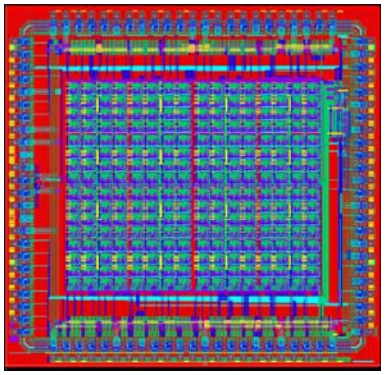
CPU and memory stack
- 80 MHz operation
- 220 MHz memory interface
- Synthesized, placed and routed in 3D with standard Cadence tools



CMOS sensor
- 5 different pixel fields
- Main array 160 x 120 pixels, 5 x 5 um pixels
- 2.4 um pitch interconnect
- 100% array efficiency
- Back side illumination



FPGA
- 12 vertical interconnects/logic block
- Shows tight 3D integration capability

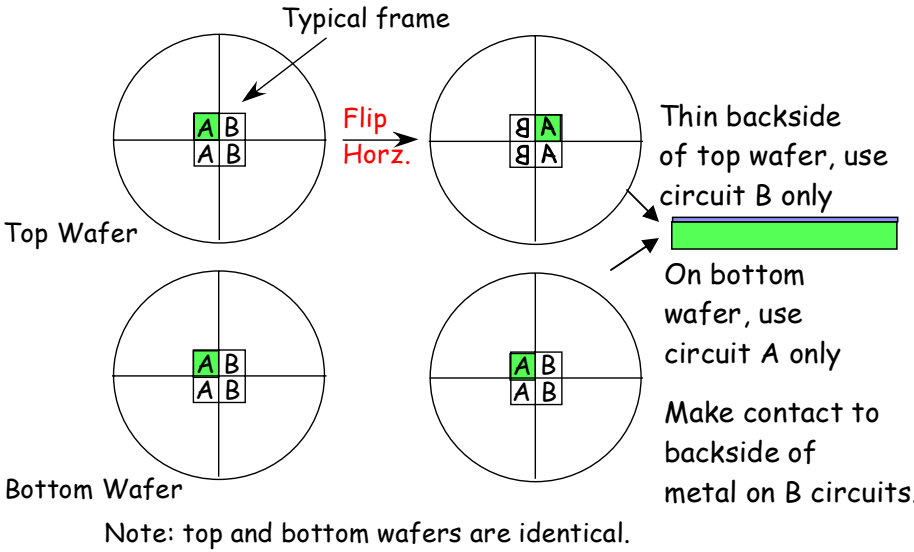


Advantages

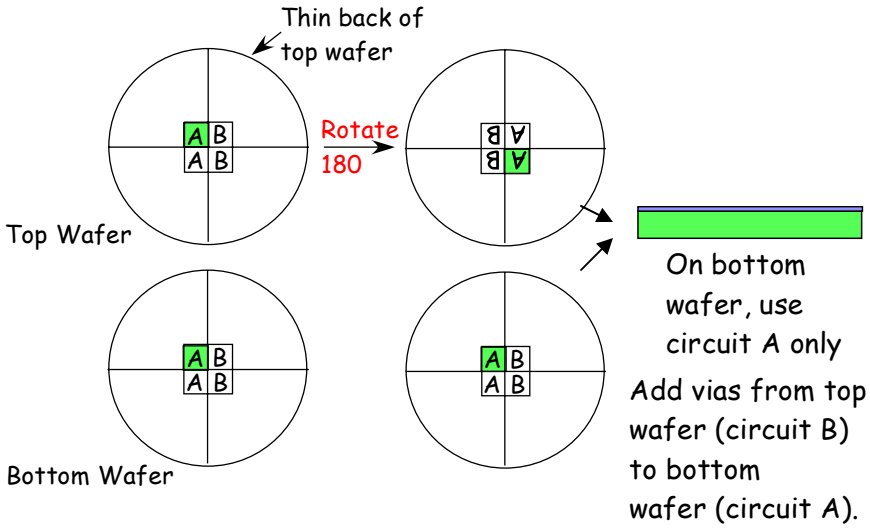
- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Good models available for Chartered transistors
- Thinned transistors have been characterized
- Process supported by commercial tools and vendors
- Fast assembly
- Lower cost

Fermilab 3D Multi-Project Run

- Fermilab will be submitting a 3D multi project run using Tezzaron.
- There will be only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks. (Useful reticule size 16 x 24 mm)
- The wafers will be bonded face to face.
- Bond pads will be fabricated for bump bonding to be done later at Ziptronix



Face to Face Bonding



Back to Face Bonding

Cost/Delivery

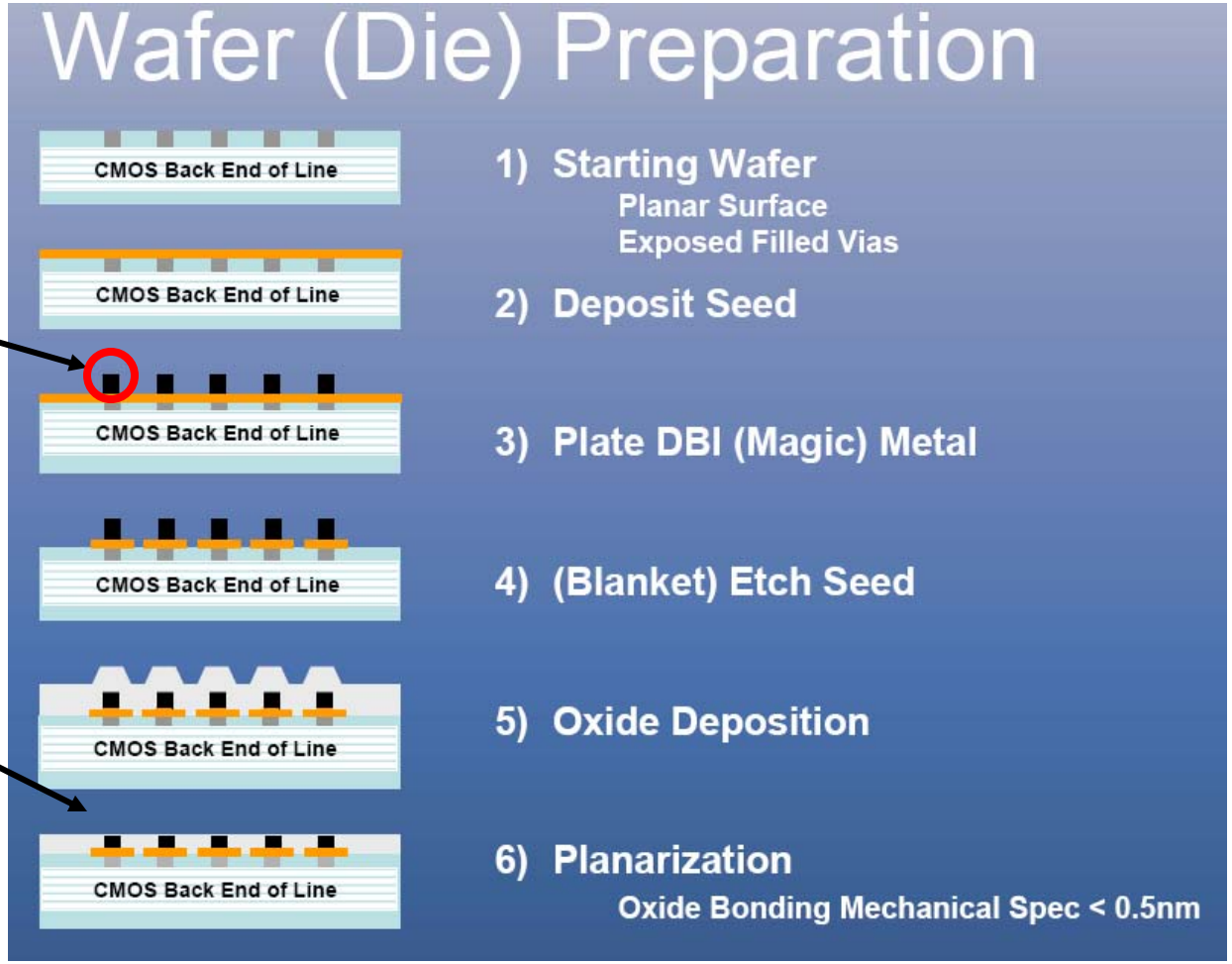
- We expect to receive 12 fully processed 3 D wafers (made from 25 eight inch wafers).
- We expect the total cost to be less than $250K (~150K Euro)
- We expect delivery to be approximately 12 weeks after delivery of the loaded reticule to Tezzaron.

Ziptronix

- Some parts received from Tezzaron will be bonded to sensors.
- Fermilab sensors are being made at MIT LL.
- Some 3D bond processes introduce significant material between bonded layers.
  - Conventional solder bumps or CuSn pose a problem for low mass fine pitch assemblies
- IC bonding to a detector will be done by Ziptronix using the Direct Bond Interconnect (DBI) process.[8]
  - Xo << 0.01%
- Tezzaron and Ziptronix have formed an alliance.
  - Good communication between companies for pad metallization for sensor bonding, etc. now exists.
- Ziptronix is located in North Carolina
- Fermilab has current project with Ziptronix to bond BTEV FPIX chips to 50 um thick sensors.
- Orders accepted from international customers

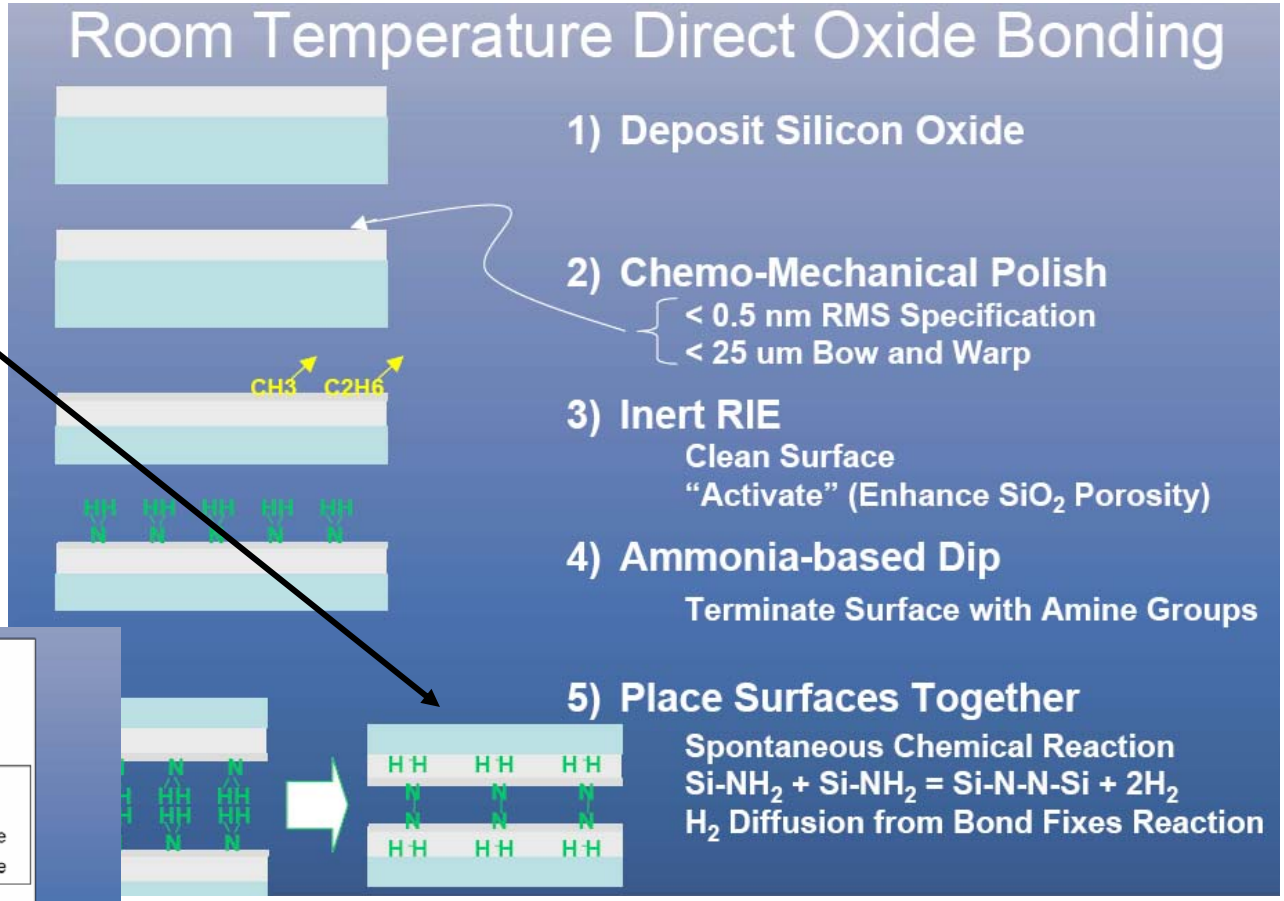
DBI Process

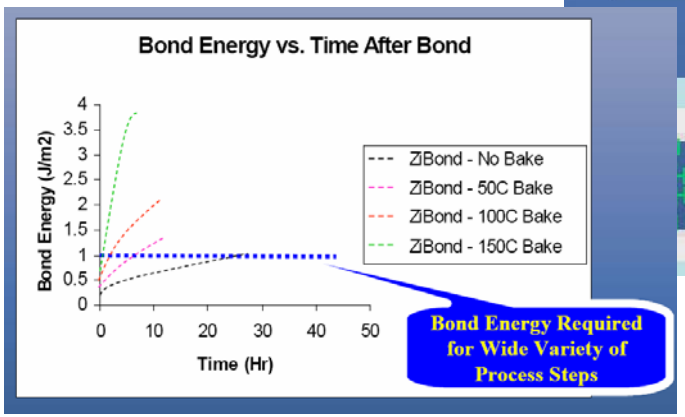
- Add Magic metal for electrical connections
- Prepare surface for oxide bonding



Oxide Bonding

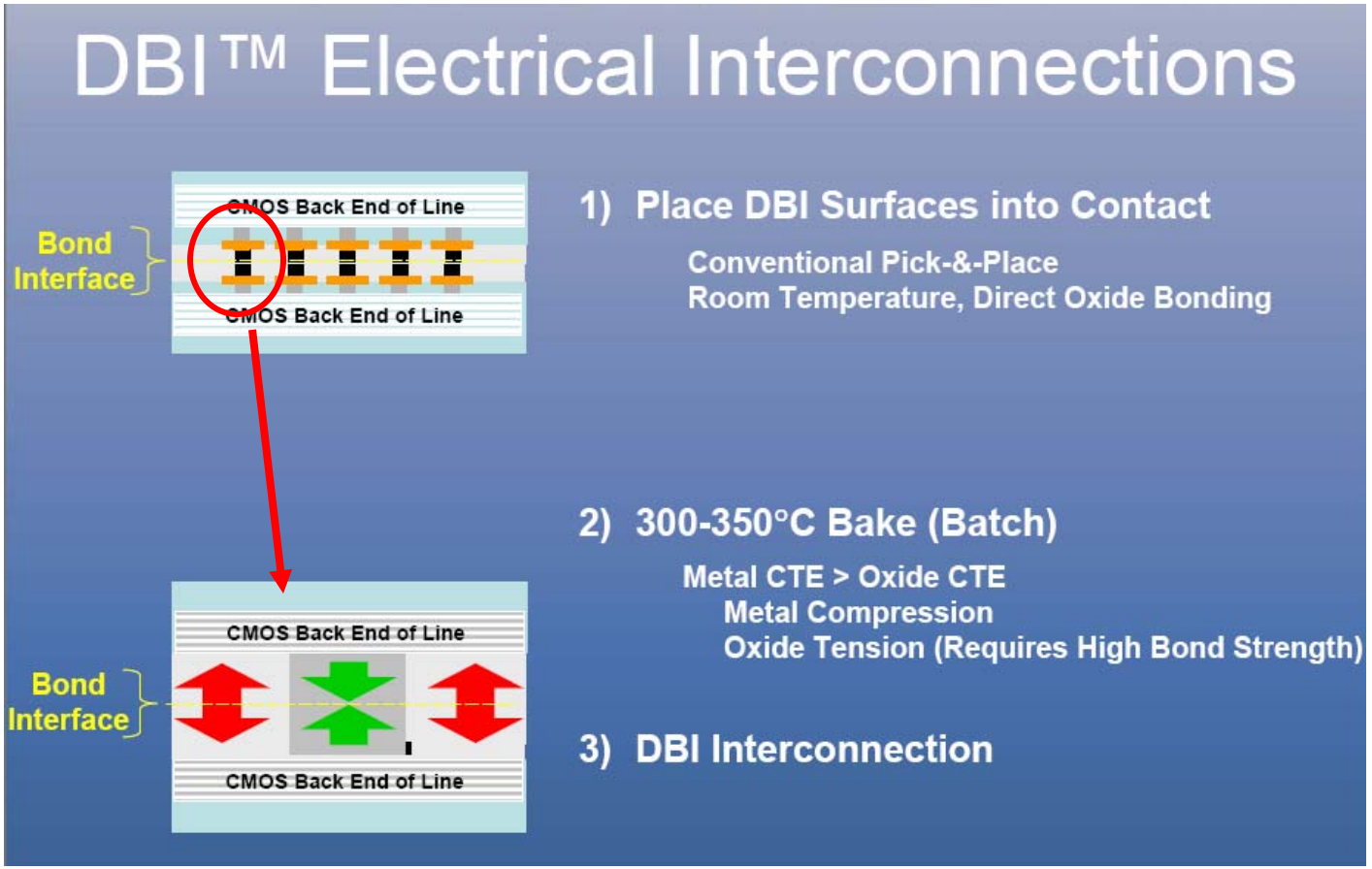
- Surfaces bond immediately due to Van der Waals force.
- Bonding occurs at room temperature
- Bond strength increase with time





DBI Electrical Connections

- After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.



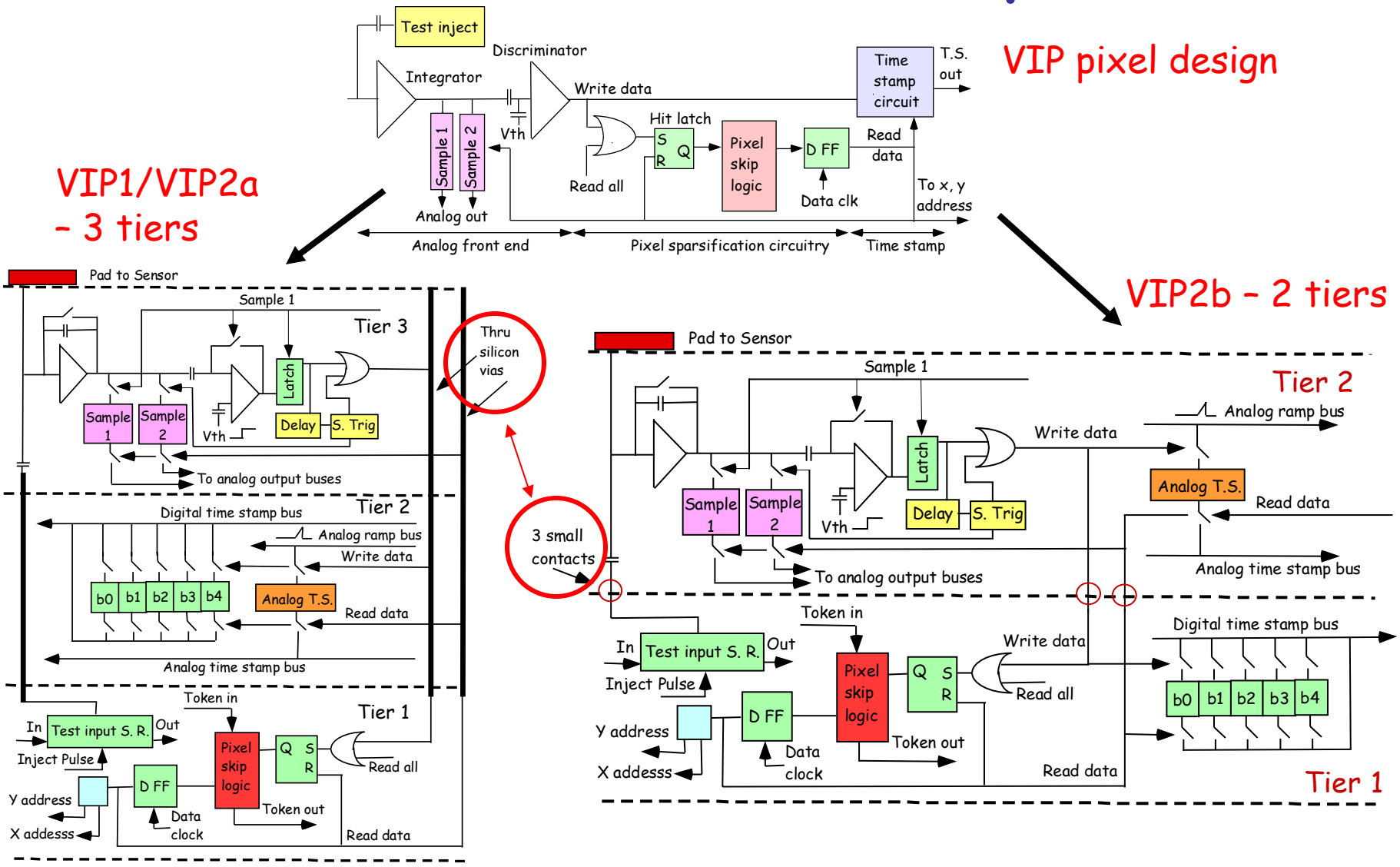
Design Plans for Fermilab in 2008

- Submit VIP2a design to 3rd MPW run at MIT LL later this year.
  - Three tiers of circuits with new features
  - Process upgraded to 0.15 um feature size (still in SOI)
- Submit Fermilab MPW run to Tezzaron later this year
  - Two tiers of circuits
  - Use Chartered Semiconductor 0.13 um CMOS process
  - Process options chosen for pixel applications
  - Reticule from Fermilab currently expected to include
    - VIP2b design (same basic design as VIP2a)
    - Concept chip for CMS to demonstrate 3D capability for super CMS upgrade
      - Moving from 0.25um technology to two tier 0.13um could increase circuit density up to a factor of 7. Circuit density can be traded for pixel size.
    - Numerous test structures
      - Same test circuits as already submitted to OKI and MIT LL
      - Test structures to further study bonding and via performance
    - New design from Valerio Re proposed to test 3D MAPS concept

VIP2b design at Tezzaron

- VIP2b design essentially the same as VIP2a.
- Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
- Radiation tolerance of Chartered 0.13 um process is currently being studied by another group.
- Going from 3 layers in 0.18 um technology to 2 layers in 0.13 um technology should reduce pixel size below 20 um.
- Using the via first process at Chartered eliminates the wasted area needed for vias in the MIT LL process.
- Chartered provides fully characterized process and models at commercial foundry along with standard cell libraries.
- VIP2b requires significantly less 3D processing than VIP2a

VIP2a and VIP2b Comparison



Summary

- 3D circuit design is gaining attention for HEP[9]
- Fermilab is continuing to test the VIP1 chip from MIT LL
  - One known processing problem has been identified
    - MIT is working to correct the problem
  - Some other problems have been observed
  - Yield on the VIP1 is poor, reasons not yet clear
  - Fermilab expects to submit a VIP2a to MIT LL later this year
- Fermilab is moving toward using commercial vendors for its 3D processing
  - Aiming to submit a MPW run with several designs to Tezzaron by end of 2008 or early 2009.
  - Expect to use Ziptronix to provide low mass connection to sensors.
- We are inviting other interested groups to join us in our 3D MPW run submission to Tezzaron.

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