Development of Vertically Integrated Circuits for Particle Detectors

M.Trimpl

On behalf of the Fermilab Pixel Group:
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outline

- Motivation / Advantages of 3D
- Fermilab's activities towards 3D integration
- MIT-LL run(s) and current MPW with Tezzaron
- FNAL 3D-IC Designs: VIPIC, VICTR, VIP2b
- Summary

global 3D activities – very hot topic right now

7th International Meeting on Front-End Electronics

from **Monday 18 May 2009 (08:00)**
to **Thursday 21 May 2009 (18:30)**
at **Montauk Yacht Club**
chaired by: ***Paul O'Connor***
support: poc@bnl.gov

Monday 18 May 2009 | Tuesday 19 May 2009 | Wednesday 20 May 2009 | Thursday 21 May 2009 |

Monday 18 May 2009

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08:30->*09:00* Welcome and Introduction

08:30	Welcome and Introduction (20') (Slides)	Paul O'Connor (*BNL*)

09:00->*18:00* Session 1: 3D/Vertical Integration and Advanced Interconnect (Convener: Ray Yarema (*FNAL*))

09:00	Vertical integration with Chartered Semiconductor and Tezzaron (1h00') (Slides)	Bob Patti (*Tezzaron*)
10:00	Direct Bond Interconnect (1h00') (Slides)	Paul Enquist (*Ziptronix*)
11:00	break	
11:30	3D Integrated Imaging Systems (1h00') (Slides)	Piet De Moor (*IMEC*)
12:30	Lunch	
13:30	Low cost wafer bumping and low stress assembly for large devices at ultra fine pitches (1h00') (Slides)	Thorsten Teutsch (*PacTech*)
14:30	Facilitation Group for Monolithic and Vertically Integrated Pixel Detector R&D (1h00') (Slides)	Valerio Re (*Bergamo*)
15:30	break	
16:00	Front End Electronics using 3D Integrated Circuits (30') (Slides)	Grzegorz Deptuch (*Fermilab*)
16:30	Fast Binary Readout Monolithic Active Pixel Sensors: From CMOS to 3DIT (30') (Slides)	Yavuz Degerli (*IRFU Saclay*)
17:00	Fully Differential Circuits for Dual Readout of 3D Sensors (30') (Slides)	Michael Karagounis (*Bonn*)
17:30	3D deep N-well MAPS with sparse readout for high resolution, highly efficient particle tracking (30') (Slides)	Lodovico Ratti (*Pavia*)

Tuesday 19 May 2009

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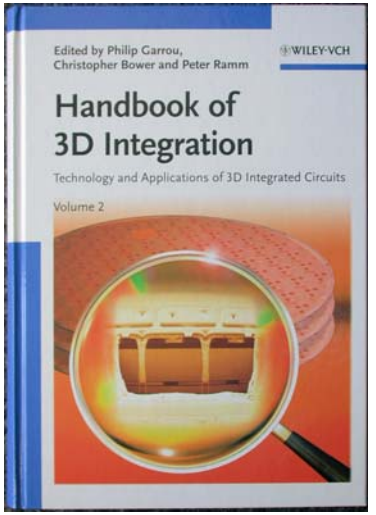
08:30->*09:30* Session 1: 3D/Vertical Integration and Advanced Interconnect Continued (Convener: Ray Yarema (*FNAL*))

08:30	Ultra Thin, Fully Depleted MAPS based on 3D Integration of Heterogeneous CMOS Layers (30') (Slides)	Wojciech Dulinski (*Strasbourg*)
09:00	Interconnection of thinned pixel sensors and read out electronics using the IZM SLID process (30') (Slides)	Hans-Gunther Moser (*MPI Munich*)

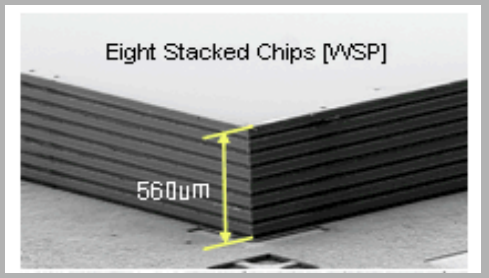


Introduction / Motivation towards 3D

3D device is a vertical integration of multi layers (of semiconductor) to **one 'monolithic' unit.** This includes thinning, bonding and interconnecting these layers.

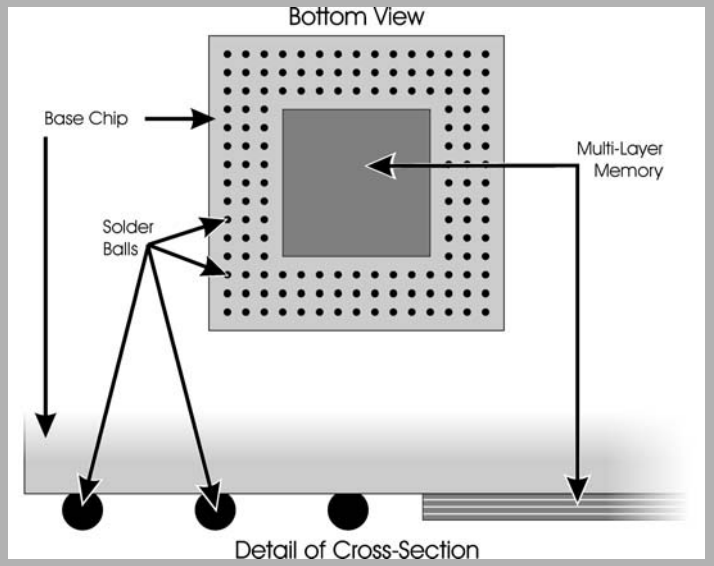
Industry has various fields of interest:

- overcome Moore's law,
- memory on processor (multi cores),
- stacked memory,
- cell phones cameras



Samsung : 16GB Stacked Flash

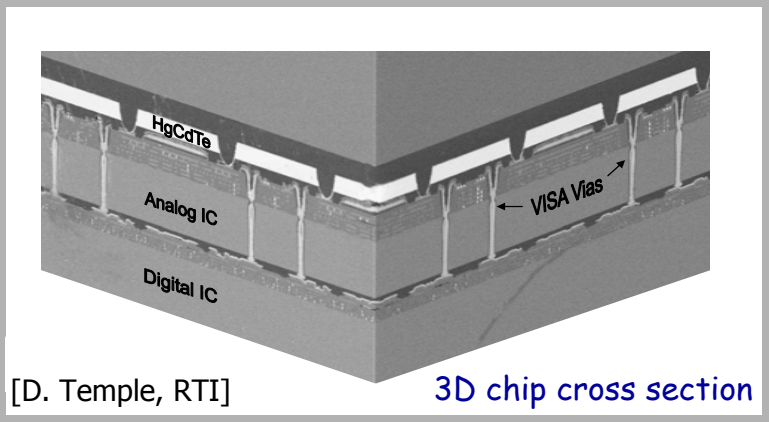
I will not talk about this!



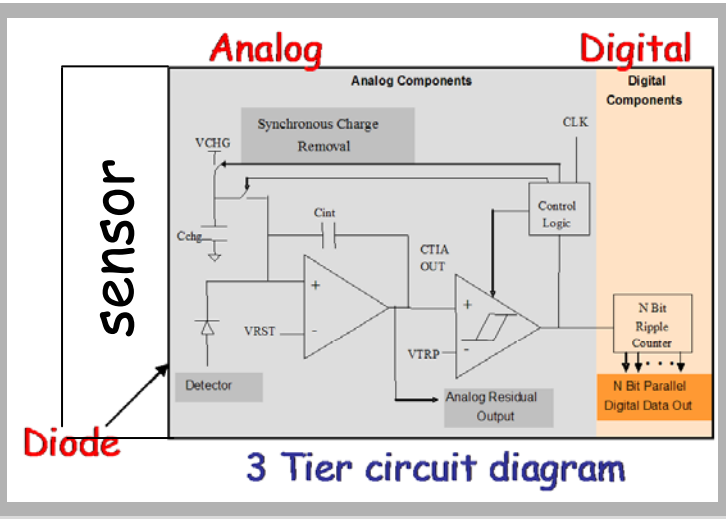
why is 3D interesting for us?

- 3D is not only a more dense design (# transistors per mm^2)
- it also offers some interesting opportunities for detector design / assembly

3D Example: 3 Tier Vertically Integrated
256 x 256 Pixel Array:



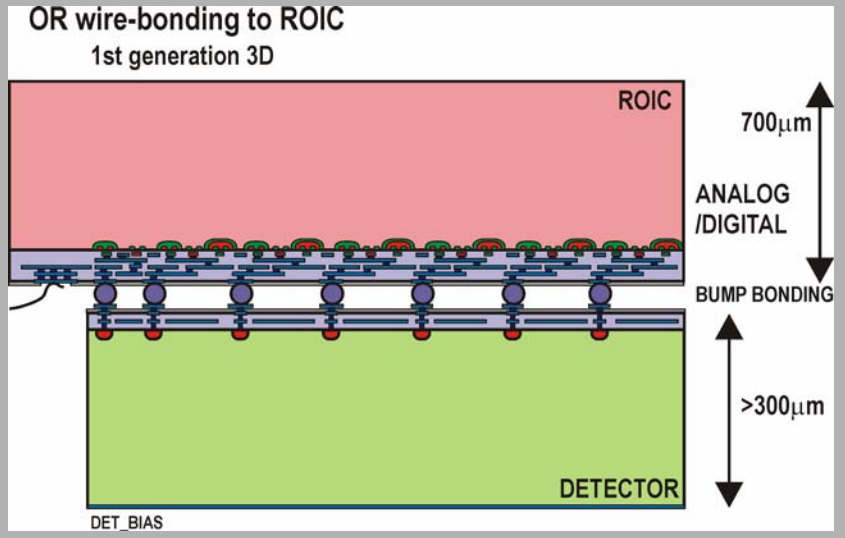
[D. Temple, RTI] 3D chip cross section



3 Tier circuit diagram

→ Fermilab started exploring 3D technologies 2006

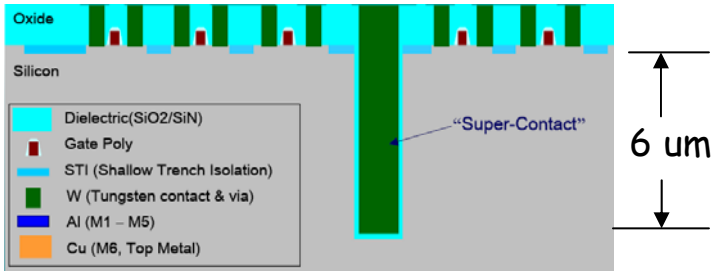
conventional assembly:



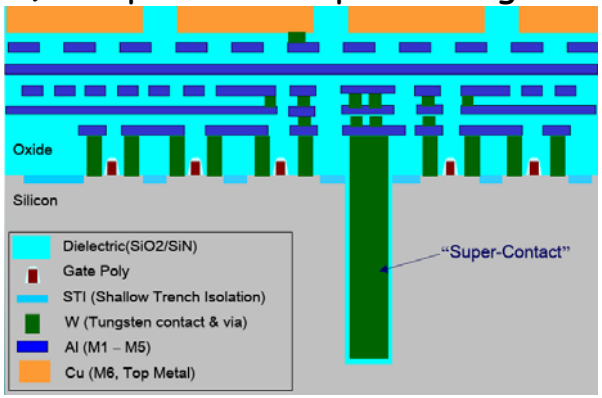
Process Flow for Tezzaron 3D Chip

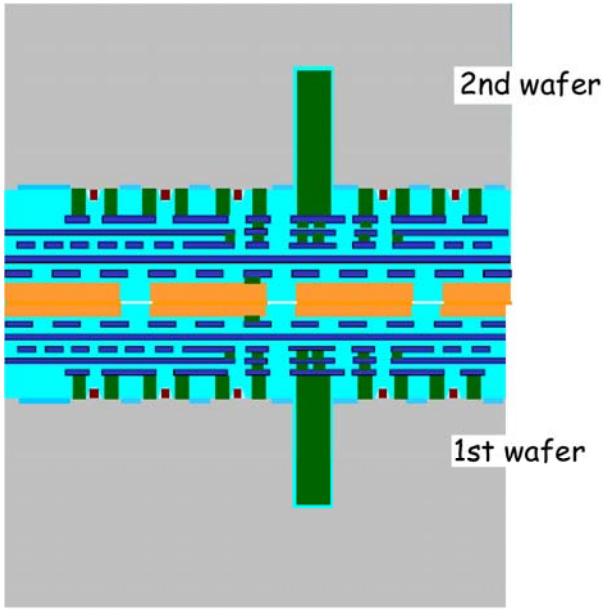
- two tier assembly (additional tiers can be added)
- vias formed just after transistor fabrication (via first), M1 not blocked
- uses Chartered bulk CMOS high volume production process

1) Complete transistor fabrication, form, passivate and fill super via



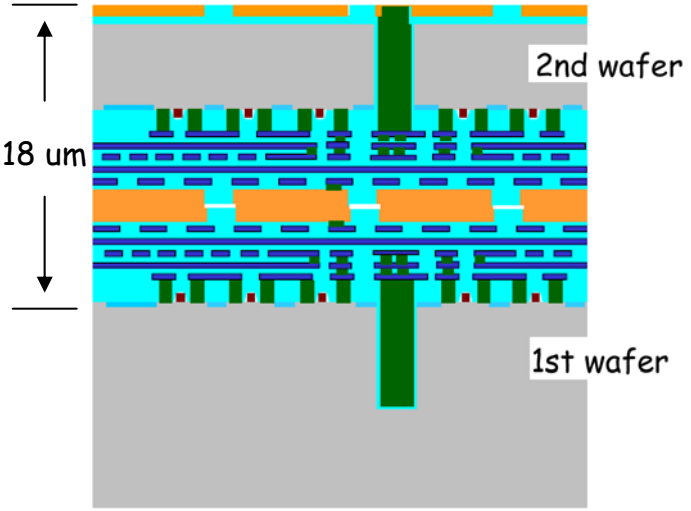
2) Complete BEOL processing





3) Flip 2nd wafer on top of first wafer

Bond 2nd wafer to 1st wafer using Cu-Cu thermo-compression bond

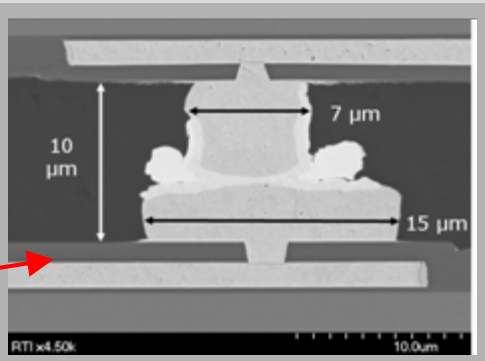


4) Thin 2nd wafer to 12 um to expose super Contact.

Add metalization to back of 2nd wafer for bump or wire bond.

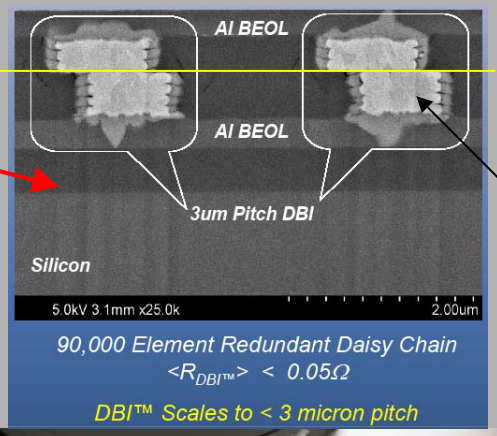
bonding processes for VI

- **3D bonding technology to replace bump bonds in hybrid pixel assemblies.**
- Bonding options being explored by Fermilab:
  - **CuSn eutectic with RTI**
  - **Direct Bond Interconnect (DBI) with Ziptronix. 3 um pitch, wafer to wafer and chip on wafer, relies on oxide bond**
  - **Cu-Cu fusion with Tezzaron**
- Excellent strength and yield obtained with 7 um CuSn pillar on a 20 um pitch. However, 10 um of CuSn covering 75% of bond area would represents Xo=0.075. Too high for some HEP applications.
- CuCu fusion and DBI offer the lowest mass bond required by many HEP experiments.



CuSn bond cross section

20 micron pitch



bond interface

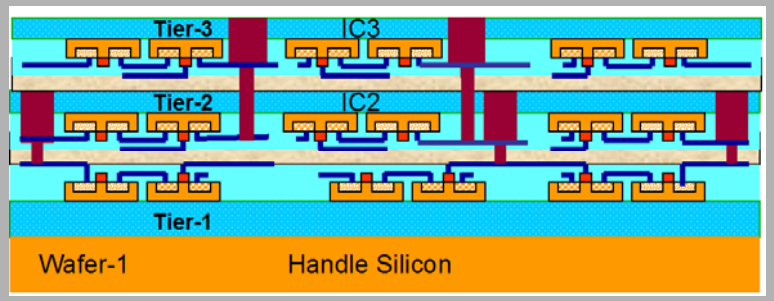
compression bond using 'magic metal'

25 Pixel sensors bonded to BTEV ROIC wafer

Sensors thinned to 100 µm after chip to wafer bonding

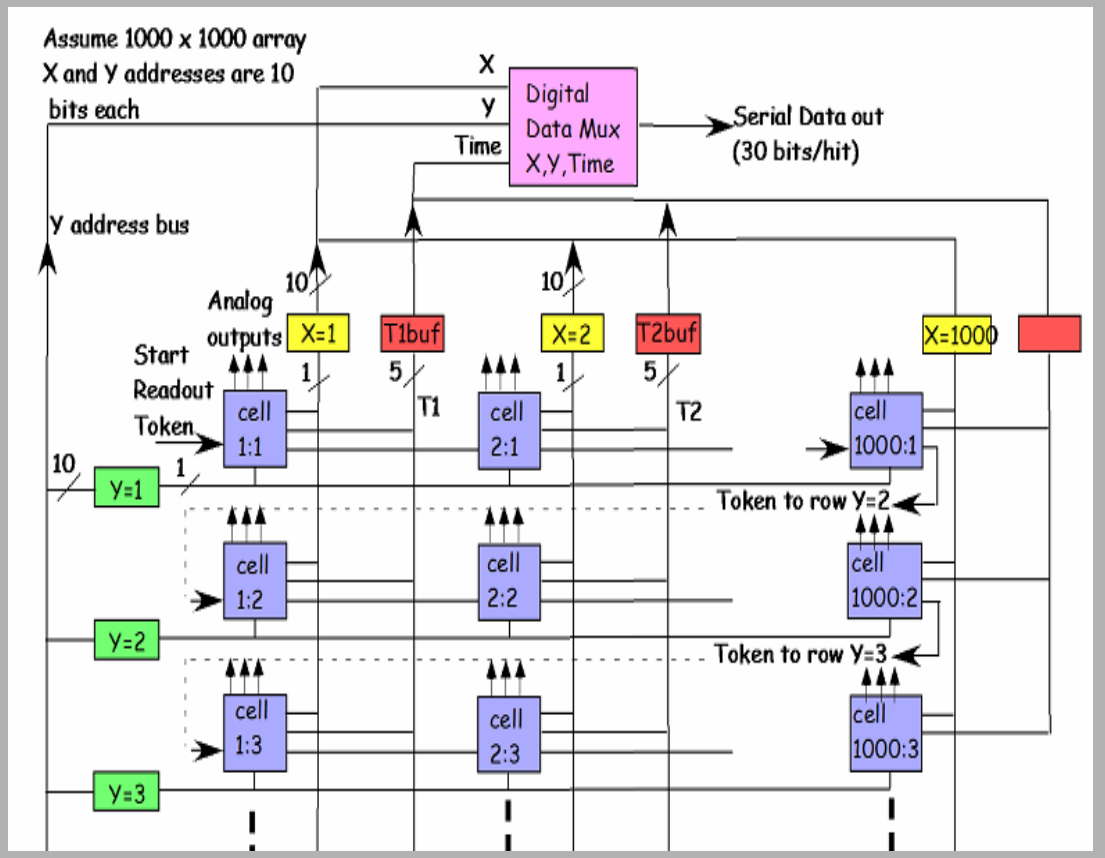
Fermilab's start in 3D-IC: VIP with MIT-LL

- readout between bunch trains
- high speed data sparsification (token passing)
- analog output after CDS
- digital and analog time stamping options: 5-10 bit design (resolution 3-100 BX)
- Test input for every pixel
- 4096 pixel array with 20um pixels,
- scalable to 1 MPix



MIT process: 3 tier, via last, FD SOI

Demonstrator chips for ILC vertex pixels (driven by ILC specs), submitted 2006

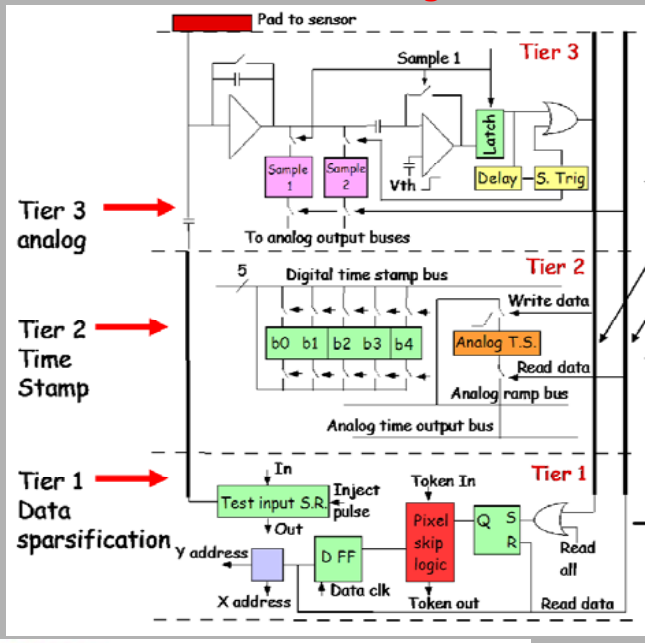


VIP1 Functional block Diagram

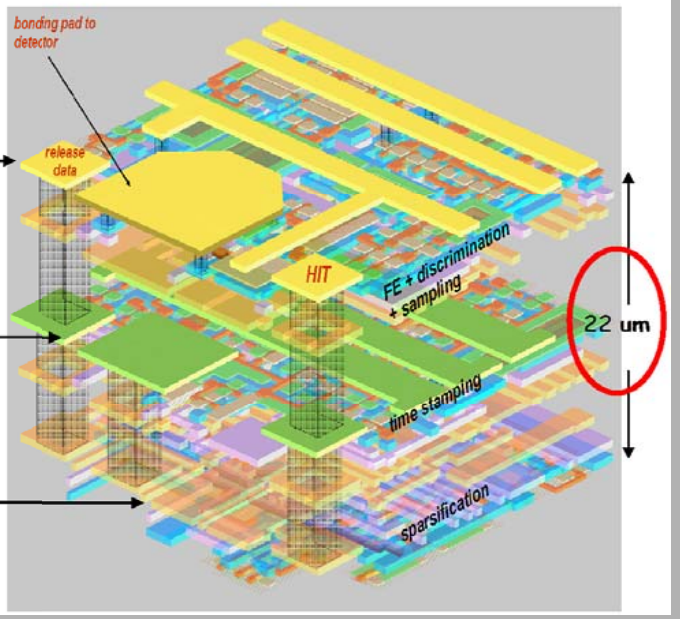
VIP1 and VIP2a with MIT-LL

- VIP1 designed in 3 tier MIT-LL 0.18 um SOI process
- no sensor layer utilized

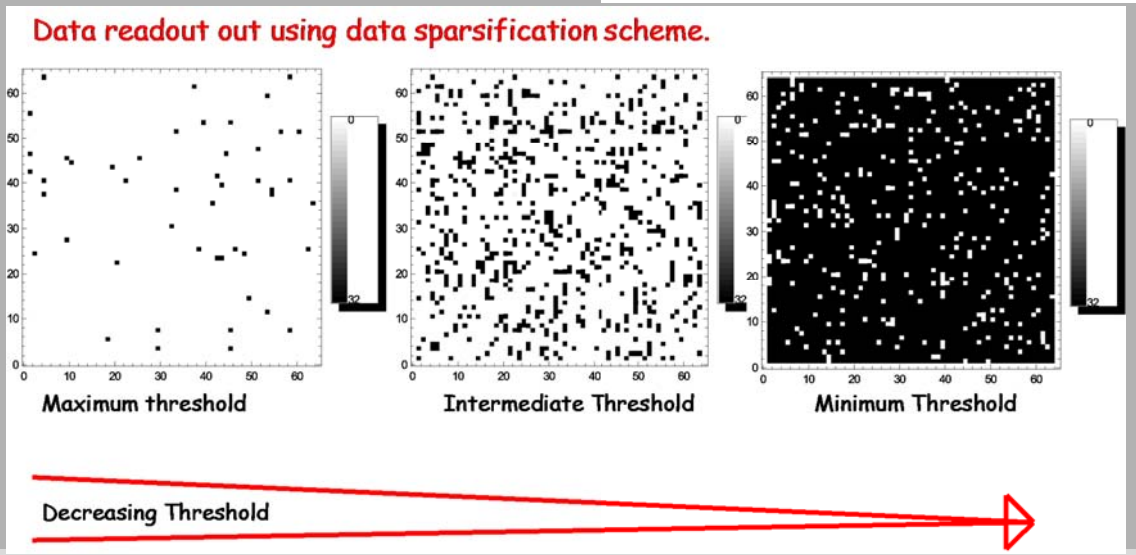
Pixel block diagram



Pixel Layout



VIP1 Test Result



- VIP1 found to be functional.
- VIP1 Yield was low.
- VIP2a designed to improve yield:
  - increased sizes in FD SOI
  - improved power distribution
  - wider traces
  - at expense of larger, 30 um, pixel size
- VIP2a is in fabrication
- Focus has shifted from SOI to CMOS processes

Consortium formed for 3D Design

- Organized by Fermilab (late 2008)
- Benefits
  - Sharing of designs (e.g. ASD from LBNL and DACs from CPPM used in VICTR)
  - Development of special software tools
  - Development of libraries
  - Design reviews
  - Sharing of results
  - Frequent meetings
  - Cost reduction

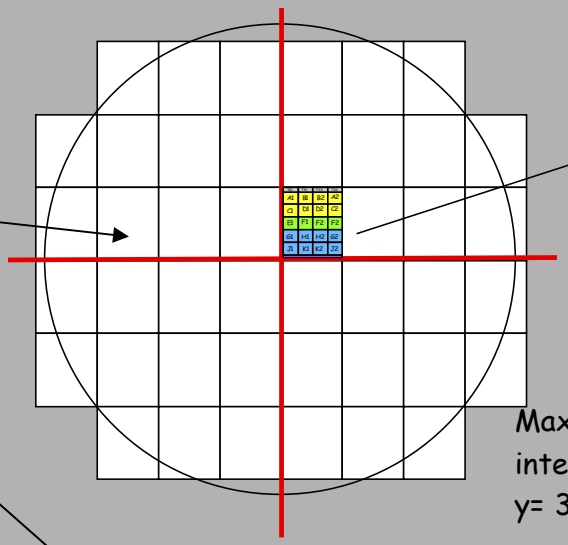
!!!

- First MPW run with Tezzaron closed
- contributions from Fermilab: VIPIC, VICTR, VIP2b (6.3 x 5.5 mm chip size)

- Currently 15 members (others joining)
  - Fermilab, Batavia — USA
  - University at Bergamo — Italy
  - University at Pavia
  - University at Perugia
  - INFN Bologna
  - INFN at Pisa
  - INFN at Rome
  - CPPM, Marseilles — France
  - IPHC, Strasbourg
  - IRFU Saclay
  - LAL, Orsay
  - LPNHE, Paris
  - CMP, Grenoble
  - University of Bonn — Germany
  - AGH University of Science &Technology — Poland

First Tezzaron MPW Run

- Wafers fabricated in **Chartered 0.13 um CMOS process**
- Frame divided into 12 subreticules among consortium members
- One set of masks used for both top and bottom tiers to reduce cost of 2 tier circuit.
  - Identical wafers **bonded face to face** by Tezzaron.
  - Backside metallization by Tezzaron.
- **More than 25 separate designs** (circuits and test devices)
  - sLHC: CMS strips, ATLAS pixels
  - ILC pixels
  - B-factory pixels
  - X-ray imaging
  - Test circuits
    - Radiation damage, SEU tolerance
    - Cryogenic-T operation
    - Via and bonding reliability and yield

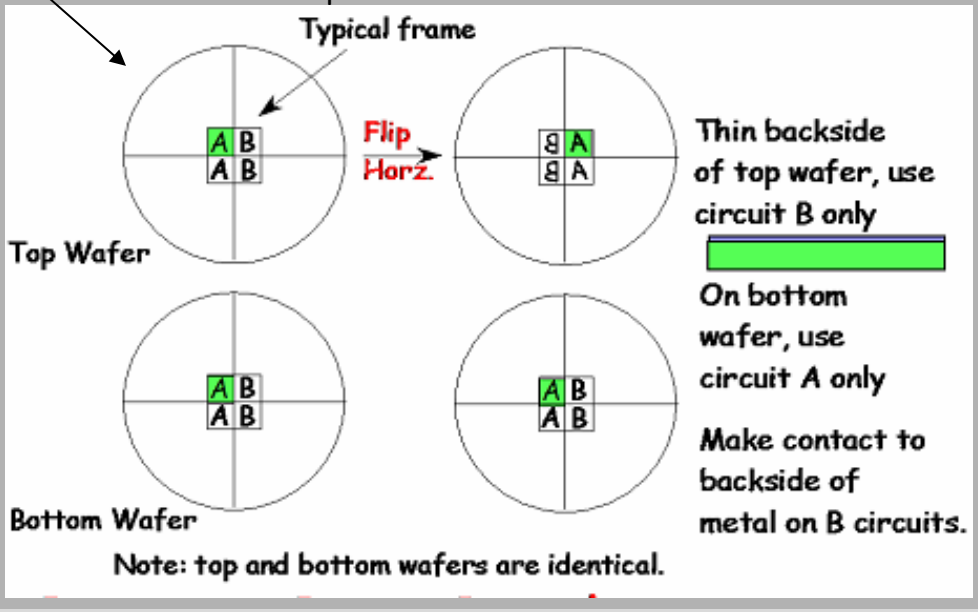


Wafer Map

TX1	TY1	TY2	TX2
A1	B1	B2	A2
C1	D1	D2	C2
E1	F1	F2	F2
G1	H1	H2	G2
J1	K1	K2	J2

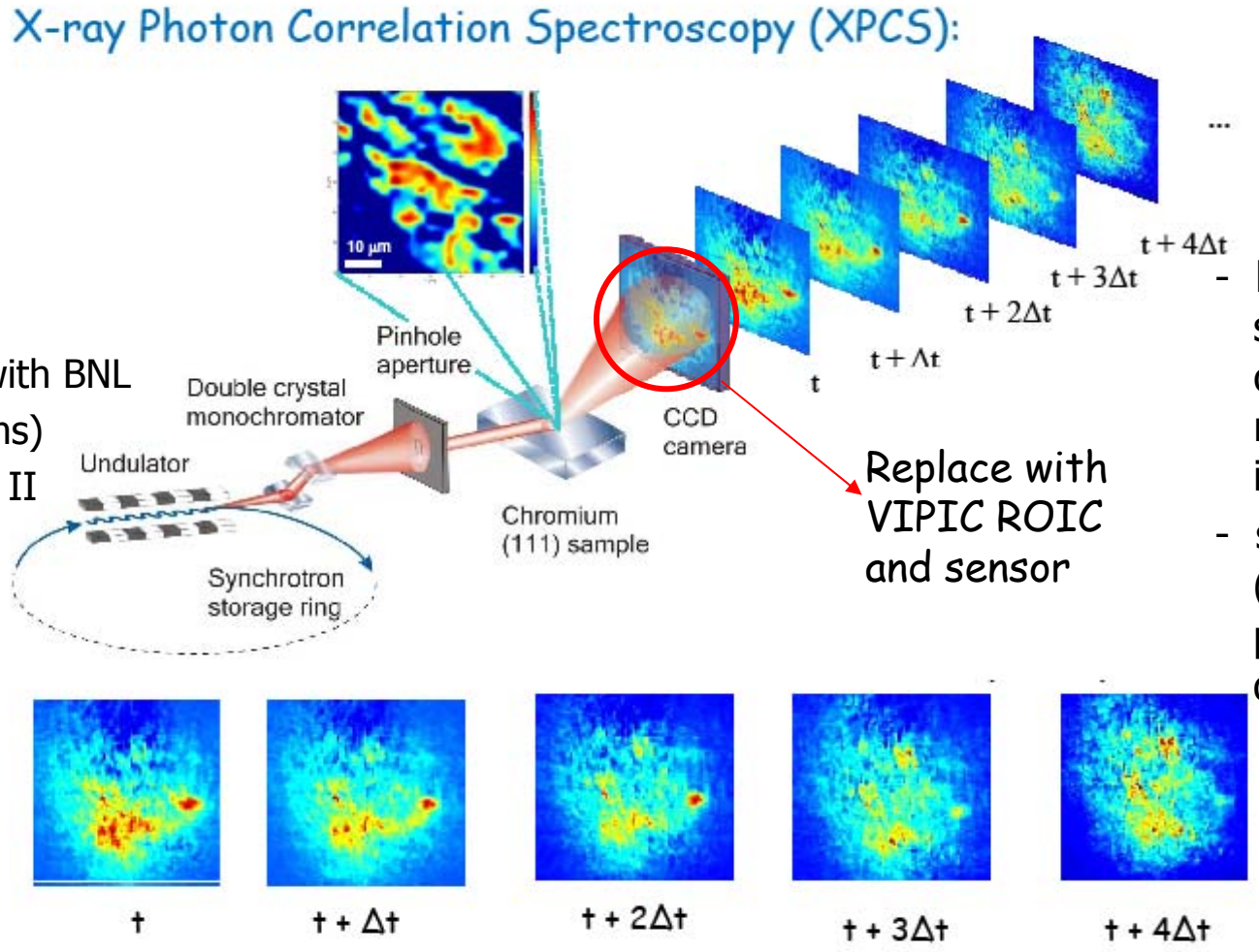
Frame layout

Max frame layout area including internal saw streets: x=25.760 mm y= 30.260 mm.



XPCS project (VIPIC chip)

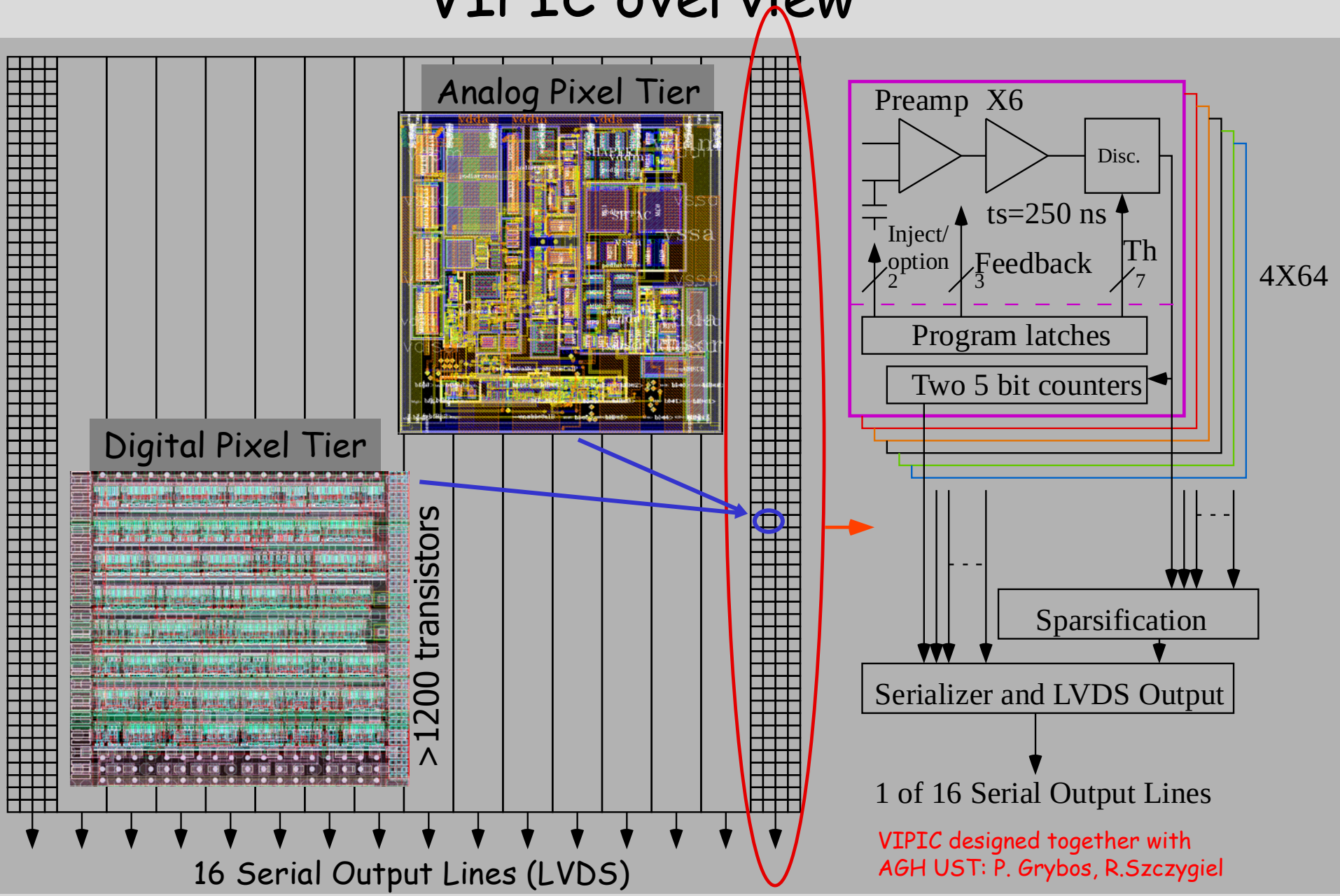
project with BNL (P.Siddons) for NSLS II



O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

- based on generating s*peckle pattern* by scattering of coherent X-rays from a material where spatial inhomogeneities are present
- studies *dynamics of materials* (e.g. diffusion constants, phase transformations, domain relaxation times)

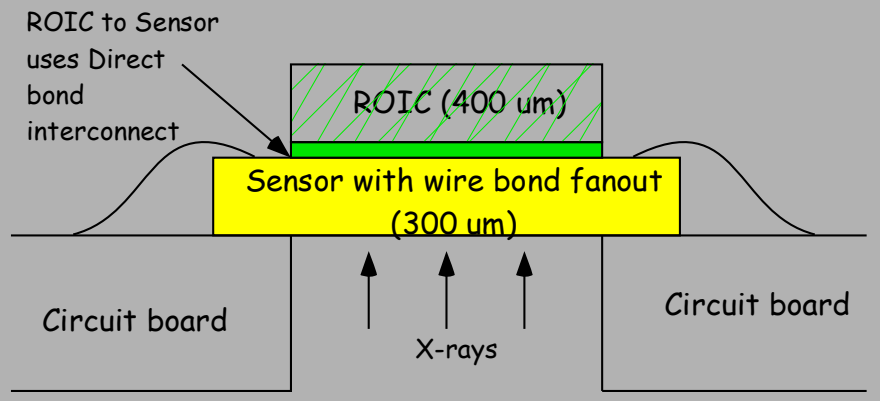
VIPIC overview



VIPIC designed together with
AGH UST: P. Grybos, R.Szczygiel

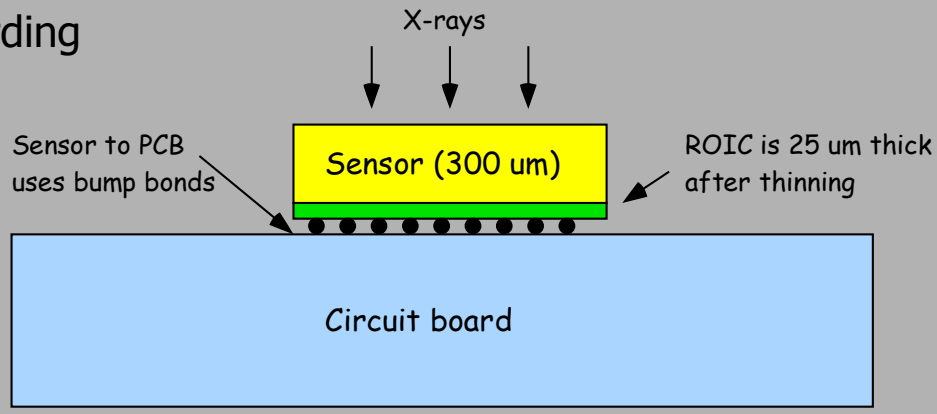
VIPIC (Vertically Integrated Photon Imaging Chip)

- **Specifications**
  - 64 x 64 array of 80 micron pixels
  - Dead timeless, triggerless operation
  - Sparsified data readout
  - Binary readout (no energy information)
  - High speed frame readout time
    (10 us. min, occupancy 100 photons/cm2/usec)
  - Optimized for photon energy of 8keV



Option 1 - Less Aggressive Mounting

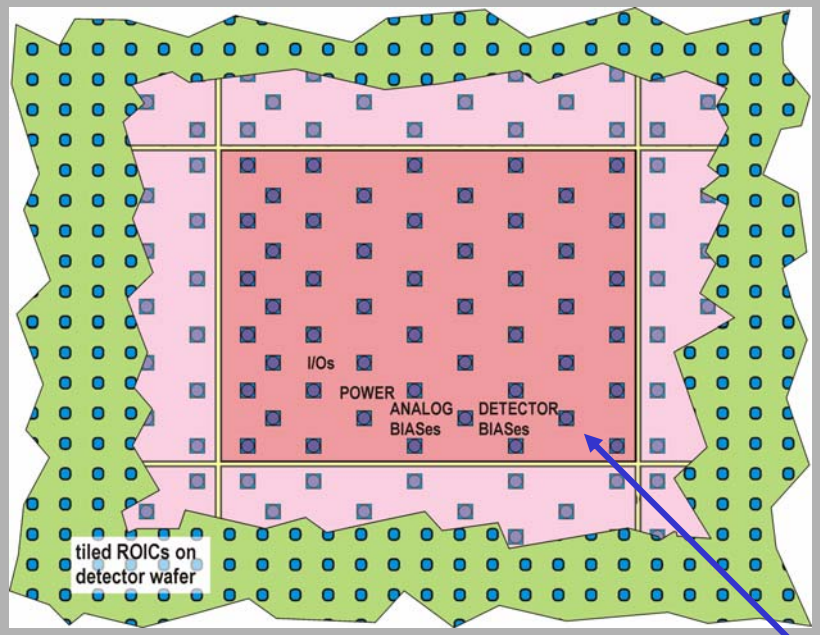
- **Features (5.5 x 6.3 mm die size)**
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Address generated by circuit using binary tree architecture <5ns
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tiers, separate analog and digital sections
  - Adaptable to 4 side buttable X-ray detector arrays

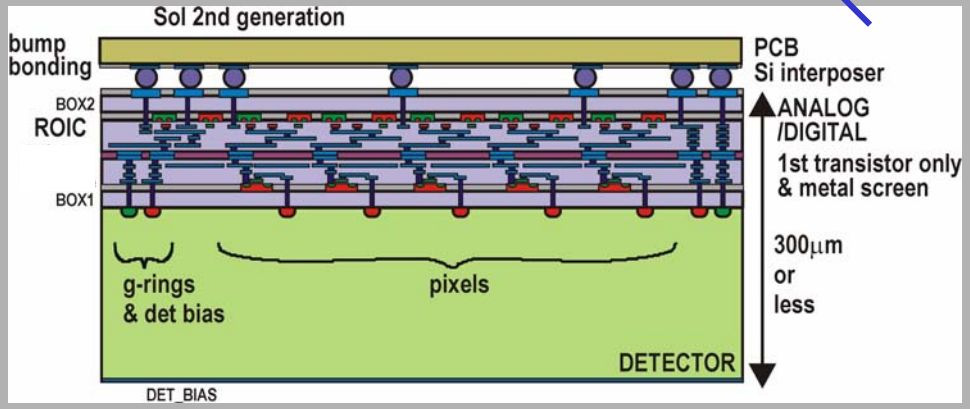


Option 2 - More Aggressive Mounting
for four side buttable sensor arrays

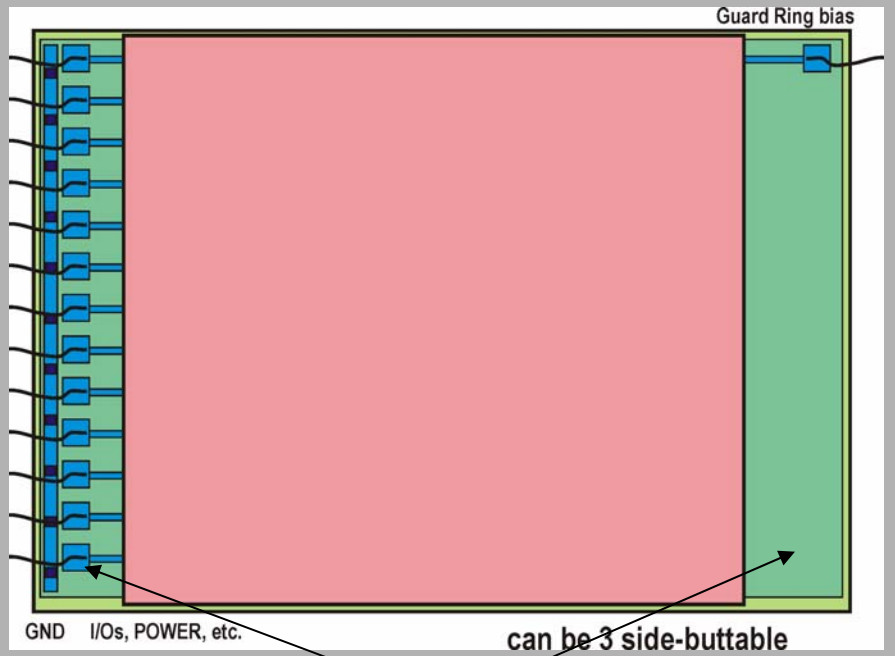
VIPIC mounting

top view - 4 side buttable assembly



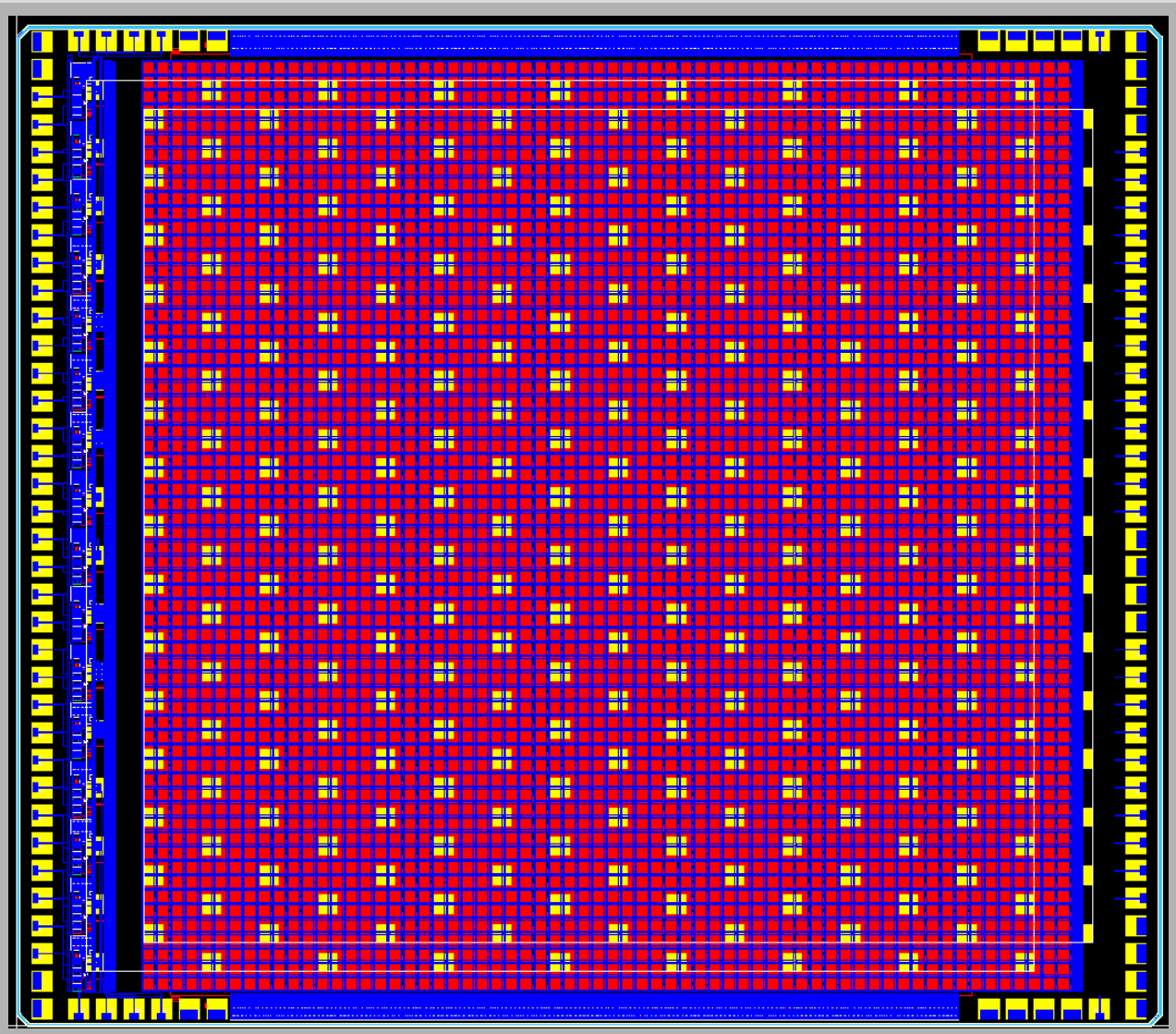


vs. conventional setup:



⇒ large sensor area with uniform power distribution

Backside bump bonding for VIPIC



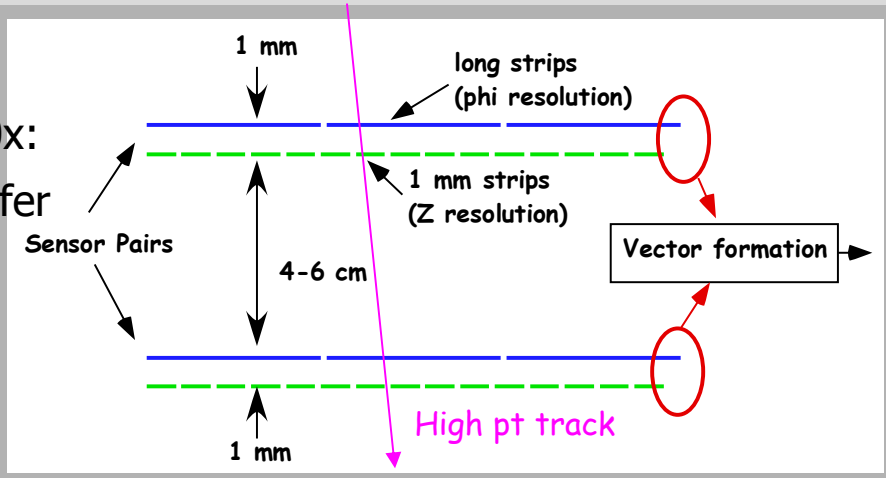
Digital Tier Layout with pads for detector fanout and backside bump bonding

VICTR (tracker/trigger for sCMS)

- increase of luminosity in sLHC to the planned 10^{35} $cm^{-2}s^{-1}$

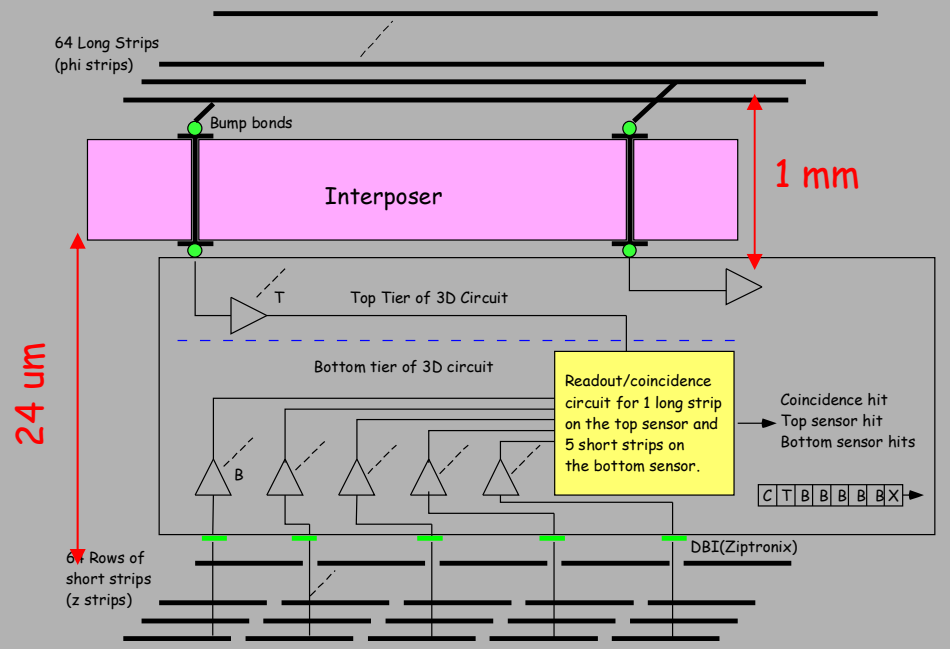
requires **L1 trigger** in tracking layers to reduce data 100-200x:

- identify hits associated with pt above 2 GeV for data transfer
- identify high pt tracks with pt above 15-25 GeV
- provide good Z vertex resolution of about 1mm for tracks above 2 GeV



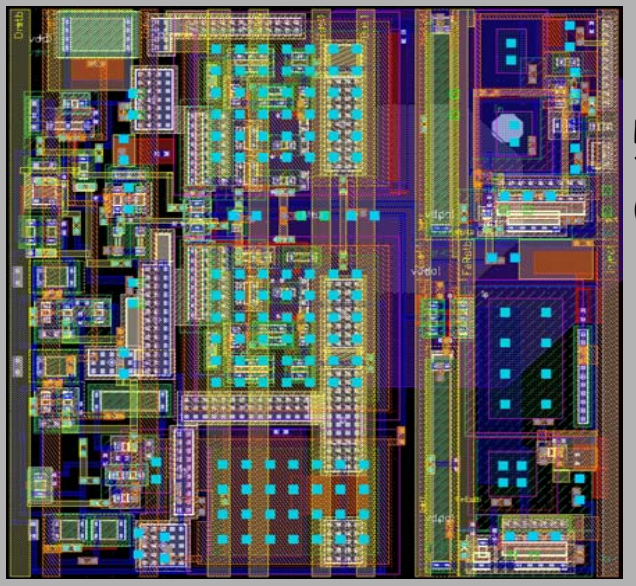
- **pair of sensor planes** with about 1mm separation and VICTR **(Vertically Integrated CMS Tracker**) chip
  - Locally collect hits from both sensors
  - Finds hit pairs with pt>2GeV
  - Transfers data to vector forming circuit
- **Vector forming circuit**
  - Locally collect hit pairs >2GeV from two barrels of detector modules
  - Form track vectors for identification of high pt tracks
  - Rejects track vectors with low pt to further reduce data rate before transferring data off the detector

Simplified Functional View of CMS Demonstrator Chip

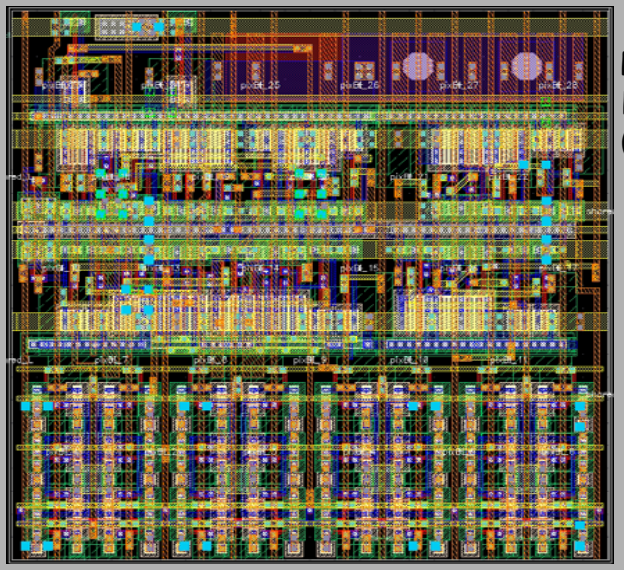


VIP2b

- sensors unders separate fabrication
  thick sensors: collaboration with BNL,
  thin sensors: planned run with XFAB
- Based on VIP1 and 2a with changes:
  - Converted 3 tier design to 2 tiers
  - Removed analog time stamping
  - Increased digital time stamp
    from 5 bits to 8 bits for ~3.9 us resolution
  - Switch for collection of h+ or e-
  - Larger array 192 x 192
  - Pixel size increased to 24 um to accommodate extended digital time stamp and maintain sampling of analog data on MiM capacitors.
- Expect better yield from commercial CMOS process
- Expect better radiation tolerance (compared to SOI)
- (VIP2b designed in 2 tier Tezzaron/Chartered 0.13 um bulk CMOS process)



Pixel
Top Tier
(analog)



Pixel
Bottom tier
(digital)

Summary / Outlook

- Two different processes for replacement of conventional solder bump bonds demonstrated.

  The lower cost **CuSn technology (RTI)** was shown to work at a pitch of 20 um and has better yield and strength than PbSn.

  DBI (Ziptronix) is a higher cost process but has much lower mass and pitch (3 um), and has greater strength for post bond thinning.

- Fermilab has been working with two different vendors for 3D chip fabrication. **MIT LL** (SOI process) and **Tezzaron** (CMOS process) with Cu-Cu bonding.

- International consortium of 15 HEP institutions to develop 3D chips formed.

  The first MPW run to Tezzaron is closed and ready for fabrication.

- Designs from Fermilab for ILC pixels, CMS strips, and X-ray imaging were described showing the range of opportunities for 3D circuits in instrumentation.

Backup slides

ziptronix

3D IC Company

DBI® Process Flow

1) **Starting Wafer**
   - Planar Surface
   - Exposed Filled Vias (W or Cu)

2) **Deposit Seed**

3) **Pattern / Plate DBI® Metal (Ni)**

4) **Blanket Etch Seed**

5) **Oxide Deposition**
   - Oxide Bonding Mechanical Spec < 0.5nm

6) **Planarization**

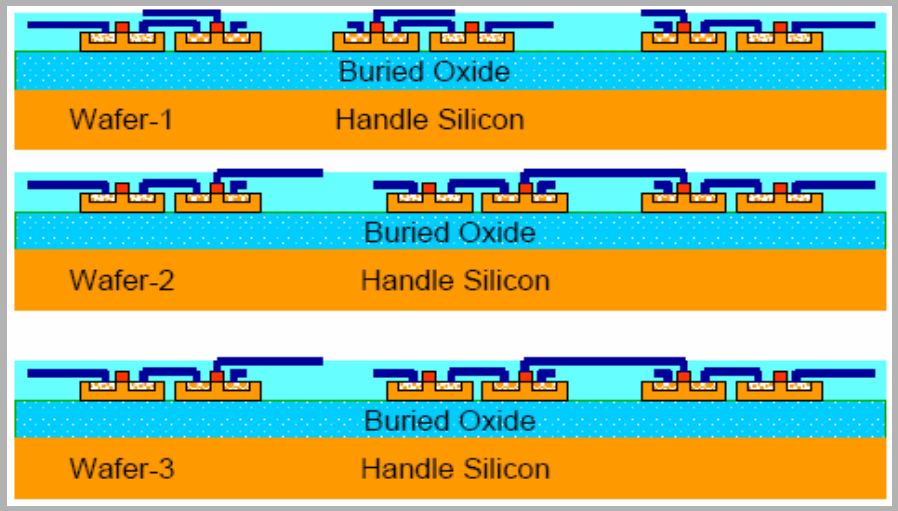
3D Interconnect Characteristics

	SuperVia™	SuperContact™	SuperContact™	Bond Points	Chip to Wafer
	Via First, BEOL	200mm Via First, FEOL	300mm Via First, FEOL		
Size L X W X D Material	4.0 μ X 4.0 μ X 12.0μ Cu	1.2 μ X 1.2 μ X 6.0μ W	1.6 μ X 1.6 μ X 10.0μ W	1.7 μ X 1.7 μ Cu	10 μ X 10 μ Cu
Minimum Pitch	6.08 μ	<2.5 μ	<3.2 μ	2.4 μ	25 μ
Feedthrough Capacitance	7fF	2-3fF	6fF	<<	<25fF
Series Resistance	<0.25 Ω	<0.6 Ω	<1.5 Ω	<	<

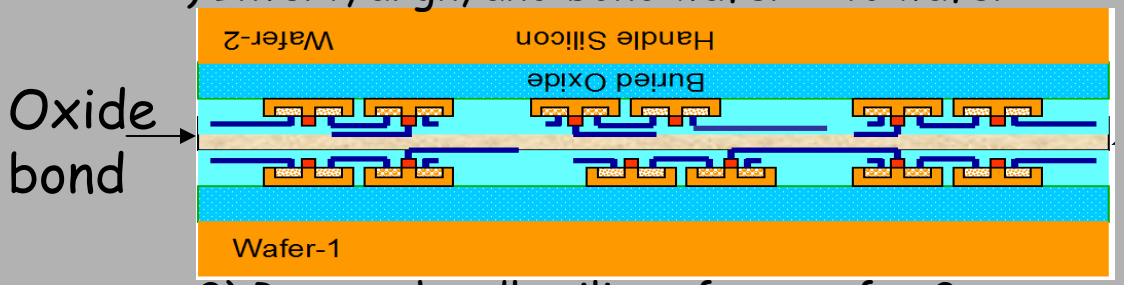
Process Flow for MIT LL 3D Chip

- 3 tier chip (tier 1 may be CMOS)
- Vias formed after FEOL and BEOL processing is completed

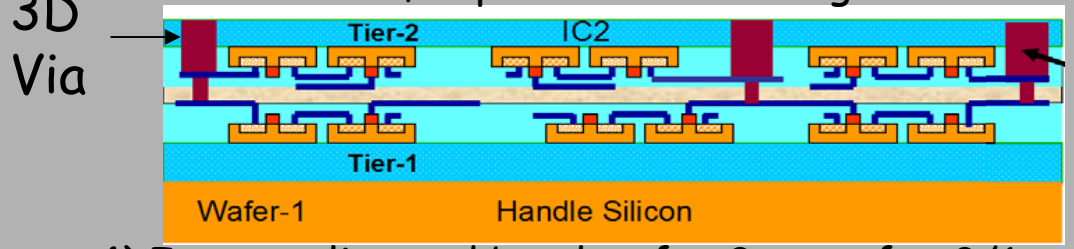
1) – fabricate individual wafers



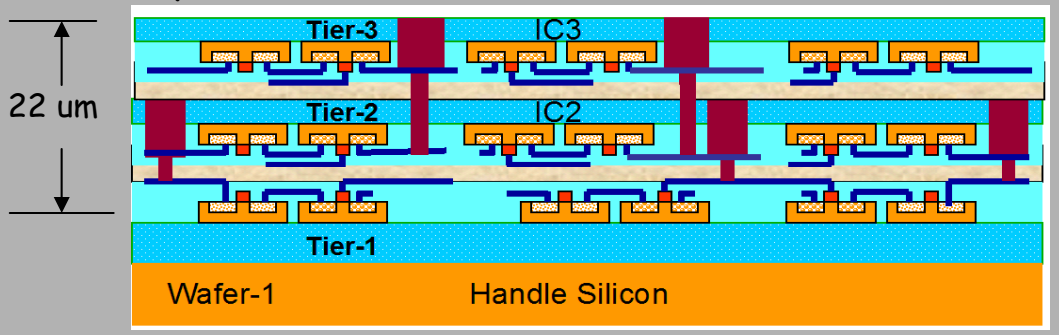
2) Invert, align, and bond wafer 2 to wafer 1



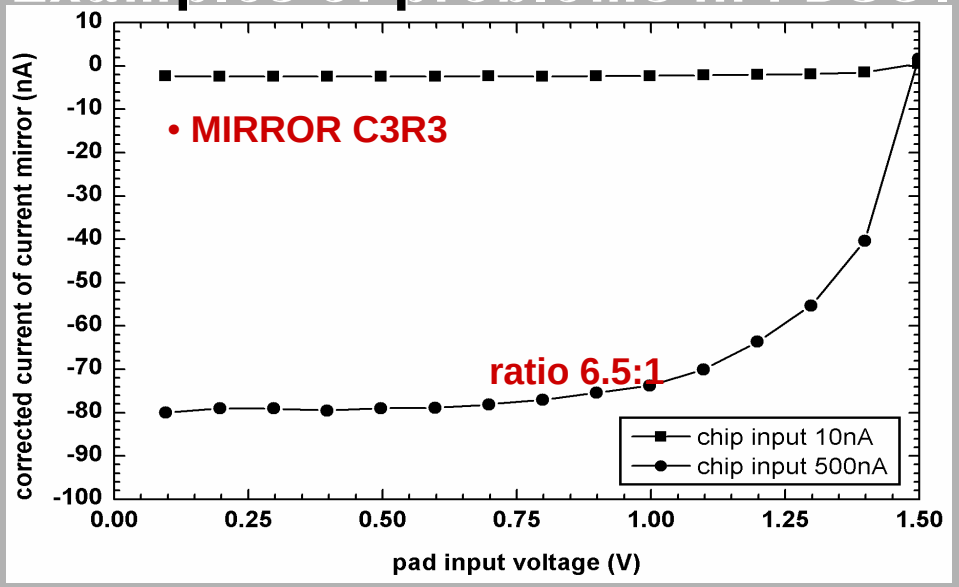
3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



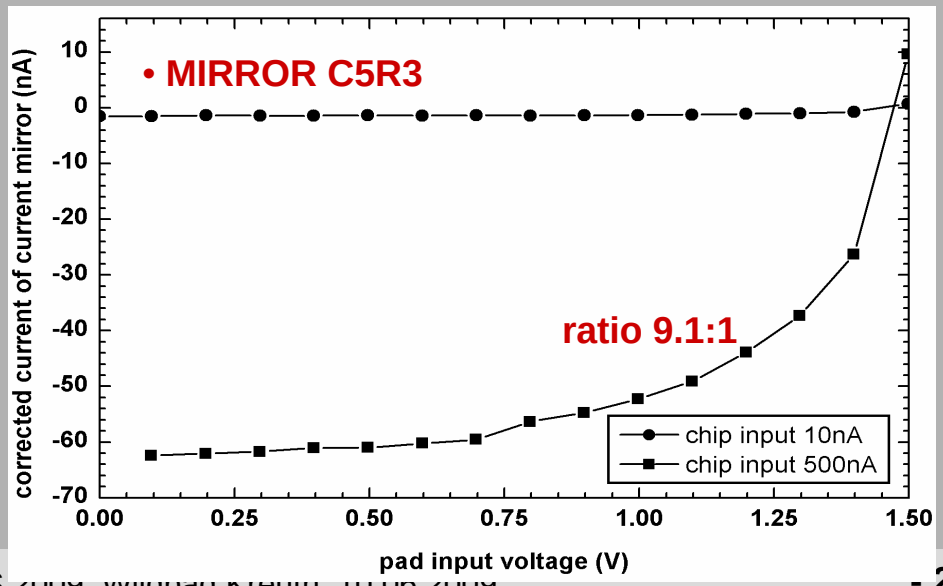
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3

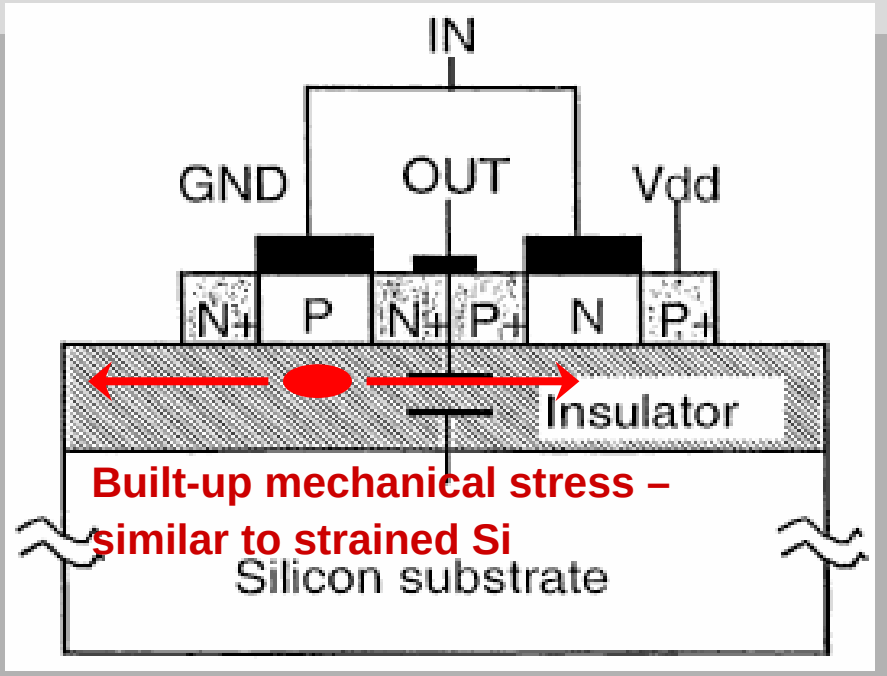


Examples of problems in FDSOI:



designed mirror ratio 10:1





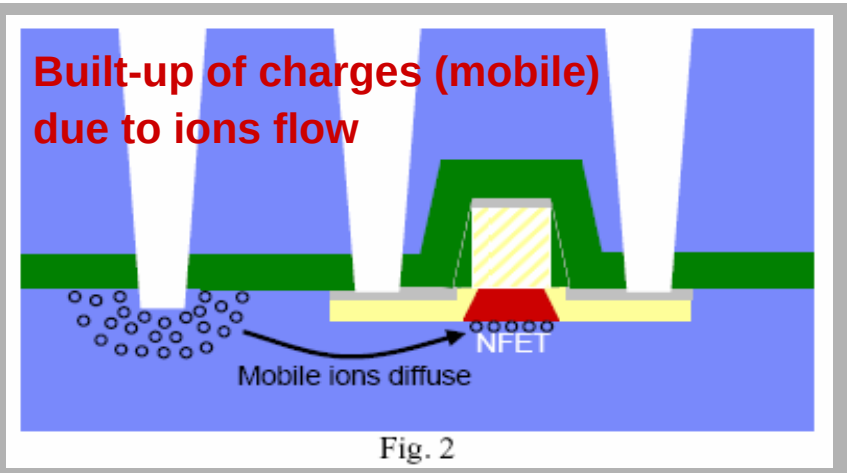


Fig. 2

M. Connell, et all. Impact of Mobile Charge on Matching Sensitivity in SOI Analog Circuits, 2007 IEEE/SEMI Advanced Semiconductor Manufacturing Conference

Examples of problems in FDSOI:

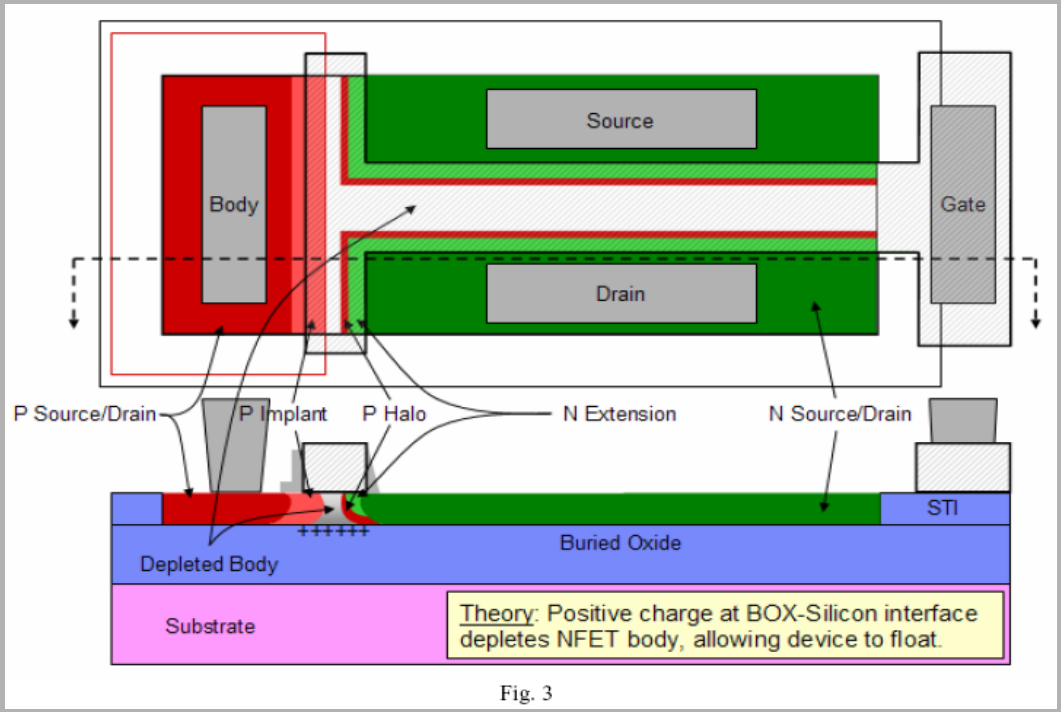


Fig. 3

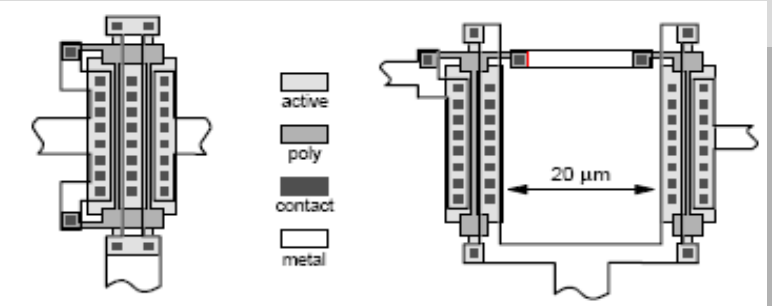


Figure 2: Shared source and separated mirror layouts.

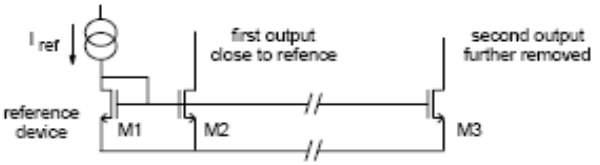
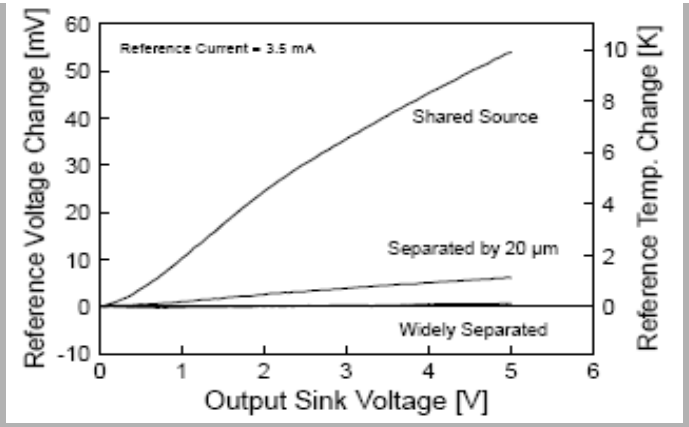


Figure 4: Schematic of current mirror with dual outputs.



Poor quality of transistor bulk contacts, even using so called H-gate transistors; due to charge accumulation in oxide bulk is floating

Self heating of tranistorsdue to poor heat transfer and varying power dissipated on both sides of current mirrors

B M Tenbroek, et al., Drain current mismatch in SOI CMOS current mirrors and D/A converters due to localised internal and coupled heating