Single Event Upset Tolerance in IBM 0.13μm

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Introduction

- A continuation of the experimentation that began several years ago with TSMC's 0.25μm process.
- Troubles ahead?
- Recent evidence indicates that 0.25um might have been the optimal SEU tolerant technology
- "Soft Error Rate Increase for New Generations of SRAMs", Granlund, Granborn and Olsson, IEEE Trans. Nucl. Sci., Vol 50, No. 6, Dec. 2003, pp. 2065-2068

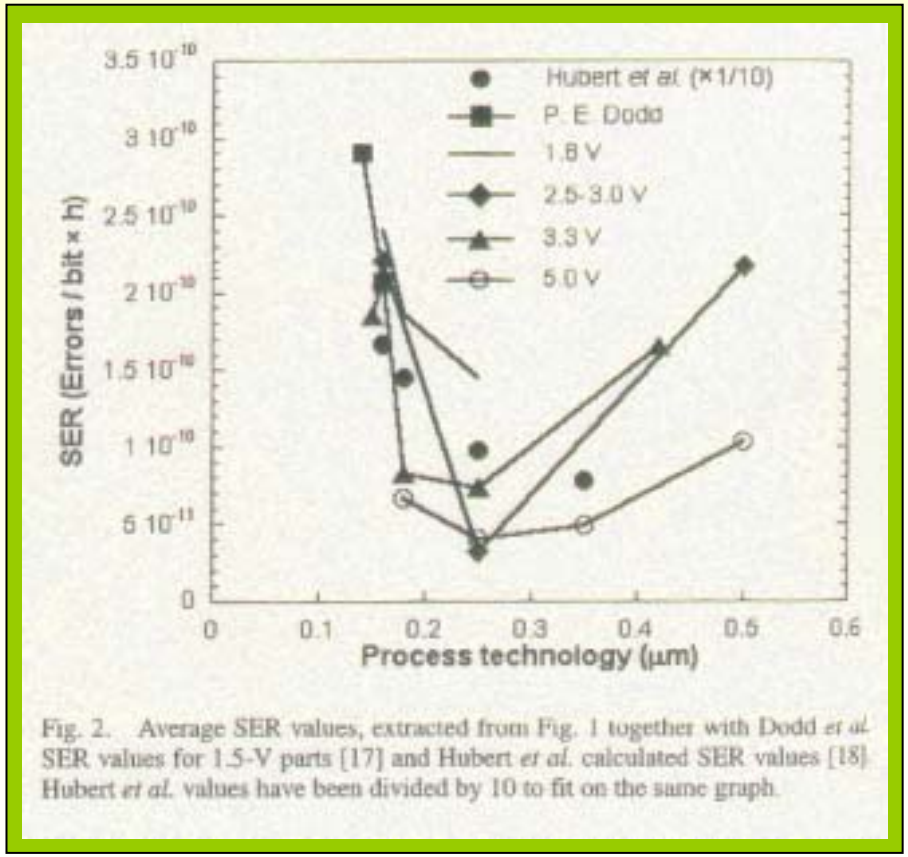


Fig. 2. Average SER values, extracted from Fig. 1 together with Dodd *et al.* SER values for 1.5-V parts [17] and Hubert *et al.* calculated SER values [18]. Hubert *et al.* values have been divided by 10 to fit on the same graph.

Introduction

- Each type is configured as Master-Slave type positive-edge triggered D-flip-flop.
- Each flip-flop is arrayed as a 1xN shift register.
- The shift registers are supplied by a common input and controlled by a common clock. Their outputs are selected by a multiplexor and driven through a common output.
- All inputs and outputs are LVDS.

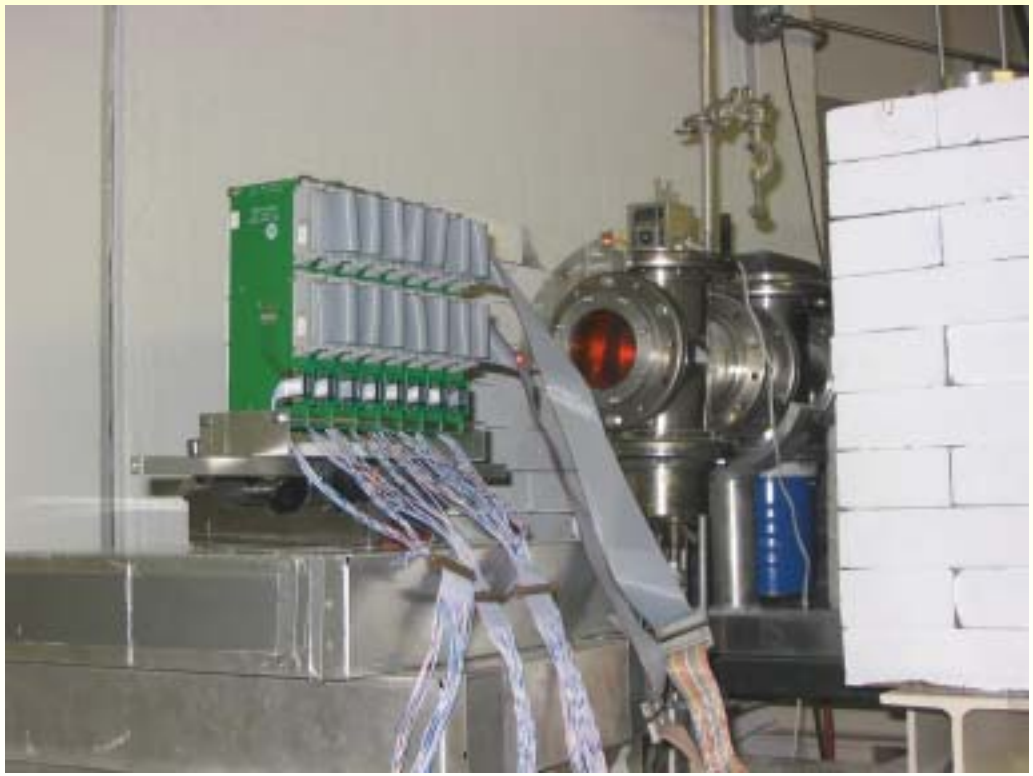
Registers Tested

Type	Transistor Geometry	Notes
LBL Dice	Enclosed	DICE cell (t-gate dice latch) designed and laid out by LBL
RT Dice[1]	Enclosed	Pure 12-transistor DICE cell (Cern)
RT Seuss	Enclosed	Seuss cell (Fermilab) SEU tolerant SR-flip-flop
RT SR-ff	Enclosed	D-latches created from standard SR-flip-flops
RT normal	Enclosed	D-latches created from cross-coupled inverters
TR Seuss	Rectangular	Triple-redundant, EDC latches
TR SR-ff	Rectangular	Triple-redundant, EDC latches
Hit [2]	Rectangular	"Heavy Ion Tolerant" cell
Liu [3]	Rectangular	Classic Liu-Whittaker cell
Dice[1]	Rectangular	Pure 12-transistor DICE cell
Seuss	Rectangular	Seuss cell (Fermilab) SEU tolerant SR-flip-flop
SR-ff	Rectangular	D-latches created from standard SR-flip-flops
Artisan	Rectangular	Normal flip-flop from the Artisan 0.13μm library
Normal	Rectangular	D-latches created from cross-coupled inverters

Device Under Test

Tests performed at the Indiana University Cyclotron Facility.

200 MeV Protons



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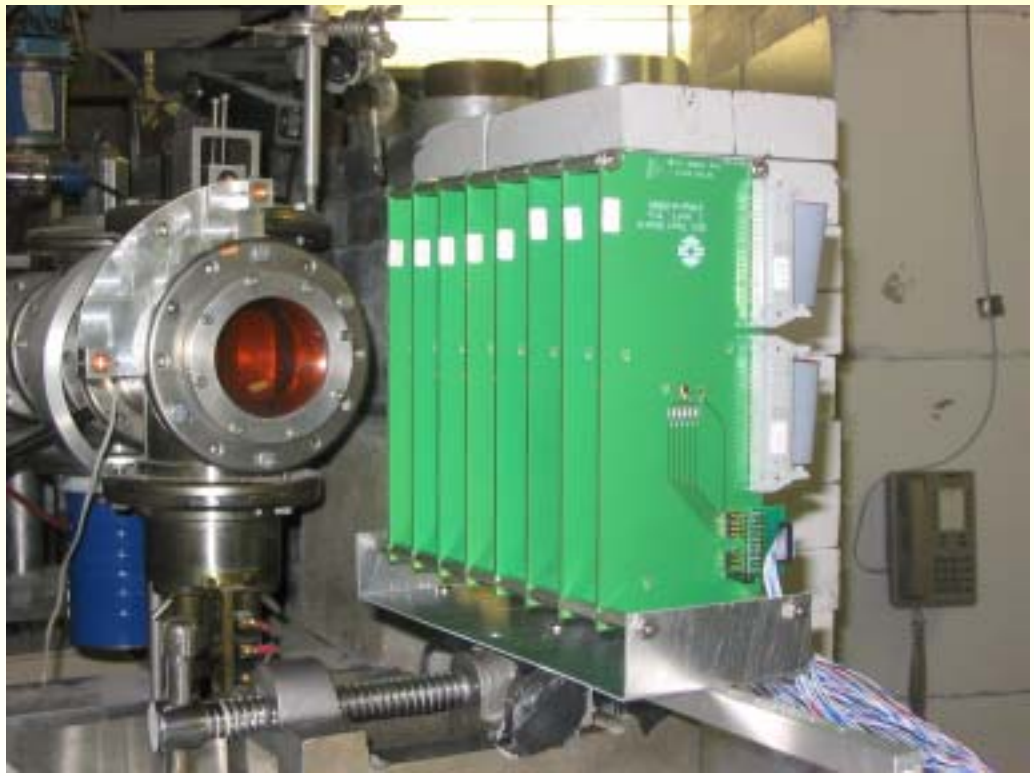
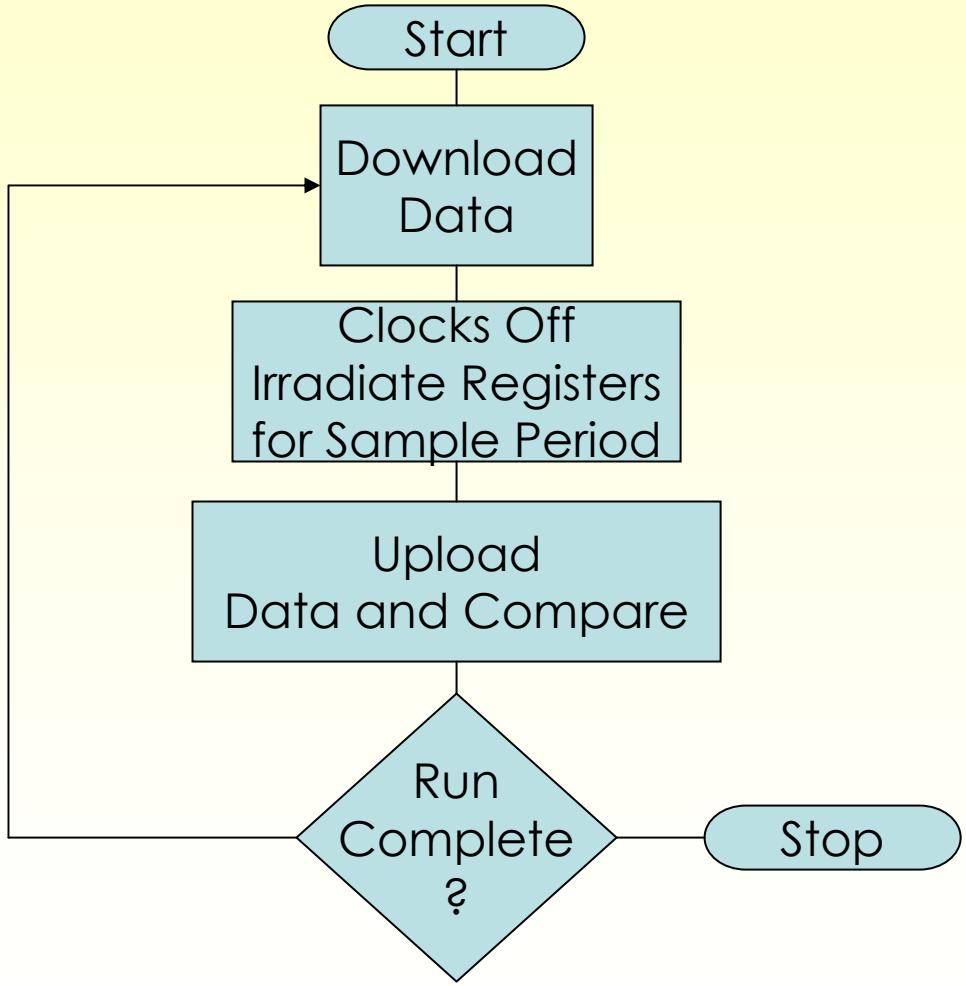


Experimental Flow

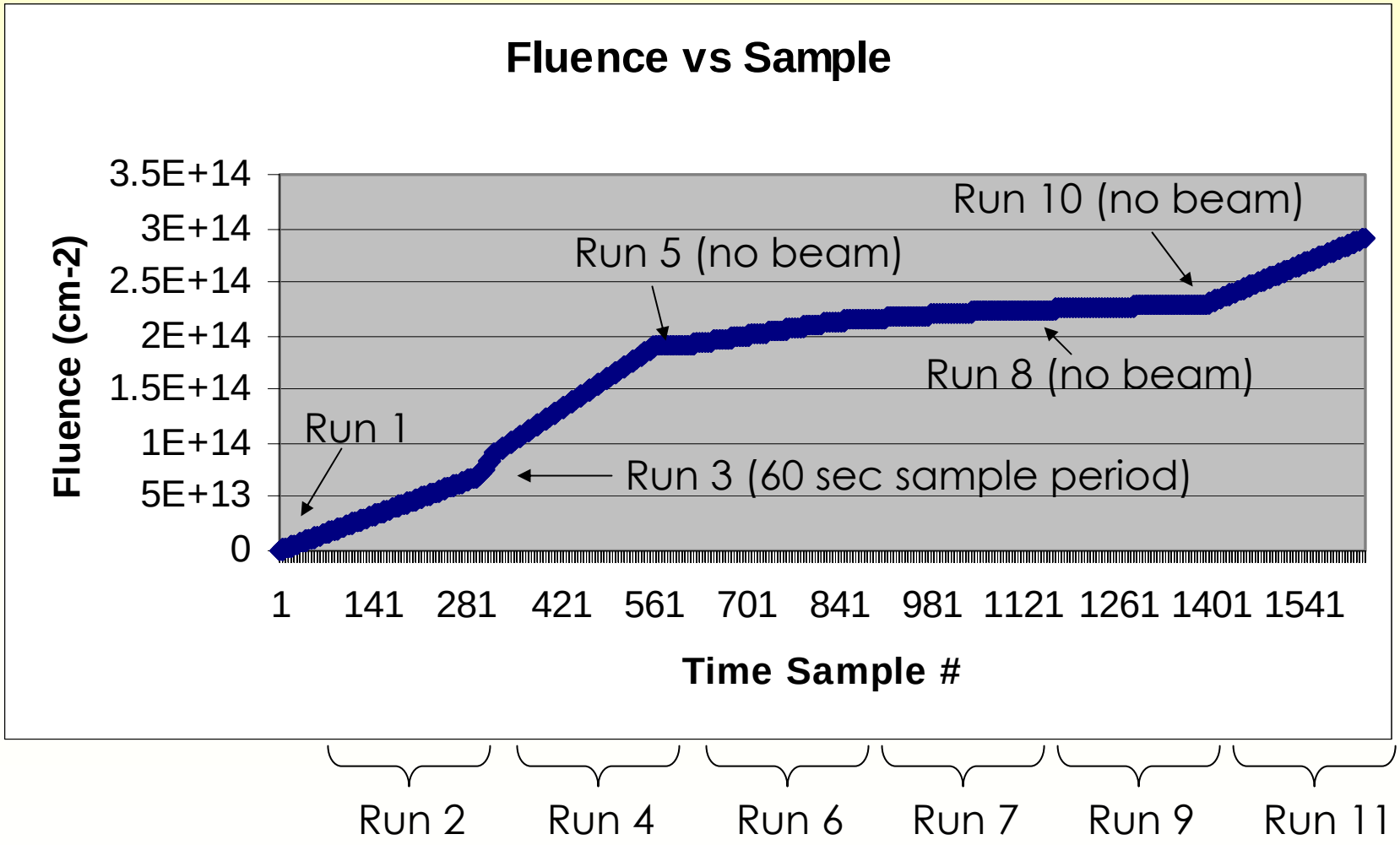
	Pattern
1	0000 0000
2	1000 1000
3	1100 1100
4	1110 1110
5	1111 1111
6	1010 1010
7	0101 0101
8	1111 1111
9	0111 0111
10	0011 0011
11	0001 0001
12	0000 0000



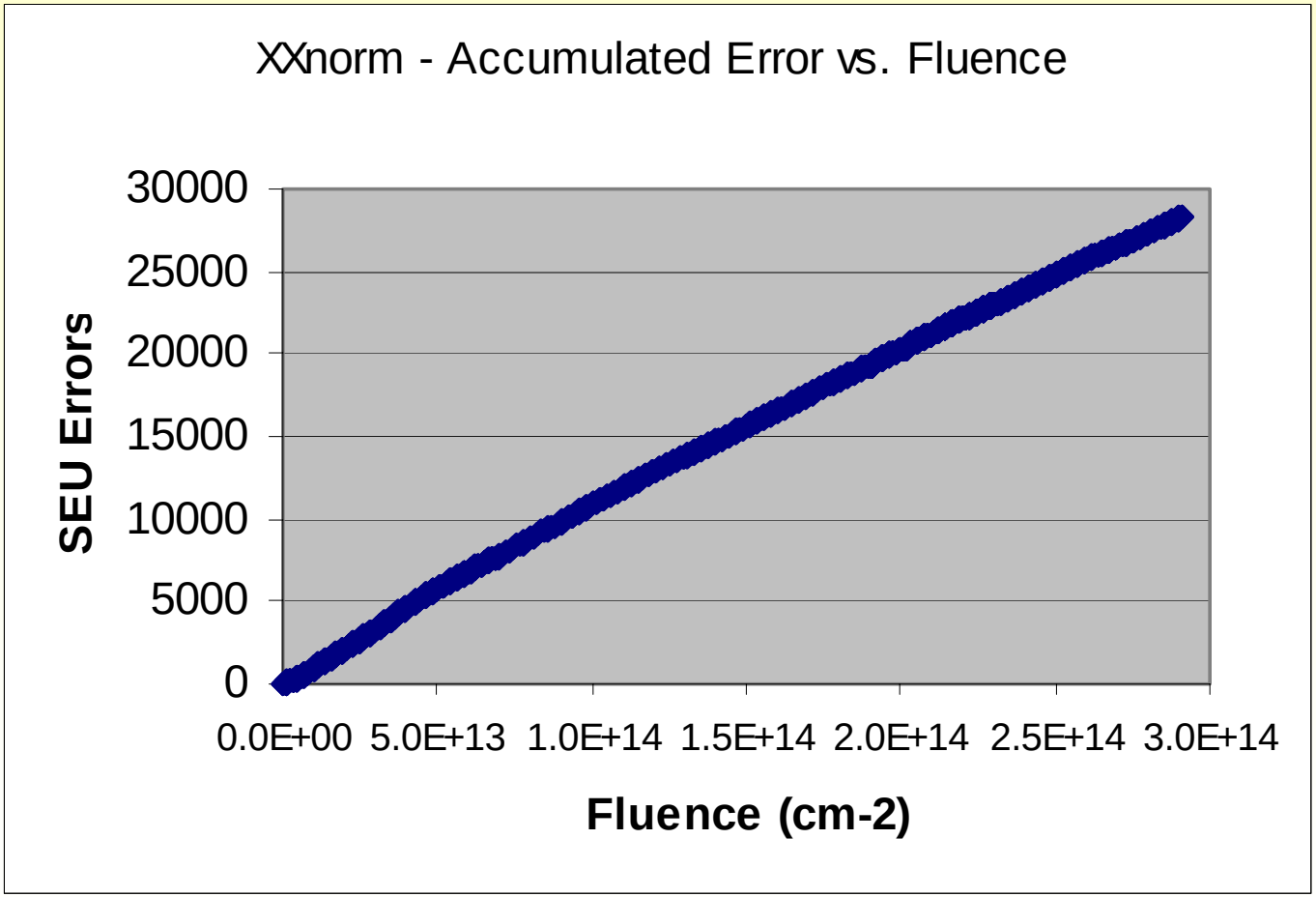
Runs

#	Duration	Flux	Sample Period
Warm-up	36 hours	No beam	3 minutes
Run 1	15 minutes	1.57e10 cm^{-2} sec^{-1}	15 seconds
Run 2	60 minutes	1.53e10 cm^{-2} sec^{-1}	15 seconds
Run 3	24 minutes	1.47e10 cm^{-2} sec^{-1}	60 seconds
Run 4	60 minutes	2.76e10 cm^{-2} sec^{-1}	15 seconds
Run 5	9 minutes	No beam	15 seconds
Run 6	60 minutes	1.57e10 cm^{-2} sec^{-1}	15 seconds
Run 7	60 minutes	0.65e10 cm^{-2} sec^{-1}	15 seconds
Run 8	9 minutes	No beam	15 seconds
Run 9	60 minutes	0.15e10 cm^{-2} sec^{-1}	15 seconds
Run 10	9 minutes	No beam	15 seconds
Run 11	60 minutes	1.70e10 cm^{-2} sec^{-1}	15 seconds

Fluence as a function of Run



Errors vs Fluence



More

Results (200 MeV Protons)

Type	Errors	Cross Section
LBL Dice	14 (4↓ + 10↑)	3.84e-17 cm^2/bit
RT Dice	8 (1↓ + 7↑)	5.86e-17 cm^2/bit
RT Seuss	118 (65↓ + 53↑)	1.03e-15 cm^2/bit
RT SR-ff	6323 (2576↓ + 3747↑)	3.85e-14 cm^2/bit
RT normal	5888 (243↓ + 5645↑)	3.23e-14 cm^2/bit
TR Seuss	854 (0↓ + 854↑)	4.7e-15 cm^2/bit
TR SR-ff	1561 (7↓ + 1554↑)	8.91e-15 cm^2/bit
Hit	290 (280↓ + 10↑)	1.59e-15 cm^2/bit
Liu	49 (32↓ + 17↑)	2.69e-16 cm^2/bit
Dice	828 (522↓ + 306↑)	4.55e-15 cm^2/bit
Seuss	1925 (1065↓ + 860↑)	1.05e-14 cm^2/bit
SR-ff	18279 (9002↓ + 9277↑)	5.02e-14 cm^2/bit
Artisan	44211 (13104↓ + 31107↑)	4.86e-14 cm^2/bit
Normal	20490 (7654↓ + 12836↑)	5.63e-14 cm^2/bit

$$\sigma = \frac{U}{NF}$$

The SEU cross section.

U is the total number of upsets (↓ and ↑)

N is the number of registers of a particular type in the beam

F is the Fluence of the beam (in this case, 2.03e14)

Protons all normal incidence

Results Normalized for Comparison

Type	Cross Section	Normalized
LBL Dice	3.84e-17 cm^2/bit	0.00079
RT Dice	5.86e-17 cm^2/bit	0.0012
RT Seuss	1.03e-15 cm^2/bit	0.021
RT SR-ff	3.85e-14 cm^2/bit	0.79
RT normal	3.23e-14 cm^2/bit	0.66
TR Seuss	4.7e-15 cm^2/bit	0.097
TR SR-ff	8.91e-15 cm^2/bit	0.183
Hit	1.59e-15 cm^2/bit	0.033
Liu	2.69e-16 cm^2/bit	0.0055
Dice	4.55e-15 cm^2/bit	0.094
Seuss	1.05e-14 cm^2/bit	0.216
SR-ff	5.02e-14 cm^2/bit	1.03
Artisan	4.86e-14 cm^2/bit	1.0
Normal	5.63e-14 cm^2/bit	1.16

Small is good

The LBL Dice looks quite good

Results: Comparison with 0.25µm

Type	0.13µm	0.25µm
LBL Dice	3.84e-17 cm^2/bit	n/a
RT Dice	5.86e-17 cm^2/bit	9.22e-18 cm^2/bit
RT Seuss	1.03e-15 cm^2/bit	1.38e-17 cm^2/bit
RT SR-ff	3.85e-14 cm^2/bit	n/a
RT normal	3.23e-14 cm^2/bit	4.4e-16 cm^2/bit
TR Seuss	4.7e-15 cm^2/bit	5.76e-18 cm^2/bit
TR SR-ff	8.91e-15 cm^2/bit	n/a
Hit	1.59e-15 cm^2/bit	n/a
Liu	2.69e-16 cm^2/bit	n/a
Dice	4.55e-15 cm^2/bit	n/a
Seuss	1.05e-14 cm^2/bit	n/a
SR-ff	5.02e-14 cm^2/bit	n/a
Artisan	4.86e-14 cm^2/bit	n/a
Normal	5.63e-14 cm^2/bit	n/a

A comparison to similar tests performed on the 0.25µm doesn't look so good. Shown here are only those registers that by register architecture and transistor geometry are comparable in both tests. Results similar to that found by Granlund, ***et al.***

Discussion

- Layout is becoming increasingly important. Note that there are three Dice cells, all with very similar schematics, and yet they range from 4.55e-15 cm^2/bit to 3.84e-17 cm^2/bit. Some of this can be explained by ELF vs. Rect. Transistors, but much of it must be attributed to careful layout.

Discussion

- One of the most surprising results was the poor performance of the triple-redundant registers. Again, layout is exceptionally important, but what percentage of the performance degradation can be attributed to dynamic SEUs on the Error Detection and Correction nodes? In the deep submicron processes, will triple-redundancy without EDC outperform triple-redundancy with EDC?

Future work

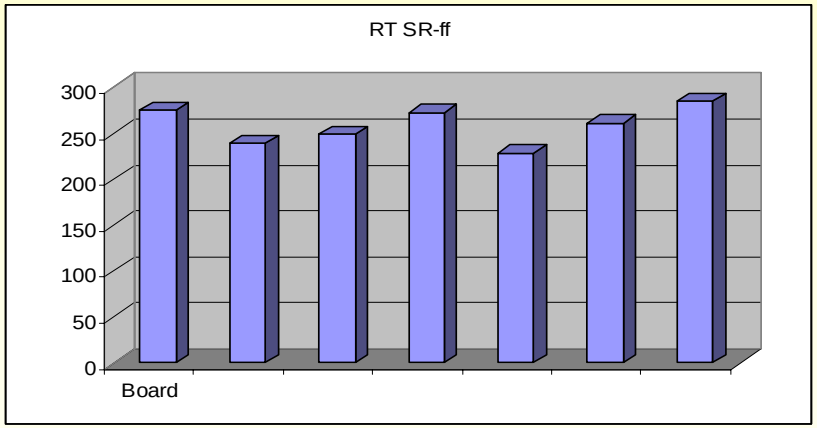
- Many of us are talking about other foundries such as TSMC and STMicroelectronics. This experiment supported earlier work that suggested that things are getting worse. Other experiments have suggested that things are still getting better. More experimentation needs to be performed.
- Layout optimization of particular architectures. The LBL Dice performed rather well, but can we do better? The Seuss is very flexible especially as a SEU tolerant SR-ff, but the rectangular FET version did not perform as well as hoped.
- Triple-redundancy is a fall-back many of us have used in the past. Layout optimization as well as EDC vs. no EDC needs to be tested.
- The pessimistic view is that 0.13 is worse than 0.25 and that we can only expect things to get worse yet. We need to check 90nm and, when it becomes more common, 65nm.
- A simultaneous 0.25, 0.13, 90nm experiment in which the same registers are used and simply scaled according to their design rules might determine, once and for all, how bad things are getting.

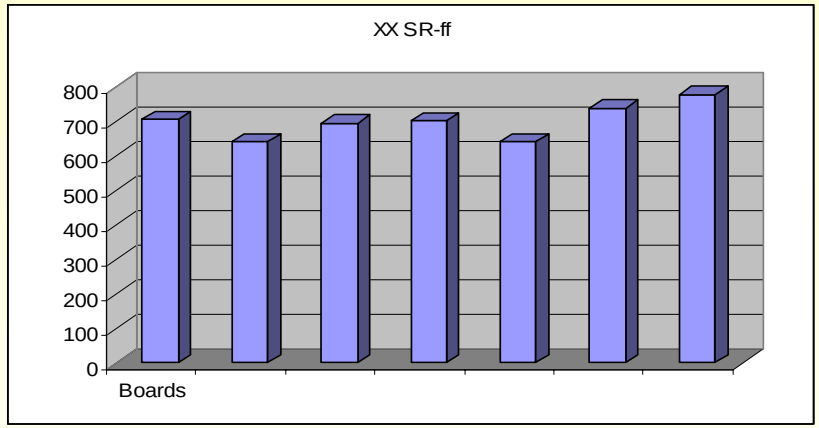
References

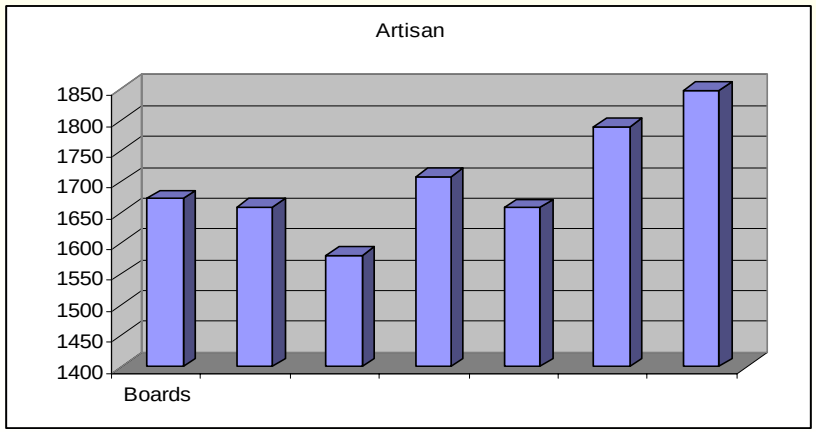
1. T. Calin, M. Nicolaidis, R. Velazco, IEEE Tran. Nucl. Sci. Vol 43, No. 6, p. 2874 (1996)
2. D. Bessot, R. Velazco, "Design of SEU-Hardened CMOS Memory Cell", RADECS '93, p. 563, 1993 INSPEC 4744705
3. M. Liu and S. Whitaker, IEEE Trans. Nucl Sci, Vol 39, No 6, p. 1670 (1992)

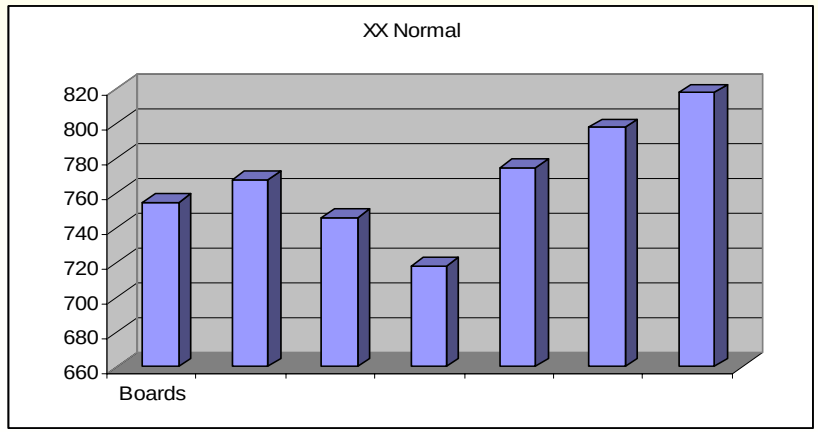
Beam Penetration

Errors on all boards demonstrate that the 200 MeV Protons Penetrated to all boards

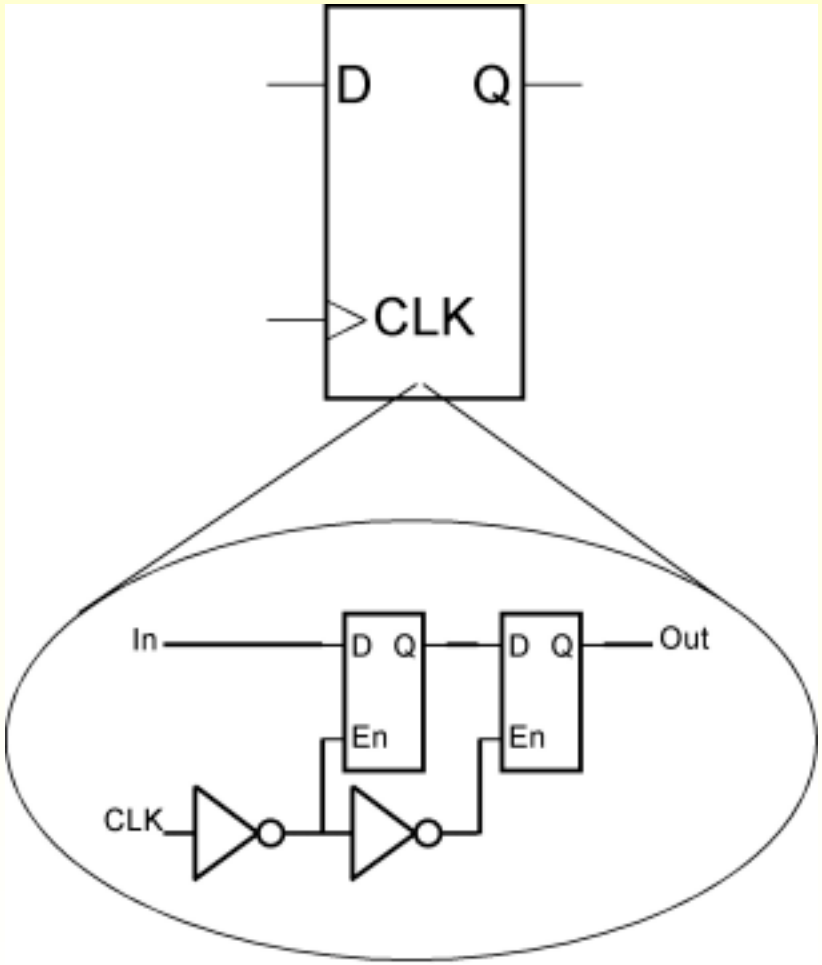






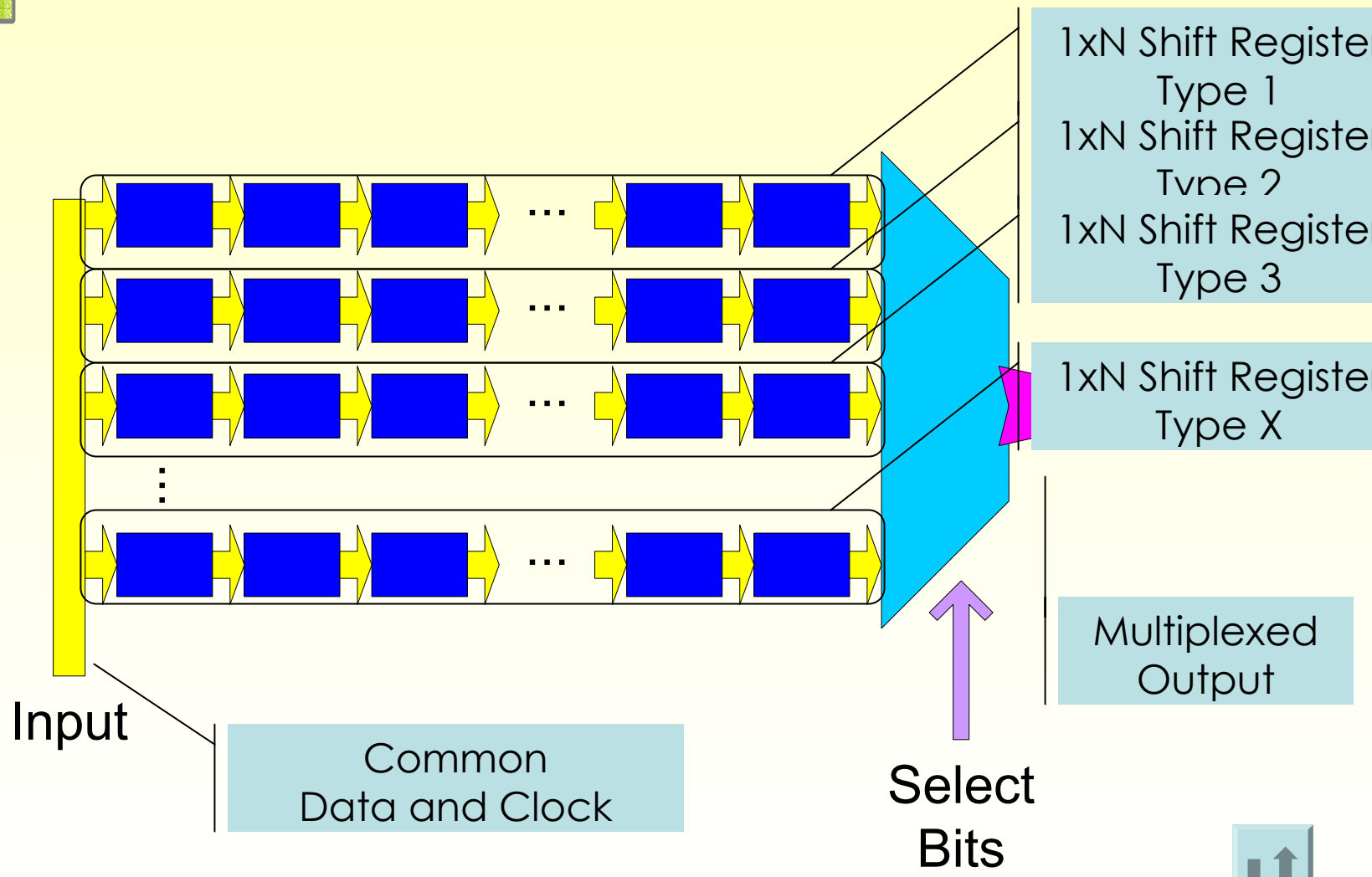


General Register Architecture



All registers in the experiment, regardless of type are organized as shown.

Two simple D-latches are used to create a single Master-Slave postive-edge-triggered D-flip-flop. The self-generated internal clocks ensure that clock loading cannot contribute to SEUs


1xN Shift Register Type 1
1xN Shift Register Type 2
1xN Shift Register Type 3
1xN Shift Register Type X
Multiplexed Output
Input
Common Data and Clock
Select Bits