Opportunities for HEP Instrumentation Using 3D Circuits

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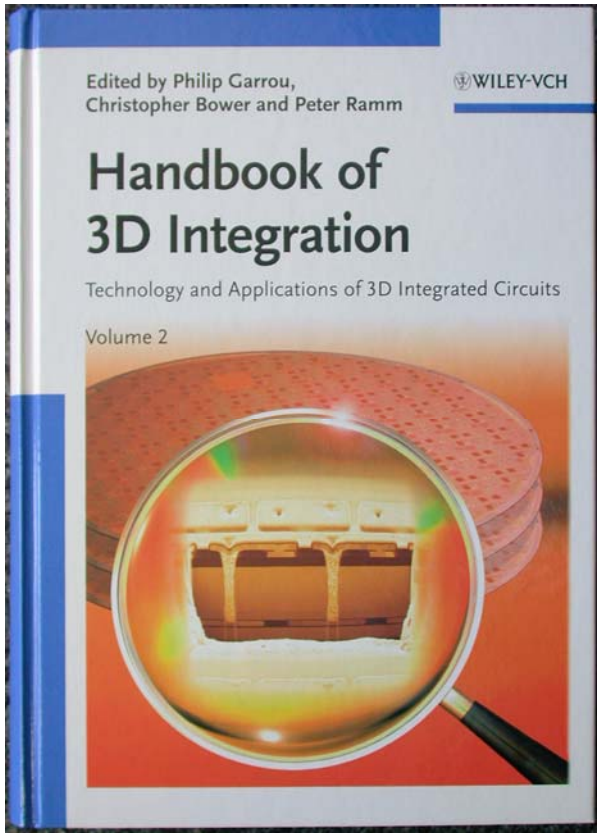
Introduction

The development of 3D integrated circuits has recently received much attention in trade journals such as Semiconductor International, Chip Scale Review, and Advanced Packaging. In addition, special sessions have been arranged various IEEE meetings, and dedicated meetings such as 3D Architectures for Semiconductor Integration and Packaging have taken place. All of this attention is generated by industry seeking to perpetuate Moore's Law. In particular industry is focusing on several 3D IC applications: stacked memory chips, pixel arrays for imaging, logic and memory stacking on microprocessors, and FPGAs. The 3D technology is being driven entirely by industry. However, the time has come when HEP can begin to benefit from work the in progress.

Fermilab began exploring 3D technology for HEP several years ago and submitted the first 3D IC (VIP1) for HEP to MIT Lincoln Labs in October 2006.

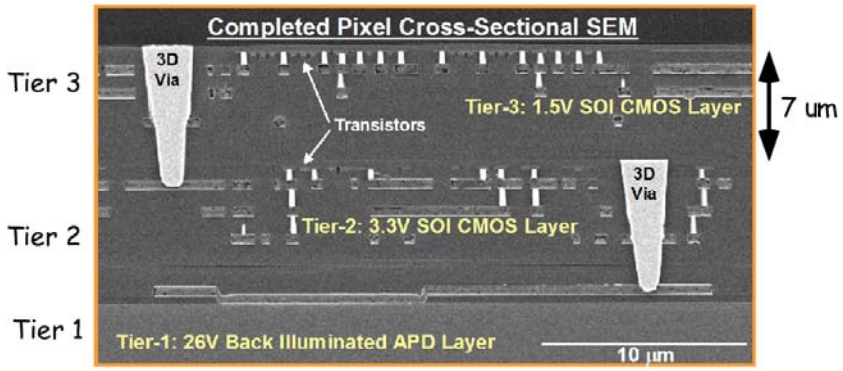
Definition

- The Handbook of 3D Integration[1] defines 3D integration as " the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers"
- The Handbook
  - Identifies the major groups active in 3D development
  - Describes the key technologies for 3D circuit fabrication
    - Review the technologies that allow new opportunities for HEP

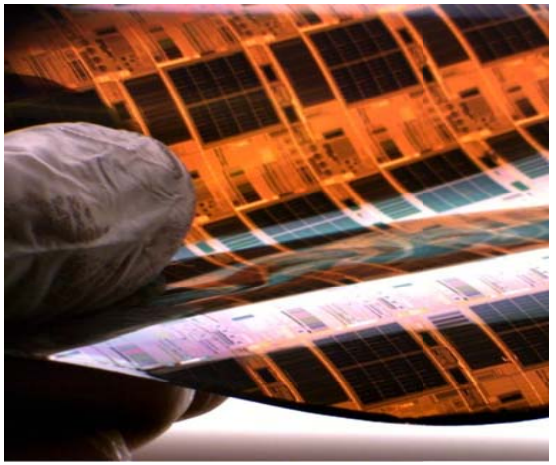


Key Technologies for 3D

1) Via formation and metallization
   - Vias typically have an aspect ratio of 5-8:1
   - Vias fabricated after the Back End of Line (BEOL) foundry processing are know as "via last". Vias that are fabricated as a part of the IC foundry process are known as "via first" and use less silicon real estate.
   - CMOS wafers require passivation of the vias before metallization to avoid shorts
   - SOI wafers do not require via passivation
2) Thinning
   - To minimize space for vias in small pixel designs, thin substrate as much as possible



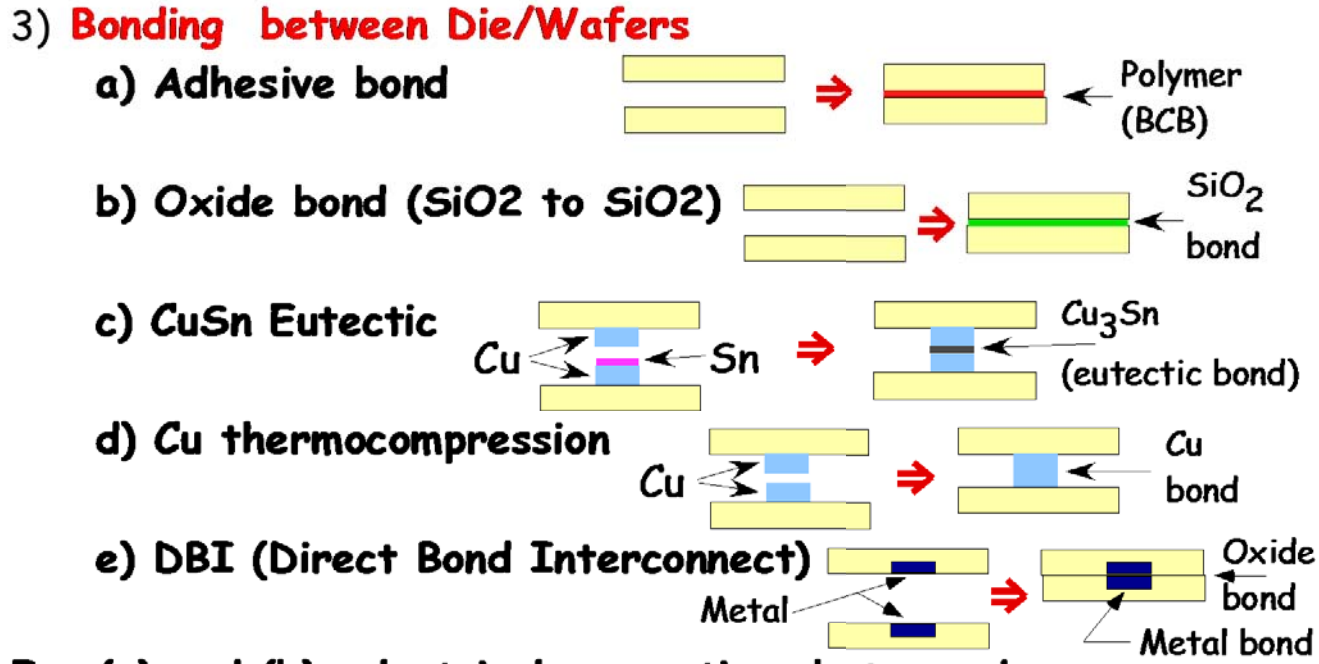
MIT LL via last process in SOI[2]



6 inch SOI wafer thinned to 6 um and mounted to 3 mil kapton for support at MIT LL

Four Key Technologies for 3D

3) **Bonding between Die/Wafers**



Fermilab experience

(MIT LL)

(RTI)

(Tezzaron)

(Ziptronix)

For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

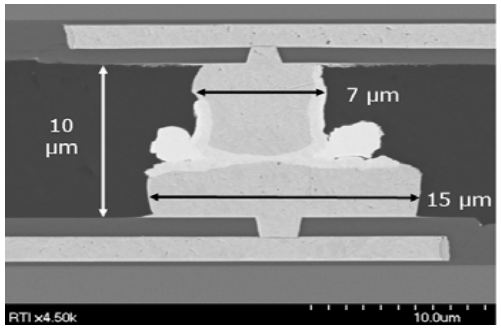
4) Precision alignment of better than 1 um (3 sigma) is now possible with wafer to wafer bonding.

3D Technology Advantages for HEP

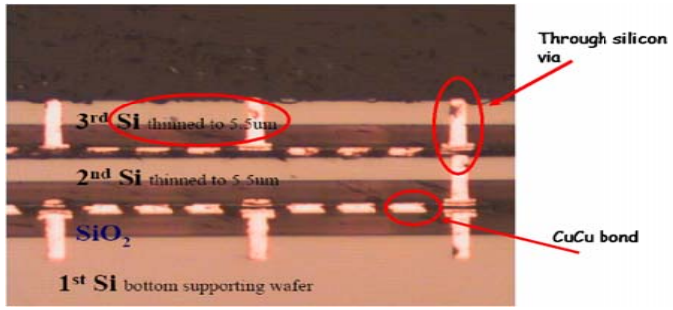
- Aggressive thinning leads to low mass circuits resulting in low particle scattering applications such as the ILC vertex detector.
- New bonding technologies for 3D lead to alternatives to conventional bump bonding that can provide lower mass, finer pitch, and enhanced mechanical robustness for additional mechanical processing (thinning without destroying the connections)
- Via formation allows for increased circuit density with multiple tiers, and/or allows for 4 side butt able circuits.
- 3D via formation allows for mixed circuit technology design and independent analog and digital substrates.

Decreasing Mass and pitch

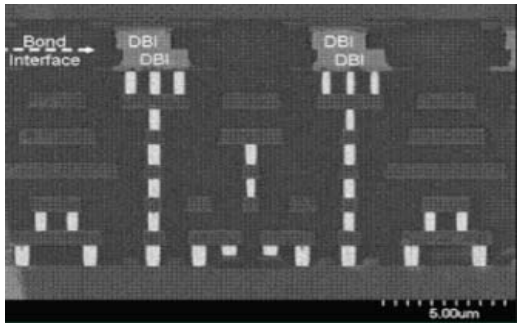
New Bonding Options



Copper/tin pillar[3]



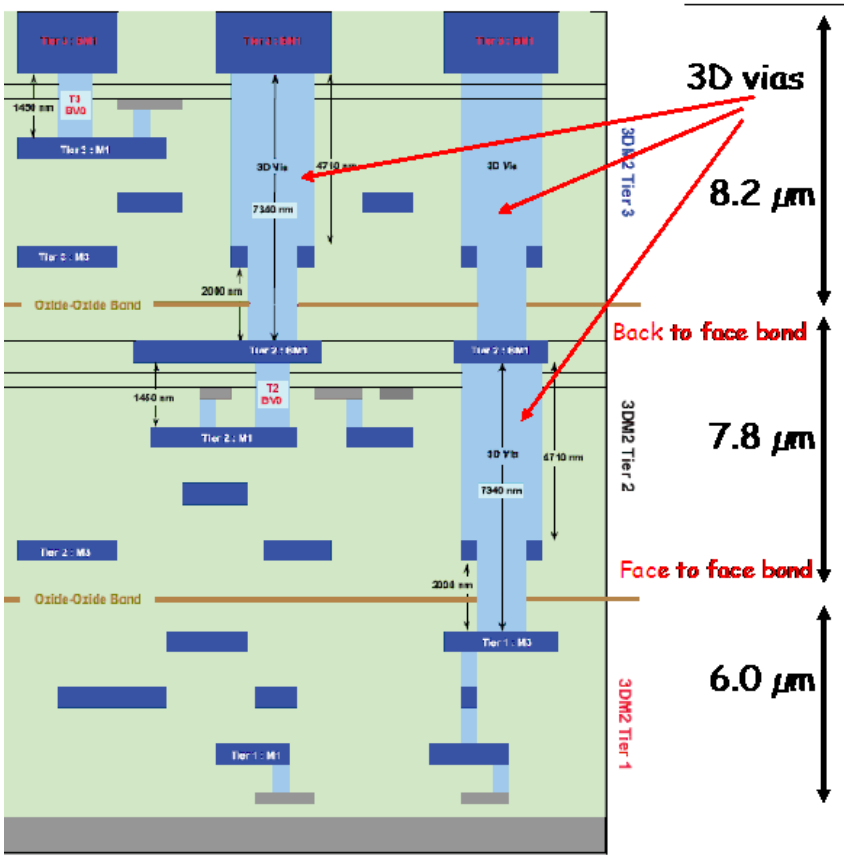
Copper/copper fusion



Direct bond Interconnect

Milestones Achieved in First HEP 3D Circuit called VIP1

- Demonstrated increased circuit density by integrating 3 circuit tiers
- Showed that extreme circuit thinning (7um) was possible
- Showed that small vias (~1.5 um) were possible thus allowing for small pixel sizes.
- Showed that 3D vias and bonding were reliable



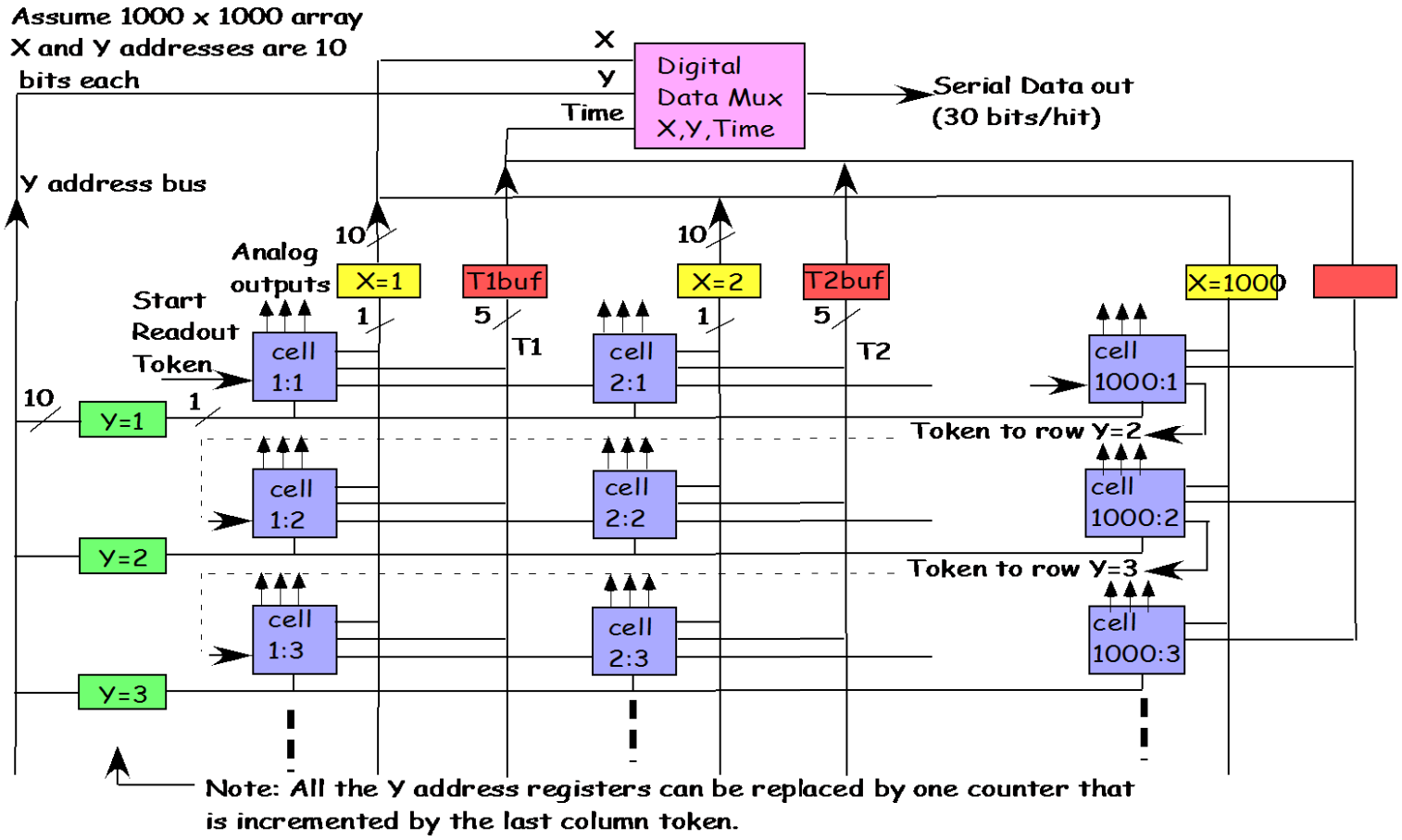
MIT LL 3 Tier Assembly

3D Demonstrator Chip for ILC Vertex Detector

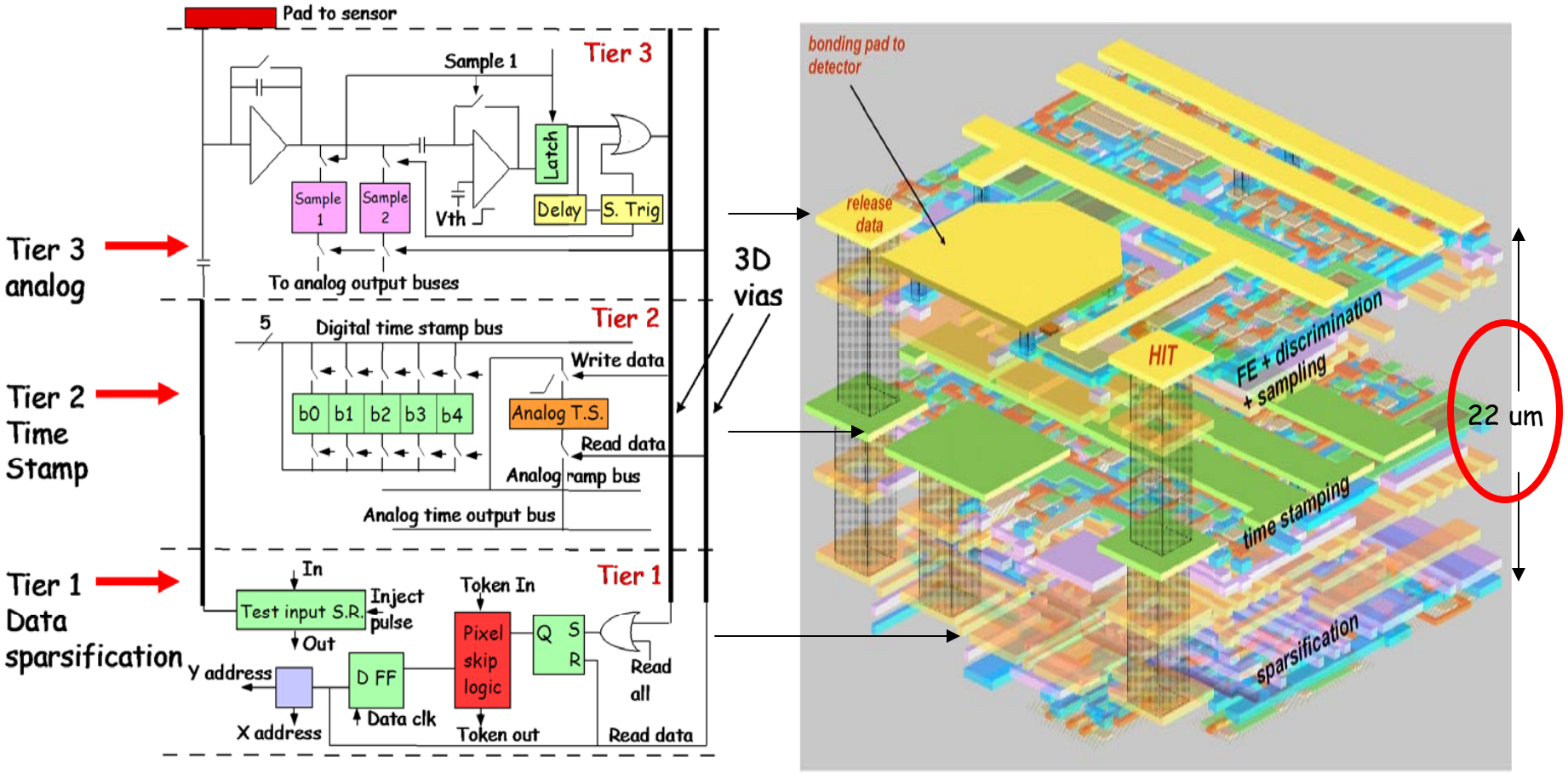
- VIP1 (vertically integrated pixel) designed as three tier circuit fabricated in MIT LL 0.18 um SOI process using oxide bonding and via last process.
- Details of VIP1 chip design and operation presented at 12th LHC electronics workshop[4]
  - Readout between ILC bunch trains
  - High speed data sparsification included
  - Analog output available for improved resolution
  - Five bit digital (30 usec resolution) and analog time stamping options explored
  - Test input for every pixel
  - 4096 pixel array with 20 um pixels, scalable to 1 Mpix

VIP1 Block Diagram

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out.
- During pixel readout, token scans ahead for the next hit pixel

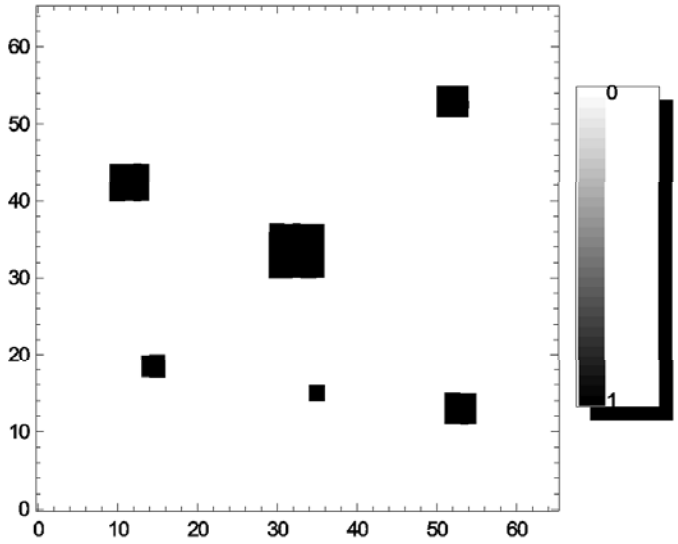


VIP1 Pixel Layout in 3D

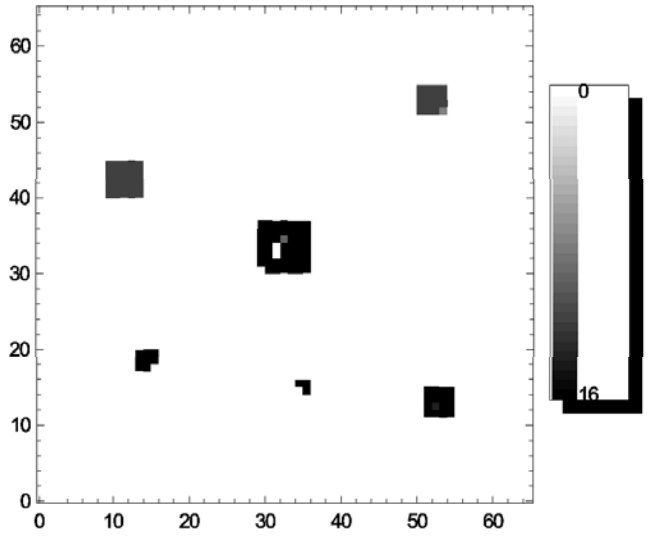


VIP1 Test results[5]

- Functionality of chip proven through series of tests
  - Propagation of readout token
  - Pixel threshold scan to measure dispersion
  - 5 bit digital time stamp OK, analog TS poor.
  - Test input charge scan with full sparsified data readout
- Yield was poor due to poor models and processing issues
  - No problems found with 3D vias



Hit pattern injected into pixel array simulating an event



Hit pattern read out using token passing and sparsification scan.

Second HEP Submission to MIT LL

- Second submission (VIP2a) in October 2008
- Goals
  - Improve yield
  - Bond 3 tier chip to sensor using DBI at Ziptronix
- Design changes
  - Added test features
  - Improved power and ground layout
  - Redundant vias and wider traces in critical paths
  - 24 um pixel size to accommodate relaxed design rules
  - Increased digital time stamp to 7 bits

3D Design Consortium

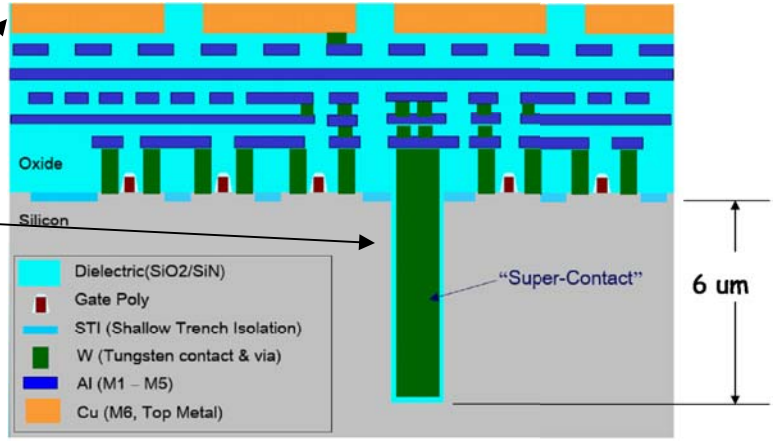
- Interest in 3D has led to formation of a consortium of 15 institutions in 2008 to design and fabricate 3D circuits using the Tezzaron Cu-Cu bond process with wafers from Chartered Semiconductor in Singapore.
  - Tezzaron uses the via first process which provides improved silicon usage.
  - Chartered is a commercial 0.13 um CMOS process which should give good yield and provide higher radiation tolerance than SOI.
  - The fabrication of 3D circuits through Tezzaron is cost effective for HEP members of the consortium.

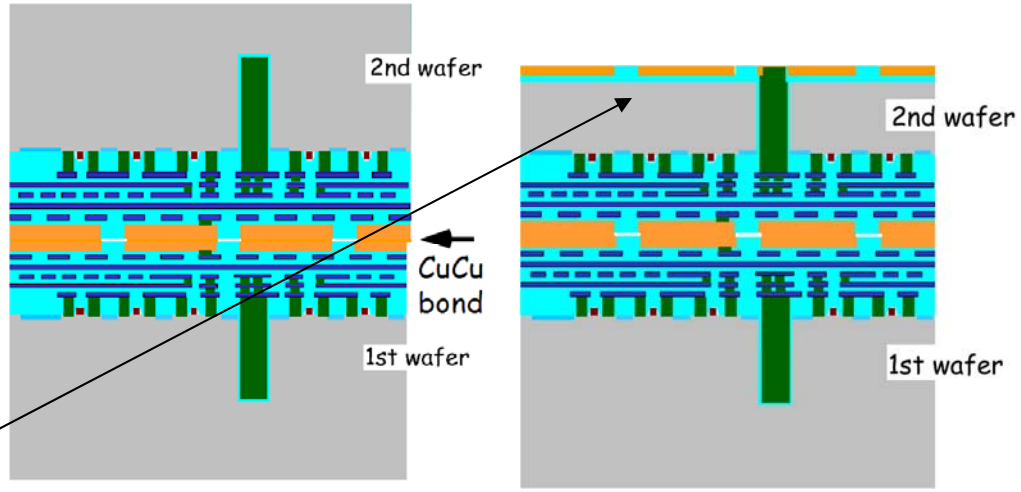
3D Consortium Institutions

- Fermilab, Batavia
- LBNL, Berkeley
- University at Bergamo
- University at Pavia
- University at Perugia
- INFN Bologna
- INFN at Pisa
- INFN at Rome
- University of Bonn, Germany
- CPPM, Marseilles
- IPHC, Strasbourg
- IRFU Saclay
- LAL, Orsay
- LPNHE, Paris
- CMP, Grenoble
- AGH University of Science &Technology, Poland

Tezzaron Process

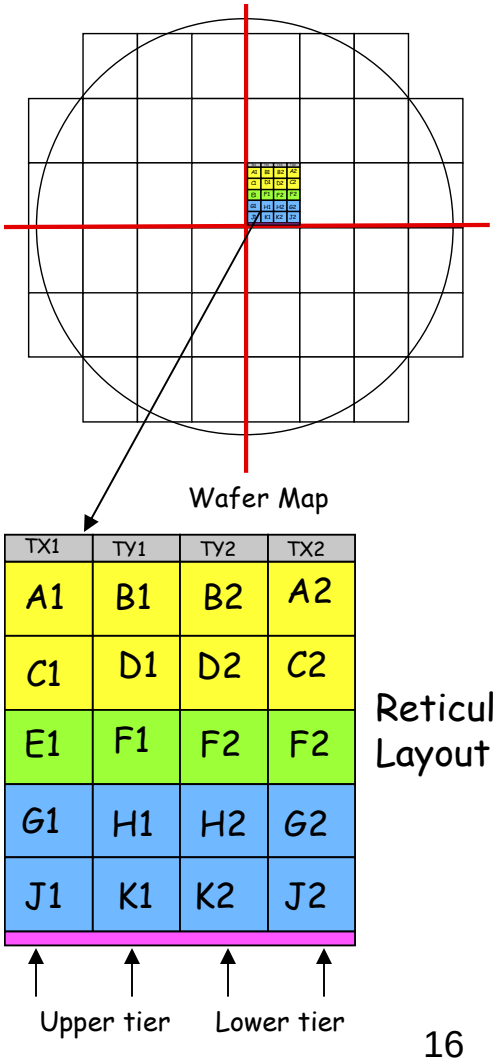
- Form super contact (via) and fill via at same time metal connections are made to transistors. Complete the BEOL processing using top metal layer for wafer to wafer bonding.
- Flip 2nd wafer (shown as identical) on top of first wafer and bond second wafer to first wafer using Cu-Cu thermo-compression bond
- Thin 2nd wafer to about 12 um to expose super via and add metallization to back of 2nd wafer for bump bond or wire bond





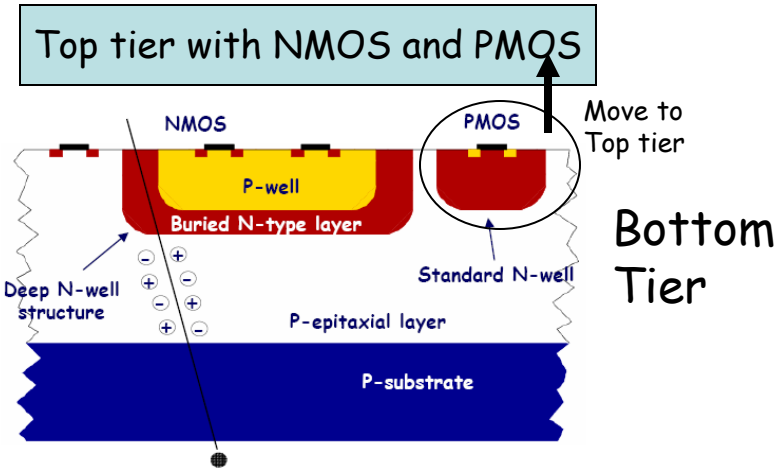
Tezzaron MPW Run to Explore New Opportunities for HEP

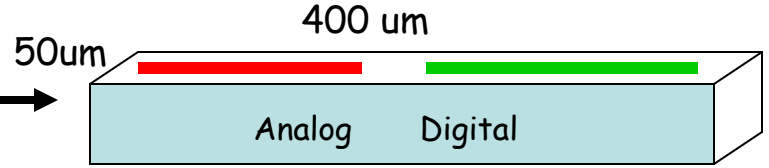
- Upper and lower tiers fabricated on the same wafer
- Ten different chip designs (A-K) plus 2 test chips (TX, TY)
- Designs explore applications for
  - ILC,
  - SLHC,
  - X-ray imaging



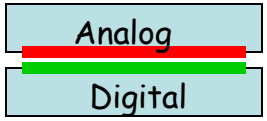
New Opportunities for HEP

- Conventional MAPS circuits use no or few PMOS devices in the sensing layer since PMOS devices require a separate NWell which takes charge away from the sensing diode. Bergamo/Pavia is exploring moving most or all the PMOS devices to the top tier of a two tier circuit.
- The ATLAS pixel upgrade group (France, Germany, US) is exploring a new pixel design for SLHC which places the analog portion of a pixel on a top tier and the digital portion of a pixel on the bottom tier. This design can allow for separate analog and digital substrates and smaller pixel sizes for a given technology





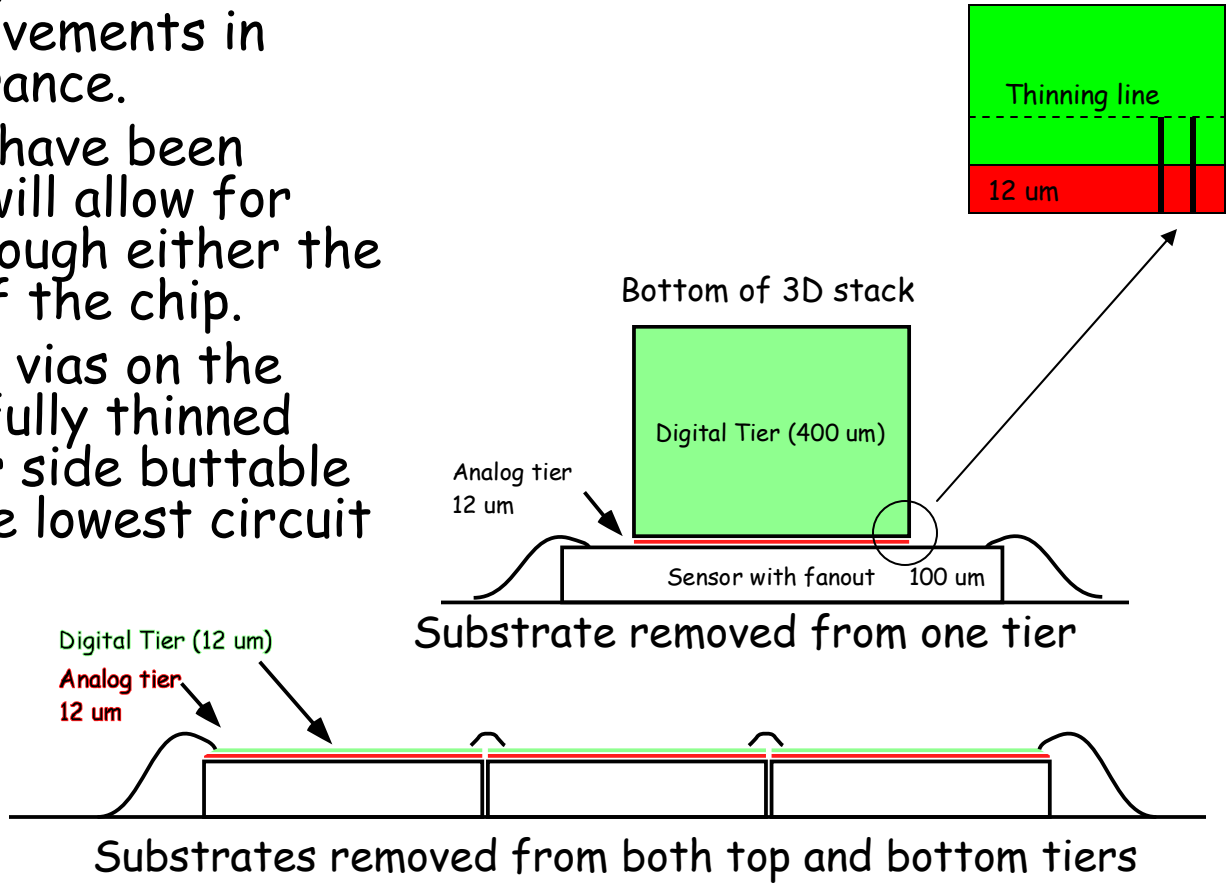
Current LHC ATLAS pixel layout



Possible future ATLAS pixel in 3D

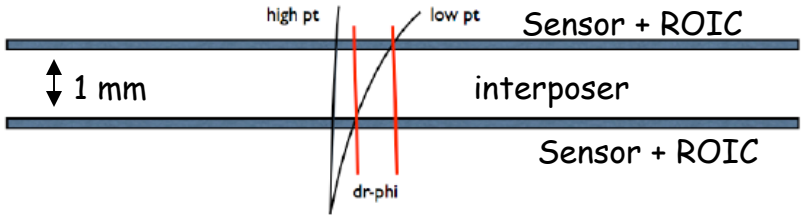
New Opportunities for HEP

- The ILC three tier VIP2 design for MIT LL has been converted to a 2 tier design (VIP2b) for Chartered with expected improvements in yield, radiation tolerance.
- Through silicon vias have been implemented which will allow for I/O connections through either the top or the bottom of the chip.
- Connections through vias on the bottom side of the fully thinned chip can lead to four side buttable layouts with absolute lowest circuit and sensor mass.

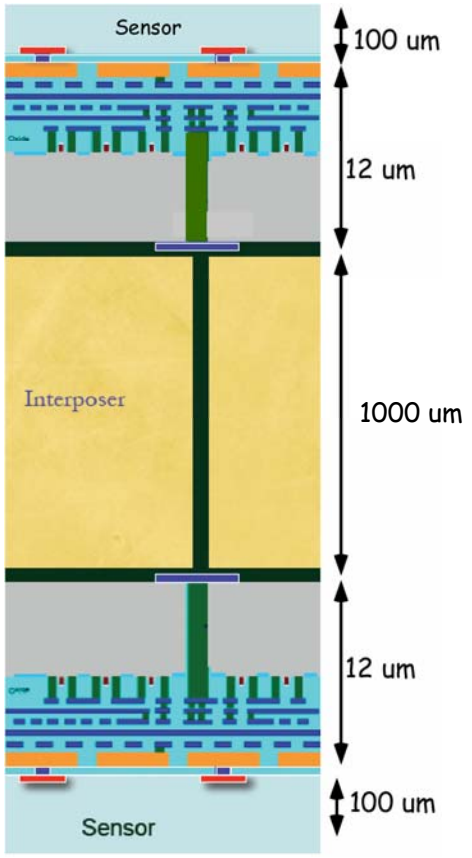


MPW Opportunities for HEP

- The through silicon via technology can be used in applications like CMS to locally identify high pt tracks and thus minimize data transfer.
- This can be done by having two layers of sensors and ROICs separated by an interposer of modest thickness (~1 mm).
- Signals would pass through the interposer locally to correlate hit information from the two sensor layers.



Note:
Not to scale



Summary

- 3D design activity is now occurring at many HEP institutions.
- A consortium has been form to submit MPW runs to Tezzaron/Chartered.
- Work is ongoing to identify the most promising applications of 3D for HEP and related areas.
- 3D technologies have the potential to allow new design concepts to be developed for HEP

References

- 1 Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits,Wiley-VCH, 2008.
- 2 B. Aull, et. al., "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit layers", ISSCC 2006, pp 26-27.
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- 4 R. Yarema, "Development of 3D Integrated Circuits for HEP", 12th LHC Electronics workshop, Valencia, Spain, Sept 25-29, 2006.
- 5 G. Deptuch, Vertical Integration of Integrated Circuits and Pixel Detectors, Vertex 2008 Workshop, July 28-August 1, 2008, Uto island, Sweden.
- 6 Bob Patti, *3D Scaling to Production*, 3D Architectures for Semiconductor Integration and Packaging, Oct 31-Nov 2, 2006, San Francisco.