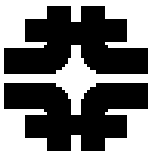
Highlights of the 5th International Meeting on Front End Electronics

Ray Yarema

Fermilab

September 2003



June 30 to
July 3

Snowmass,
Colorado

40 talks

3 tutorial talks in special session

- CMOS Technology for Next 10 Years - IBM
- Scaling and Single Event Effects – NASA
- SiGe HBT BiCMOS Technology – Georgia Tech

37 talks on Front-End Electronics

http://www-ppd.fnal.gov/EEDOffice-w/Conferences/FEE_2003/FEE2003.html

(meeting continued)

- **37 talks in other meeting sessions (no parallel sessions)**
  - **Silicon Tracking**
  - **Radiation Effects in Deep Submicron and and Other Circuits**
  - **Monolithic /CCD Devices**
  - **Reliability and Production**
  - **Special Front-End Circuits**
  - **Front-End Chips for Calorimeters**
  - **Experiments in Space**
- **Round table session on "Collaboration and Costs in new Deep Submicron Processes"**
- **Proceedings on CD – 1167 transparencies**
- **Will try to sparsify data to 30 transparencies - hit only most salient points.**

CMOS Technology for the Next 10 years (David Frank, IBM)

- International Technology Roadmap for Semiconductors - http://public.itrs.net/Files/2001ITRS/Home.htm
- Industry agreed upon targets for future technology. Typically everyone tries to beat these targets.

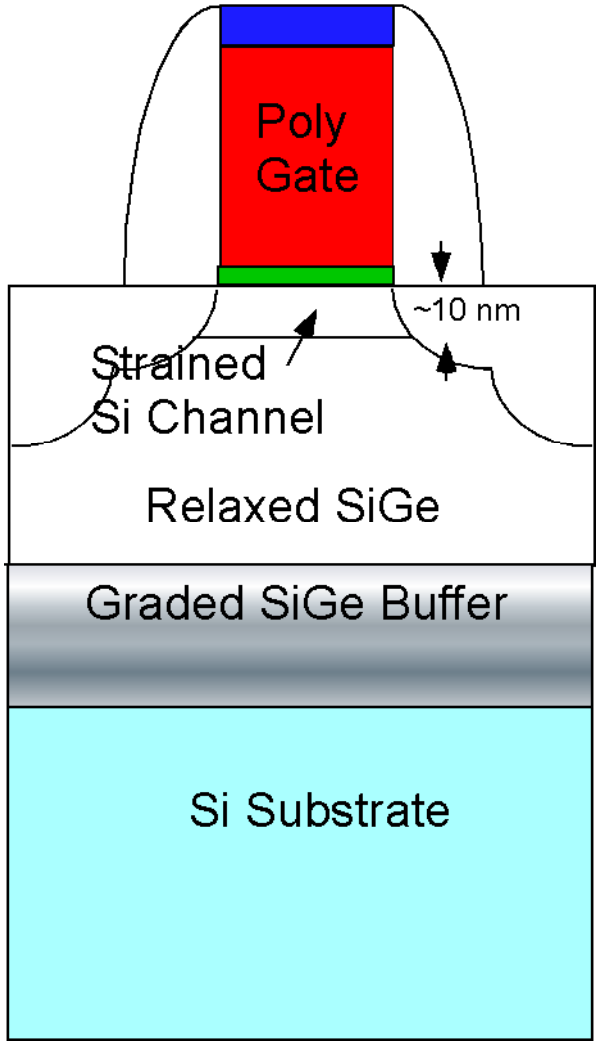
First Year of Production	2001	2003	2005	2007	2010	2013	2016
MPU Printed gate length (nm)	90	65	45	35	25	18	13
Tox electrical equivalent (nm)	2.3	2	1.9	1.4	1.2	1	0.9
Vdd high performance (volts)	1.1	1	0.9	0.7	0.6	0.5	0.4
Number of wire levels	8	8	10	10	10	11	11
Local clock speed (GHz)	1.7	3.1	5.2	6.7	11.5	19.3	28.8

Future Technology Directions for CMOS

- Two goals of technology enhancement:
  - 1. Improve performance
  - 2. Make it smaller (scaling)
- Important options under development:
  - 1. Strained Silicon (improve performance)
  - 2. Metal gate (improve performance)
  - 3. High –k gate insulator (improve performance and make it smaller)
  - 4. Double-gate FET (make it smaller)

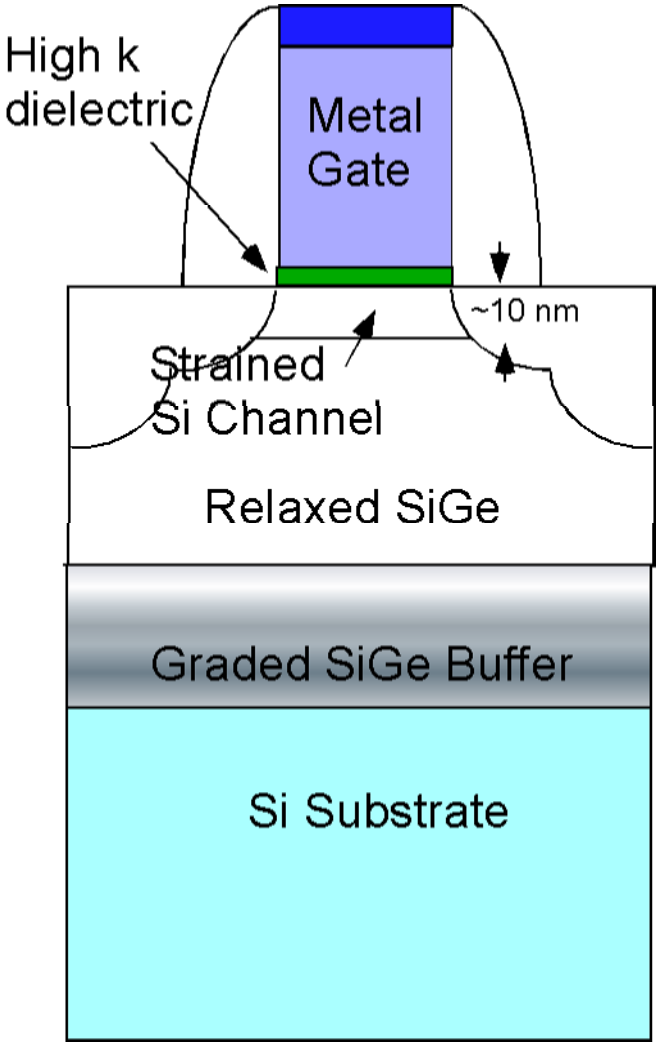
Strained Silicon for Performance Improvement

- Strained silicon channel is formed beneath gate.
- Grown on top of SiGe.
- Provides high electron and hole mobility and higher current drive.
- Compatible with CMOS processing.
- Many companies are investigating.
- IBM plans to use strained silicon in 65 nm process.



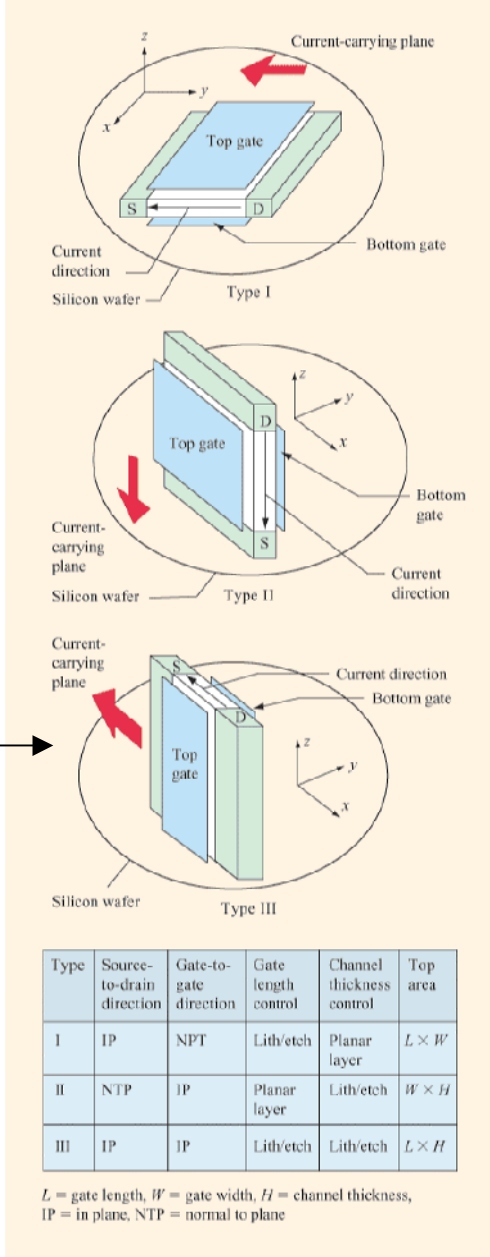
Gate Stack Improvements for Continued Feature Size Scaling

- **High–k gate dielectrics are needed**
  - **To enable further scaling**
  - **To reduce effective oxide thickness**
  - **To reduce leakage**
  - **Required by about 2005**
- **Metal gate**
  - **Needed to reduce gate capacitance degradation due to the depletion of doped poly silicon gates.**
  - **Lower temperature processing for metal gates is more compatible with low-k dielectric processing.**
  - **Expected by about 2007**



Double Gate FET

- Double gate expected to take over from planar CMOS processing. (2010?)
- Better for scaling
- Tighter control of transistor on and off states.
- Three possible layouts, Types I, II, III.
- Type III is also called the FinFET and appears to be the most manufactureable device.
- FinFET Advantages
  - **Undoped channel provides better gate control**
  - **Fin can be made very thin.**
  - **No leakage path from drain to source.**



Type	Source-to-drain direction	Gate-to-gate direction	Gate length control	Channel thickness control	Top area
I	IP	NPT	Lith/etch	Planar layer	$L \times W$
II	NTP	IP	Planar layer	Lith/etch	$W \times H$
III	IP	IP	Lith/etch	Lith/etch	$L \times H$

L = gate length, W = gate width, H = channel thickness, IP = in plane, NTP = normal to plane

Figure 14

Three possible topologies of the double-gate FET. Adapted with permission from Wong et al. [71]; © 1997 IEEE.

Future

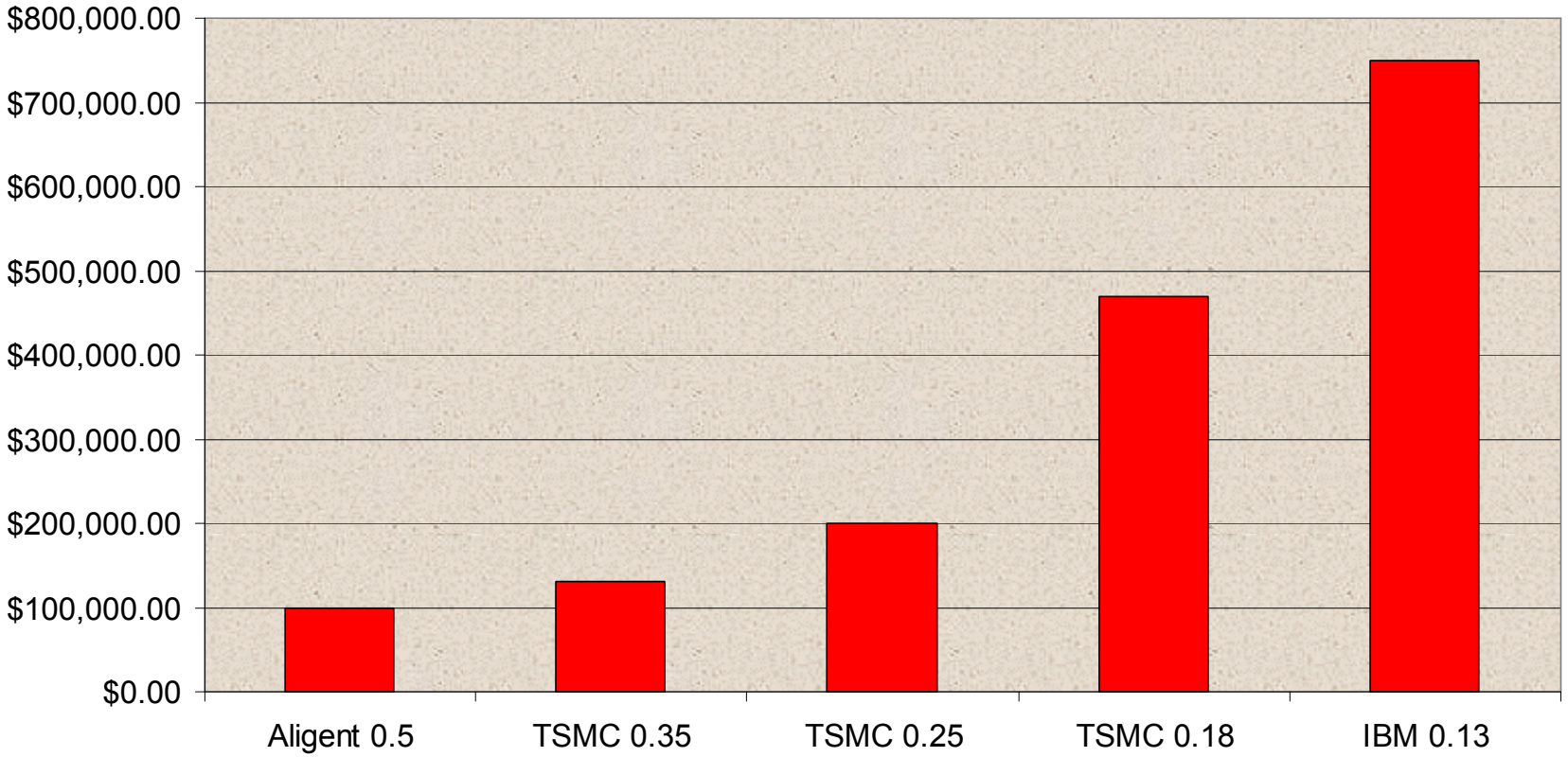
- Scaling limits will eventually be set by factors such as:
  - Tunneling currents and discrete dopant fluctuations
  - Material properties – bandgap, k, etc.
  - Thermodynamic effects and heat removal
- Massive efforts in industry will result in continued improvements in CMOS for high performance digital applications.
- CMOS analog applications will simply ride on the coattails of new digital processes.
- What does this means for HEP?

Cost and Collaboration in the new DSM Technologies

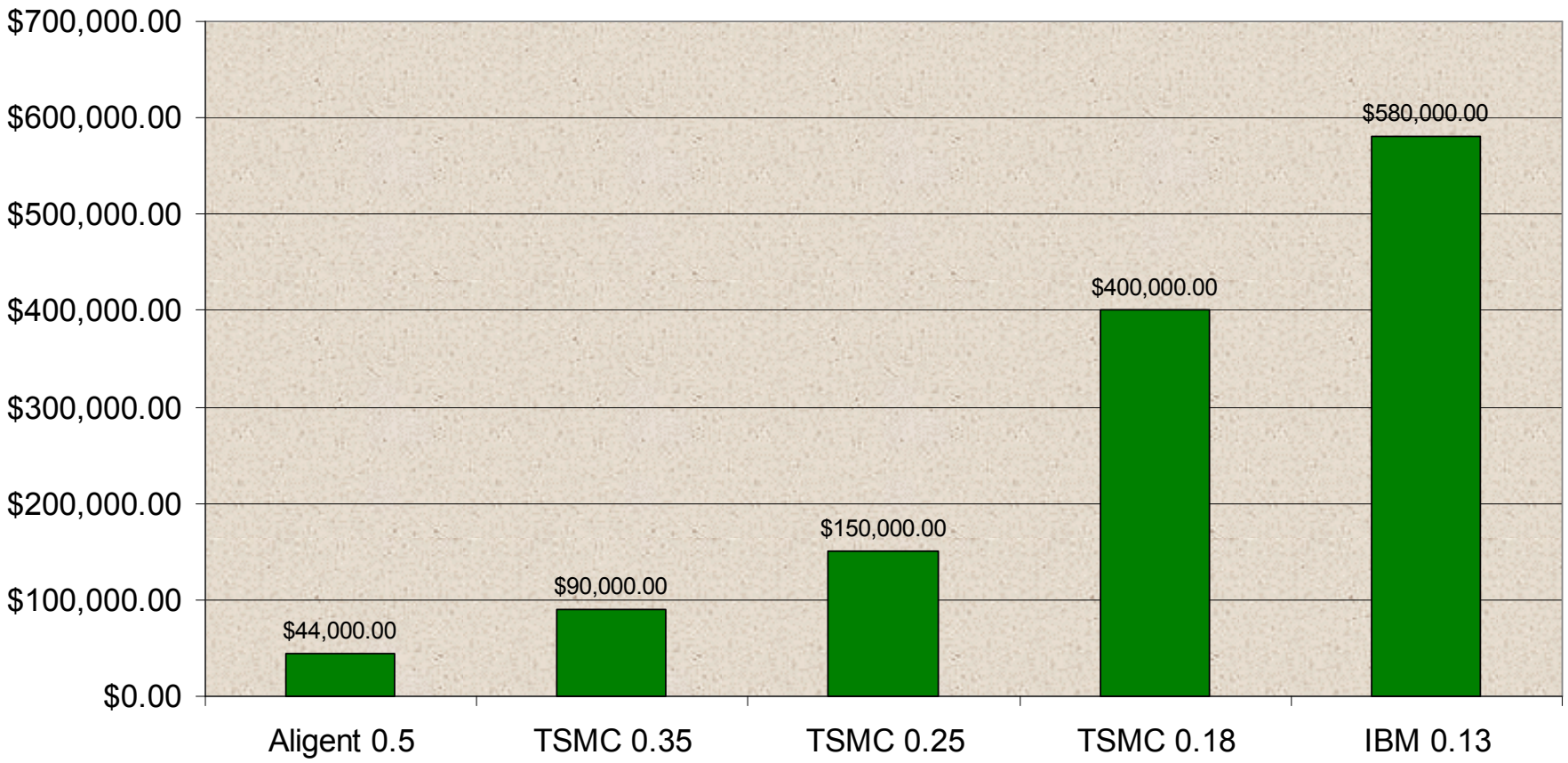
(Roundtable session – LBL, RAL, IC, BNL, FNAL)

- Need for better resolution vertex detectors, e.g. smaller pixel sizes.
- Current processes will become obsolete.
- History at Fermilab
  - 1986-89, SVX, 3.0 μ m UTMC
  - 1993-96, SVX2, 1.2 μ m UTMC
  - 1995-98, SVX3, 0.8 μ m Honeywell
  - 2000-03, SVX4, 0.25 μ m, TSMC
  - 2005 - ??
  - 2010 - ??
- Most designers are happy with 0.25 μ, but it won't last.

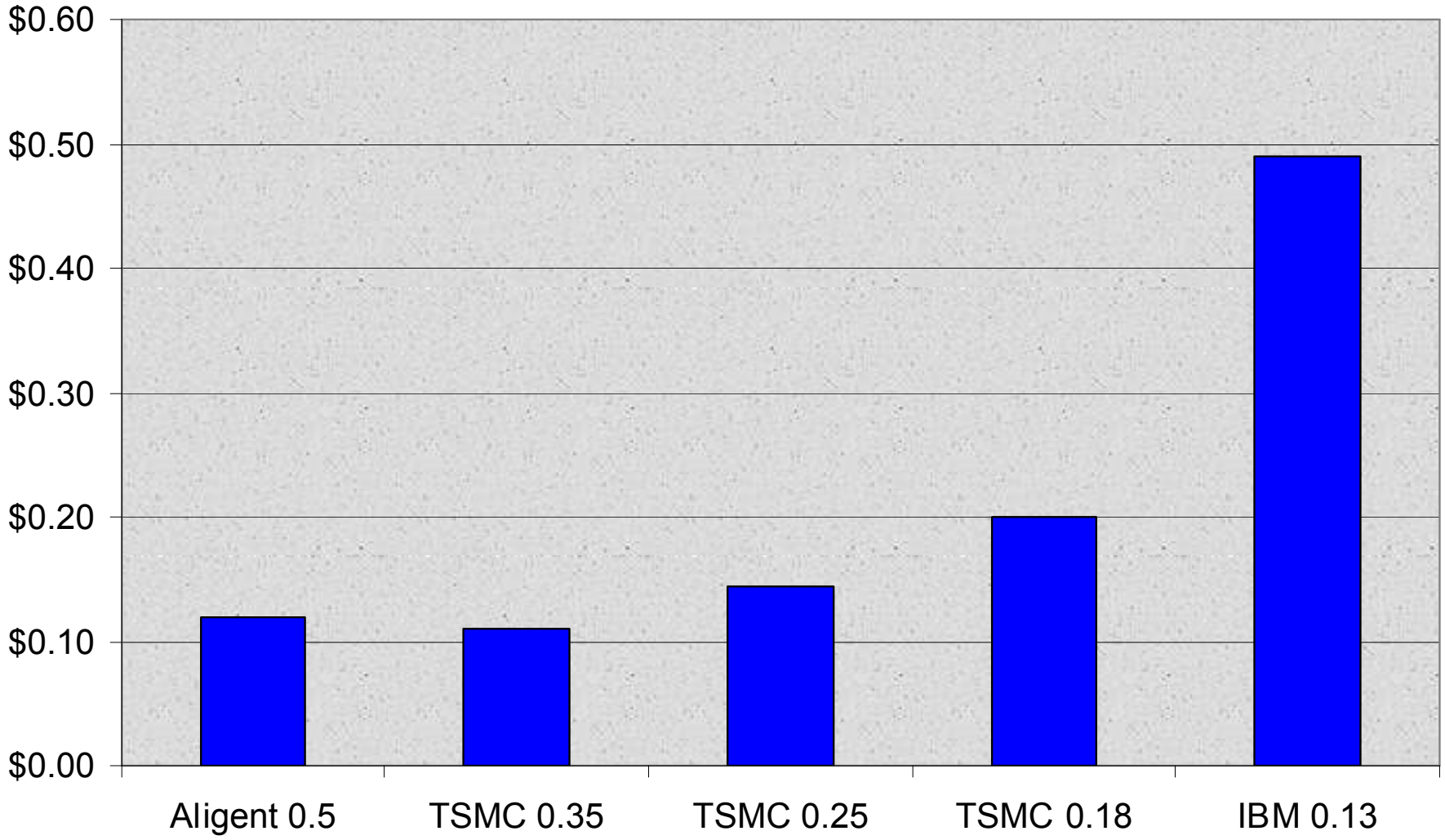
MOSIS Engineering Run Cost



Mask Costs for Engineering Runs at MOSIS



Engineering Run Wafer Cost/mm2



Cost Sharing and Reduction in HEP

- CERN frame contract with IBM has been successful.
  - Many projects have been run
  - Reduced cost for multiproject runs and production runs.
  - Must wait for all designs to be ready to submit run
  - Dealt directly with vendor to solve yield problem.
- In the U.S., Fermilab, LBNL, and BNL have used TSMC thru MOSIS for non-LHC projects.
  - Frequent scheduled MPW runs at MOSIS.
  - Fermilab did own engineering multiproject runs with MOSIS.
  - Counted on MOSIS to interface with vendor and insure success of a large number of projects for many customers
- IBM and TSMC processes now available through MOSIS. Can this make cost sharing easier between Europe and U. S.?

How should the HEP Community Proceed?

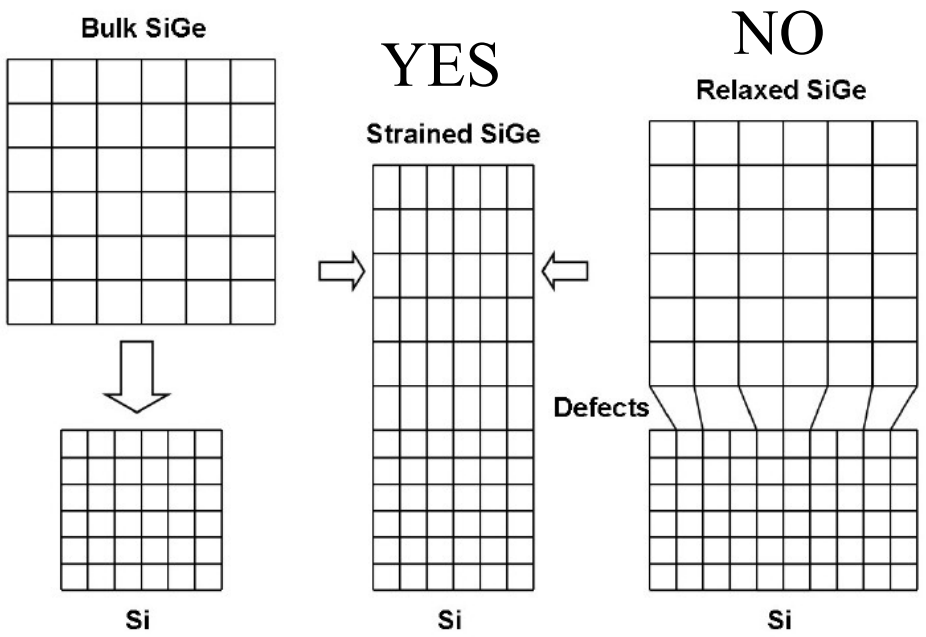
- Is there enough design demand in the near future to setup another special contract with a vendor? (SLHC, LC, space, neutrino and underground experiments)
  - Fewer projects for submission means long time to fill frame or higher project costs.
  - Need to agree on number of metal levels and other features to be successful.
- Should HEP community proceed with industry MPW submissions (e.g. MOSIS)?
  - Regularly scheduled submissions, but high cost.
  - Might rule out small quantity projects

Collaboration is Important

- Cost of future processes will be very high compared to 0.25μm.
- Qualification of and design in new technologies is expected to be a lengthy process. R&D should begin now. Money is tight. A good reason to collaborate.
- Can European and U.S. HEP communities agree on one foundry as primary and another foundry as a second source?
  - Share expensive mask cost on engineering and production runs.
  - Share SEU tolerant designs and libraries
  - Share process testing for radiation qualification, etc.
- Discussions have begun. No clear path yet.

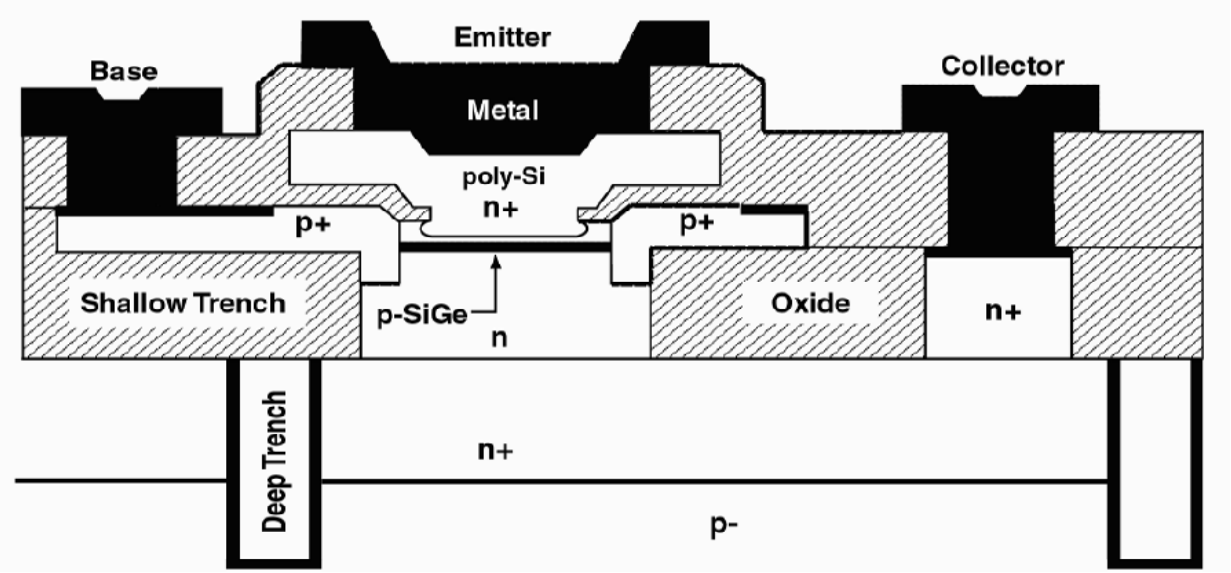
SiGe HBT Technology – J. Cressler

- **Engineered bandgap of the base material used in bipolar devices to form high performance NPN devices.**
- **Put graded Ge layer in base to form Strained Germanium Silicon**
- **Process is compatible with conventional CMOS to provide high speed BiCMOS, f_T up to 200 GHz.**
- **Process is now readily available from several foundries (13):**
  - **IBM 0.5u, 0.35 u, 0.25 u**
  - **AMS 0.8 u, 0.35u**
  - **ST 0.35 u**
- **Currently higher cost than CMOS without bipolar devices.**



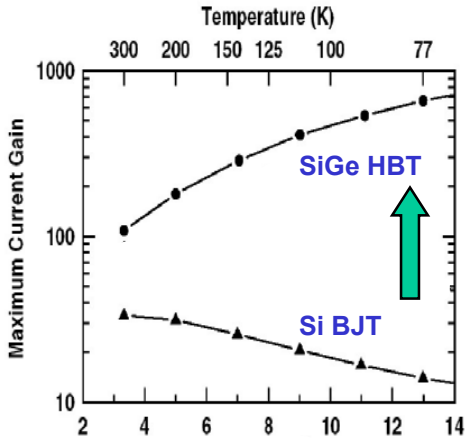
SiGe advantages over Silicon

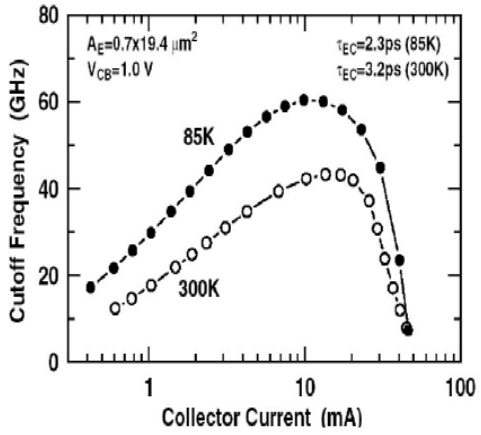
- Smaller base bandgap voltage increases electron injection (increased β).
- Field from graded base bandgap decreases base transit time (increased f_T).
- Base bandgap grading produces higher Early Voltage
- Significant improvement in broadband noise over Si BJT.
- Lower 1/f noise

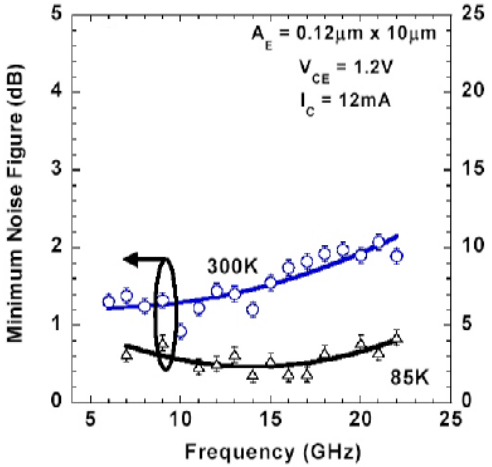


Other Special Features of SiGe Devices

- Inherently radiation hard bipolar devices due to epitaxial base structure.
- No dose rate effects as found in conventional bipolar devices.
- SiGe performance improves with cryogenic cooling (unlike normal BJT)
  - Current gain (β) and Early Voltage increase with cooling
  - Frequency response (f_T)and noise (NF) improve with cooling







Sessions

1) Silicon Tracking

2) Radiation Effects in Deep Submicron and Other Circuits

3) Monolithic /CCD Devices

4) Reliability and Production

5) Special Front-End Circuits

6) Front-End Chips for Calorimeters

7) Experiments in Space

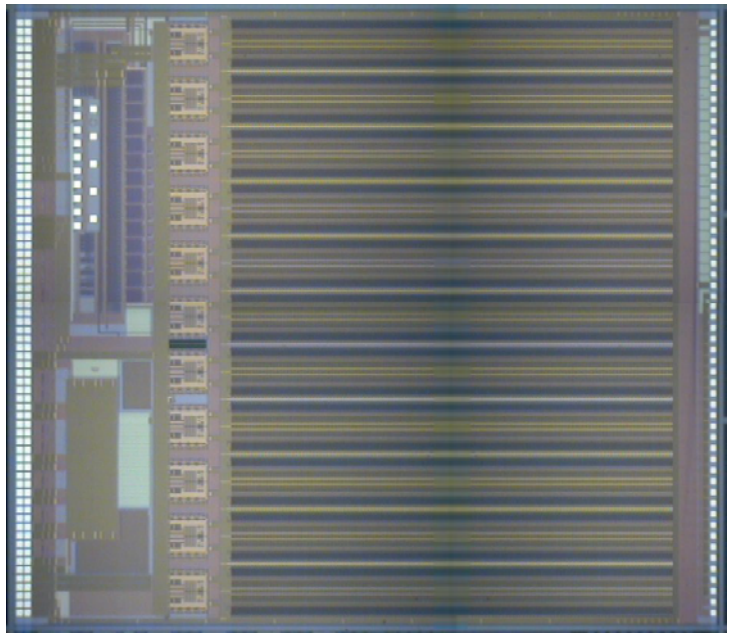
1) Silicon Tracking

- **All talks reporting on circuit designs used a 0.25 µm CMOS technology for radiation tolerance >30 Mrads.**
- **Three major designs are nearly ready for production.**
  - **Atlas pixel readout started about 10 years ago in 0.8 um rad soft process**
    - **HP => DMILL => Honeywell => IBM**
    - **18 x 160 cells, each cell is 50 x 400 µ m**
    - **Difficult time walk requirement**
    - **Uses Time Over Threshold for charge measurement**
    - **14 program bits for every cell, 40,547 program bits per chip**
    - **5 bits/cell for threshold adjust, 5 bits/cell for Time-Over-Threshold adj.**
    - **First IBM parts had low yield as well as high threshold dispersion.**
    - **Latest IBM parts have yield >90%, and good threshold dispersion.**

(tracking continued)

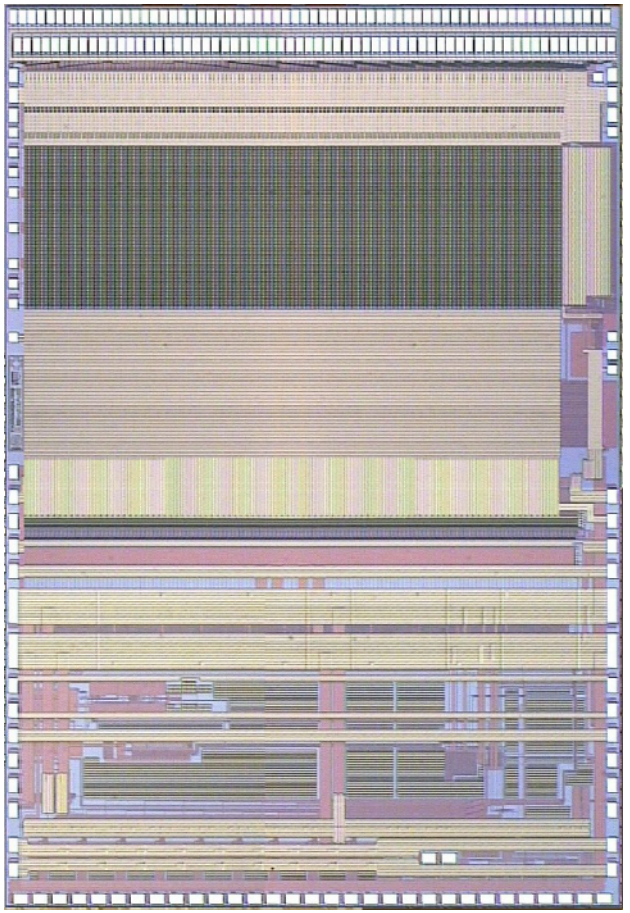
– **FPIX pixel readout development begun at Fermilab, 1997**

- **HP 0.8 μ => HP 0.5 μ => TSMC 0.25 μ**
- **22 x 128 cells, each cell is 50 x 400 μ m**
- **Designed to be used for Level 1 trigger.**
- **Has 3 bit FADC in every cell**
- **Readout every hit every beam crossing (132 nsec)**
- **Very low noise (60erms and threshold dispersion (125 erms) without trimming. (Version C)**
- **840 Mbit/sec max readout from each chip, no affect on noise**
- **Engineering run for BTEV has high yield, production pending.**



(tracking continued)

- **SVX4 silicon readout chip for CDF and DO started in 2000**
  - **TSMC 0.25 μ m process was only process used.**
  - **128 channels, 40 cell analog pipeline, 8 bit ADC, sparse readout.**
  - **Main challenge was to satisfy needs of 2 different readout systems.**
  - **Production quality parts achieved on 2nd full chip submission**
  - **Lower noise than all previous SVX designs.**
  - **Ready for production.**



2) Radiation Effects in Deep Submicron Circuits

- Total dose effects
  - V. Re reported on 0.18 μm transistors (Tox = 4 nm) irradiated to 30 Mrads, lower Vt shift than 0.25 μm, no problems found.
  - A. Marchioro reported on bandgap device in 0.13 μ m.
    - Tox = 2.2 nm, Vmin = 1.0 V
    - Non-enclosed devices, good to 120 Mrad
    - Functionally OK, but has degraded performance.
  - F. Faccio reported on test structures in 0.13 μm
    - Transistors, caps, diodes, shift registers, amps, SRAM, etc. were tested and showed good tolerance.
    - SEU cross section is higher than in 0.25 μm process, must be careful.
    - Most interesting result is that guard rings may not be necessary. Standard libraries may be acceptable except for latches.

(radiation effects continued)

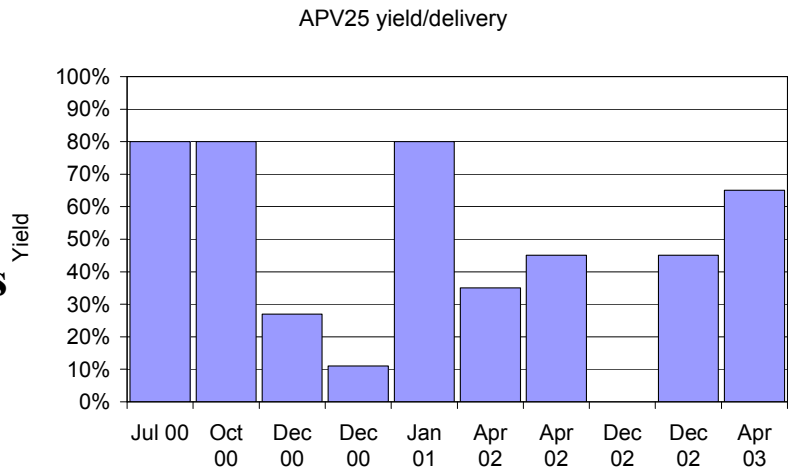
- **Single Event Effects talks**
  - **G. Gagliardi reported on SEU in the Atlas pixel Module Control Chip (0.25 µm process).**
    - **Initial design showed higher SEU than desired.**
    - **New design uses triple redundant logic throughout**
    - **New design not tested but should be acceptable.**
  - **J. Hoff compared 5 different SEU designs and layouts for SEU tolerance in 0.25µ m process.**
    - **Compared SEU tolerance and area of circuit**
    - **Heavy Ion Tolerant cell had best SEU tolerance and size.**
    - **Introduced a new cell called SEUSS that has greater design flexibility at expense of some SEU tolerance relative to the HIT cell.**
  - **Talk by T. Oldham suggests that SEE does not appear to be a problem in DSM but each new process needs to be checked.**
    - **Latch up should not be a problem because of low PS voltages.**

3) Monolithic and CCD Devices

- Relatively new area compared to developments in silicon strips and pixels - extension of shrinking electronics
- New area may represent the future for vertex detectors.
- Active Pixel Architectures (G. Marrella)
  - **Use standard 0.18 µm CMOS for sensor and readout electronics**
  - **Very small pixels (3 µm x 3 µm), frame by frame readout.**
  - **Test results not yet available.**
- Active Pixel Sensors for HEP and Space (R. Turchetta)
  - **Using TSMC 0.25 µ CIS (CMOS Image Sensor) process**
  - **In pixel amplifiers and/or storage**
  - **Thinning to 50 µm thickness**
  - **Numerous approaches being studied for applications like LC**
- Linear Collider CCD Readout (M. French)
  - **Studying parallel column readout with sparsification**

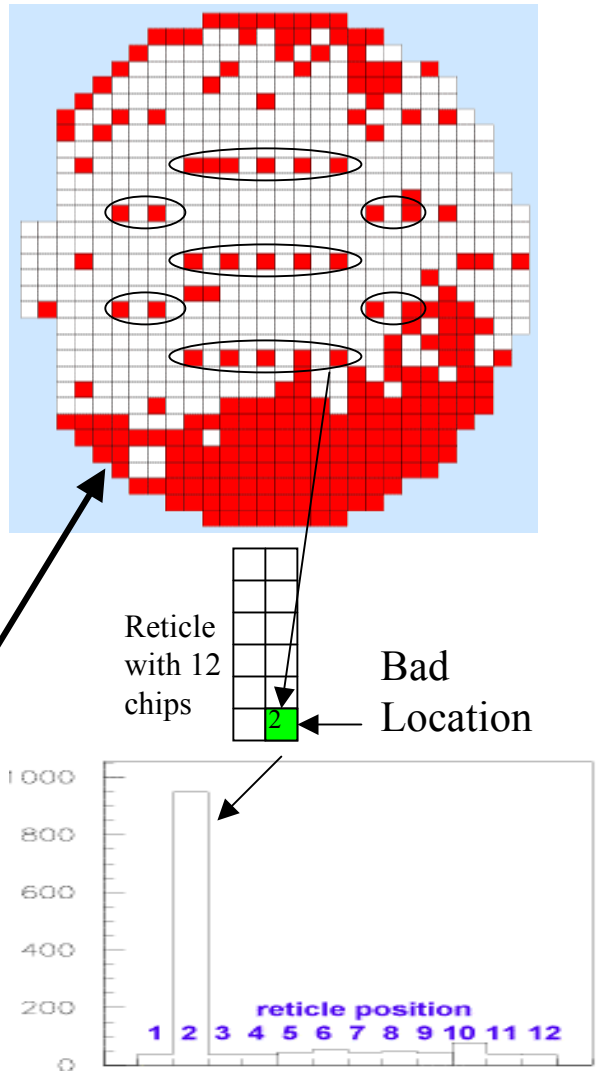
4) Reliability and Production

- **Silicon strip readout chip for ATLAS (A. Grillo)**
  - **First production run in DMILL (DMILL is now obsolete)**
  - **50,000 chips required for system, made ~ 1000 wafers (250K chips)**
  - **Wafer level probing showed relatively poor yield.**
  - **Good test system is critical for first production lots**
  - **"The unexpected is always going to happen."**
- **Yield in IBM 0.25 µm process (F. Faccio)**
  - **Yields have fluctuated dramatically**
    - **21 mask sets released, problems with 5 different projects**
    - **Yields range from 0% to 80% on a number of MPW and dedicated runs**
    - **Problem traced to incomplete vias is thought to be solved**
  - **Lessons learned**
    - **Going from prototype to production is not necessarily fast and easy.**
    - **Design rules do not cover all possible design configurations.**
    - **HEP designs are often different from typical foundry designs.**



(reliability and production continued)

- **Testing of TSMC 0.25 um Devices (W. Wester)**
  - **Wafer deliver is high, 58 out of 61 wafers started (95%)**
  - **In addition to MPW runs, had 3 engineering runs with 9 different designs (major designs include SVX4, TRIP, FPIX).**
  - **Yields on all designs is >90% including large chips.**
  - **Example: SVX4 engineering run, 98% functional, 91.2 % perfect.**
  - **On other processes, found significant failure patterns that could only be investigated if wafer level testing was done.**
  - **0.25 µm TSMC process appears to be incredibly solid with consistent high yields.**



5) Special Front End Circuits

- Many talks on a wide variety of designs
- Processes used include DMILL, IBM 0.25 μm, TSMC 0.18 μm, HP 0.5 μm, TSMC 0.25 μm, AMS 0.35 μm, UMC 0.18 μm
- Projects include
  - ASDBLR straw tube readout chip and DTMROC timing chip, both for Atlas Transition Radiation Detector.
  - Octal ASD for the Atlas Muon Detector
  - Readout chip for Visible Light Photon Counters at Fermilab (DO).
  - 32 channel GEM (Gaseous Electron Multiplier) TPC at Laser Electron Gamma Source (LEGS).
  - 0.18 μ PET front end circuit for RatCAP (RAT Conscience Animal PET), P. O'Connor

(special front-end circuits continued)

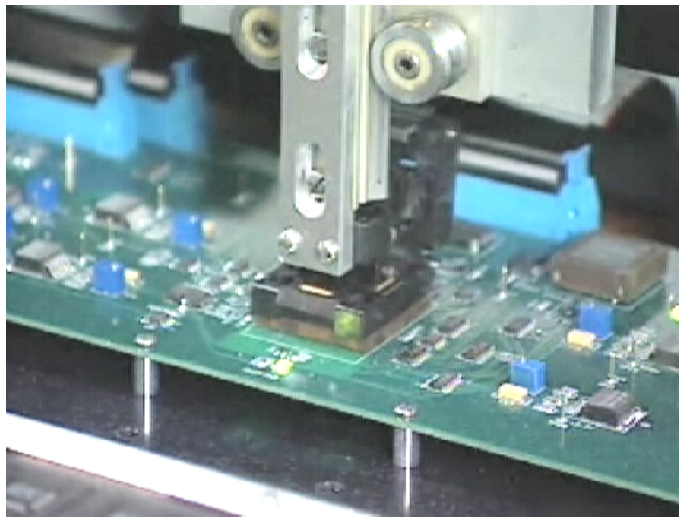
- ALICE TRD TRAcklet Processor (TRAP) – most ambitious chip in this session. (V. Lindenstrudh)
  - Eighteen 10 bit, 10 MHz ADCs
  - Digital filter with pedestal and tail correction
  - 64 time bin buffer
  - Data preprocessor
  - MIMD processor (4 RISC CPUs, 32 bit data) that fits tracklets, compresses and ships raw data
  - High speed readout
  - Serial interface for configuration registers
  - Power management circuitry (low power design)
  - Simultaneous operation of ADC and processors works well

6) Front End Chips for Calorimeters

- **Two talks (FPPA, MGPS) were presented on CMS EM Calorimeter readout chips.**
  - **The MGPA is now the baseline (July '03):**
    - **Three gain ranges (1, 6, 12) device in 0.25 um CMOS**
    - **Sends voltage output to radiation hard 12 bit ADC designed by outside vendor**
    - **MGPA seems to be working well, ADC needs work to improve NEB from 9.5 to 11**
    - **MGPA has fewer power supplies than FPPA and is much less expensive.**
  - **Now assembling boards to test MGPA, ADC, Fenix receiver chip operation**

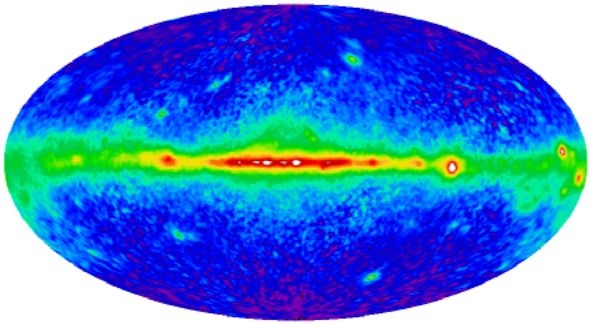
(Front End Chips for Calorimeters continued)

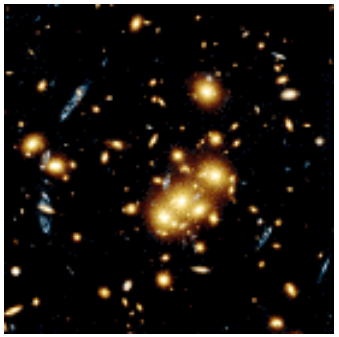
- **Charge integrating and digitizer chip (QIE8) for HPDs and PMTs in CMS hadron calorimeter (T. Zimmerman)**
  - **Switchable gain and polarity inputs for two different detectors.**
  - **Four non-binary weighted auto-selected ranges, selected range sent to FADC while range number is encoded as 2 bit exponent.**
  - **On chip 5 bit non-linear ADC provides necessary resolution**
  - **Testing of production parts with newly designed robotic tester is in progress.**
  - **Yield is good.**



7) Experiments in Space

- Numerous talks showed merging of HEP technology into space experiments
- Projects include chips for:
  - GLAST (Gamma ray Large Area Space Telescope), Sept. 2006, R. Bellazzini
    - Discussed the profound connection between HEP and Astrophysics.
    - 880,000 Silicon strip detectors from 6" wafers, 1536 CsI crystal calorimeter, 89 plastic scintillating tiles.
  - AMS 02 EM Calorimeter, anti-matter, dark matter, cosmic rays, 2005
  - PAMELA (2 talks) tungsten imaging calorimeter, and silicon tracker data acquisition system, 2004
  - SNAP CCD multi-range signal processor, ??





Dark matter

Summary

- The Front End Electronics Meeting
  - Has gone beyond scope of first meeting (1990) intended for tracking.
  - Includes other related areas needing IC design for front end electronics.
  - Primary focus is on integrated circuit design.
  - Meeting place for IC designers and other interested parties to meet and discuss progress and various problems in a relaxed setting.
- Next meeting expected to be in 2006 in Europe