Recent SPi tests and setups

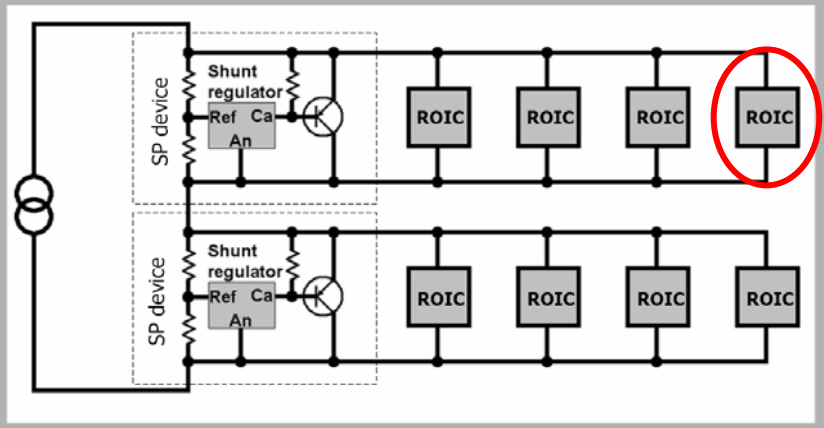
M.Trimpl, Fermilab

- SPi motivation
- chip architecture and features
- SPi 001 test results (Shunt, ADC, current alarm, power down)
- summary and outlook

on behalf of:
A.Dyer, G.Deptuch, C.Gingu, J.Hoff, A.Shenai, M.Trimpl, R.Yarema, T.Zimmerman – FNAL
R. Holt, G.Villani, M.Weber - RAL
N.Dressnandt , M.Newcomer - UPenn
D.Lynn, J.Kierstead - BNL

Serial Powering Schemes

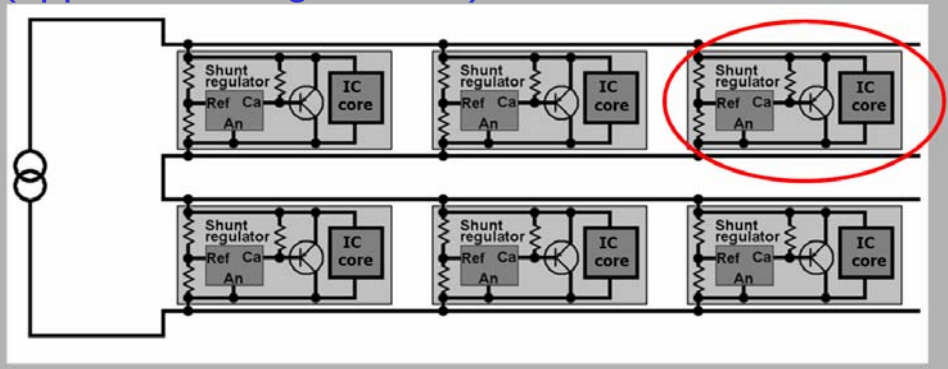
1) External shunt regulator + transistor



implies a **high current shunt**

SP device enables to operate non SP-ROIC in SP mode

2) Internal shunt regulator + transistor in each ROIC (approached e.g. in FEI4)

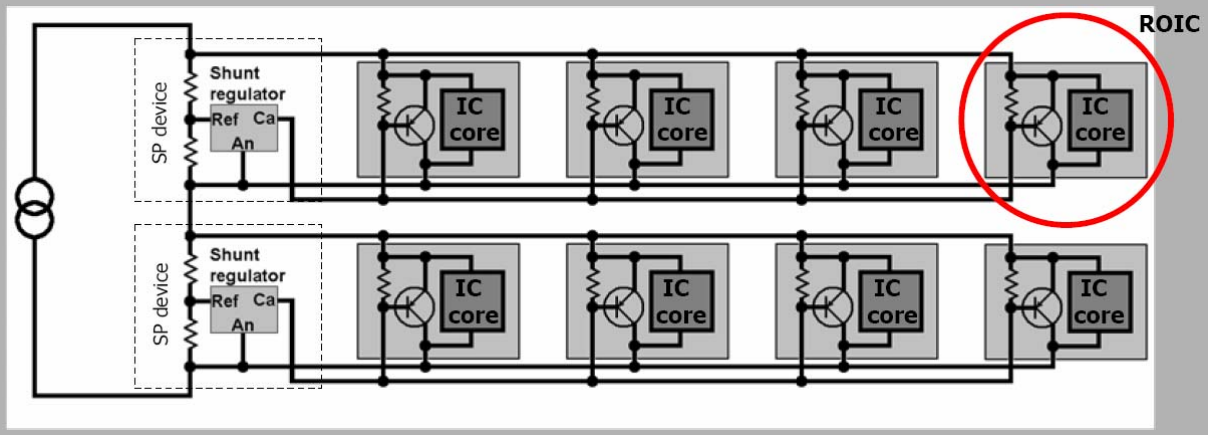


challenge: many power supplies in parallel

Matching issue can cause hot spots and potentially kill chips

adjustment/trimming scheme needed

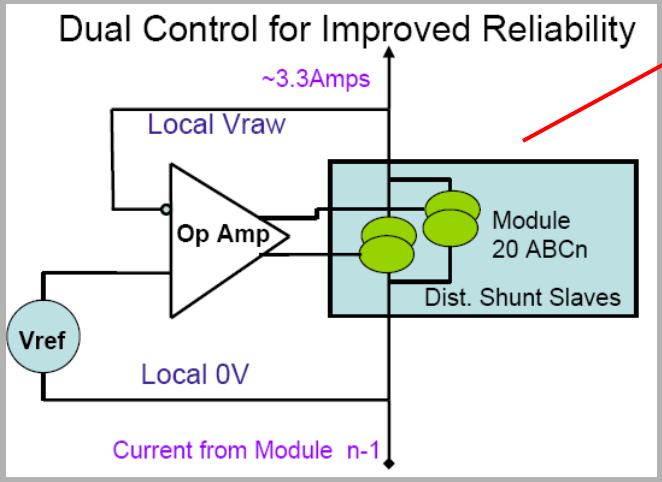
3) External SR + parallel shunt transistor in ROIC

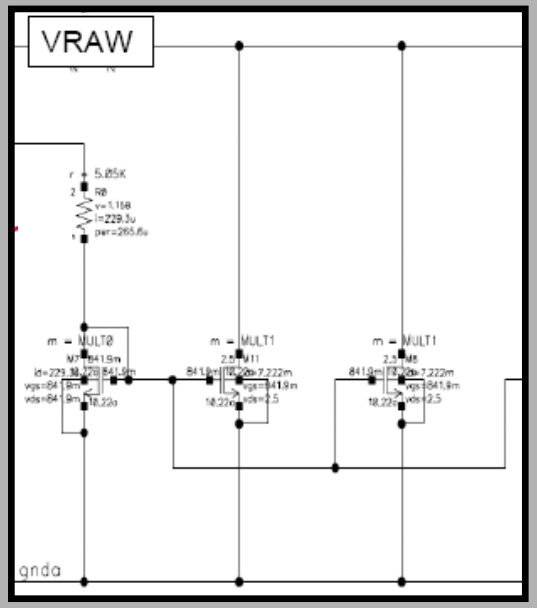


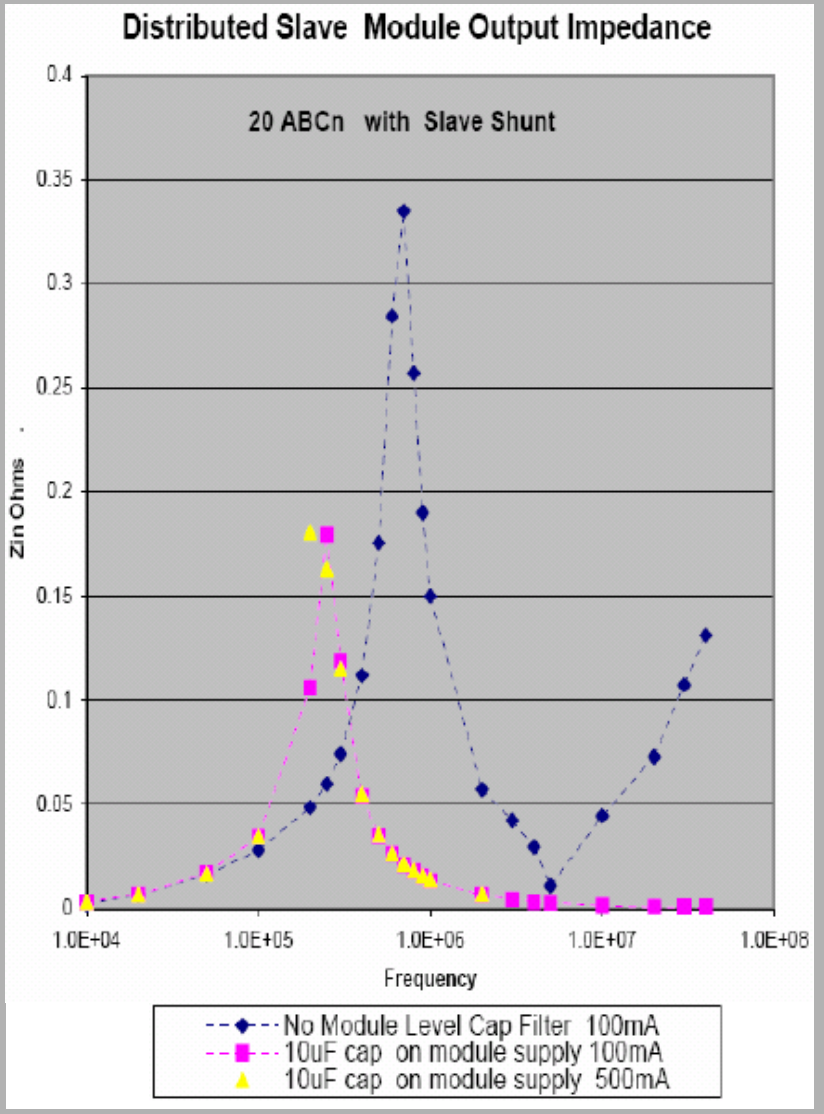
feedback however **more challenging** and depends on implementation

- choice of architecture **not obvious**, detailed studies anticipated by various groups
- scheme (2) can be realized by any ROIC standalone
- **SPi chip covers scheme (1) and (3)**

distributed shunt concept







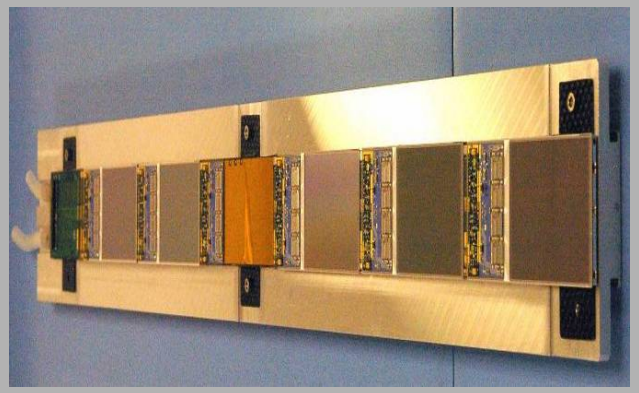
[M.Newcomer UPenn]

concept / realization

- class AB stage with dual output for redundancy
- shunt slaves are implemented in ROIC (ABCn)
- discrete OPAmp used to operate ABCn
  shunt slaves presently at RAL (p.o.c.)
- similar distribution concept (trimming currents) proposed and implemented by Dabrowski et al. in ABCn

SP setups and SPi Motivation

- Serial powering is not new (see. vertex 2002 talk T.Stockmanns, SP of ATLAS pixel)
- Setups using discrete components explored SP feasibility and new features
  (current monitoring and over current protection)

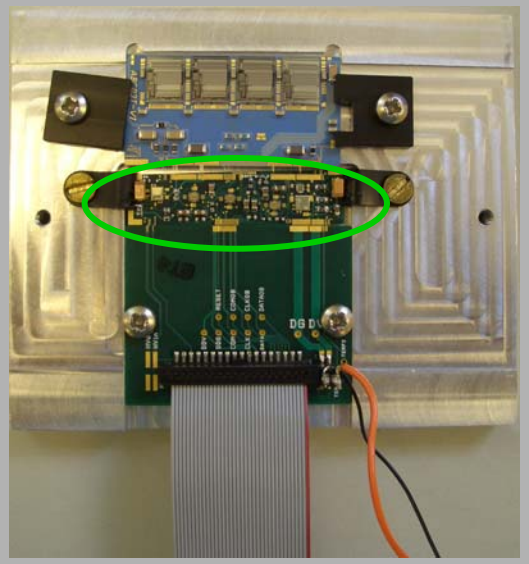


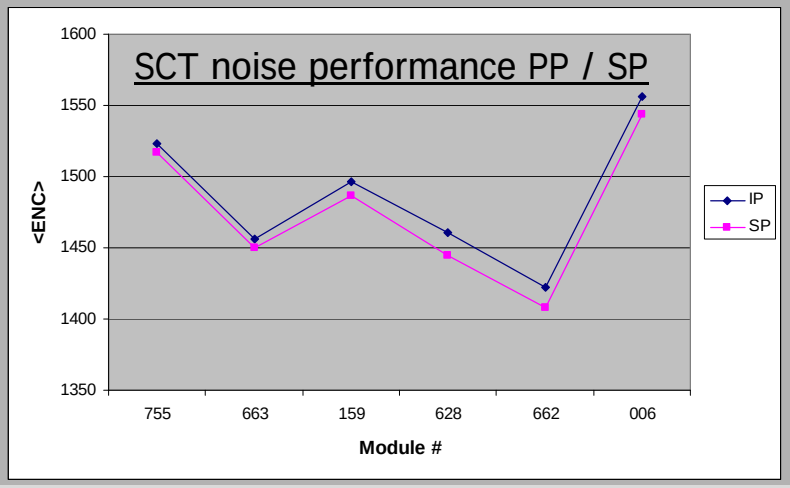
ATLAS SCT setup at RAL / LBNL
(similar setups at BNL, Atlas pixel at UBonn)

Downsides of discrete setups

- Standard Shunts typ. current limited (<< 4A)
- Power transistors not rad. tolerant
- esp. 4A for module is challenging
- spacious setup
- limited performance (e.g. dyn. impedance)

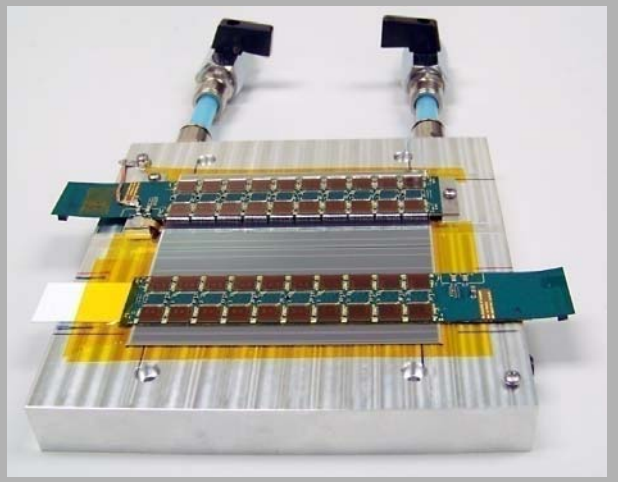
-> integrated / customized solution



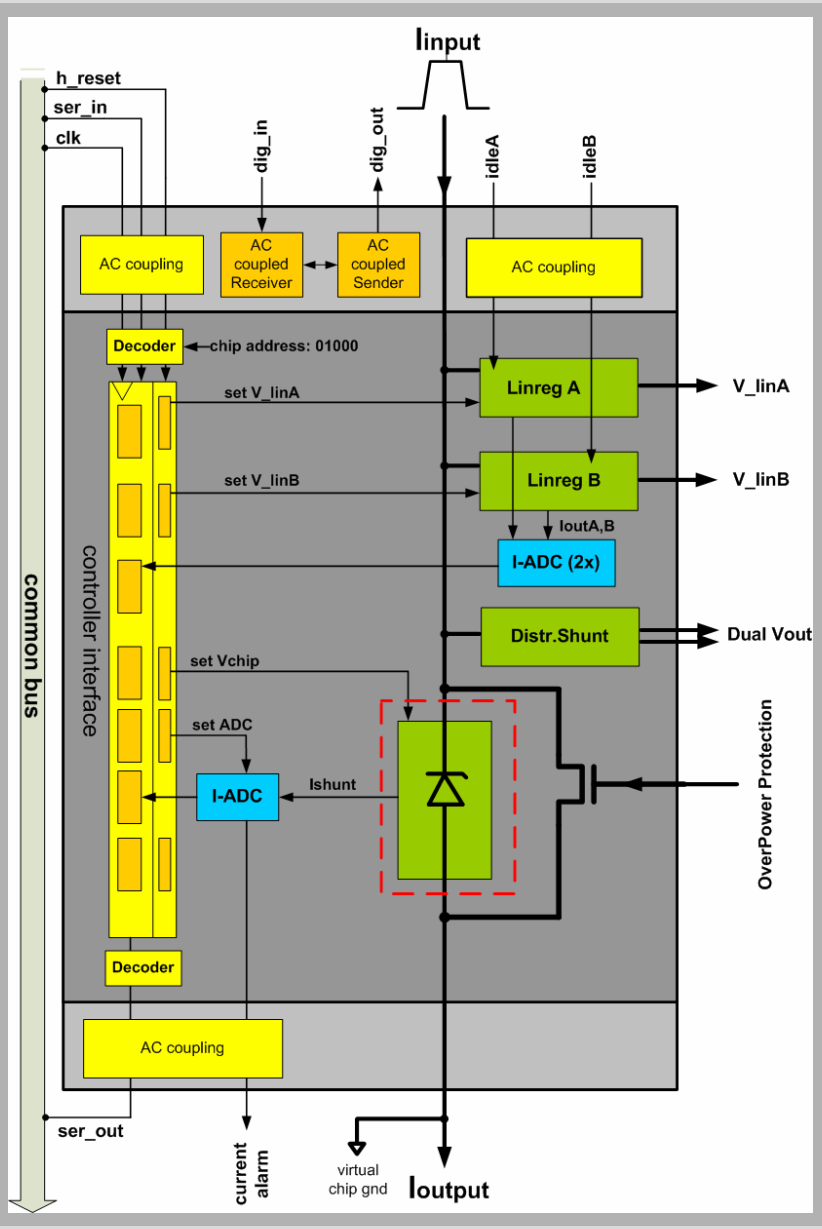


'ABCn module approach':

2x 2x10 ROIC on a module,
10 modules in a row
(clearly needs
integrated solution)



SPi – Architecture Overview

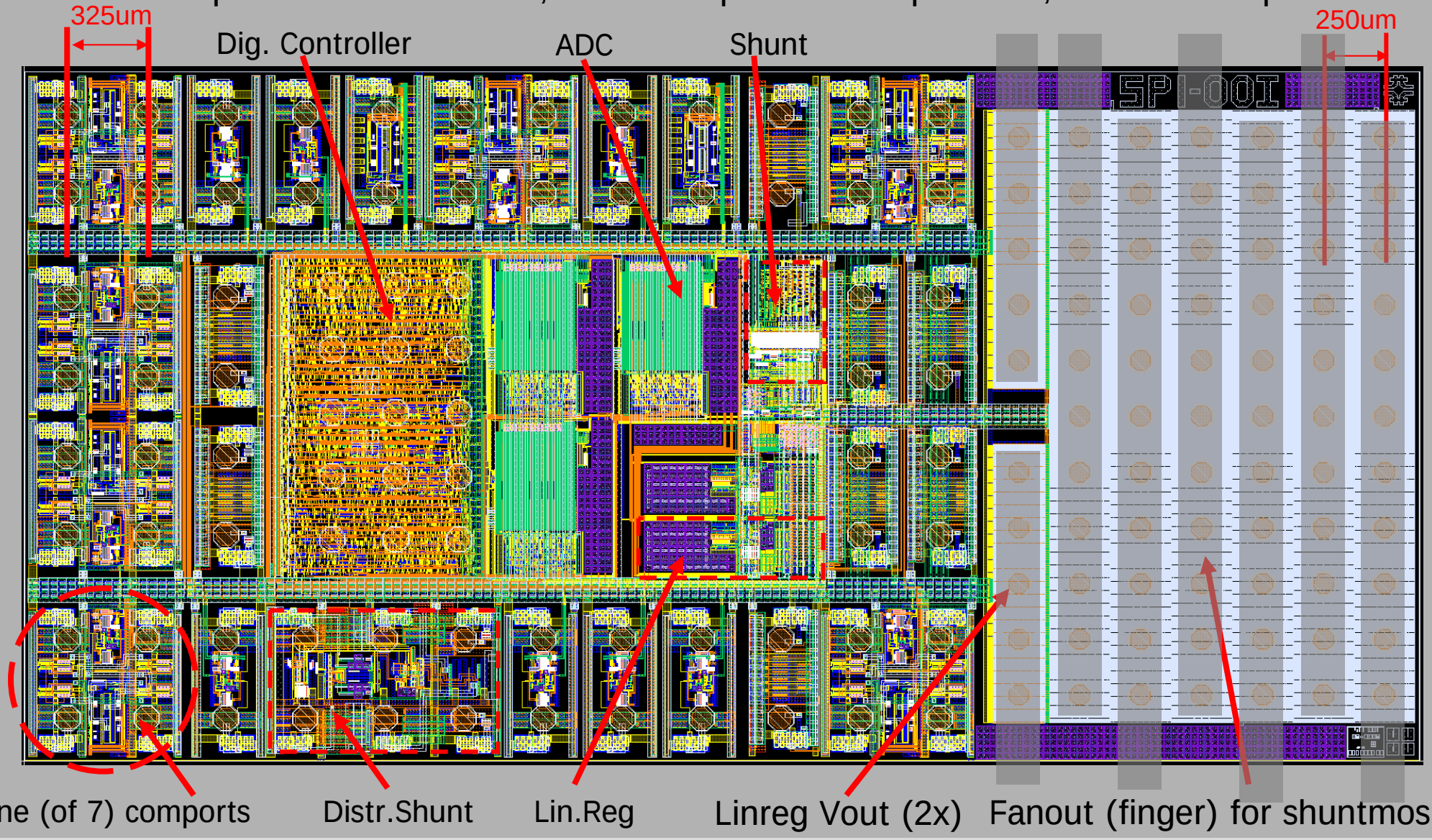


main focus on versatility - list of basic features:

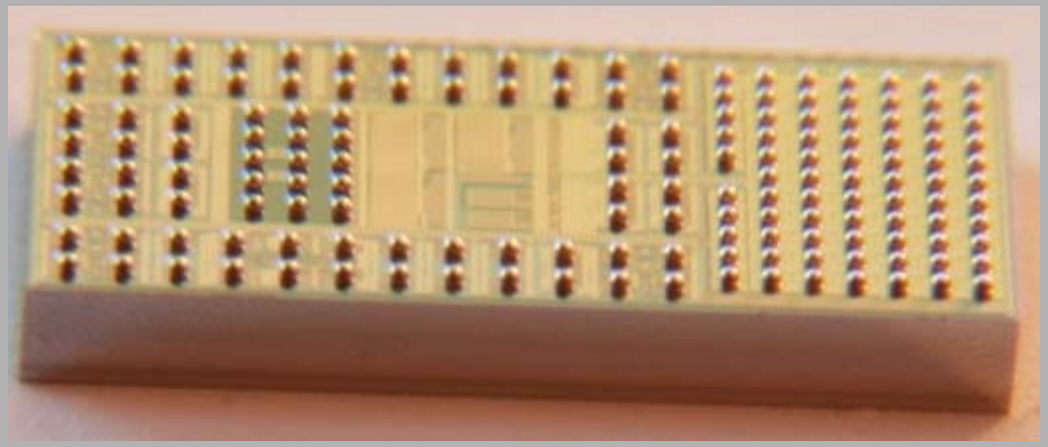
- **shunt** creates Vchip 1.2...2.7V, 4A (scheme1), distr. shunt (scheme3)
- communication via **multi drop** bus (each SPI chip has 5bit address) reduces number of str.-lines for SPI to minimum of 2 (3)
- AC coupled LVDS, spare interface port (**comports**)
- **ADC**s to monitor shunt and LR current
- current alarm with programmable threshold and trigger delay
- **OverPower** protection: power FET to bypass module
- **2x LinReg**: separate analog / digital supply: 1.2 .. 2.5V optinal feature to hook up some chips (1-3) for tests
- **radtol. design** techniques, TSMC 025MM process

SPi 001 - Layout / Floorplan

Chip size: 5.7 x 2.8 mm^2, ~150 bumps solder chip to PCB, submitted Sept08



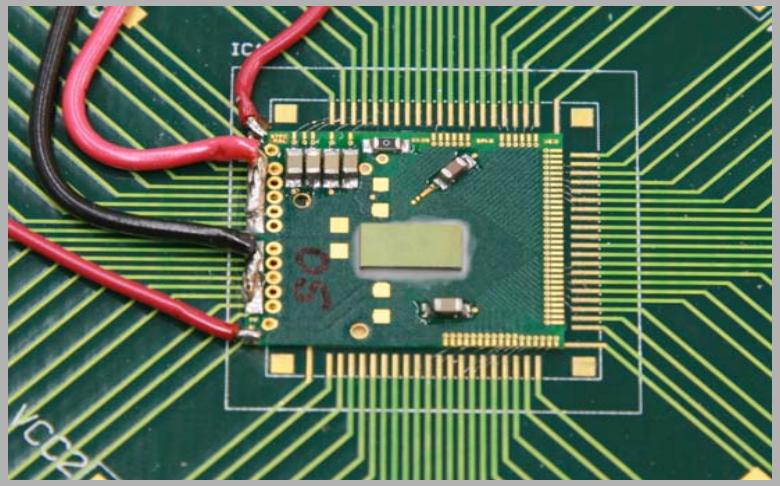
test setup /assembly



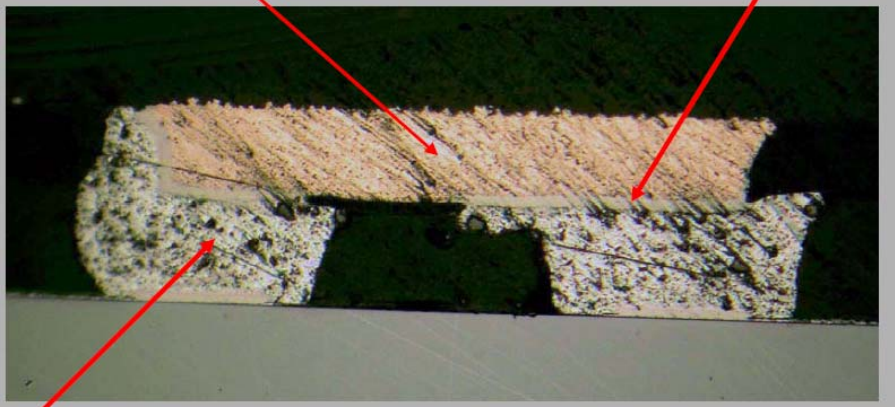
SPI001 (back since Nov2008), solder bumps placed by TSMC

Advantages of bumps bonds (for the SPI chip)

- **better routing flexibility** (high currents)
- more robust and shorter (100um vs 5mm) as wire bonds
- **reliable connection is essential in SP scheme**
- better scale ability (tailored to required current)
- chip backside fully accessible for cooling / temp.monitor

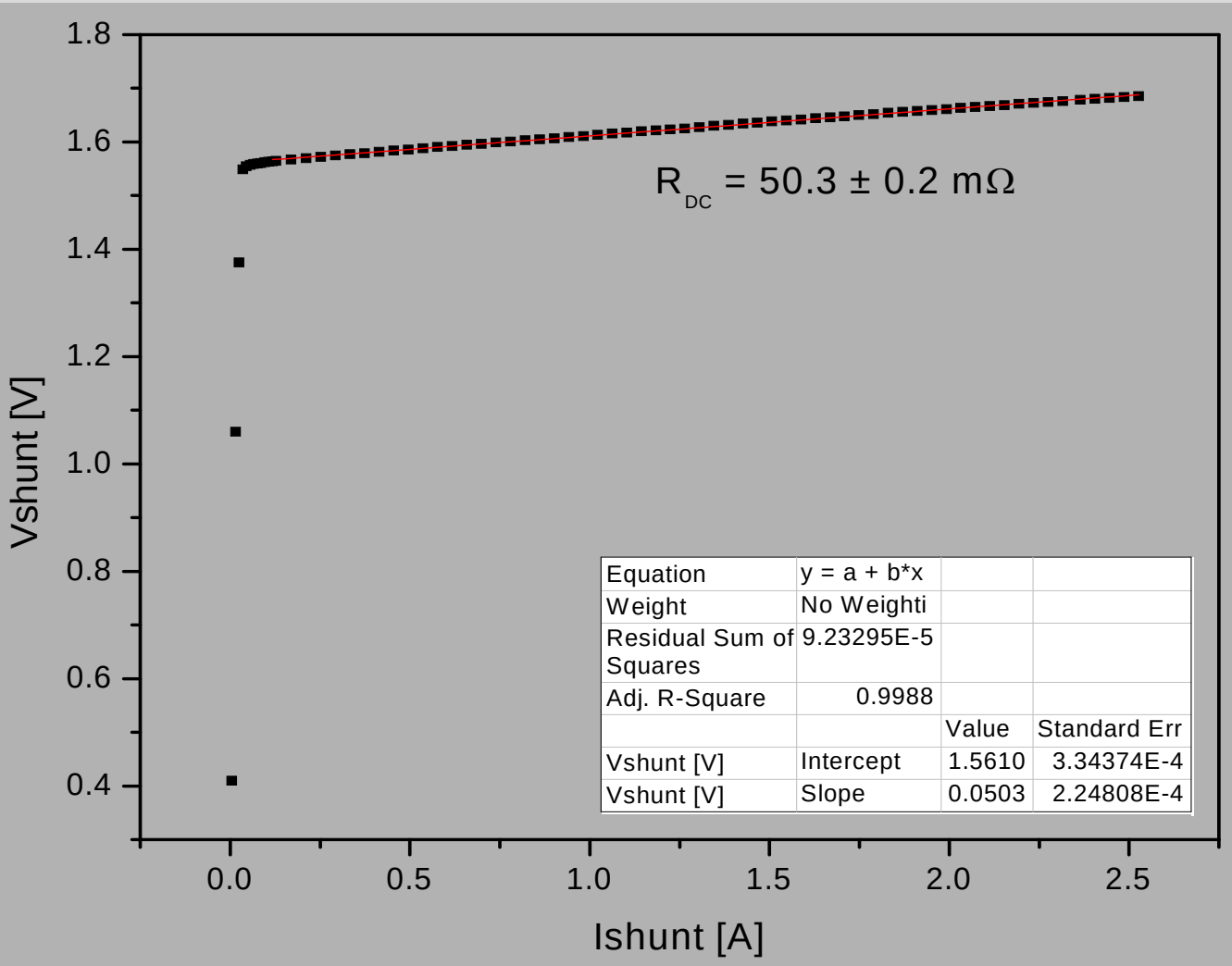


- daughter board (R.Holt, RAL)
- FCOB assembly done at SiDet (E.Skup, FNAL)



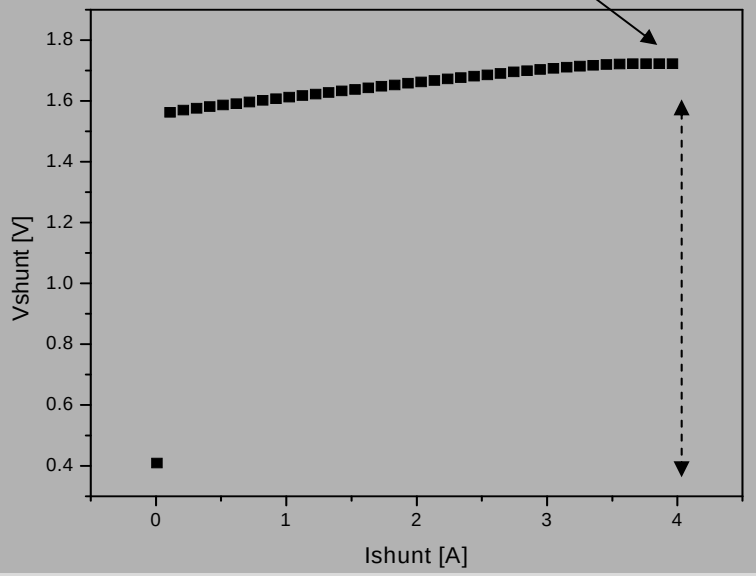
(FCOB on standard FR4)

results: DC shunt characteristics



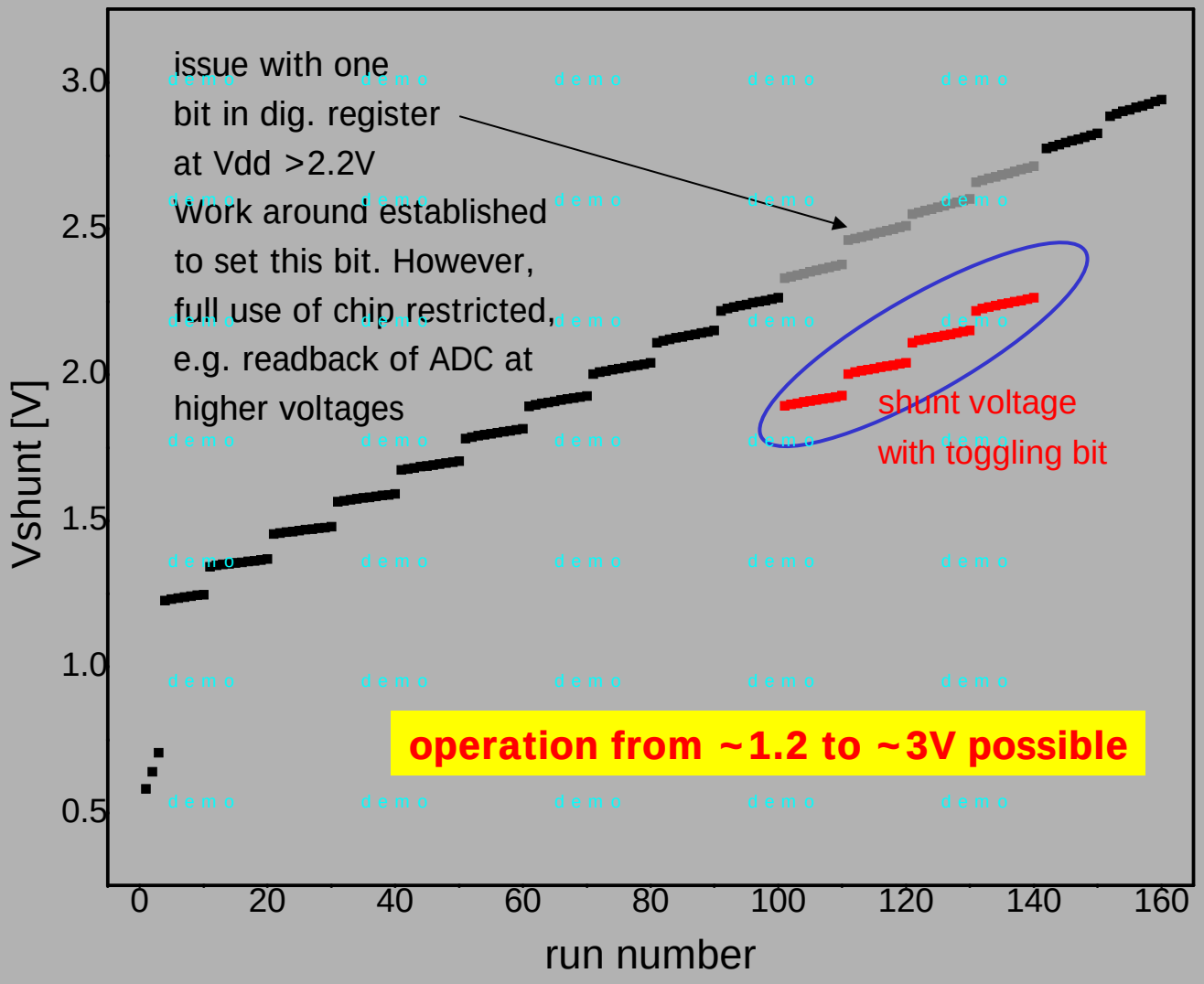
Equation	y = a + b*x		
Weight	No Weighti		
Residual Sum of Squares	9.23295E-5		
Adj. R-Square	0.9988		
		Value	Standard Err
Vshunt [V]	Intercept	1.5610	3.34374E-4
Vshunt [V]	Slope	0.0503	2.24808E-4

- power on reset to 1.5V
- 50mΩ total resistance!
- operation up to **4A @ 1.5V** demonstrated



sweeping shunt voltage

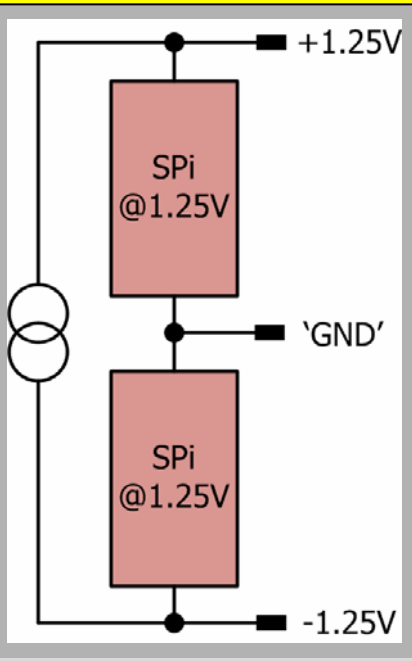
(each voltage step shows current sweep from 50mA to 500mA)



stable operation / communication at 1.25V

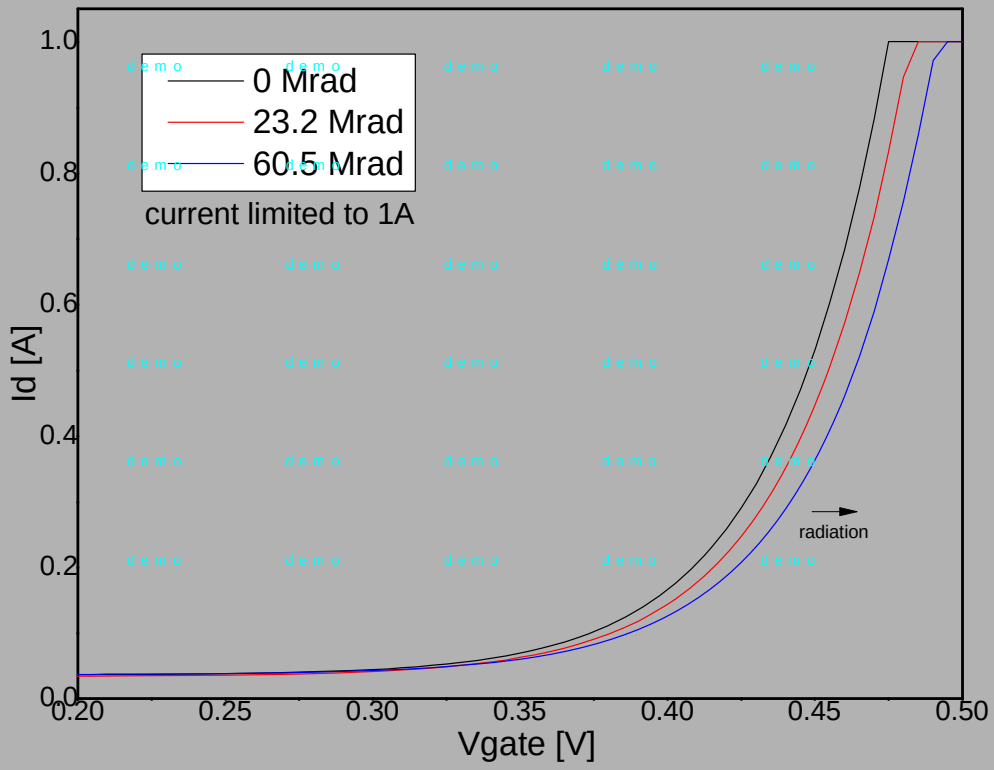
=> **opportunity to operate bipolar powered FE-designs in 0.25um** (such as the APV25)

also (potentially) ready for ABCn in 130 nm

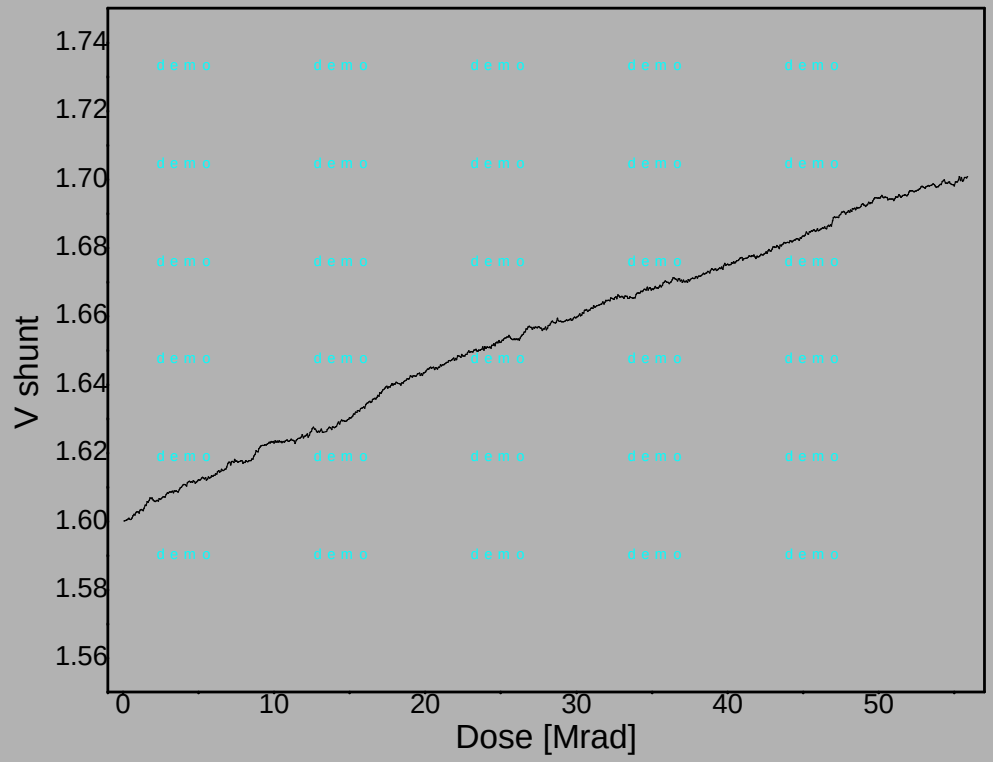


Radiation test

Bypass power-FET behavior

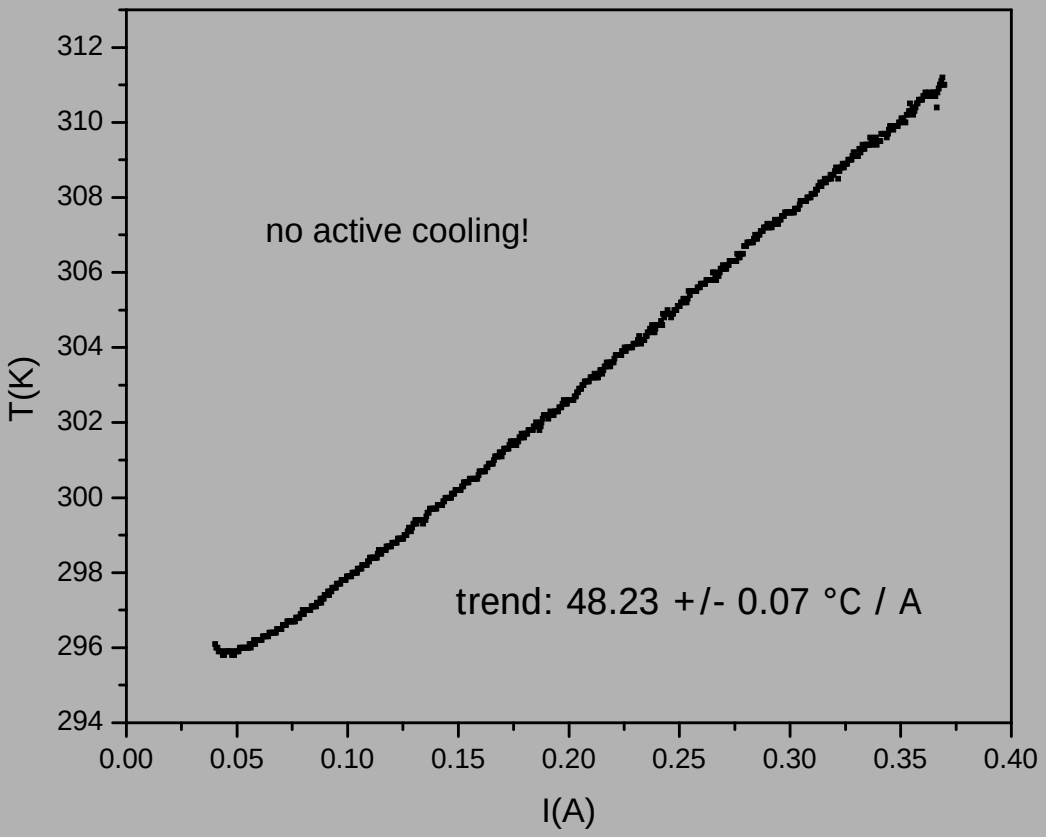


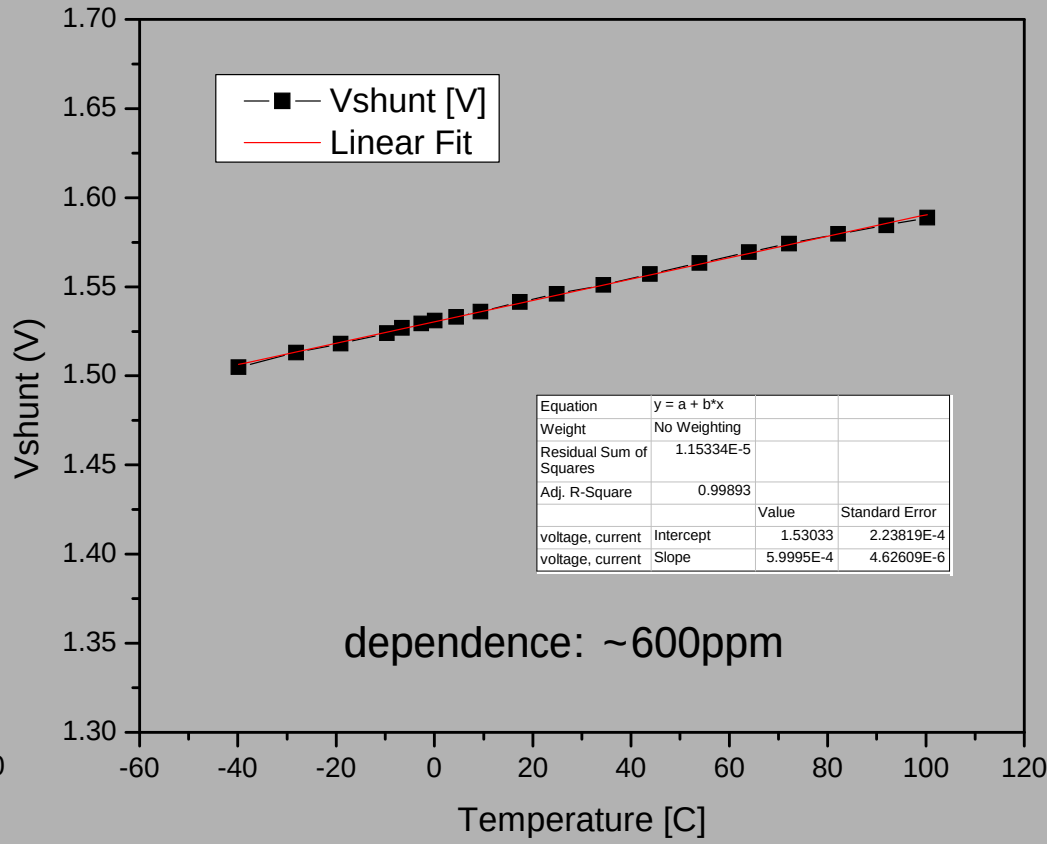
Shunt voltage dependency



- Co60 gamma at Solid State Physics Irradiation Facility at Brookhaven National Laboratory
- Fully use of annular nmos in design
- Voltage swing of 700mV to toggle FET much higher than threshold shift
- Shunt voltage shift of ~6% (100mV) after >50MRad

temperature behavior



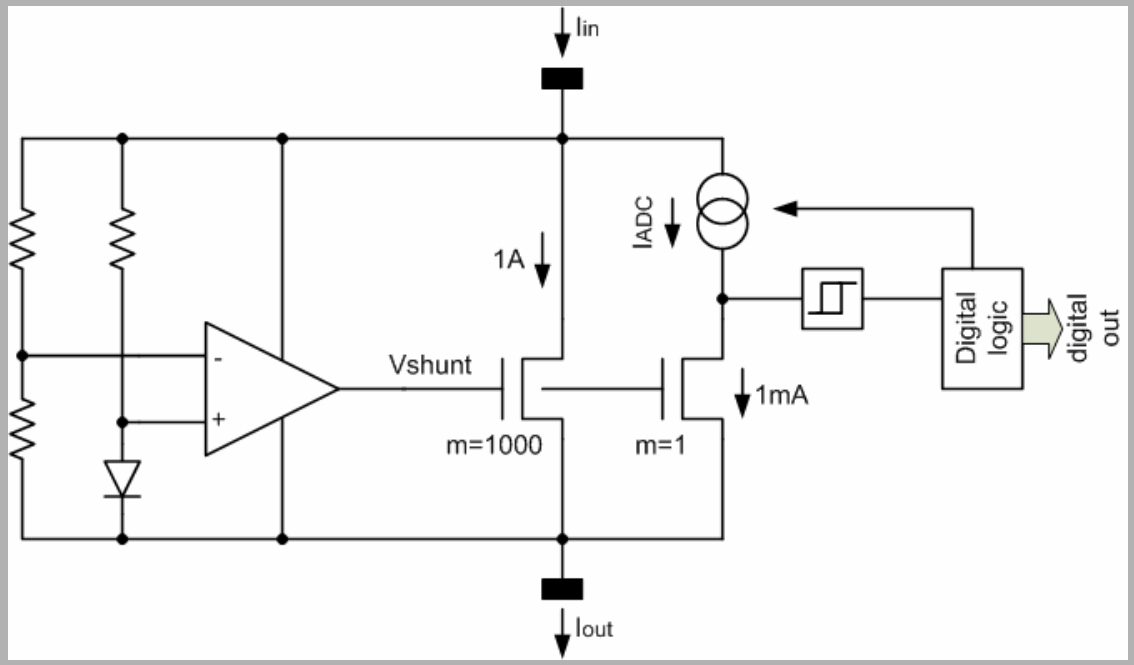


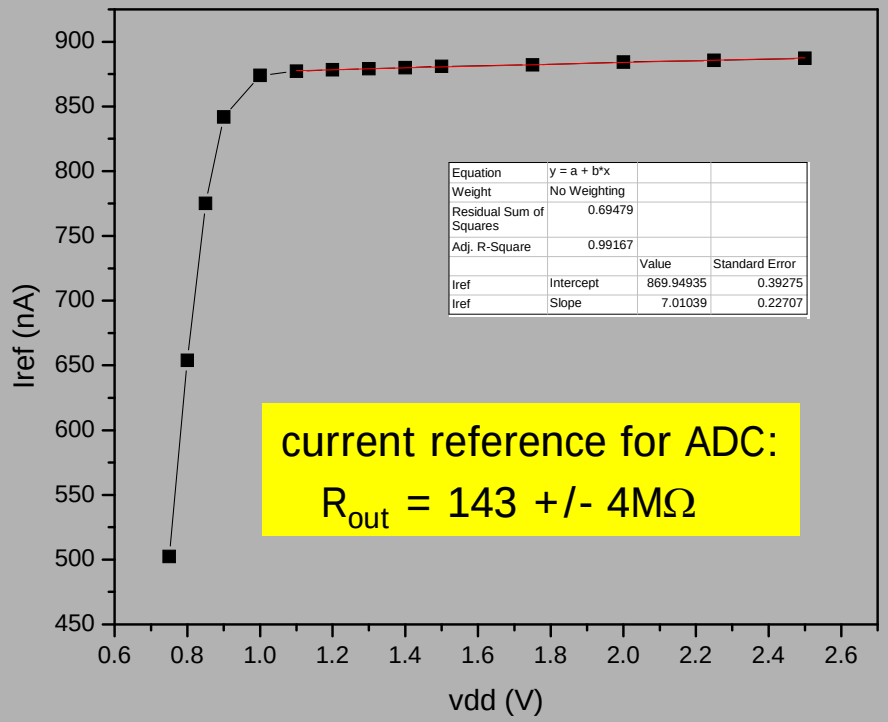
Equation	y = a + b*x		
Weight	No Weighting		
Residual Sum of Squares	1.15334E-5		
Adj. R-Square	0.99893		
		Value	Standard Error
voltage, current	Intercept	1.53033	2.23819E-4
voltage, current	Slope	5.9995E-4	4.62609E-6

- observed temperature trend: ~ 50 °C / A (no cooling)
- with CPU fan air cooling SPi backside:
  0 .. 2A @ 1.5V → T = 27...78 °C (~ 50 °C)

- operation at -40... +100 °C
- also demonstrates bump durability

'shunt' ADC – principle and implementation





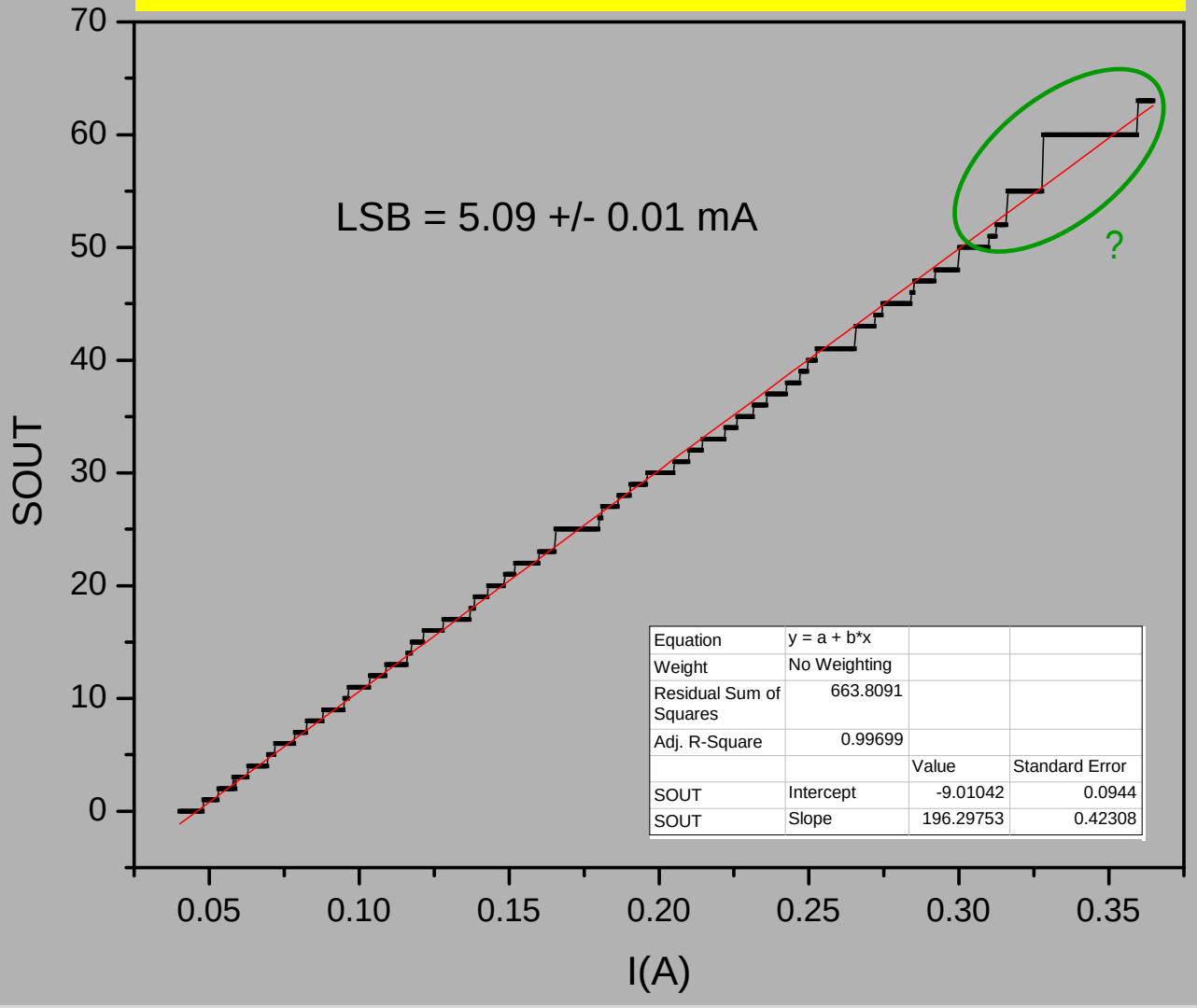
concept:

- probing shunt current using replica mos (similar to current mirror)
- current-mode ADC
  (advantageous for ultra low voltage: 1.2V in a 2.5V process!!)
- 6bit flash ADC implemented
- LSB tunable (4bit) – dyn. range ~100mA ... ~2A (probing low current or high range)
- adjustable threshold for alarm
- 4bits to tune the alarm - delay (TOT requirement): ~150us ... ~2.5ms

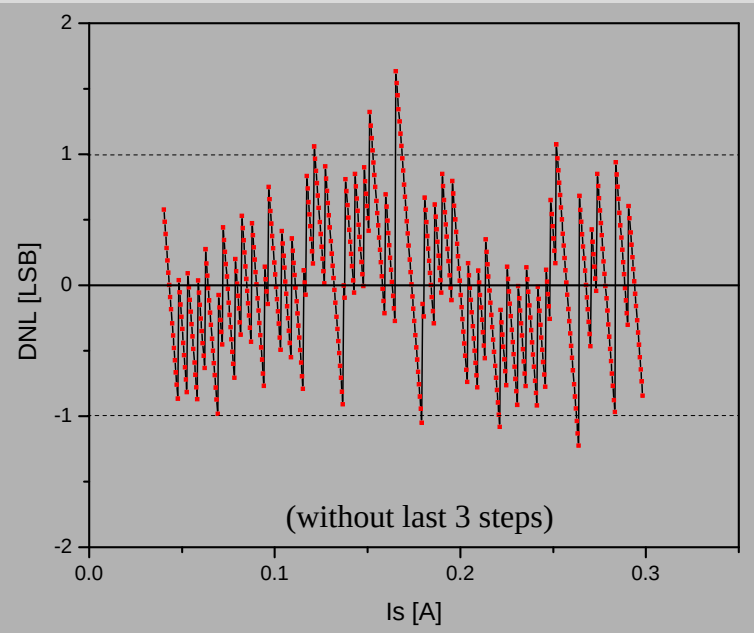
shunt ADC – quantitative behavior

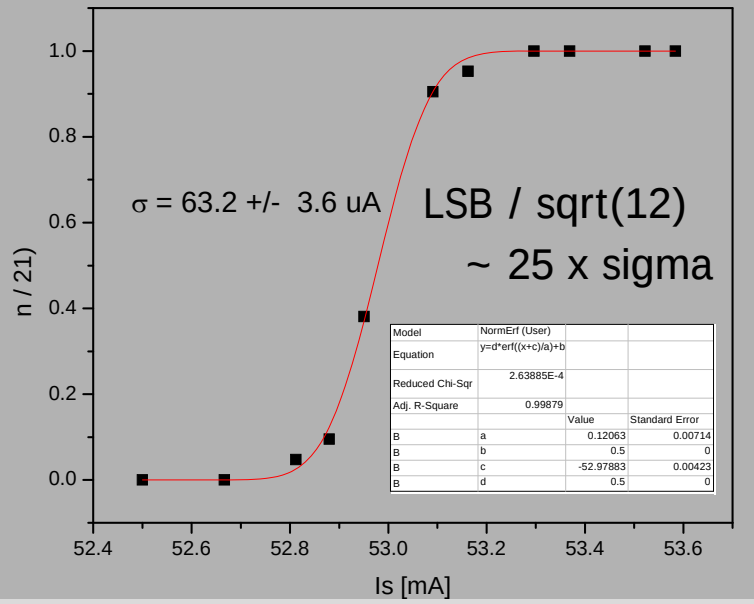
on chip ADC fully functional

and can be used to monitor the current distribution



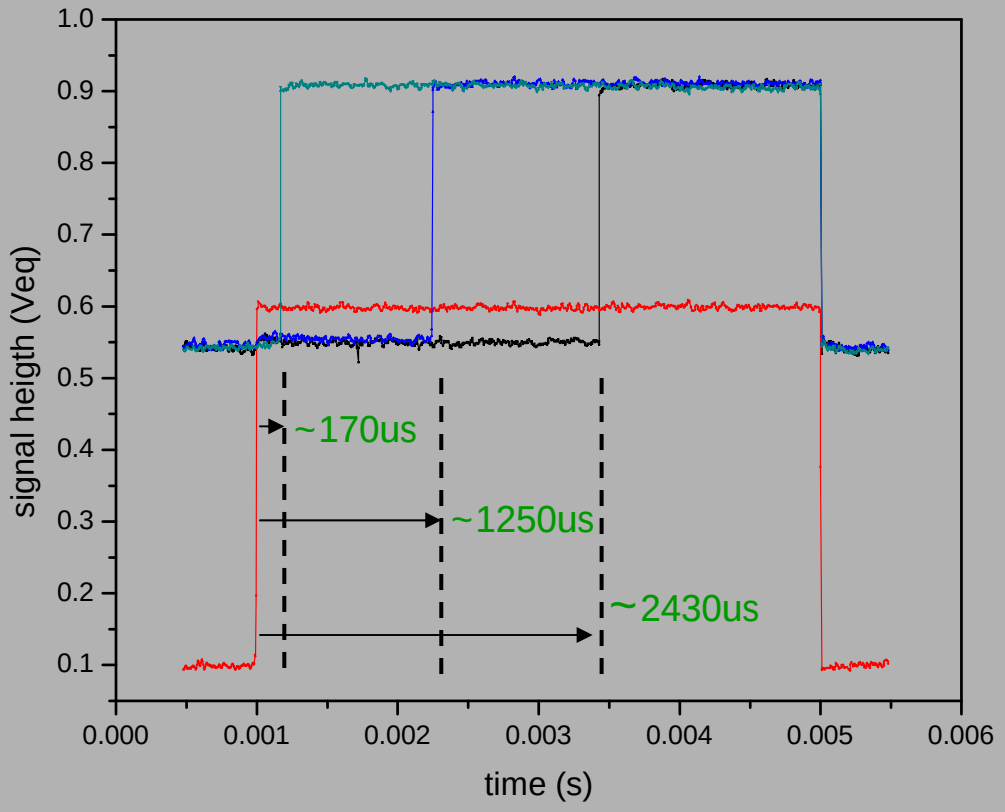
Equation	y = a + b*x		
Weight	No Weighting		
Residual Sum of Squares	663.8091		
Adj. R-Square	0.99699		
		Value	Standard Error
SOUT	Intercept	-9.01042	0.0944
SOUT	Slope	196.29753	0.42308





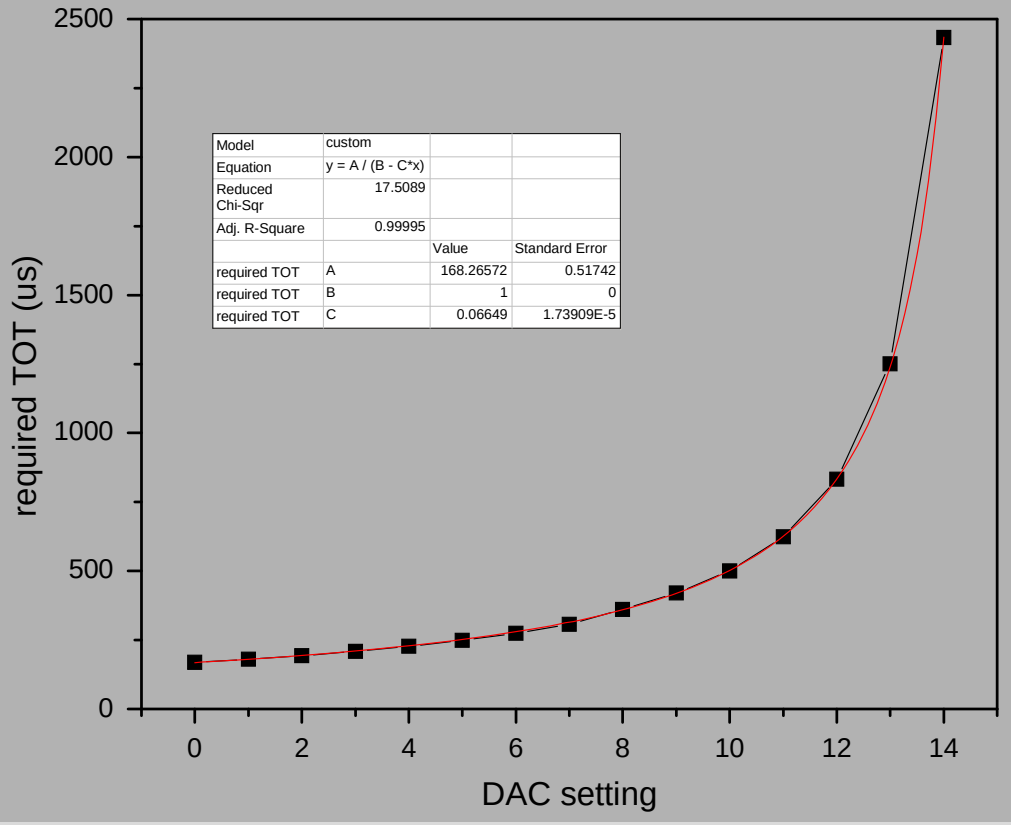
Model	NormErf (User)		
Equation	y=d*erf((x+c)/a)+b		
Reduced Chi-Sqr	2.63885E-4		
Adj. R-Square	0.99879		
		Value	Standard Error
B	a	0.12063	0.00714
B	b	0.5	0
B	c	-52.97883	0.00423
B	d	0.5	0

ADC current alarm delay



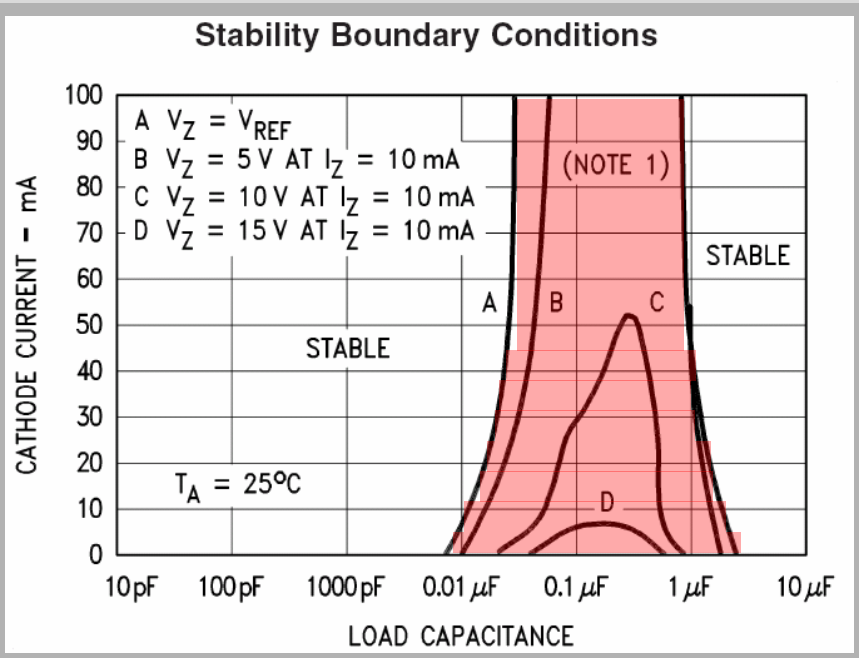
current step: 50mA... 600mA
over current alarm: (DAC delay: 0E)
(DAC delay: 0D)
(DAC delay: 00)

4bit DAC sets
tot-requirement
~150us ... ~2.5ms
for alarm trigger



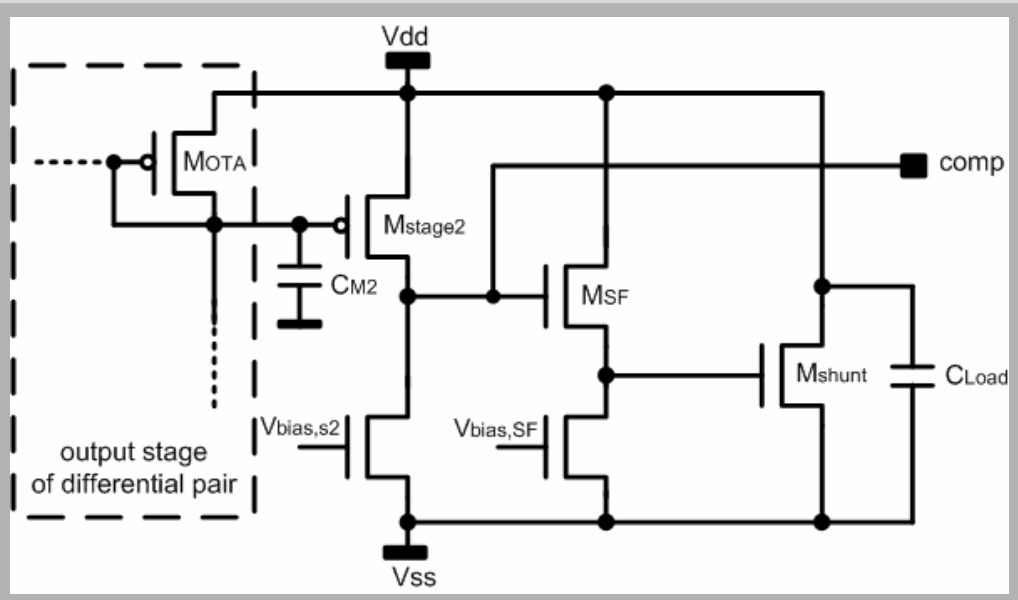
Model	custom		
Equation	y = A / (B - C*x)		
Reduced Chi-Sqr	17.5089		
Adj. R-Square	0.99995		
		Value	Standard Error
required TOT	A	168.26572	0.51742
required TOT	B	1	0
required TOT	C	0.06649	1.73909E-5

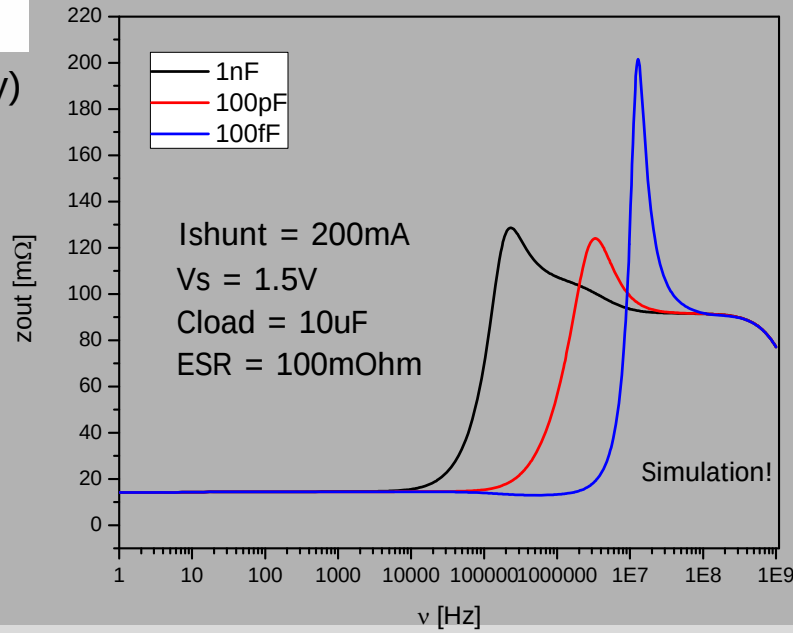
shunt stability



LM431 – National Datasheet (for illustration only)

- shunt circuit stable for high and low load capacitances
- region of instability for intermediate cap. load
- use optional compensation cap. to create dominant pole





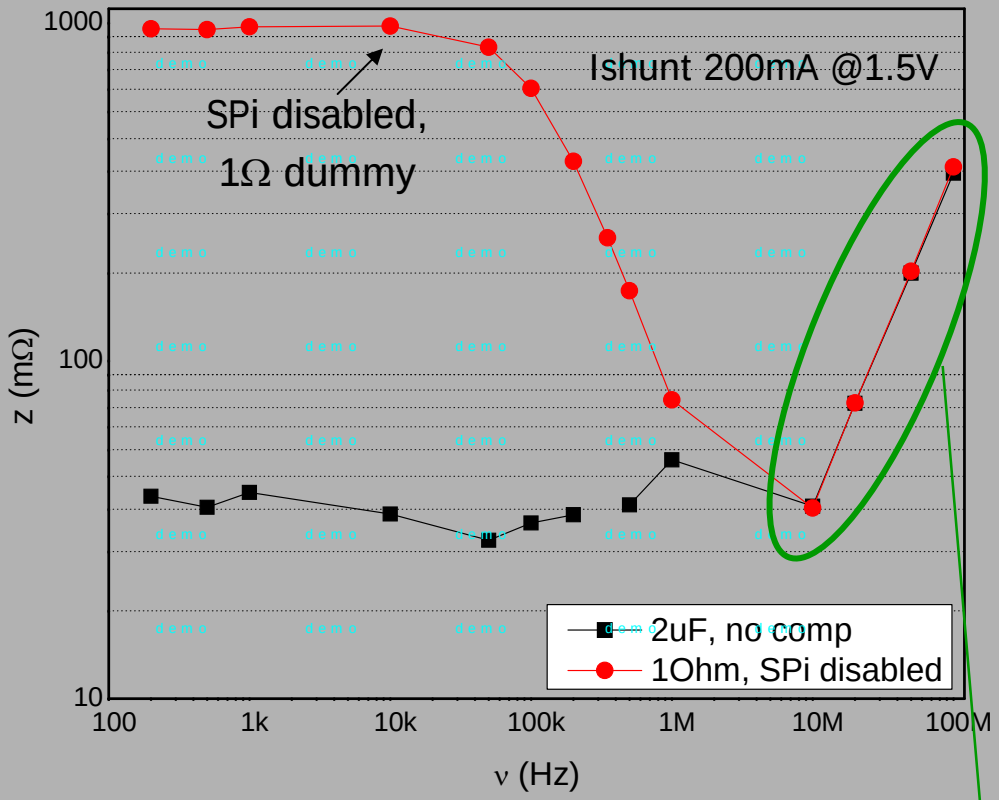
'dominant' poles:

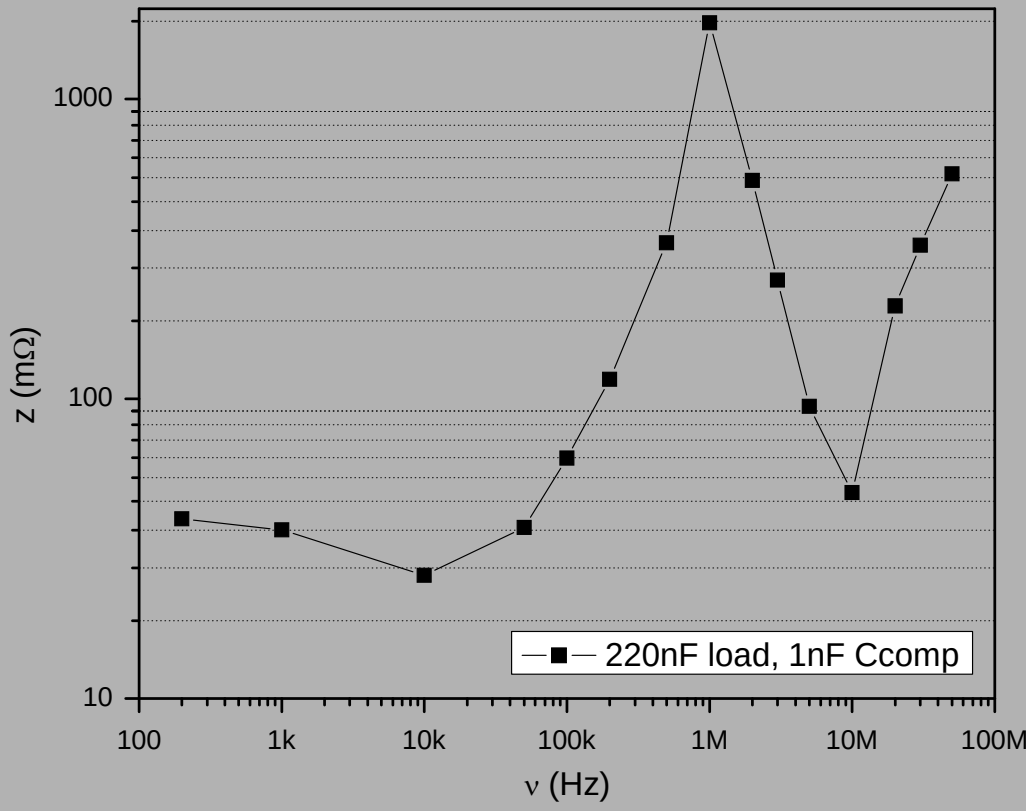
p1 = s $g_{m,OTA}^{-1}$ C_{M2}

p2 = s $g_{DS,stage2}^{-1}$ C_{comp}

p3 = s $g_{DS,shunt}^{-1}$ C_L

dynamic impedance



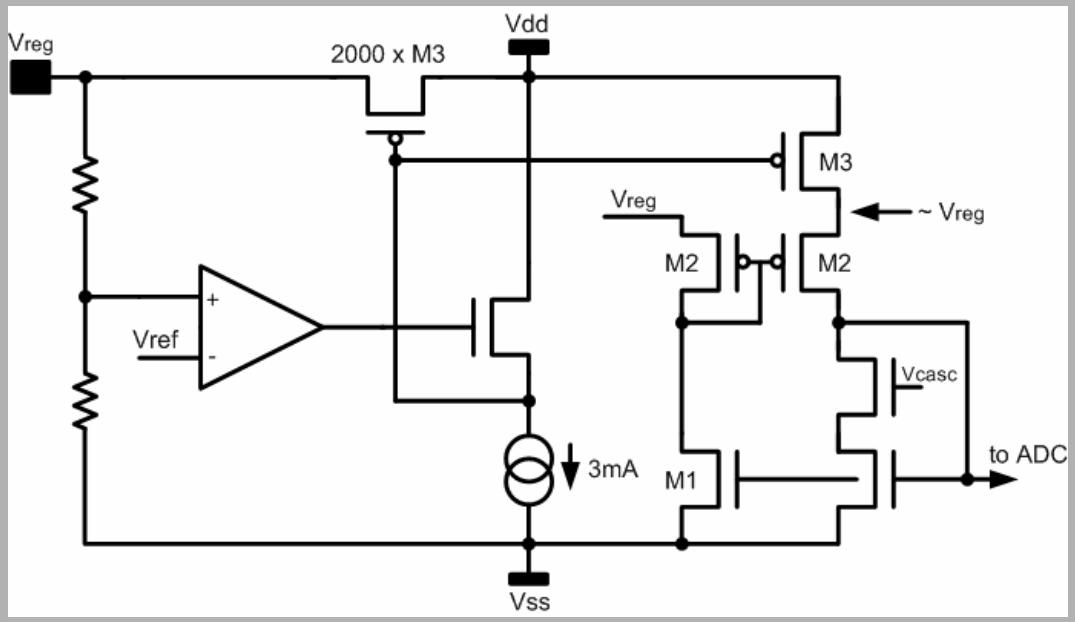


Impedance < 50mΩ

@ vh-frequency
the impedance is
given by the PCB setup

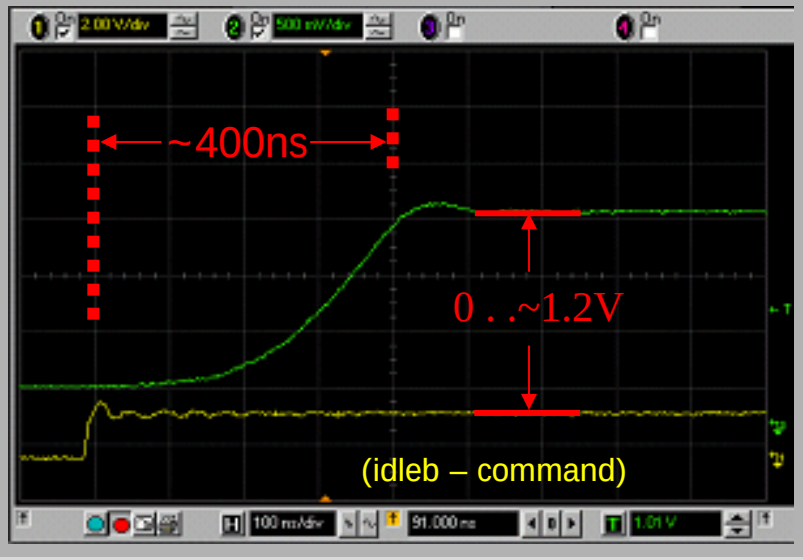
- Shunt needs about
  400-500nF load to be stable
- operation w/o load capacitance possible
  amplifier bandwidth needs to be limited

Linear Regulator

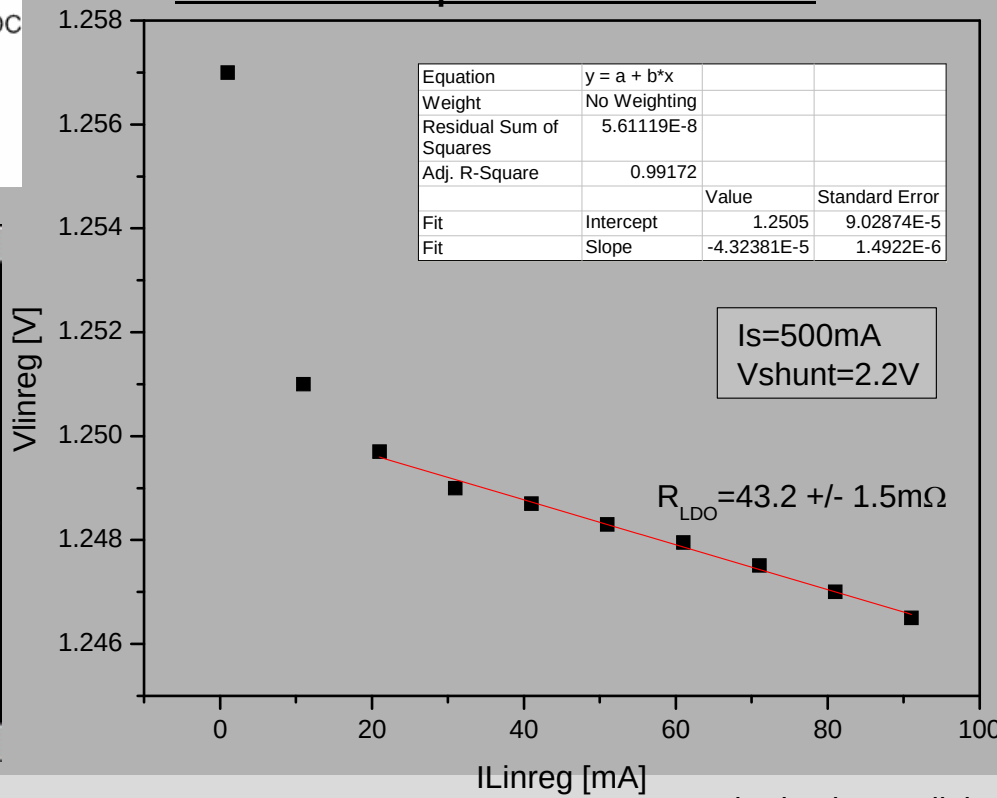


- standard LDO design
- folded cascode OTA, SF to drive output fet
- compensation for changing V_{DS} (ADC)

idle feature:

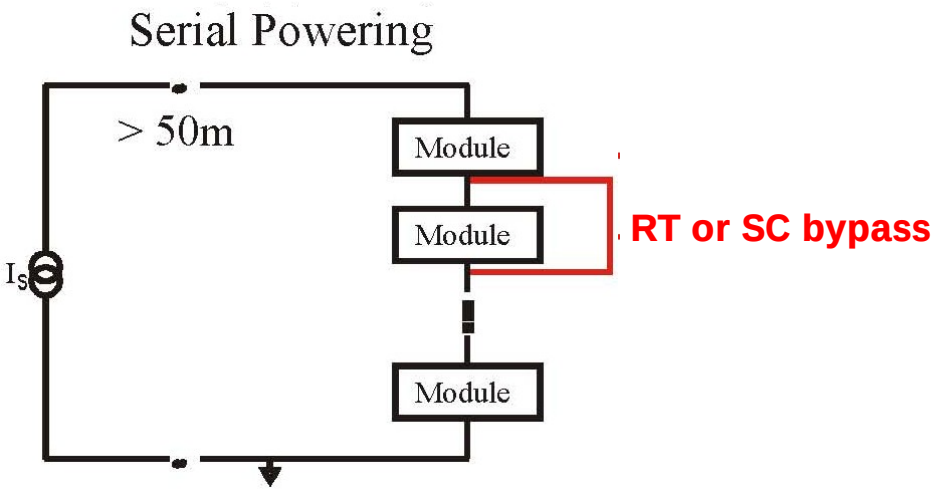


'first' DC output characteristic:



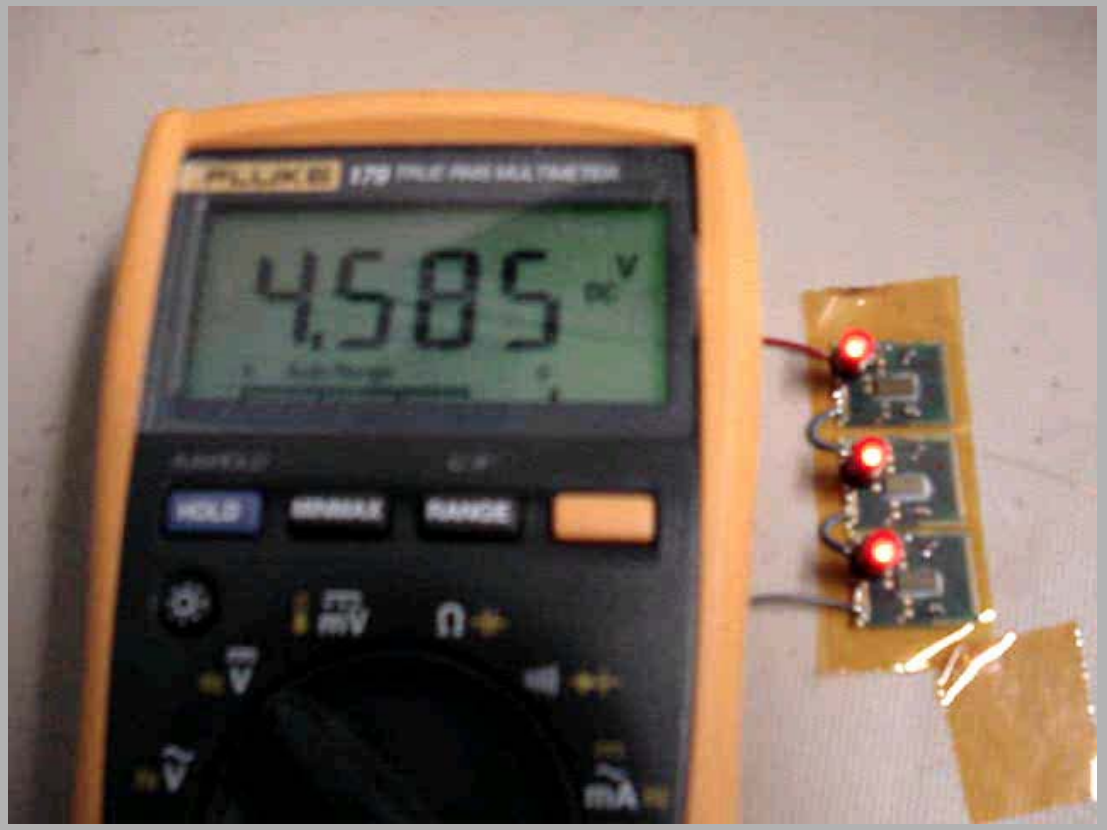
Serial Power Protection

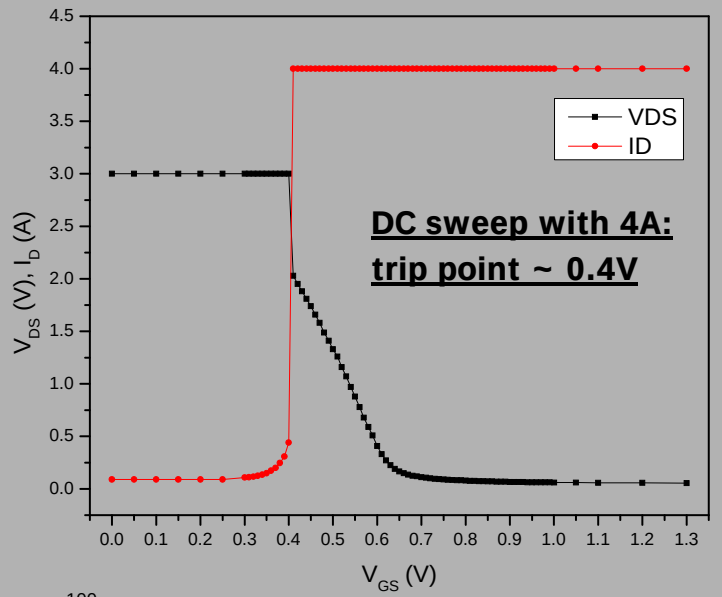
- What is needed in case an "open" develops in chain of modules?
  - Real Time Local Protection/Current Bypass
    - Current source power supply is too far away for voltage limit to protect stave
    - 200 meters/ (2/3c) ~1 us. Assume open leaves ~ 10pf, and I ~ 1 amp, then voltage across short ~ 1 A x 1 us/ 10pf = 100kV → likely may spark and could
  - Slow Control enabled bypass
    - Need a short that can bypass module in case it develops pathological behavior that adversely affects performance of stave
    - Short should be sufficiently low in impedance the resulting voltage across it will be low enough to disable module circuitry (i.e. small compared to normal module operating voltage, ideally < 100 mV)
  - Protection circuitry should not introduce additional stave failure modes

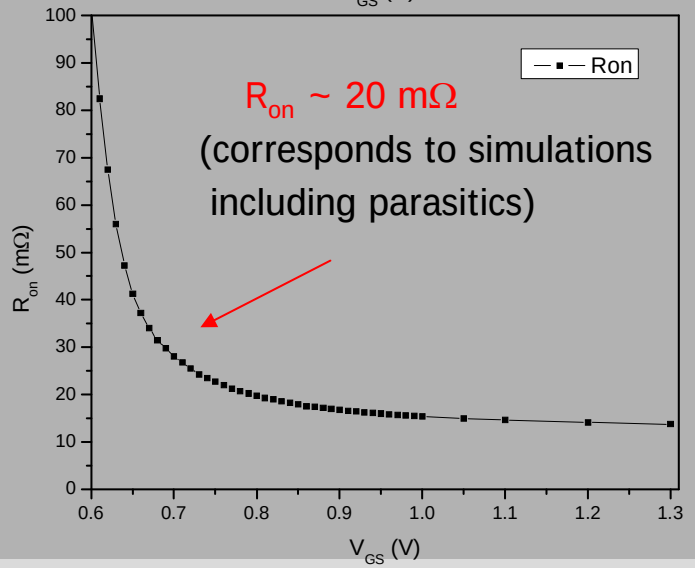


magic christmas tree (power down)

Demonstrates power down capability of chip with external signal







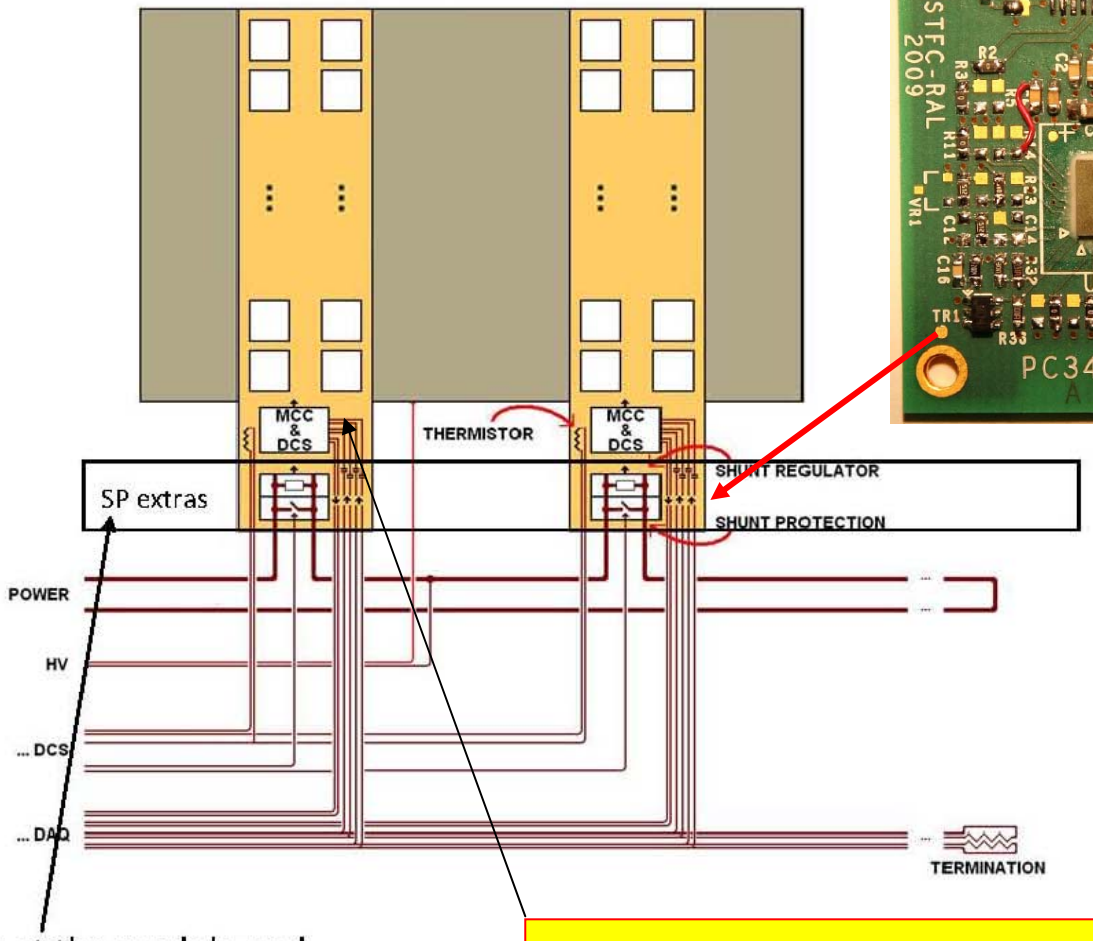
For dynamic measurements in full test setup, see talk by D.Lynn

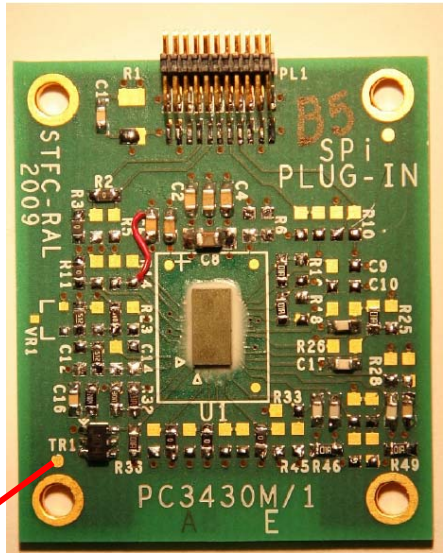
ABCn demonstrator stave

Module Controller Chip (MCC)
- Functions common to SP & DC-DC
  - multiplexes 2 data streams into 1
  - voltage monitoring
- Additional for SP
  - powered by SP
  - AC coupling of CLK & COM
    - Requires 4 capacitors
    - Everything else on chip

Temperature
- read by (stave end) DCS
  - Monitor T before power applied

Shunt protection
- under DCS control
  - Turn on modules independently





SP requires minimal extra circuitry at the module end

one module is already running SP using SPi at RAL

Summary / Outlook

- **SPi – Serial Powering Interface**: generic chip to explore SP schemes,

  evolved from discrete setups, highly integrated functionality:

  TSMC025MM, radiation tolerant design (except distr. shunt),
  high current shunt (takes total module current), distributed shunt,
  AC coupled comports, 2 Lin.regs, monitoring ADCs,
  over power protection options with power FET
- **SPi 0.01 fabricated** (120 chips) **and FCOB assembly successful,**

  RAL bought 120 new chips for stave tests recently
- chip tested fully functional: Vshunt: 1.2..3V, 4A current, Impedance < 50mΩ,

  small feature in digital controller (restricts use of SPi)
- stave operation with ABCn (**field tests**) planned at RAL, LBNL
- bypass scheme system integration (current alarm power down),
- radiation test up to 50MRad (Co60) at BNL (D.Lynn et al.)