First Results of SOI-based integrated detector and electronics at Fermilab

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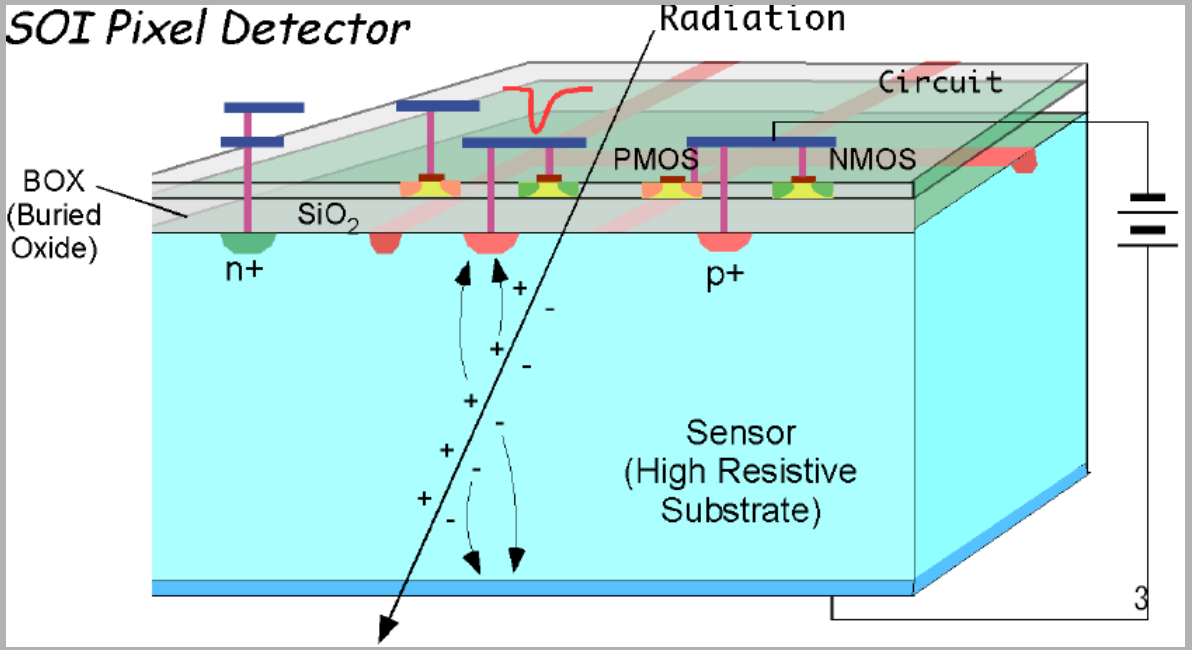
Outline

- Features / Motivation SOI
- Counting pixel matrix: MAMBO
- 3T test array to evaluate cross talk in SOI
- Summary and Outlook

Features: SOI detector

Features

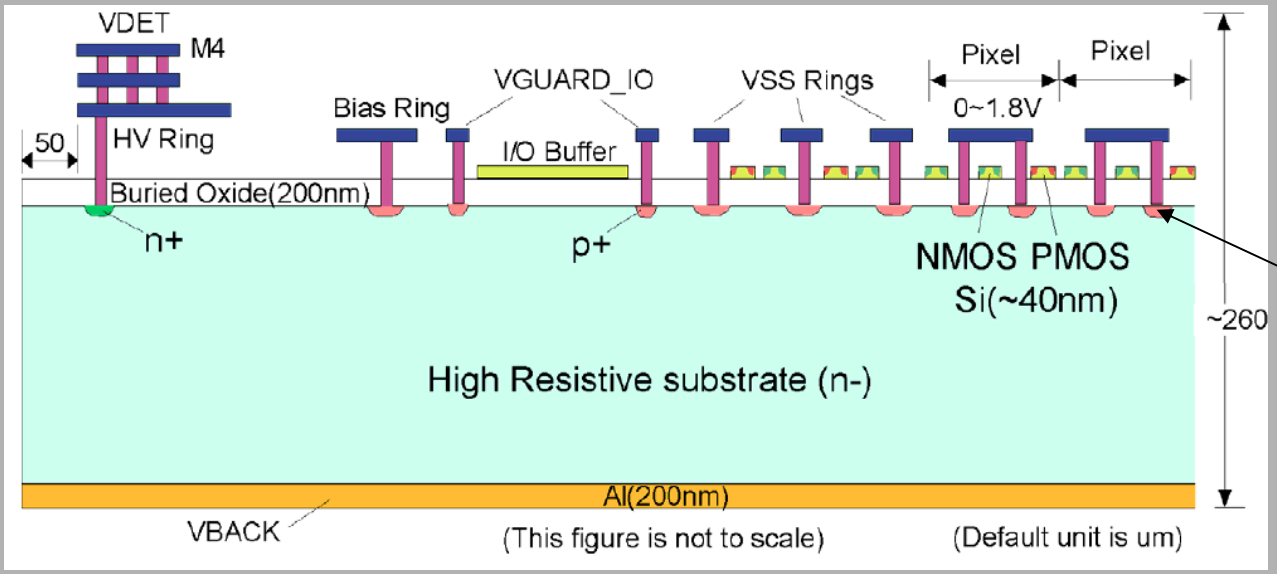
- monolithic approach (prime example)
- small diode / input capacitance
- access to full CMOS (nmos/pmos)
- **no bumping**: low mass, low cost
- thinable, no backside implant
  (50um depletion at ~15V)
- rad. tolerant (for ILC doses)



Joint SOI Effort

- Commercial SOI process on high resistivity substrate (700 Ωcm) made available from OKI via KEK
- SOI-Pix collaboration started 2007 (coordination Y.Arai, KEK):
  2 OKI-runs 2007, **2008**

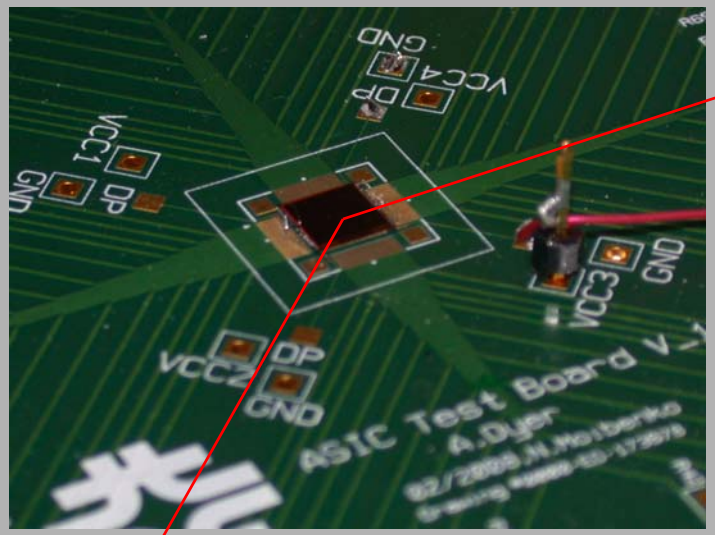
OKI - process overview



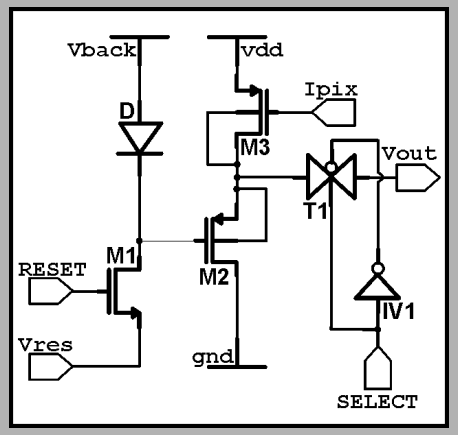
second run (2008) via OKI:

Process	0.2μm Fully-Depleted Low-Leakage, SOI CMOS, tox=4.5/7 nm, 1P4M, MIM, DMOS, Vcore=1.8 V (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick, Handle wafer: Cz、 700 Ω-cm (*n-type)*, 650 μm thick (SOITEC)
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

Fermilab designs (2008 run)

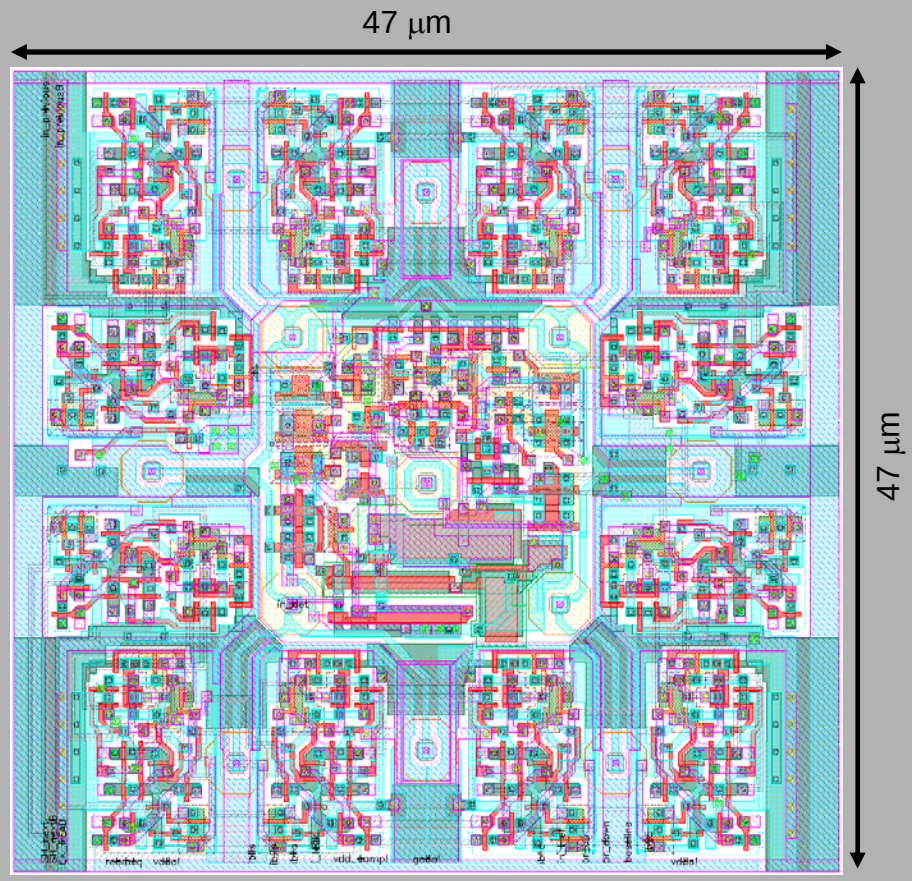


5x5 mm^2 submitted Jan. 2008,
returned Sep. 2008 (after corrected diode implantation)



3T readout (MAPS like)

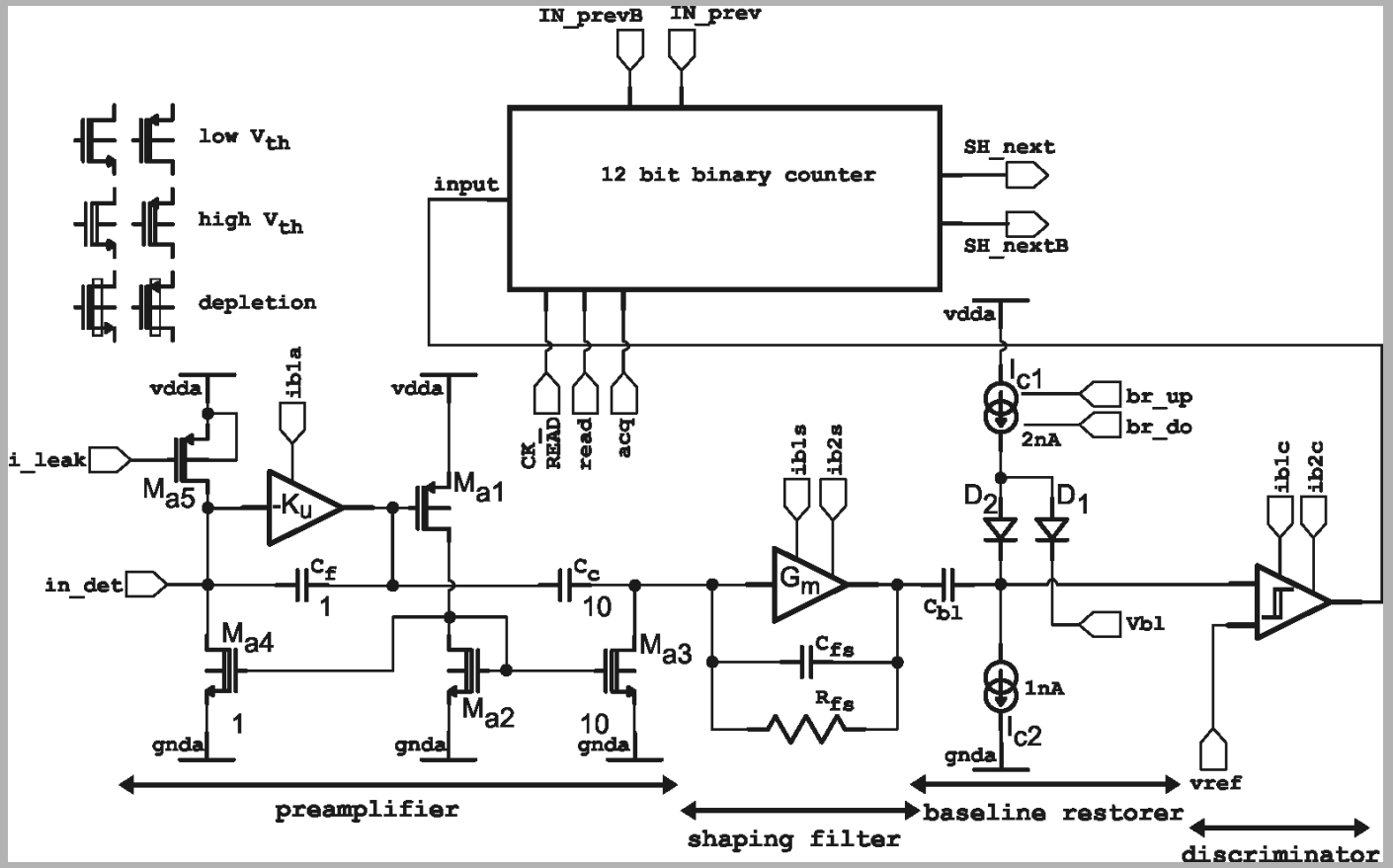
- investigate detector properties and cross talk effect
- 8x10 pixel array, 20x20µm pixel size



MAMBO (Monolithic Active Pixel Matrix with Binary Counters)

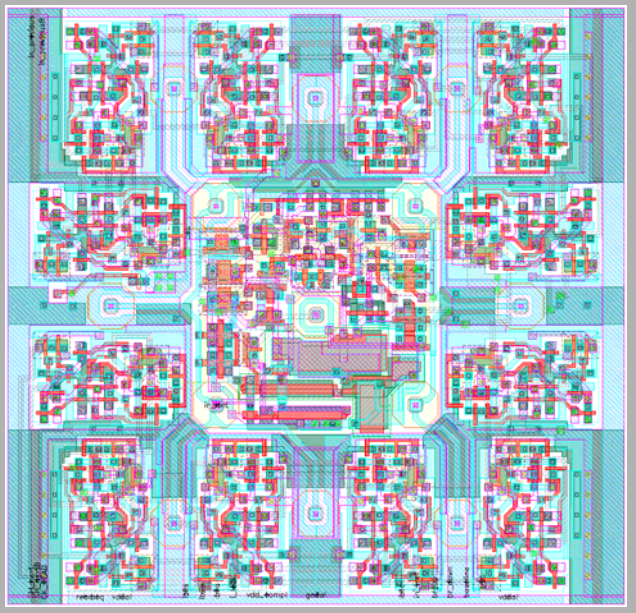
- 97x97 pixel matrix, 47x47µm pixel size
- counting pixel for imaging application

Mambo - pixel overview



each pixel:

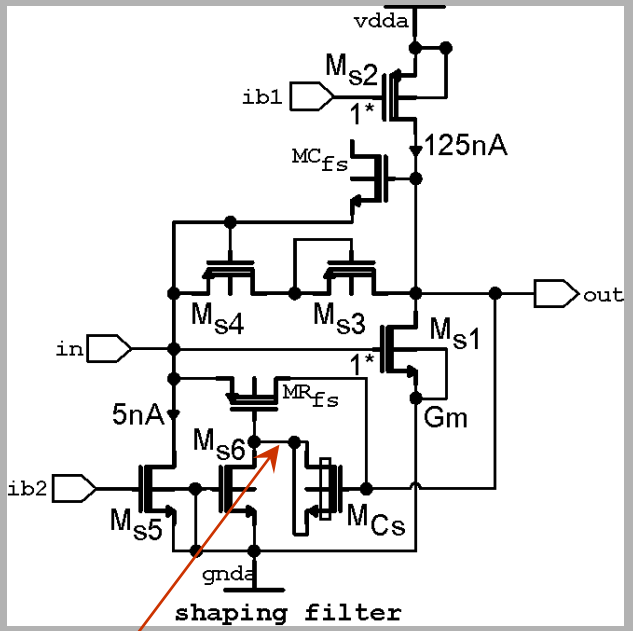
- integrating CSA w/ p-z network,
- shaping filter CR-RC^2 with τ_p=150ns; gain=~200 μV/e$^-$ (for small Q),
- multiple diodes/pixel,
- ripple counter (reconfigurable as shift register)



C_c=28 fF, C_{fs}=3.3 fF, R_{fs}=50 MΩ, G_m=5.8 mS, C_h=30 fF

(compact design excluding use of physical resistors)

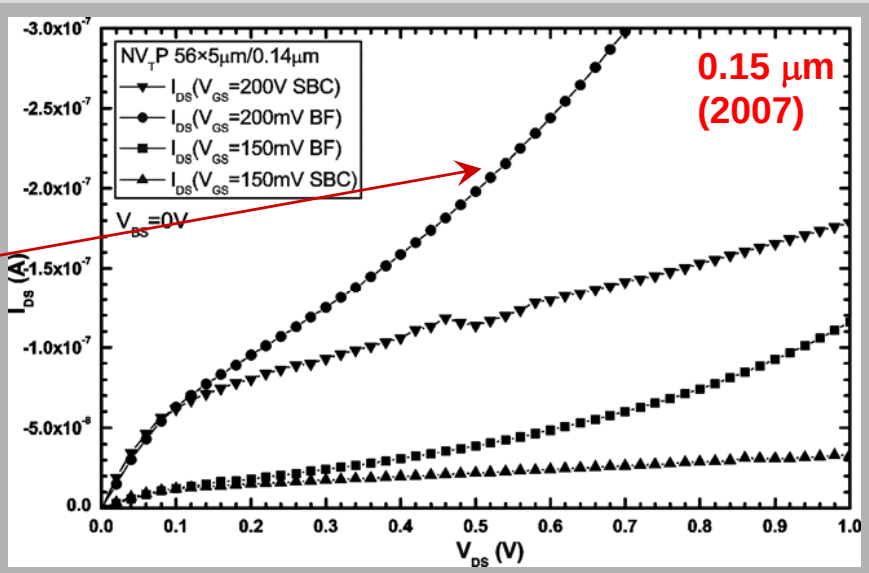
Lack of precise SOI models is design challenge



PMOS biased at V_{GS}=const as a feedback resistor (50 MΩ)

2007 run: used transistor with floating body

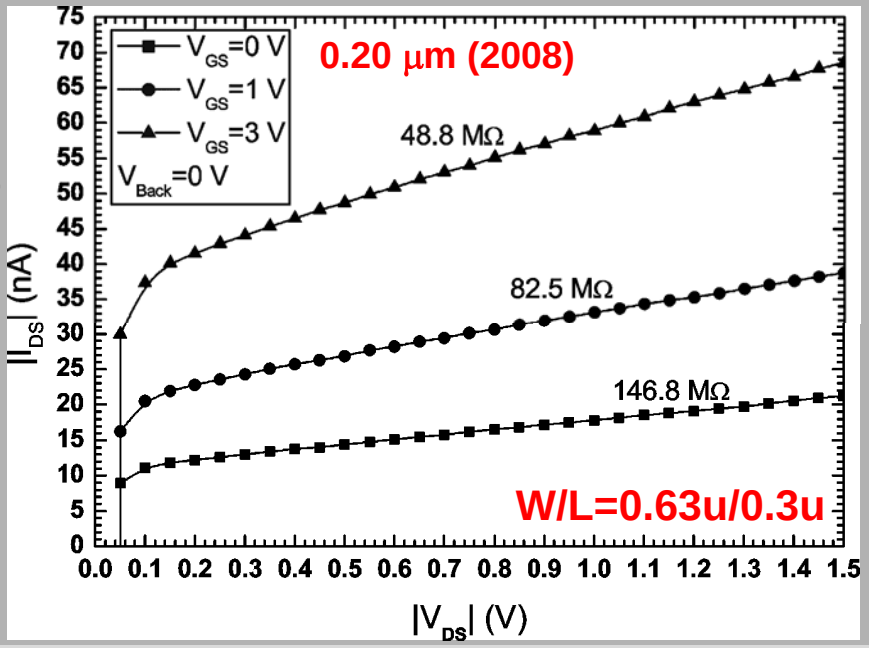
later measurements showed very small eq. resistance (SPICE models did not indicate such effect)



2008 run:

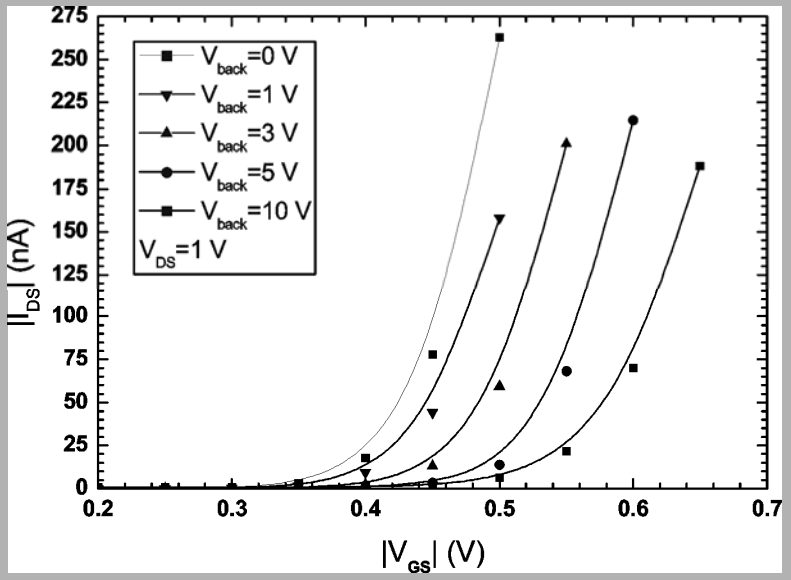
SB–connected transistor & 'half-H-gate' design for feedback transitor

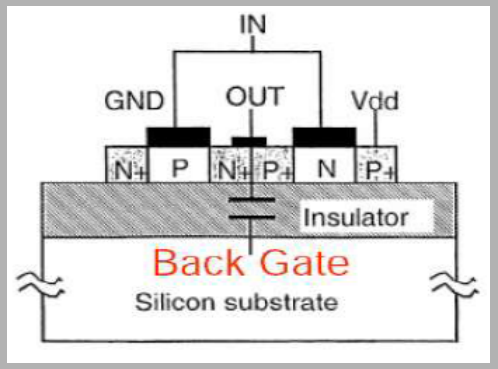
required values of feedback resistor were obtained (this was empirical approach, not driven by device models)



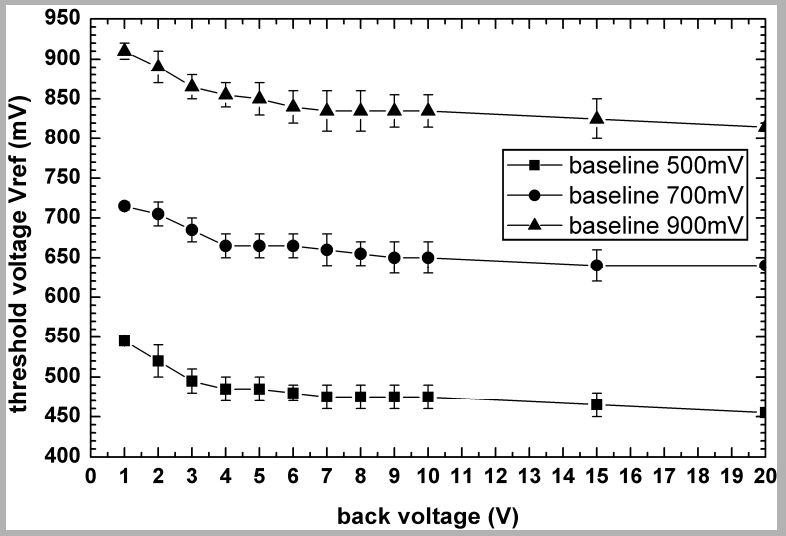
back gate effect

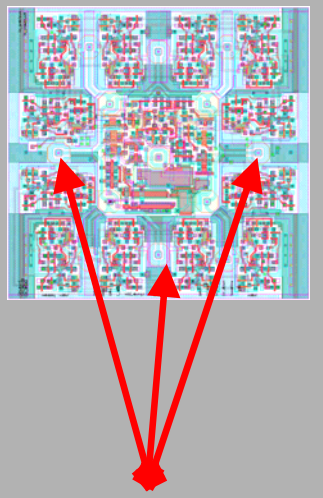
transistor from the shaper's feedback path (separate structure -> no biasing diodes)





Significant threshold voltage shifts observed, however, design techniques can reduce effects:



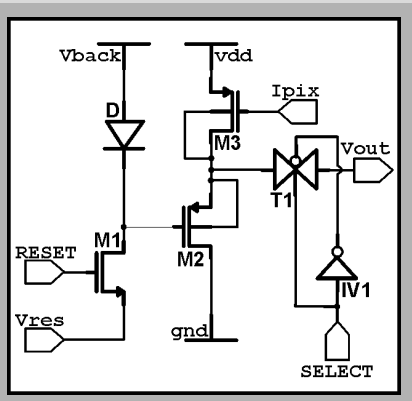


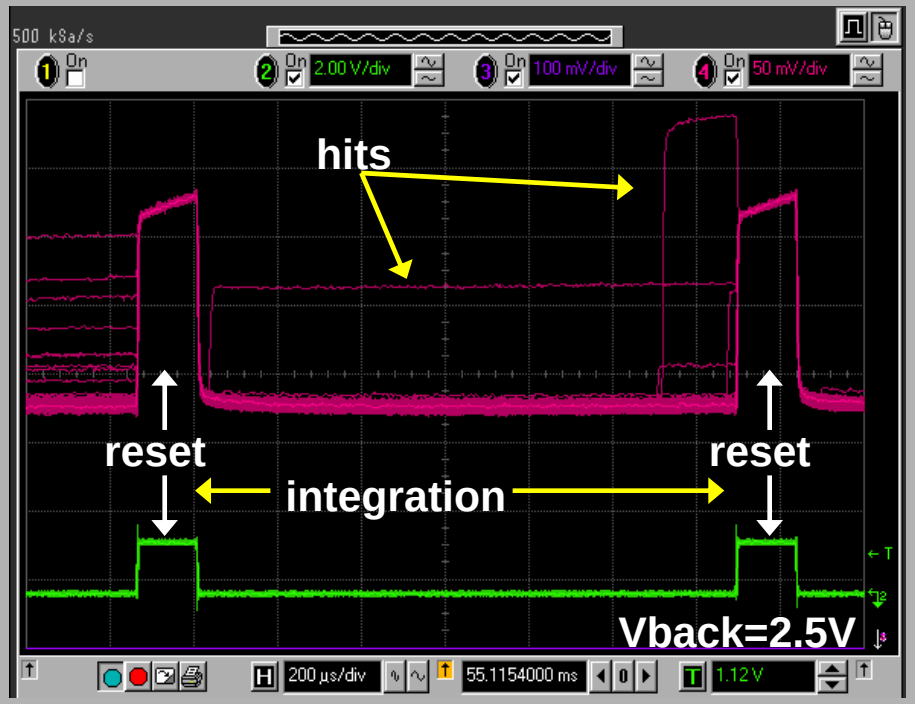
13 diodes / pixel

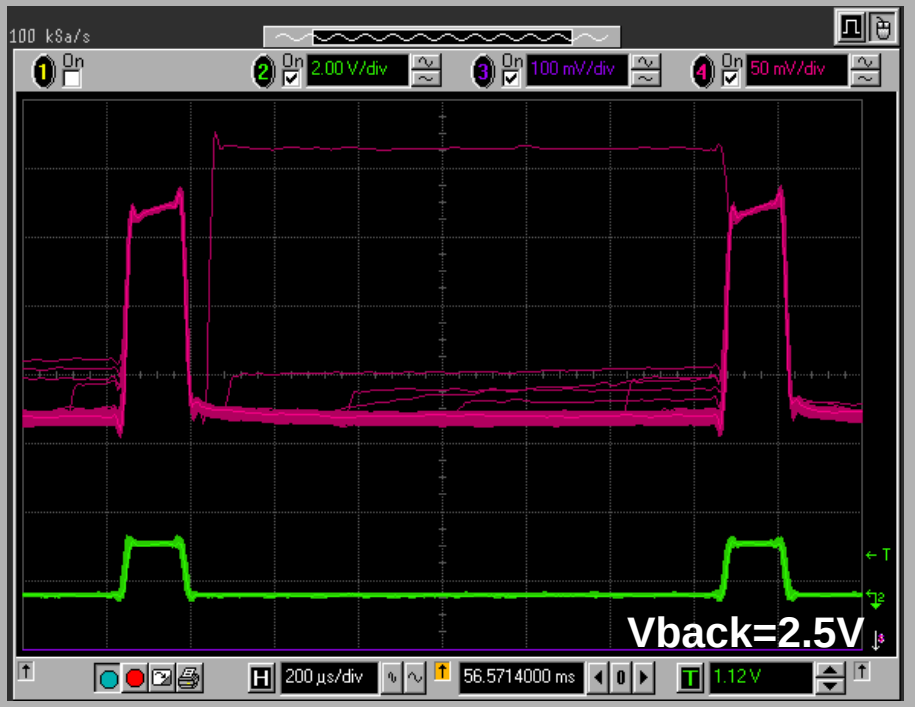
adjustment of bias voltages and currents (referred to V_{GS}) up to several tens of mV is still required for back gate voltages from the range from 0 to 10V.

array with 3T pixels architecture

^{109}Cd (22 keV γ): max. signal 200 mV ➔ Cin = 4.8 fF (33 μV/e$^-$)
Noise (RMS) after CDS ~ 1mV



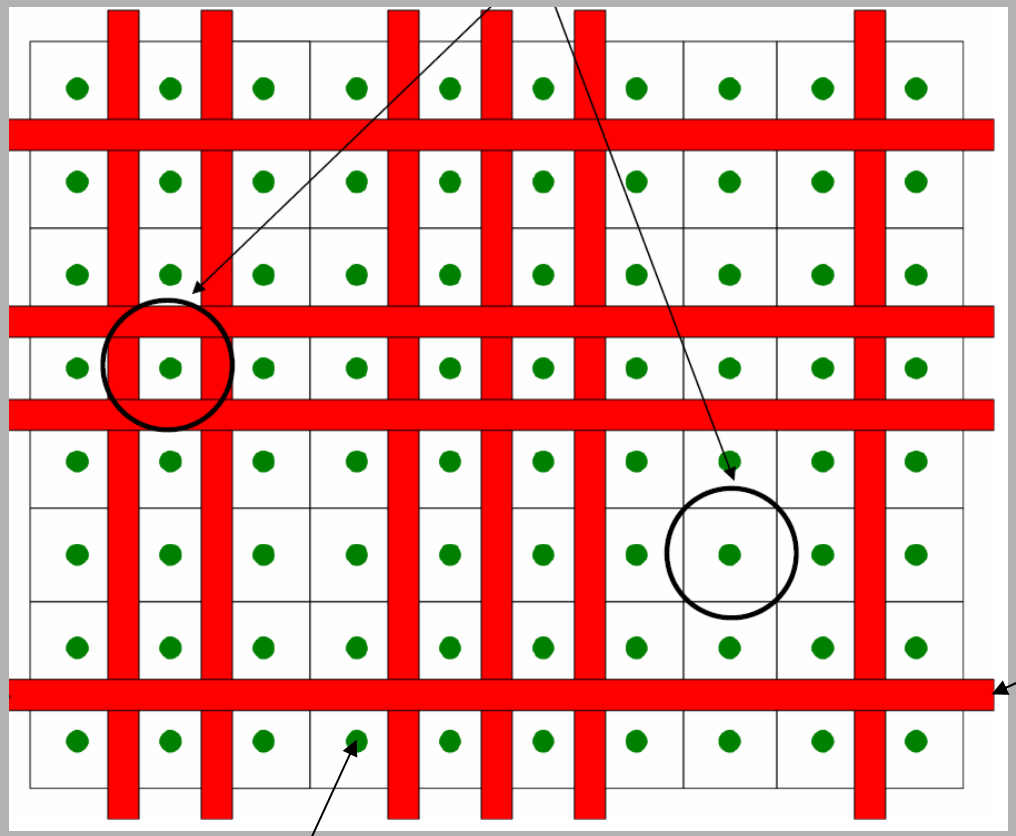




Vback = 2.5V -> ~ 20 μm depletion

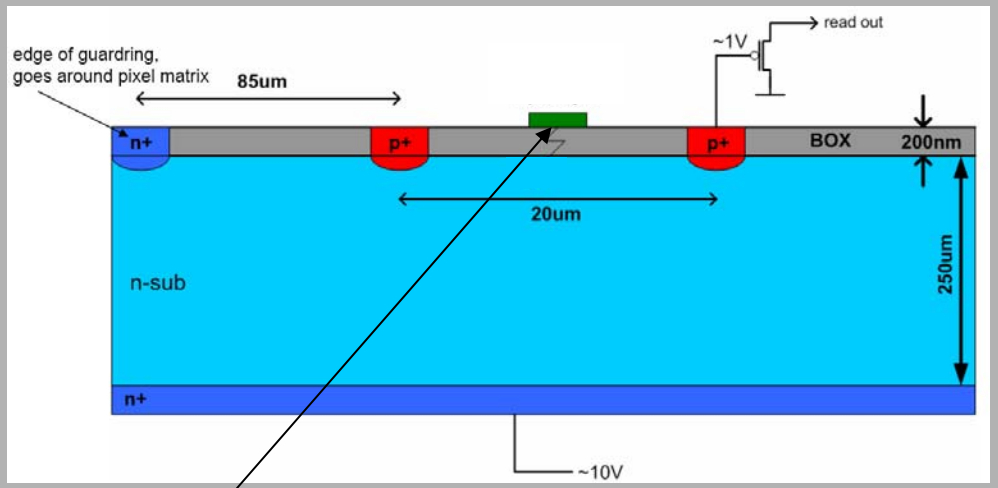
cross talk structures

grid creates **various scenarios**, here worst and best case



sensitive node: 1.2um diode p-implant, 20um pitch

cross section – cross talk arrangement



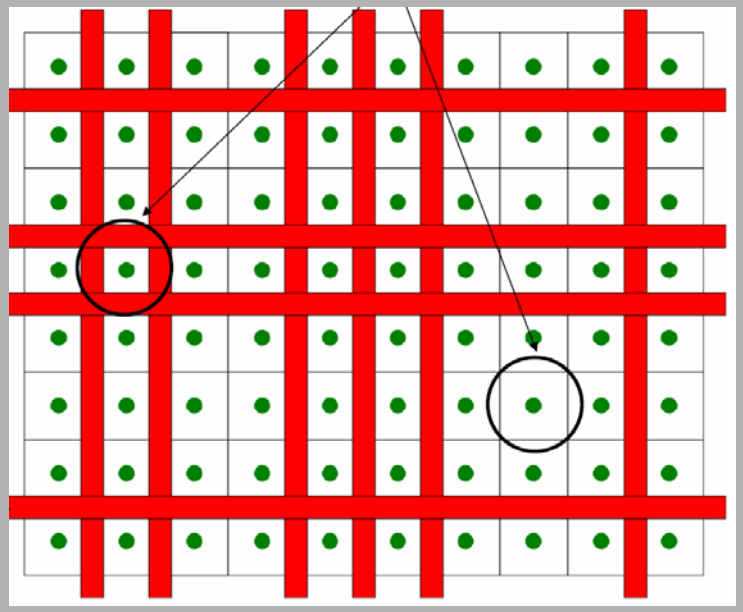
Aggressor:

- **diffusion implant** supported by metal1
- switching between two voltages
- 1.2 um wide located at pixel boundary

cross talk results - pixel array

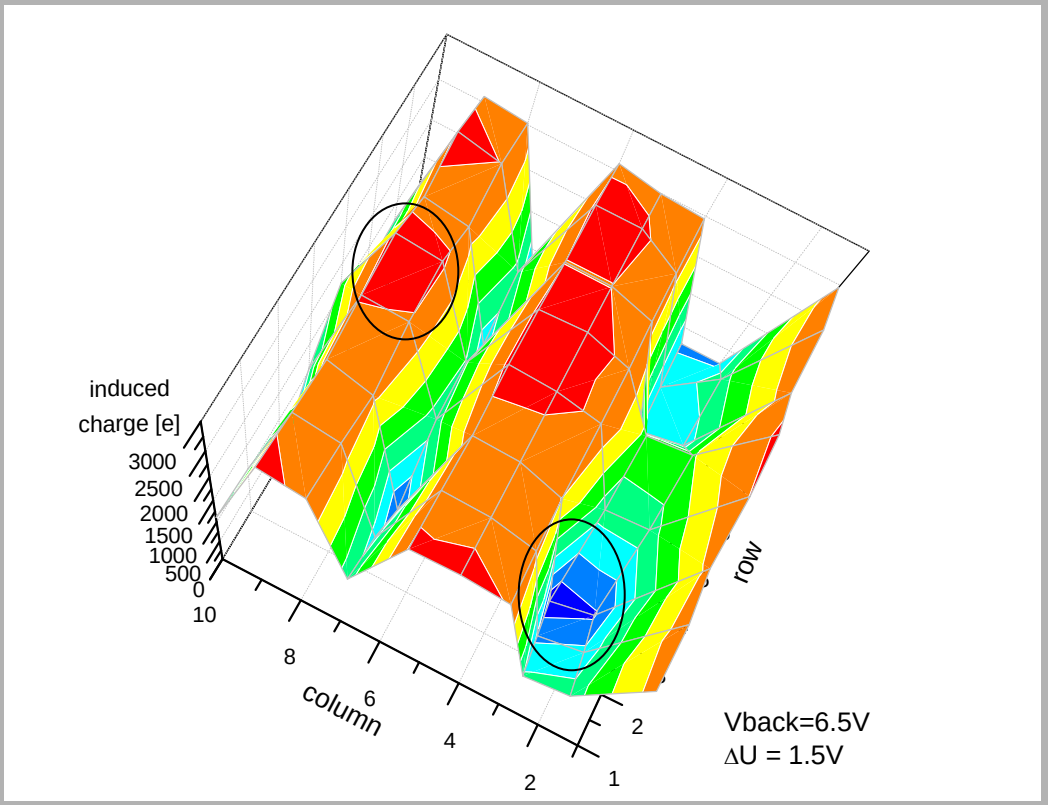
Procedure:

- reset pixel and toggle voltage during integration time
- calculate difference before and after voltage change



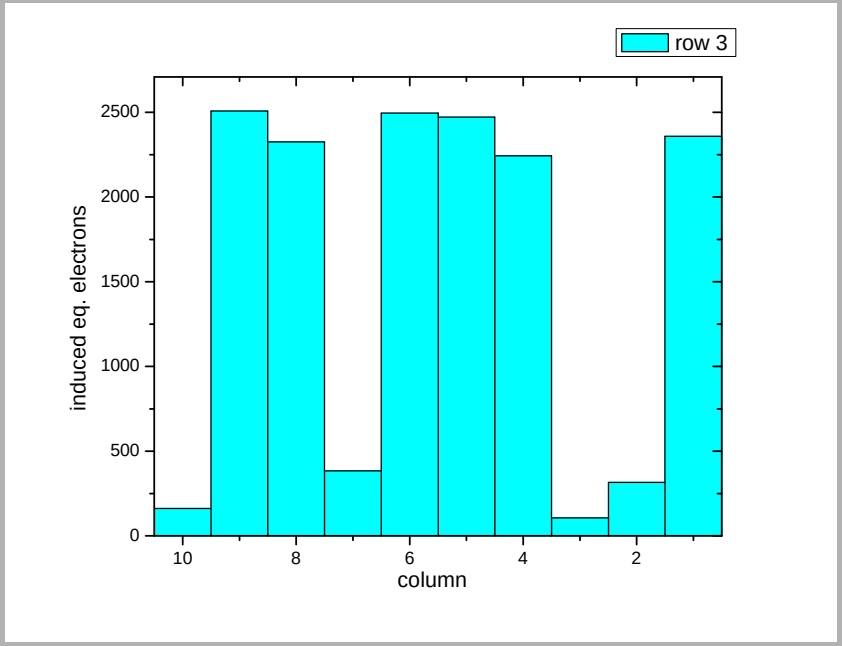
clear correlation between aggressor lines and induced charge

charge induced by falling edge of voltage swing



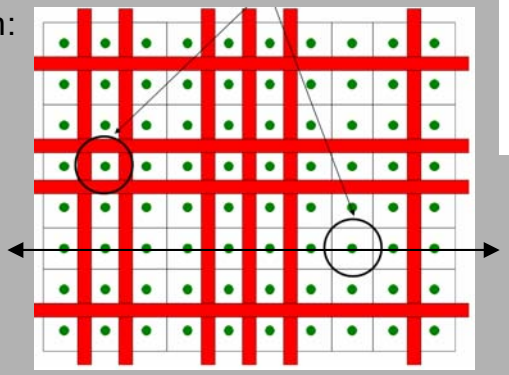
note, effect on falling and rising edge almost equivalent
(net charge ~0) -> suggests differential logic

cross talk results – pixel array (cont'd)

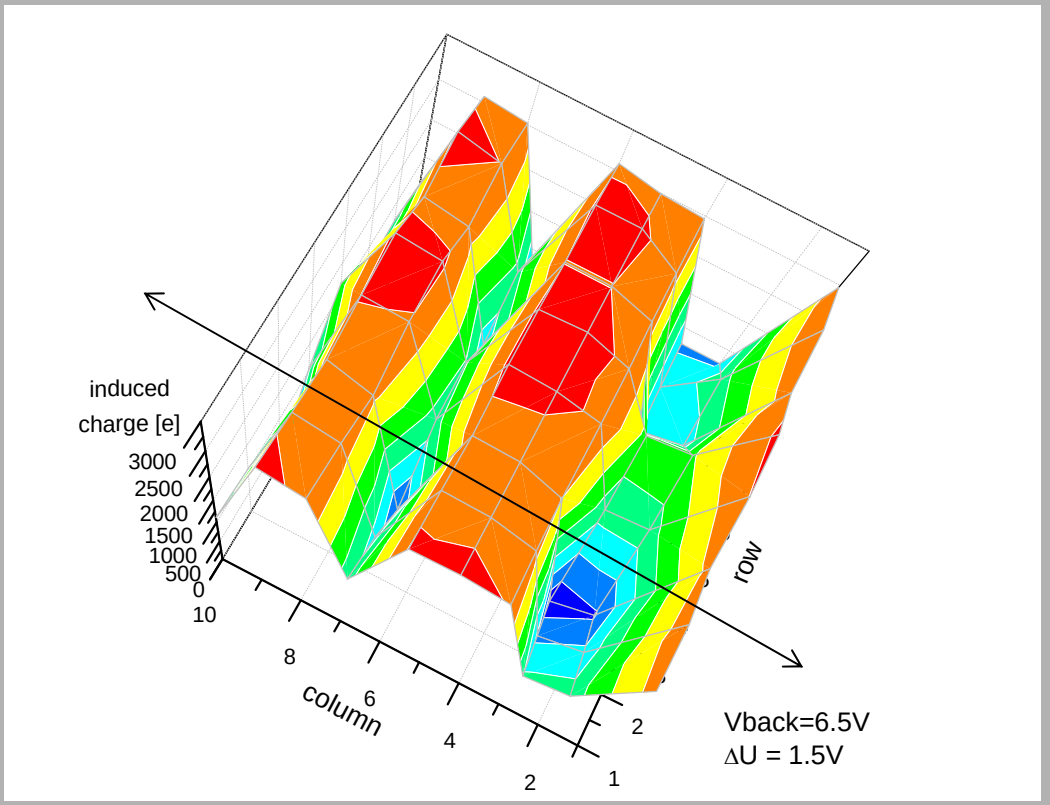


- **~ 80 % from left neighbor**
- ~ 10% from right neighbor
- top and bottom contribution: consistent but small

most significant symmetry in the pixel is left / right ..... (?!)

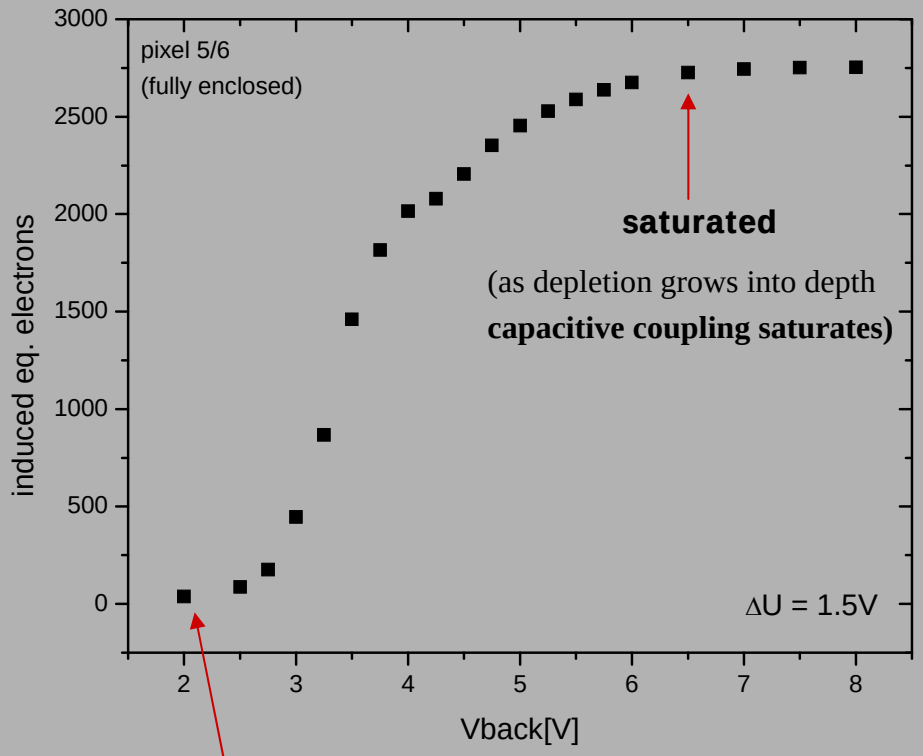


charge induced by falling edge of voltage swing



note, effect on falling and rising edge almost equivalent (net charge ~0) -> suggests differential logic

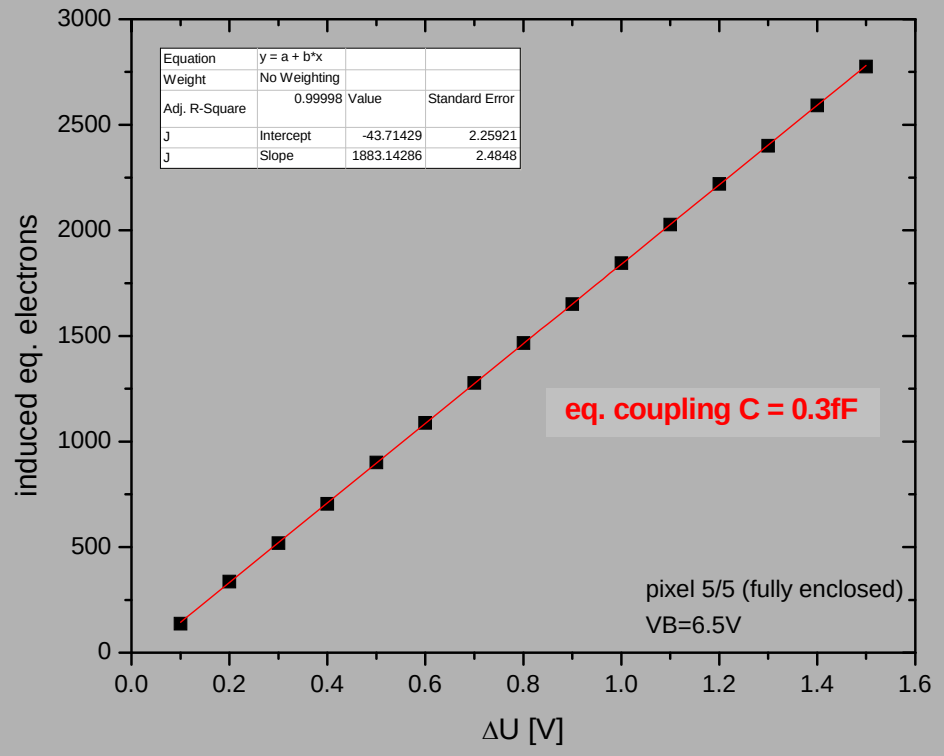
cross talk - quantification



cross talk starts at VBG > 2V

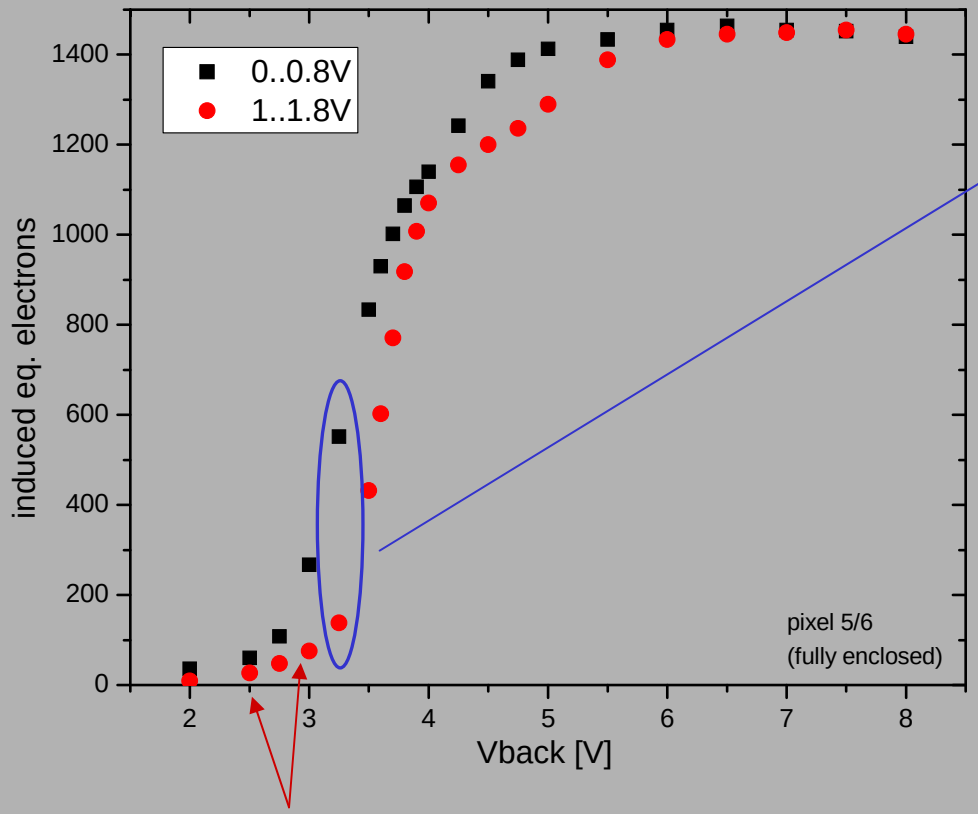
-> shows that coupling is through substrate
(and not CMOS)

linear dependence of charge vs. voltage swing
(as expected from capacitive coupling)

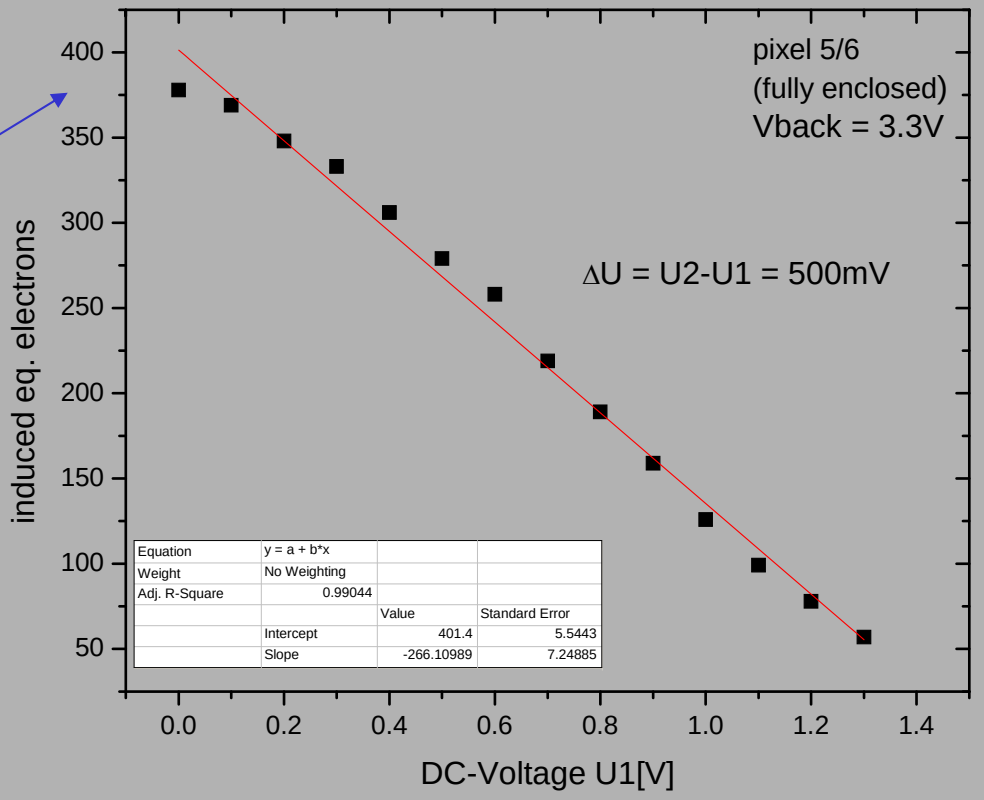


cross talk – DC level

- voltage swing constant (800mV)
- sweep starting voltage (DC pedestal)



effect starts at higher VBG by shifting DC potential at electrode
(same effect possible due to charge build up in BOX)



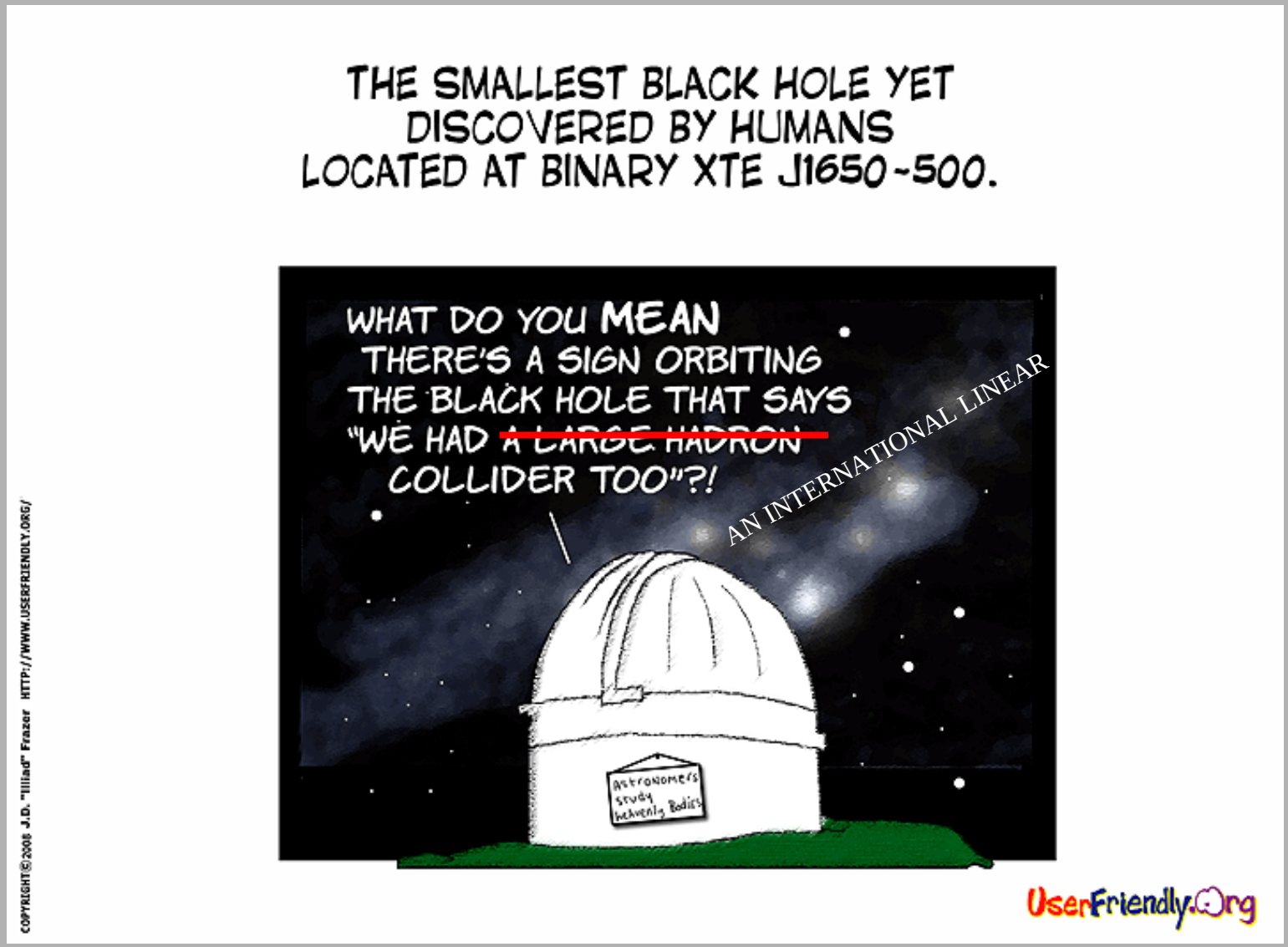
note, this dependency will disappear at higher VBG

-> high VBG (> 6V) desired, **otherwise logic states can influence potential distribution in substrate**

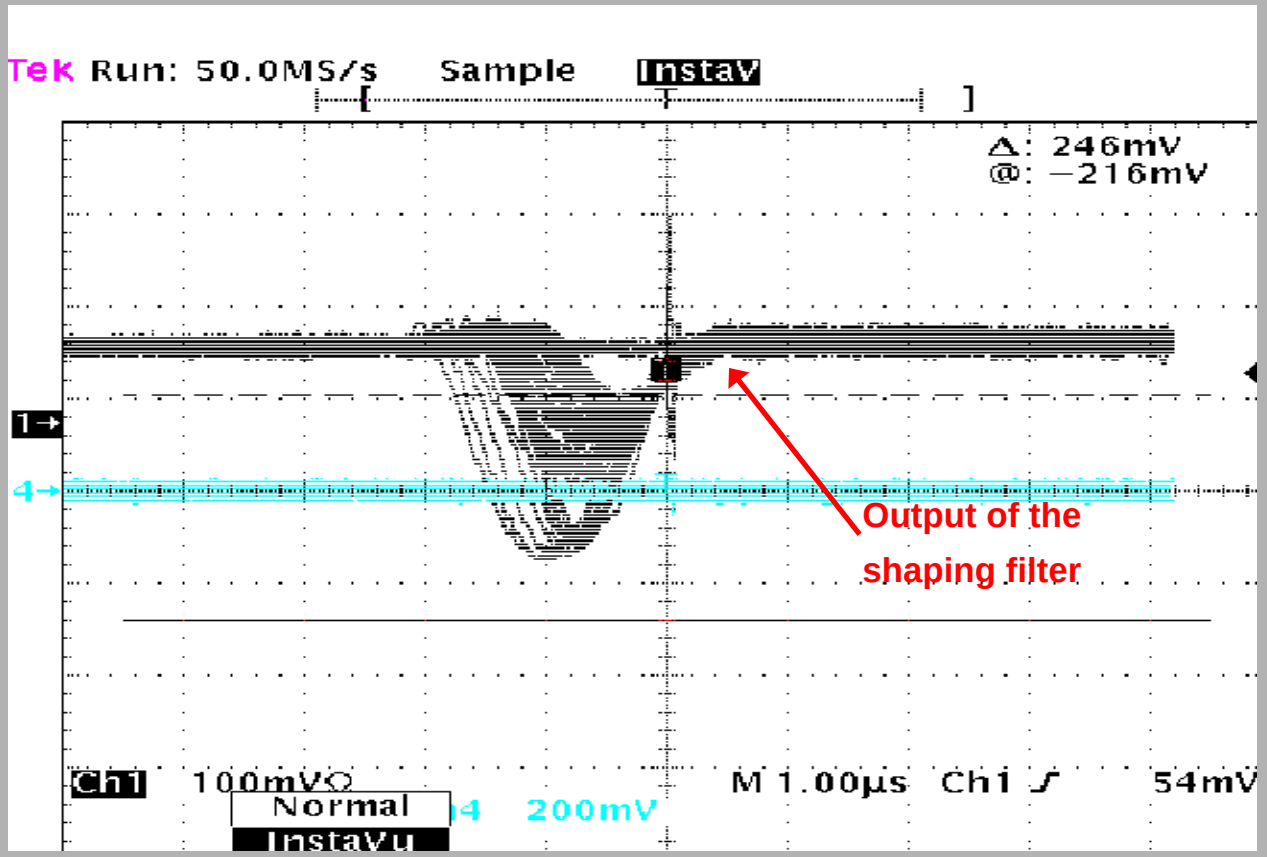
Summary / Outlook

- **SOI approach pursuit by KEK/OKI offers interesting opportunities for particle detection, yet also new challenges (backgate, crosstalk…)**
  - These effects need to be understood / analyzed to succeed in complex circuit designs
- **MAMBO – counting pixel matrix**
  - corrected design of 2nd gain stage expected back: End Nov. 2008
  - USB DAQ-System is build to operate Mambo for imaging application
- **Test structures to analyze cross talk**
  - Parasitic extraction for vertical integration designs (SOI, 3d) is important (effects are huge due to high integration level)
  - Available Tools at Cadence Level very limited / not existing to date
  - Cross check some effects with Silvaco Simulation (dominating left neighbor)
- We appreciate being part of the SOIPIX collaboration around KEK and hope that we can push SOI design to a next level

Backup Slides



single pixel exposure to ^{109}Cd source



- Pixel responses to the radiation events, polarity of signal is reversed and amplitude attenuated – it is believed that a depletion transistor (capacitor) is biased too shallow in inversion – changed in corrective submission in August 08,
- problems encountered with switching counters to shift register – more thorough tests are underway

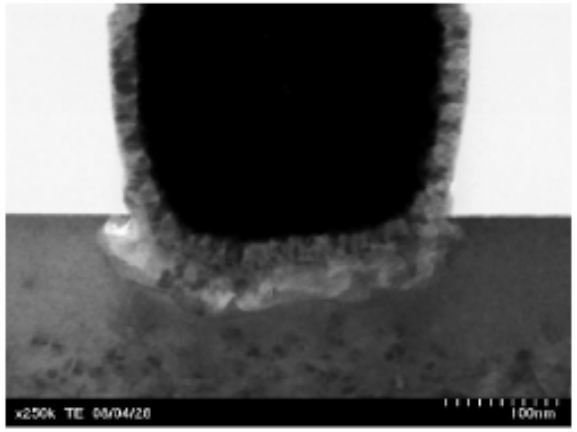
Contact Creation Error

At first, we didn't notice the wafer bend, and this leaded to redo of contact process 3 times.

Finally this caused thin oxide layer under the contact.

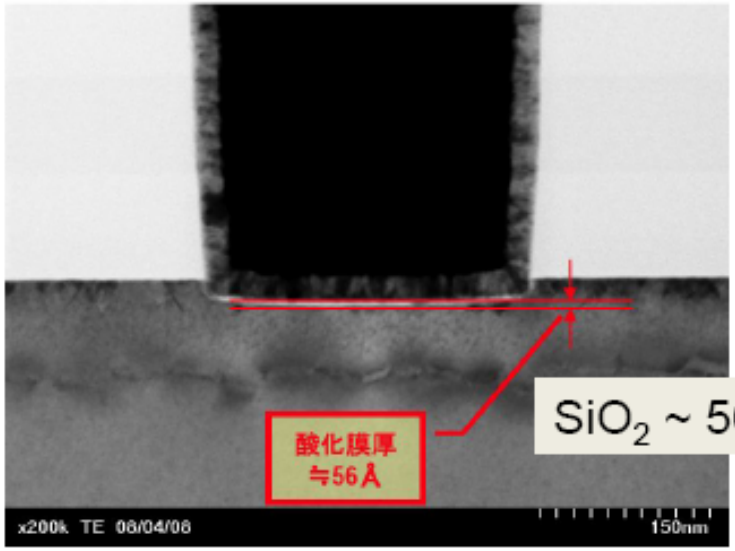
Process step was changed to avoid this even the redo is done.

PSUB上2CS(002J)



Good

PSUB上2CS(001J)



Not Good

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