

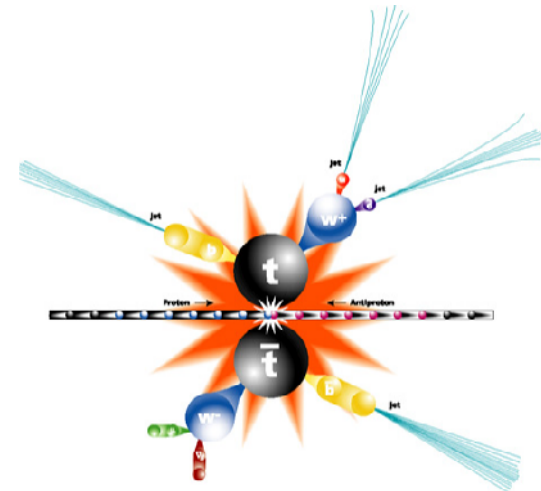


preFPIX2: Core Architecture and Results

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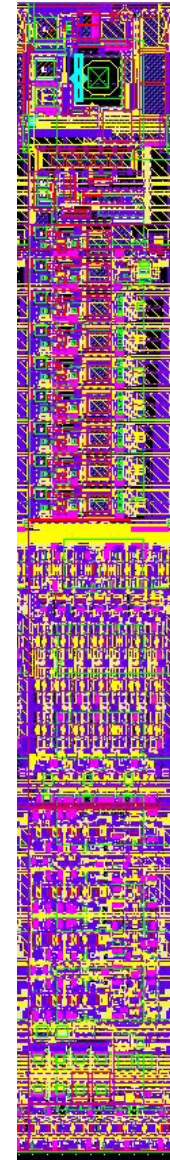
2000 Nuclear Science Symposium, Lyon France





FPIX

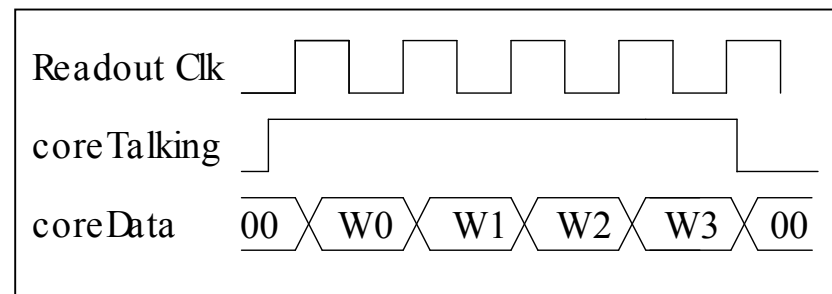
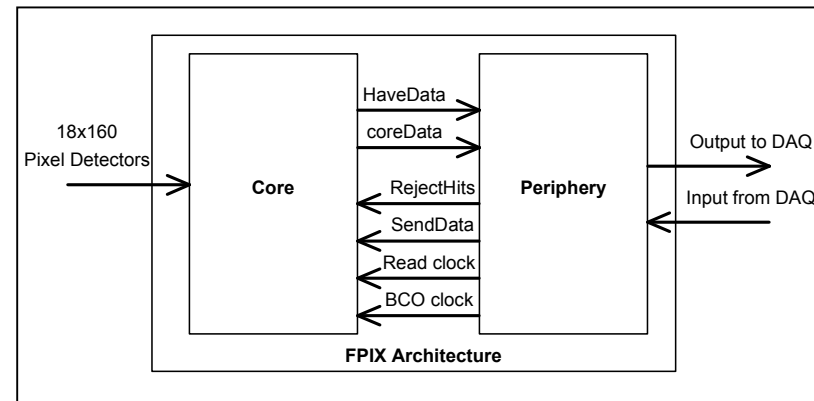
- A pixel architecture designed for colliding-beam experiments at the Tevatron
 - Most important application: BTeV
- Deep submicron with radiation tolerant design techniques
- Architecture substantially modified over earlier versions
- preFPIX2 a developmental step





Core vs. Periphery

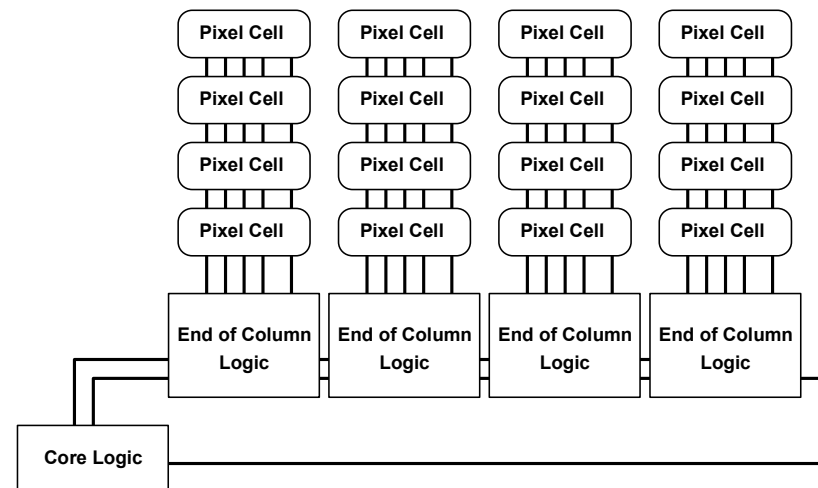
- All functions independent of Experiment organized into the Core.
- All functions dependent on changes in DAQ system, etc, organized into the Periphery.
- Core converts hits into a predictable data stream
- Periphery converts the data stream into whatever the Experimenters want.





Core Organization

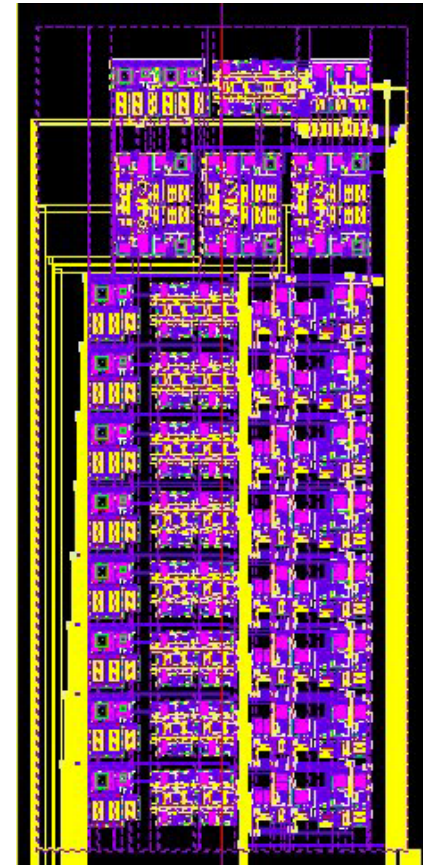
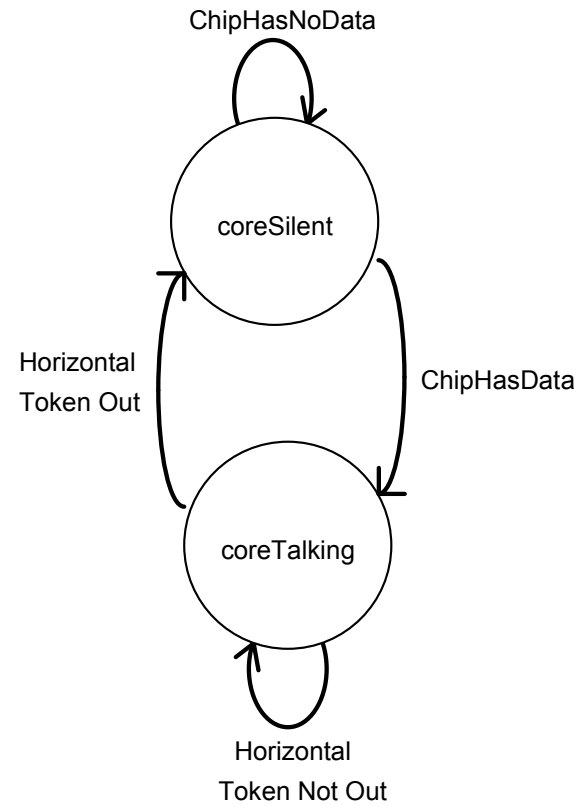
- Column-based architecture
- Indirect addressing scheme
- Three mutually-dependent parts:
 - Core Logic
 - End-of-column Logic
 - Pixel Cells





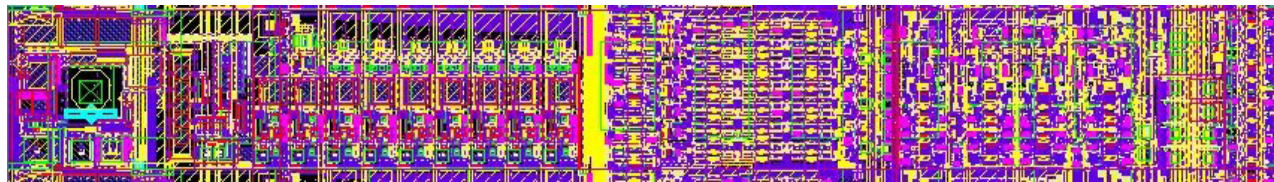
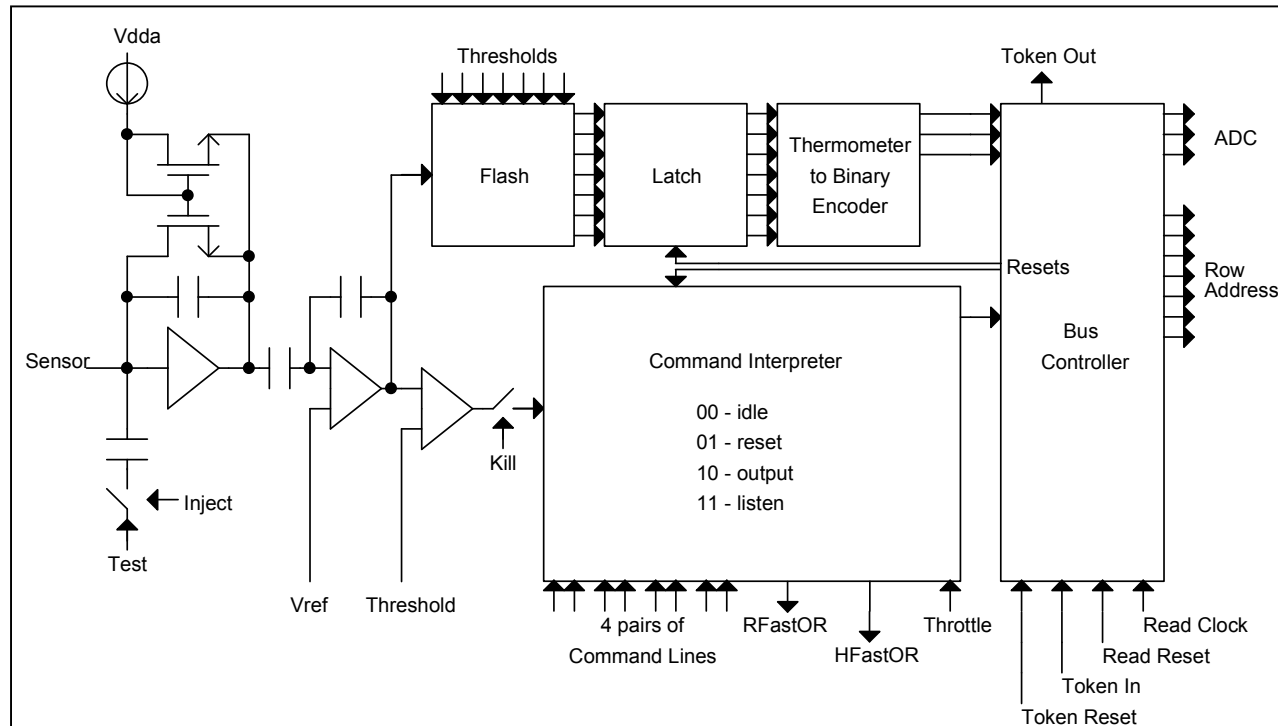
Core Logic

- Broadcasts timestamps
- Simple state machine controls output





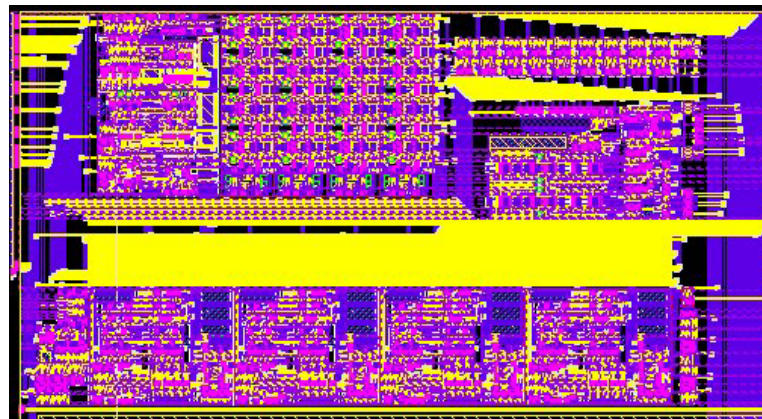
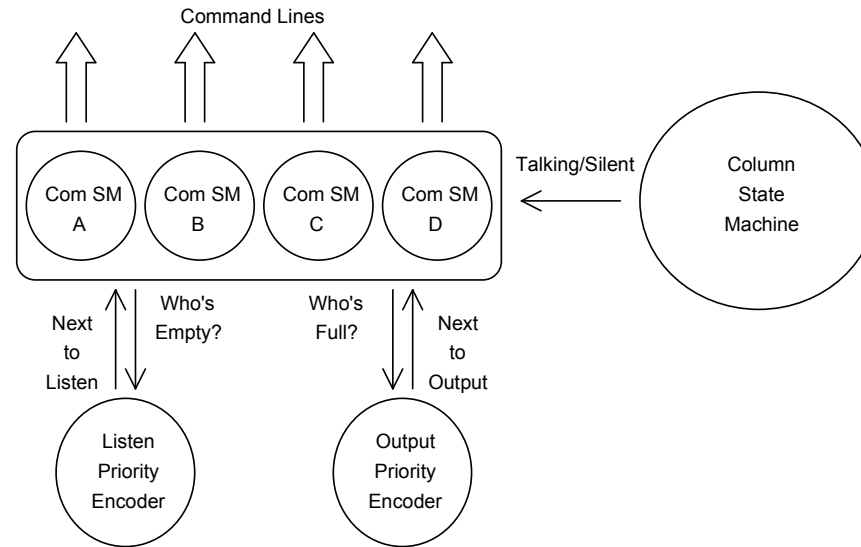
Pixel Cell





End-of-column Logic

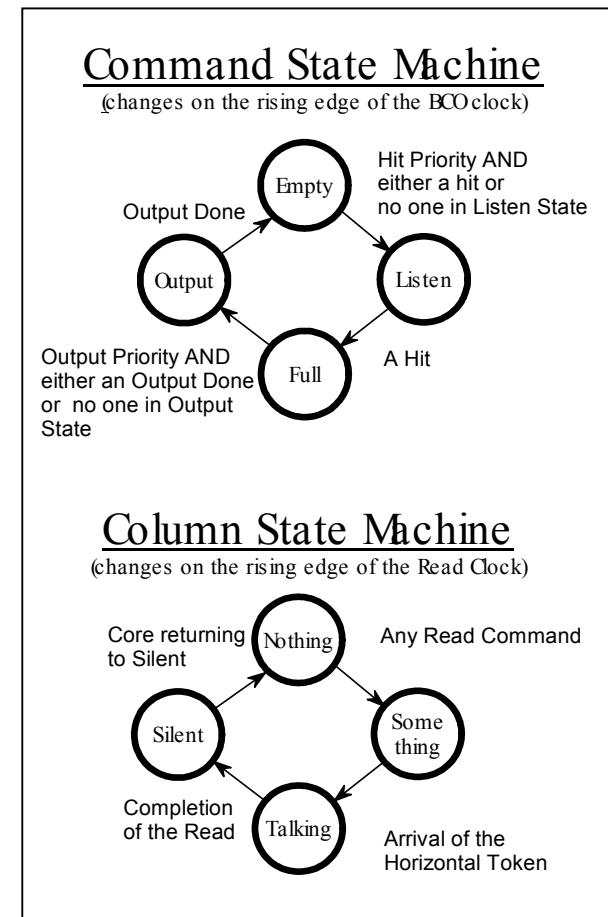
- Issues 4 sets of Commands to Pixels
- Registers Hits
- Latches timestamps



Changes to the End-of-column

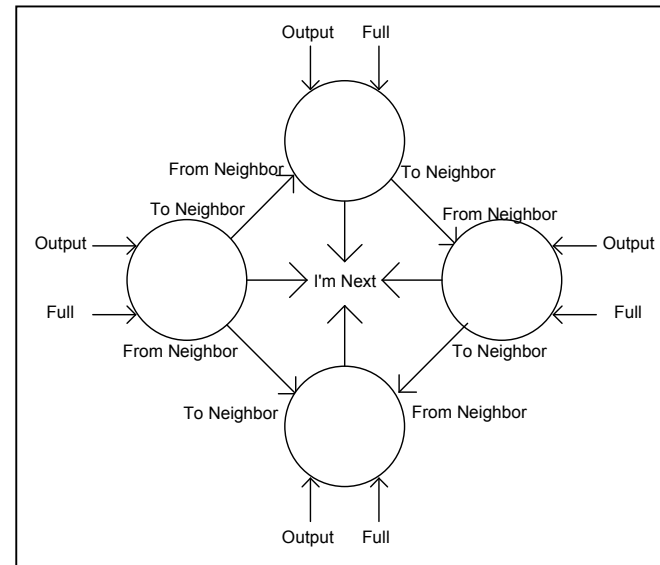
New Organization

- Added the Column State Machine
- Developed a more sophisticated Command State Machine
- Separated the clocks
- Replaced the Hit Priority Encoder State Machine with combinatorial logic
- Added an Output Priority Encoder



Changes to the End-of-column Output Priority Encoder

- Old architecture did not require an Output Priority Encoder
- Cannot permit “low-priority” hits to stagnate in the End-of-column Logic
- Must be combinatorial

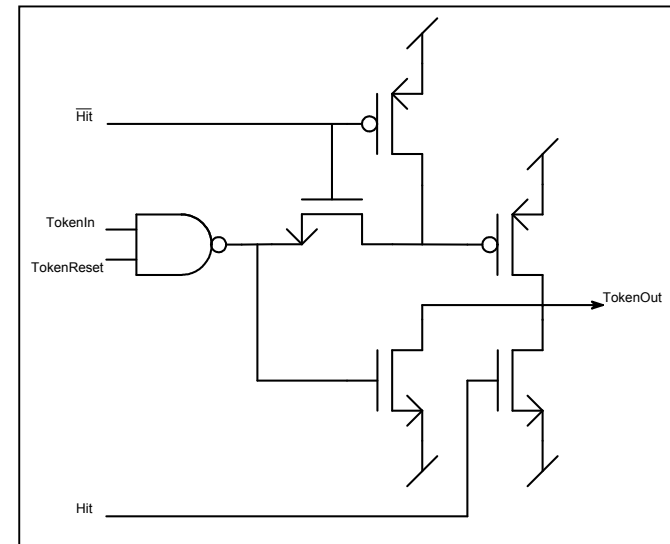




Changes to the Pixel Cell

Token Passing

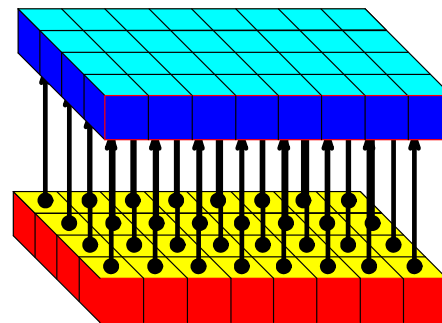
- Limitations to Readout speed
 - Column Token Skip Frequency
 - Column Token Reset
- New Architecture
 - Skipping frequencies between 7 and 8 GHz
 - Resettable





Monte Carlo-Verilog Simulation

- Structurally modeled digital architecture
- Behaviorally modeled detector and analog front end
- Converted Monte Carlo simulations of interaction chamber into Verilog input
- Simulates device under real conditions for extended periods of time



Chip Array
 Structural Model
 Models digital delays

Detector Array
 Behavioral Model
 Models "timewalk" delay
 Feeds "Hit" and "Magnitude" information to Chip Array

Luminosity	# of hit pixels in the input list	# of unmatched members of the input list	# of unmatched members of the output list
$1 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-2}$	1342	0	0
$2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-2}$	2751	2	3
$4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-2}$	11643	33	16



Conclusions

- Readout efficiencies greater than 99.6%
- preFPIX2_T bench tests successful
- preFPIX2_I still in transit
- preFPIX2_T2 (shown) recently submitted
- Anticipate full FPIX2 submission in fall 2001

