The SPI (Serial Powering Interface) chip
as an integrated power management device for serial powering

M.Trimpl, Fermilab

- Powering Schemes / SPI Motivation
- Chip architecture and Features
- Flip Chip (on PCB) Assembly
- Interface Controller, I-ADC, Shunts, Linear Regulator, OverPower Protection
- Summary and Outlook

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Serial Powering Schemes

1) External shunt regulator + transistor

- Good approach, but implies a high current shunt
- -> limited experience in HEP-IC community
- SP device enables to operate non SP-ROIC in SP mode

2) Internal shunt regulator + transistor in each ROIC

- Disadvantage: many power supplies in parallel
- Matching issue can cause hot spots and potentially kill chips

3) External SR + parallel shunt transistor in ROIC

- choice of architecture not obvious,
- detailed studies anticipated by RAL/LBNL (M.Weber, C.Haber)
- scheme (2) can be realized by any ROIC standalone
- SPI chip covers scheme (1) and (3)

feedback however more challenging and depends on implementation
Present setups and SPI Motivation

Setups using discrete components explored SP feasibility and new features (current monitoring and overcurrent protection)

**Downsides of discrete setups**
- Standard Shunts typ. current limited (100mA)
- Power transistors not rad. tolerant
- esp. 4A for module is challenging
- spacious setup
- limited performance (e.g. dyn. impedance)

-> integrated / customized solution

ATLAS SCT setup at RAL (similar setup at LBNL, Atlas pixel setup at Bonn U.)

abc-n module approach:

2x10 ROIC on a module
20 modules in a row (clearly needs integrated solution)

~1Ω at 1MHz, >50Ω for >10Mhz

[C.Haber, LBNL]
SPI - Architecture Overview

versatile SP chip - list of basic features:

• **shunt** creates Vchip (scheme1), distr. shunt (scheme3)

• communication via **multi drop** bus
  (each SPI chip has 5bit address)
  reduces number of str.-lines for SPI to minimum of 2 (3)

• spare AC coupled interfaces (**comports**)

• **ADCs** to monitor shunt and LR current

• **2x LinReg**: separate analog / digital supply
  to hook up some chips (1-3) for tests
  Not proposed as a scaleable solution
  for a whole module (linregs should be part of ROIC,
  as e.g. in the ABCn)

• **OverPower** protection (avoids detector hot spots)
  (more a open backdoor than a feature right now)

• **radtol. design** techniques, TSMC 025MM process
**Power on Reset:**
all Registers set to a default condition when chip power comes up
(current alarm default: ‘hard wired’ to ‘false’!)

**AC coupled interface:**
7 separate comports, bi-directional (input/output)
rate: $\sim 200$MHz (selectable drive current max. 6mA),
point to point and multidrop with 10 receivers
LVDS receiver with hysteresis

**Main Shunt** sets operation voltage: $\sim 1.5 \ldots 2.5$V (1.2...2.7??)
(4.3bit to select, default: 1.5V),
current capability: 1A min. (conservative number - high current designs are new!)

**Distr. Shunt:** class AB stage with dual output (redundancy)
shunt slaves are implemented in ABCn ROIC

**Linear regulator:**
LDO regulator (folded cascode OTA and output stage)
Vout: $\sim 1.2 \ldots \sim 2.5$V (VDO $\sim 200-300$mA for 500mA), with ext. 1uF min. for stability
4bit to select voltage -> $\sim 100$mV steps
Final Layout / Floorplan

Chip size: 5.7 x 2.8 mm², ~150 bumps solder chip to PCB
Final Layout / Floorplan

Chip size: 5.7 x 2.8 mm², ~150 bumps solder chip to PCB

- Dig. Controller
- ADC
- Shunt
- Linreg Vout (2x)
- Fanout (finger) for shuntmos

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**bump bonding of SPI**

**Advantages of bumps bonds (for the SPI chip)**

- **better routing flexibility (esp. on chip, similar to 3d IC-approach)**
- more robust and shorter (100μm vs 5mm) connection as wire bonds: **reliable connection is essential in SP scheme**
  - more robust in magnetic field (5T) while ramping high currents (2A)
- **better scale ability (if higher currents are needed)**
- chip backside is still fully accessible for cooling

**TSMC is placing the solder bumps!**

*In house assembly*
(e.g. Suess MA8 @ FNAL)

**First alignment test** *(step1)*
using glass samples and adhesive:

- <10μm misalign. on 8mm
  - (good enough for SPI pitch)
- 200μm squares with 12μm spacing

optional backside cooling (air / heat sink)
chip-on-board assembly at FNAL

- All bumps show continuity, no shorts
- Improvised measurement revealed $<< 10\text{m}\Omega$ per bump
- Confirmed by IZM (4 point measurement) : $1\text{m}\Omega$
- Daisy chain loaded with $200\text{mA}$ for several days -> no problem
  Note, we have 33 bumps in parallel on the SPI001

Cross section of one sandwich side:

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Limitation is precision of **solder mask opening** on the PCB (can be improved if necessary). However, good enough for 300μm pitch!
'shunt' ADC - principle and implementation

concept:

- probing shunt current using replica mos (similar to current mirror)
- current-mode ADC
  (good approach for ultra low voltage 1.3V in a 2.5V process!!)

- implementation chosen as flash ADC: simple and fast (also faster to design ;-) )
- 6bit, LSB tunable (4bit) – dyn. range ~100mA … ~2A (probing low current or high range)
- adjustable threshold for alarm
- 4bits to tune the alarm - delay (TOT requirement): ~150us … 3ms
single ADC (full) simulation
on-chip shunt

- total RMS < 100μV
- No internal compensation, but external Ccomp pad
- Two shunt transistors with 1/10 aspect ratio

[CMOS Version of TL432/A/C principle]

- Ishunt = 100mA
- total RMS < 100μV
- No internal compensation, but external Ccomp pad
- Two shunt transistors with 1/10 aspect ratio

[Graph showing dynamic range: 1.0 to 3.0V accommodates for dispersion]

Not enough phase margin for Cload >10uF (w/o Ccomp)
Shunt performances

\[ Z \leq 0.5 \text{mV/10mA} = 50 \Omega \]

\( I_{\text{shunt}} = 100 \text{mA} \) (\( I_{\text{sin}} = 10 \text{mA} \)), \( C_{\text{Load}} = 1 \mu F \)

**Compared to 1 .. 50\( \Omega \) for discrete components setup**

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OverPower Protection (option)

1. OverPower is **NOT** OverCurrent
   - current should stay the same in SP scheme!
2. Power reduction by 
   **collapsing the chip voltage**
3. Goal: reduce Vchip to minimum
   - e.g. 50mV and 4A -> $P \sim 200\text{mW}$
   - in the order of nominal operation
   - comparable to ROIC on module
   - **no hot spot**!

Sounds crazy, but serial powering is already!

**Procedure (Option) for SPI:**
1. ADC reports **current alarm**
2. Vshunt overwritten by external source (vdd)
   - forces shunt-mos in lin.region & reduces Vchip (Ron*I)
   - whole chip collapses, only shunt maintains operation

Future challenge on PCB side: voltage conserving techniques (module RnD: G.Villani)
Upon successful demonstration: integration of most promising approach in SPI
Power shunt (DC)

Note, 4 finger pairs assumed (old), actual design uses 3 finger but more bumps -> similar or better performance expected
Power shunt (DC)

Spice-Simulation with **1A per finger pair** @120°C, Vshunt=1.5V (worst case overpower-protection scenario)

-> average current per bump: ~100mA, max rating 240mA

Voltage drops:

- 20mV from pure MOS model (Ron)
- 5mV from on chip routing (bump bond approach helps here a lot!)
- 25mV from ‘Off chip’ routing: Rbump, Rtrace

\[ \text{Vdrop,total} \sim 50\text{mV} \]

Conclusion:

- Take these numbers with a grain of salt!
- However, they give good indication for feasibility e.g. a different routing topology which didn’t look too bad at first resulted in ~500mV drop
- **For 1A total current we should be on a safe side** (note, this simulation uses 1A per finger (4 of them!))
interface controller

**32 bit command word** (7bit header, 4 bit trailer) (internal state machine)

```
[1100111 CCCCC RRRRR III DDDDDDDDD 0000]
```

- **C**: 5bit Chip Adr. (30 chips on module)
- **R**: Register Adr. (20 config + 3 ADC data-register)
- **D**: 8bit register word
- **III**: Instruction Code
  - Reset Register
  - Set Register
  - Default (hard coded)
  - Read ADC / Write Register

Chip and Register wildcard 10101 (21d)
  - configure register in all chips in a setup
  - reset all registers in all chips to default

Verilog description then auto place and route using CERN radtol lib.
Full chip simulation (startup & Vshunt)

Initial condition is $I_{SPI} = 0.0 \, \text{A}$

- Database: SPI_Sub_Vshunt 7-Sep-2008
- Current ramped to 0.8A
- $C_{load}=10\mu\text{F}$
- All default conditions achieved

- Vshunt = 2.2V
- PWRon Reset pulse generated $\rightarrow$ chip in default condition
- $s_{\text{in}}$: command sent to change Vshunt to 2.2V

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Full chip simulation (I-alarm)

- Lower threshold (greater than check)
- Delay from max (~3ms) to min (~150us)
Summary / Outlook

- Discrete SP setups went through many iterations, limitations reached (features vs size vs performance)
- **SPI - Serial Powering Interface**: generic chip to explore SP schemes
  - TSMC025MM, radiation tolerant design (except distr. shunt), High current shunt (1A+), distributed shunt, AC coupled comports, 2 Linregs, monitoring ADCs, (explore) over power protection options
  - For 'single shunt on module' approach **flip chip** is the way to go
    - Solder bumps (SnPb) placed by TSMC, gold ball approach at RAL
    - **Chip on Board** (solder) assembly at 300μm pitch demonstrated at FNAL
- **SPI 0.01 submitted via GUC**, silicon back early Nov08
  - 120 chips (40 with solder bumps, 80 w/o)
- Intensive tests in preparation at RAL (M.Weber et al.)

*Though size may not matter - power for sure does!*
THE SMALLEST BLACK HOLE YET DISCOVERED BY HUMANS LOCATED AT BINARY XTE J1650-500.

WHAT DO YOU MEAN THERE’S A SIGN ORBITING THE BLACK HOLE THAT SAYS “WE HAD A LARGE HADRON COLLIDER TOO”?!
Full chip simulation (discharge cap)
Output impedance

Method
SPICE calculated transient response using 100 and 500mA Sine source \[ V_{\text{supply}} \div I_{\text{drive}} = Z_{\text{out}} \] stepped over frequency.

- No Module Level Cap Filler 100mA
- 10uF cap on module supply 100mA
- 10uF cap on module supply 500mA

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Some numbers...

- Lorentz Force:

\[ B = 5 \text{T}, \ L(\text{bump}) = 100 \text{um}, \ I_{\text{max}} = \frac{2 \text{A}}{20} = 100 \text{mA} \]

\[ F_{\text{max}} = q \, v \, B = L \, I \, B = 50 \mu\text{N} \]

idle - feature
VREF=Vshunt as function of T
Comport = Bidirectional Driver/Receiver
Linreg Performance

output impedance (measured with transient simulation):
20kHz 9m Ohm
200kHz 90m Ohm
2MHz 780m Ohm
20Mhz 1.2 Ohm (fits the step response)

total rmsNoise: 400…600uV (depending on vdd)

Here, impedance at high frequency limited by external ESR (10uF, 2Ohm)
However, simulation show stable behavior down to Resr~500mOhm,
I measured 670mO at 10uF caps in the lab as series resistance

transient step: 400mA to 460mA (like 3 ABCn)
Selectable internal comp caps depending on the op-region
Frequency behavior / output impedance

I_{shunt} = 100mA
C_{load} = 1\, \mu F \text{ and } 10\, \mu F
TSMC is placing the solder bumps!

Very first alignment tests done using glass samples and adhesive:

\(<10\mu m\) misalign. on 8mm

**Suess MA8 FC-Bonder at Fermi**

-> in house assembly

Alignment marker:

1cm² alignment mask (glass):

(2mm targets shown)

200\(\mu m\) squares with 12\(\mu m\) spacing

-> sufficient for SPI bumping (wrt alignment)

**Next step:**

Daisy chains modules from IZM (300\(\mu m\) pitch)
to test solder assembly