Recent Test Results on Comtel airplane backplane using Pulsar 2b

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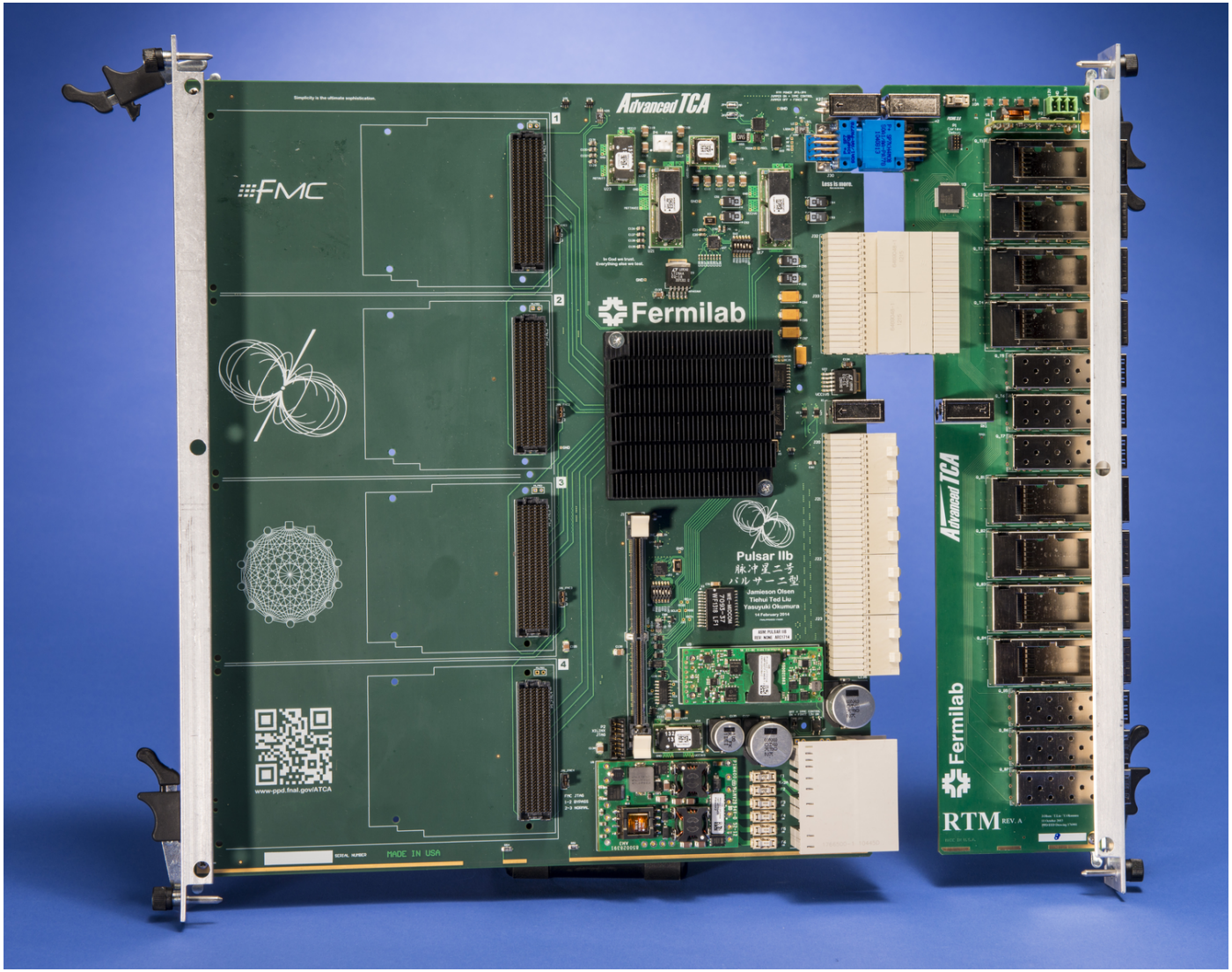
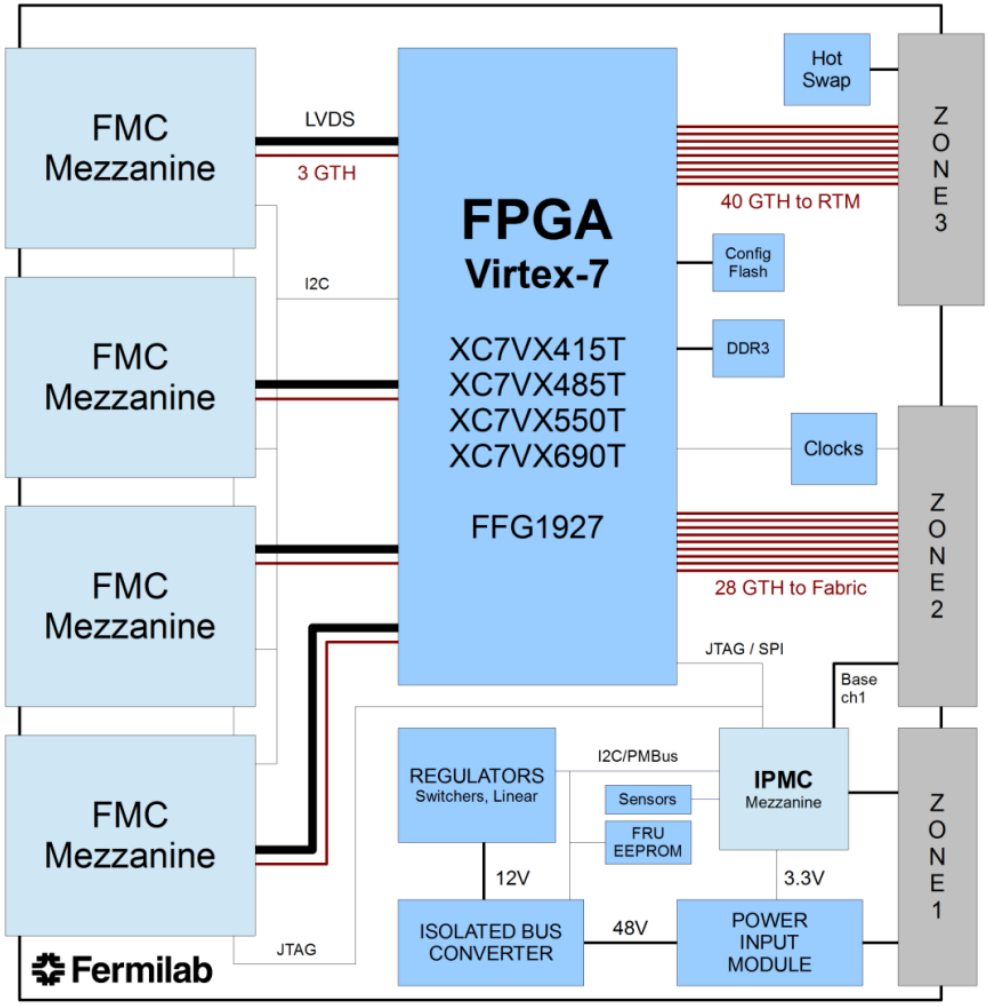
Pulsar II Hardware



Pulsar IIb Features



Xilinx Virtex 7 FPGA

Up to 80 GTH transceivers

- 13.1 Gbps (in -3 speed grade)
- 40 for RTM
- 28 for Full Mesh Fabric
- 12 for Mezzanines

Four FMC Mezzanine Cards

- 35W, up to 60W possible
- LVDS up to 34 Gbps unidirectional
- 3 x GTH up to 30 Gbps bidirectional

DDR3 256MBytes

IPMC Mezzanine Card

Backplane clock distribution

- M-LVDS on CLK3A and CLK3B

This is the original Pulsar IIb board design. No revisions or "green wire" modifications have been required thus far.

Backplane Testing I

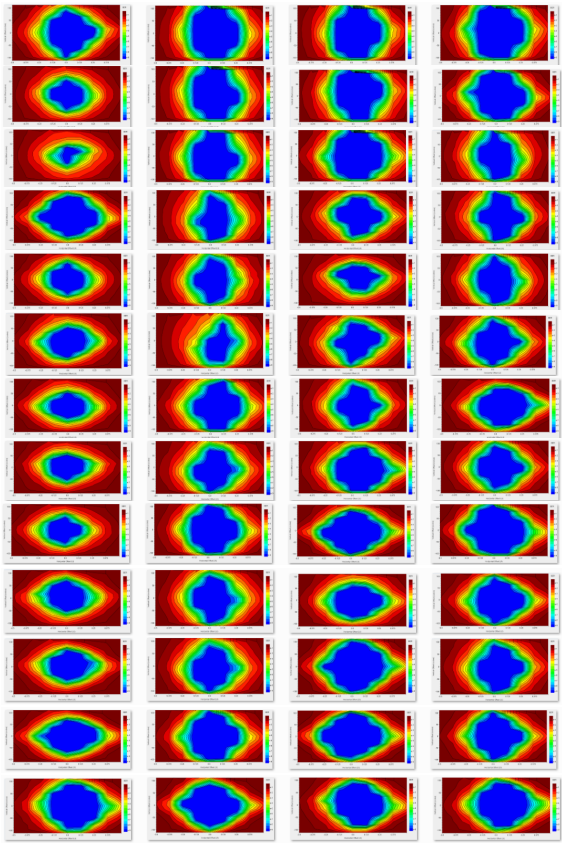
- Install Pulsar IIb boards in the shelf
- Program IBERT firmware image into each board
- Enable PRBS test pattern generation/checking on all board to board connections
- Use the Vivado Serial Link Analyzer tool to apply link settings, reset BER counters, etc.
- The same boards are installed in the same slot positions when doing shelf comparisons

Backplane Testing II

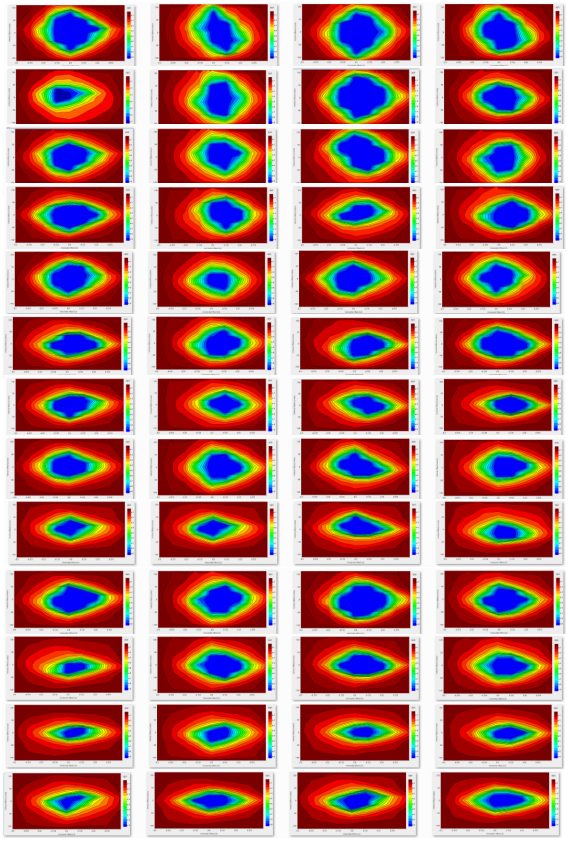
- As you will see in the following slides it is difficult to interpret backplane link performance
- At high data rates many factors influence link performance
  - Crosstalk
  - Attenuation
  - Impedance mismatch and
  - Reflections from via stubs, connectors, etc.
- Why do some links look great, while other links have a small eye and occasional bit errors?
- Over the past year one of the primary challenges we faced is how to determine if the Pulsar IIb design or the backplane design is dominating the link performance…

Early shelf test @ 10Gbps

Shelf A



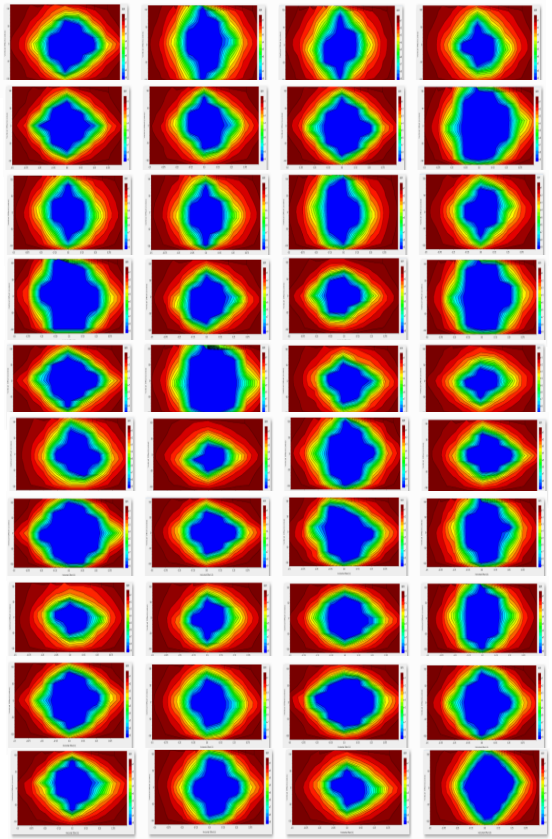
Shelf B



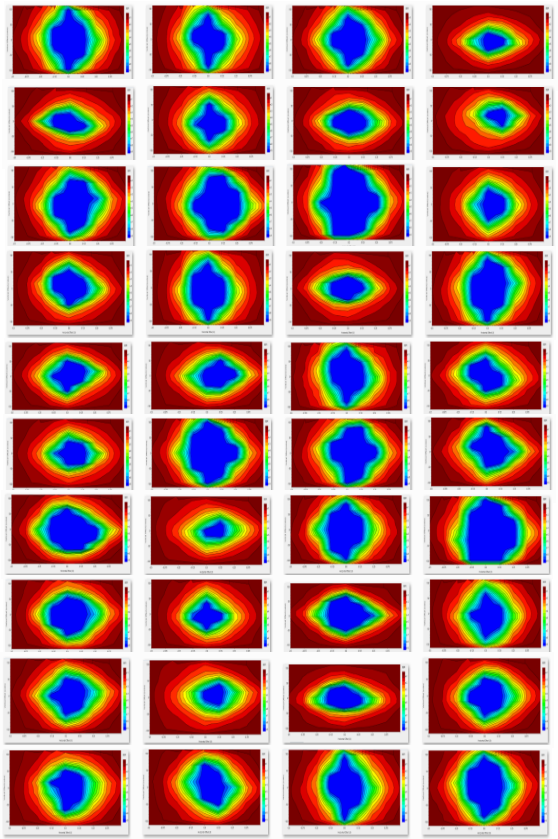
In this test one Pulsar IIb board was installed in slot 1, and another Pulsar IIb board was cycled through the other 13 backplane slots.

Multiple Board Backplane Testing

Shelf A



Shelf C: Old Comtel



Five Pulsar IIb boards are installed and tested simultaneously at with links running at 10Gbps. A is better than C, but we still see large variations in the eye size in both cases. Tuning is required to get these boards to run error free for several days.

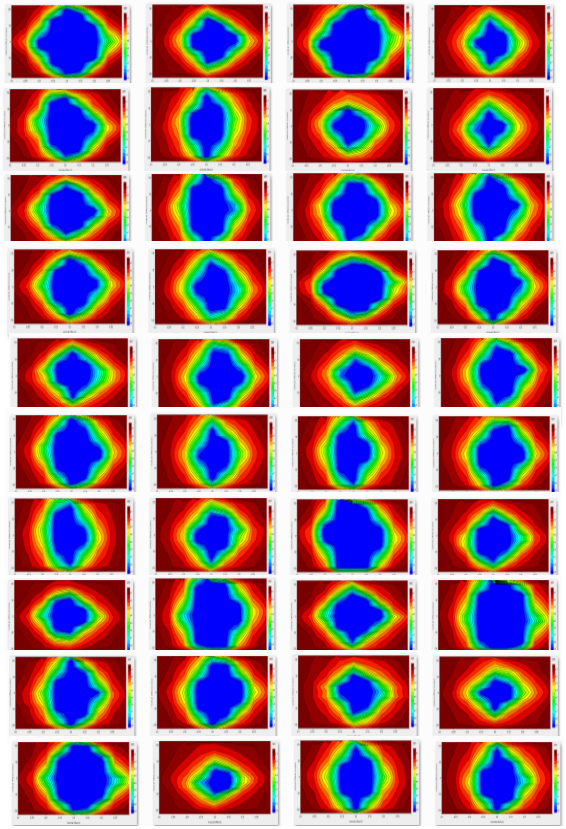
New COMTEL Backplane

- We have been taking part in technical discussions with COMTEL Engineers over the past year regarding the next generation high performance full mesh ATCA backplanes
- As a result we are one of the first companies to test their latest backplane design, called Air-/-Plane
- This is one of the very first 100G full mesh backplane designs on the market
  - 1 channel = 4 ports running up to 25Gbps each
  - Split Zone1/Zone2 backplane design for easy upgrades

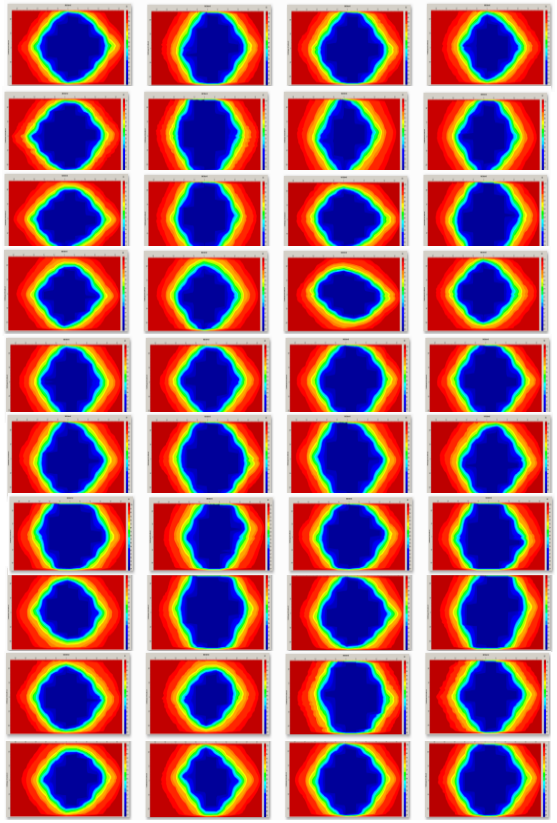
COMTEL ELECTRONICS

New Shelf received December 2014

Shelf A

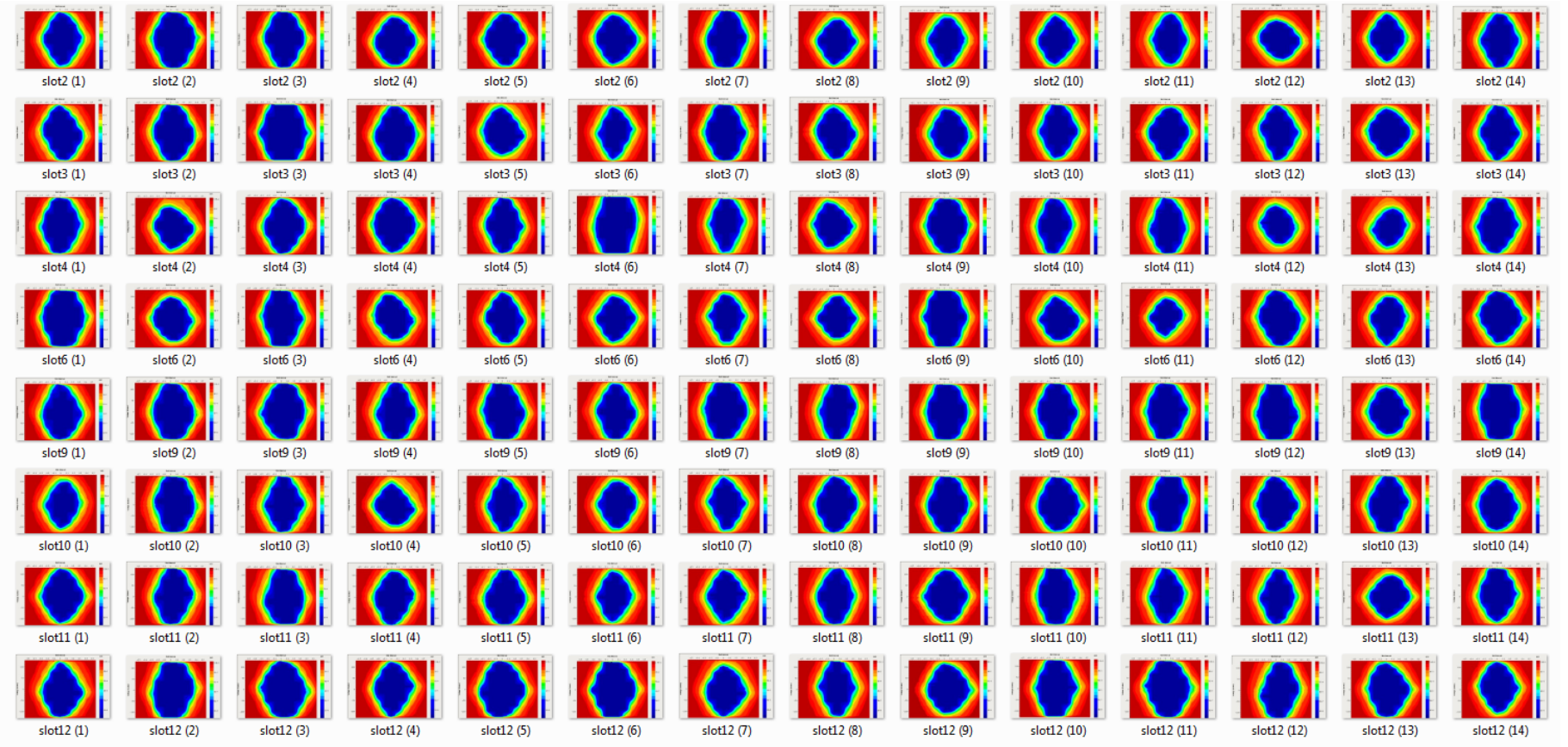


COMTEL Air-/-Plane



Shelf A results are with 7 boards installed, after GTH tuning. The COMTEL results are with 8 boards installed *and no link tuning*. Note the color difference is due to the way Vivado and ISE-Chipscope display the eye. In either case blue = BER of 10^{-9}.

8 Boards Installed in the Air-/-Plane Shelf @ 10Gbps



All 112 links between the eight Pulsar2b boards are shown here. This test ran for 4 days with **no errors**, achieving a **BER < 3x10^{-16}**. This backplane has the *largest*, and *most consistent* eye diagrams we have ever encountered. And this is without tuning.

Backplane Testing: Conclusion

- Prior to the Air-/-Plane backplane we were testing a combination of the Pulsar IIb characteristics and backplane characteristics.
  - Difficult to determine which parts were effecting backplane link performance
- With the Air-/-Plane backplane we are now getting a clearer picture of the Pulsar IIb board performance
- Pulsar IIb fabric links are fairly consistent at 10Gbps
- In the past with other crates, marginal links were caused by backplane, not the Pulsar IIb
- The performance of Pulsar IIb and Comtel Air-/-Plane seem to match very well