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**PPD / EED / Infrastructure Group**

Technical Note: IG\_ 20140001

Michael S. Matulik

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**USCMS HCal ngCCM**

**Design Review**

**Findings Report**

**Overview:**

This Design Review of the USCMS HCal next generation Clock and Control Module (ngCCM) was requested on 13-Jan-2014. Information for the review was supplied by USCMS and by HCal management using the following links:

<https://cms-docdb.cern.ch/cgi-bin/DocDB/ShowDocument?docid=11876>

Information made available, and used to complete this review, includes; a preliminary schematic (Rev. 0.9) dated 09-Jan-2014 and a Bill of Materials (.xlsx format) dated 09-Jan-201. Additional overview information was supplied via the introductory E-mail request.

**Scope of the Review:**

The schematic was examined in several passes, first for the safe delivery / distribution of power. Subsequent examinations looked at; the distribution of the MCLK and Data signals, circuitry used to obtain temperature, voltage and current draw information.

**Findings:**

Power (V1V2) is delivered to the module via the J1 Eurocard (Type-C) connector using 9 contacts. Each contact is rated at 1.5A (DIN41612). The stated value of fuse F1 is 6.3A, which complies with the rule-of-thumb value of 2/3 used to de-rate power carrying contacts in parallel.

The number of power return pins (backplane Ground) is sufficient.

The stated desired trace width / current carrying capacity for power traces (V1V2 and VIN) on the schematic is 0.150 inch wide / 10A. Using IPC-2221 design charts and assuming a maximum 20˚C temperature rise, the desired cross sectional area for internal traces carrying 10A is 0.700 in2. For external traces, the desired cross sectional area decreases to 0.25 in2. Using this standard, and the stated trace width, the anticipated minimum finished copper thickness for internal and external layers would be 0.0047 in. and 0.0017 in. respectively.

The voltage converters used to generate 3.3V, 2.5V and 1.5V are listed as the CERN AMIS5MP DC/DC converter modules. Information about these DC/DC converters suggest that they are not available in production versions, but as a “representative prototype”. Production versions may possibly be available in early 2014 and will be pin-to-pin compatible with the prototype versions. Documentation suggests that these devices are / will be radiation and magnetic field tolerant.

The stated current carrying capacity for power traces (3V3, 2V5 and 1V5) are 4A (maximum stated output of AMIS5MP) and calls for a trace width of 0.045 inches. Using IPC-2221 design charts and assuming a maximum 20˚C temperature rise, the desired cross sectional area for internal traces carrying 4A is 0.175 in2. For external traces, the desired cross sectional area decreases to 0.075 in2. Using this standard, and the stated trace width, the anticipated minimum finished copper thickness for internal and external layers would be 0.0039 in. and 0.0017 in. respectively.

The 1.2V power net is generated by an LP38853 adjustable voltage regulator from Texas Instruments. The stated maximum current delivering capacity of this device is 3A. There is no mention of the radiation hardness of this device in T.I. documentation. Has this device been tested in an environment similar to what it would be expected to be exposed to in the CMS detector hall? The input, output and bias capacitors for the LP38853 indicated on the schematic are consistent with values recommended on the T.I. datasheet.

The stated current carrying capacity for the power trace 1V2 is 3A and calls for a trace width of 0.030 inches. Using IPC-2221 design charts and assuming a maximum 20˚C temperature rise, the desired cross sectional area for internal traces carrying 3A is 0.125 in2. For external traces, the desired cross sectional area decreases to 0.050 in2. Using this standard, and the stated trace width, the anticipated minimum finished copper thickness for internal and external layers would be 0.0042 in. and 0.0017 in. respectively.

The component values and circuit structure for the MC100LVEP111 Clock Distribution integrated circuits are consistent with the datasheet for the device. There is no mention of the radiation hardness of this device in the ON Semiconductor datasheet. Has this device been tested in an environment similar to what it would be expected to be exposed to in the CMS detector hall?

The circuit structure for the AD7417A ADCs is consistent with the datasheet suggestion for the device. There is no mention of the radiation hardness of this device in the Analog Devices datasheet. Has this device been tested in an environment similar to what it would be expected to be exposed to in the CMS detector hall?

The circuit structure and component values for the LTC2945 power monitor are consistent with data sheet suggestions for the device. There is no mention of the radiation hardness of this device in the Linear Technology datasheet. Has this device been tested in an environment similar to what it would be expected to be exposed to in the CMS detector hall?