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**PPD / EED / Infrastructure Group**

Technical Note: IG\_ 20140005

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**Results of Visual, Electrical and Mechanical Inspection U.S. CMS Forward Pixel HDI Flexible Printed Circuits Received 19-Sep-2014**

**Overview:**

On September 19th 2014, Fermilab received 150 U.S. CMS Forward Pixel HDI (Rev. C) flexible printed circuits. In accordance with an agreement made with the vendor (Compunetics), these circuits were delivered in a combination of singulated and circuits left on one of three panels. Further, the three panels were processed differently where the application of the bottom layer solder mask / cover coat is concerned. Specifically, those circuits from Panel SN1 were processed adding the traditional polyimide cover coat to the bottom side copper layer. Those circuits from Panels SN2 and SN3 received a standard thickness of epoxy flexible solder mask before receiving and additional polyimide cover coat. The circuits in Panel SN2 were singulated (removed from the panel) prior to the application of the cover coat.

The Rev. C HDIs received earlier in the year suffered from problems relating to the ability to realize robust / reliable aluminum ultrasonic wire bonds to the nickel / gold plated wire bond pads. The most recently delivered circuits were provided after members of the U.S. CMS FPix collaboration discussed our concerns with a representative of Compunetics and were, in part, to be used to evaluate the ability of Compunetics to deliver circuits that could be successfully wire bonded and in part to provide the U.S. CMS FPix information for better specifying such circuits in the future.

**Results:**

Sections made of some of the circuits from each panel indicate that the copper thickness of the four layers was more uniform, with noticeable increase in the copper thickness of the upper layer (where wire bond pads are located). Within our abilities to do so, we measured thicker nickel / gold plating on the wire bond pads as well. We suspect that the increased thickness of the nickel / gold layers was primarily due to increase in the nickel layer thickness. The combination of thicker copper and thicker nickel thicknesses meet the request made by the FPix Collaboration to Compunetics during a meeting in August of 2014. We will use this data to specify the minimum copper thickness (expected to be 20μm) and to request thicker nickel layer thickness (5μm) for production circuits.

In general the ability to successfully wire bond to circuits from these three panels was judged to be better than those delivered in the initial shipment of Rev. C circuit, but a number of caveats need to be discussed. Note that the wire bonding results for these were not as good as those observed for the first batch of HDIs (variously identified as either prototype or Rev. A) we received.

**Short found on a circuit that had passed Electrical Test:**

Visual inspection revealed a suspected short between wire bond pads for one Read Out Chip position on one circuit. This particular circuit (SN2 – P5) exhibited the stamp from MicroCraft indicating that it had passed their electrical test. Careful testing with a pair of probes revealed that the wire bond pads in question were indeed shorted, exhibiting a resistance of ~4Ω. This causes some amount of concern regarding the accuracy of electrical testing. Comments on this observation are welcome.



1. Short on electrically passed circuit SN2-P5

**Wire Bond Pad Width:**

The nominal width of the wire bond pads located along the two long edges of the HDI is expected to be 100μm. Measured pad widths for circuits from all three panels were significantly narrower, averaging about 80μm. Comparison of the width of Read Out Chip wire bond pads for 5 different circuits, some dating back to our first prototype order for these circuits are depicted in Figures 2..6. Pads on previously received Rev. C circuits were much closer to the expected nominal value. While bonding to these pads in mode in which these tests were conducted resulted in generally acceptable wire bonds, collaboration members expressed concern that narrow pads would cause inefficiencies in the production wire bonding process, as the desired center-of-pad sweet spot for landing wire bonds would be more difficult to hit consistently. The TBM wire bond pads located in the center of the circuit are also narrower than expected, by about the same amount leading us to the conclusion that (at least) the upper layer of the circuits was over-etched. We feel that we would be able to return for replacement circuit where pad width (for Read Out Chip wire bond pads) was measured to be less than some minimum (considering 90μm). Comments on this suggestion are welcome.

2. HDI Rev A: #59 Width : 90 - 95μm



3. HDI Rev C: 2-P28 Width 95 - 100μm



4. HDI New: SN1-P33 Width: 75-80μm



5. HDI New: SN2-P22 Width: 75-80μm

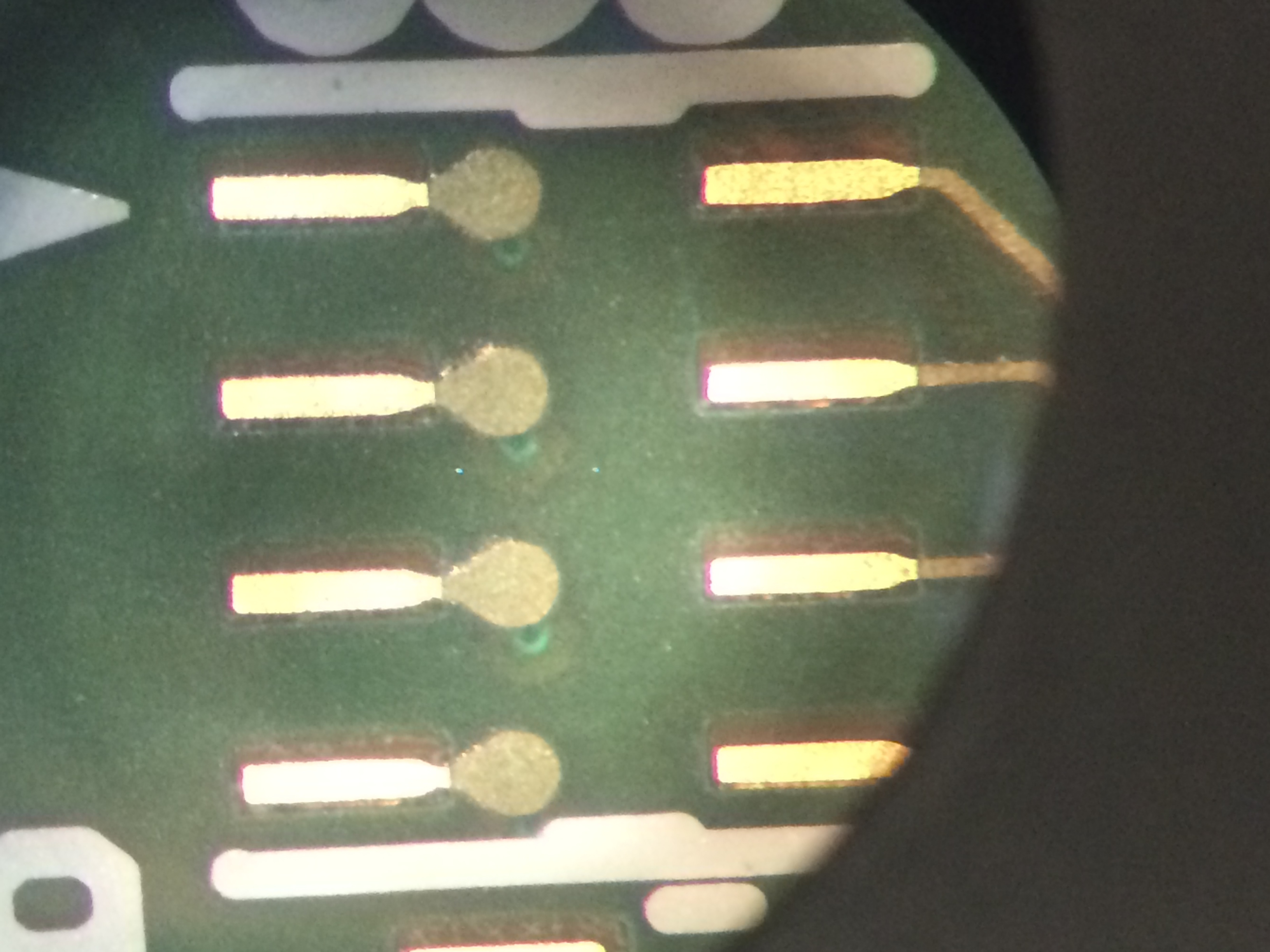


6. HDI New: SN3-P3 Width 80-85μm



**Via Breakout:**

Visual examination of the received circuits revealed some number (mostly those that had not passed electrical testing) exhibited evidence of vias not fully captured by pads on the upper copper layer. See an example in Figure 7. It is assumed that in future orders this sort of defect will not be observed in future delivered circuits as this deemed to be a violation of IPC standards.



7. Via breakout from upper layer pads

**Shifted Circuit Outline Routing:**

Unlike the vast majority of circuits we’ve received from Compunetics in the past most of the most circuits recently received exhibit a shift in the routed circuit outline with respect to copper features in the circuit. This was particularly noticeable along the two long edges of the circuit, where the Read Out Chip wire bond pads are located. The nominal distance from the edge of the wire bond pads to the routed edge of the circuit is expected to 225μm for both long edges. Measurements of several circuits suggest circuit outline shifts of up to 90um. Measurements of the dimensions of the outlines themselves match well with the expected dimensions furthering our assertion that the routed outline is shifted. An example of the shift in circuit outline can be observed in Figure 8. The dark brown area is the opening in the upper layer solder mask. It was also noted that wire bond pads that wound up closer to the routed edge of the circuit exhibited discoloration. We have no information regarding the effect of this discoloration on the ability to wire bond to these pads. We are still investigating the effect of the shifted outline on the various assembly steps the circuit will be subjected to. We are aware that the nominal location of the circuit outline has a tolerance with respect to upper layer copper features in the circuit and are interested in learning what this location tolerance might be.

8. Shifted Circuit Outline on one HDI

**Metallic Splatter Surrounding Wire Bond Pads:**

Examination of the circuits from panel SN1 exhibited what appears to be splatter around the wire bond pads. Inspection was unable to determine the material that comprises the splatter, but our suspicion is that it’s metallic in nature. Comments on this observation are welcome.



9. Metallic spatter between wire bond pads

**Orange Peel Appearance of Bottom Layer Polyimide:**

It was noted that the appearance of the bottom side cover coat on many circuits exhibited a structure best described as “orange peel”. This structure does not have any obvious relationship to the bottom copper structure and has not been noted on previous circuits received from Compunetics. Unsupported speculation suggests some effect of over-heating of the adhesive in the cover coat product. This visual structure was apparent on circuits from all three panels. While it’s not clear that this structure is a problem for our fabrication processes (circuits with this appearance appear to hold vacuum), we are interested in learning the source of this appearance.

**General Quality of Circuits:**

Aside from the width of the upper copper layer pads, the quality of the circuits was generally acceptable. Visual inspection revealed some “features” that we would feel comfortable returning for replacement should they be received in the production order. Examples of these features include, but are not necessarily limited to: Missing or contaminated pad plating, particularly if it’s judged to negatively affect the ability to wire bond or solder to the pad. Exposure of upper copper layer features through the solder mask, particularly in the limited locations where such an exposure is likely to result in a short to a top-side mounted metalized component. Severe discoloration of wire bond pads; to the point that successful wire bonding is unlikely. Comments on these observations are welcome.

Our initial evaluation of the circuits from the three different panels leads us to lean toward those that have the bottom layer polyimide cover coat laminated over (under?) the bottom layer solder mask. As Compunetics has expressed some concern regarding the long-term reliability of the interface between the cover coat adhesive and the epoxy solder mask, we are interested in evaluating the aging of this interface. Examining the expected environmental contributors that these circuits would expect to be exposed to, we are most concerned about the response to radiation. Flexible printed circuits have been subject to radiation in the past and data for this exposure exists. Please provide the product used for the bottom layer cover coat so that we can investigate if the adhesive in this product has been evaluated for radiation damage.