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**PPD / EED / Infrastructure Group**

Technical Note: IG\_ 20140007

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**U.S. CMS Forward Pixel HDI**

**Internal Review**

**Ancillary Information**

**Overview:**

The HDI is a 4 layer flexible printed circuit that performs 4 primary functions for the U.S. CMS Forward Pixel effort:

* Provide the interface between sixteen PSI46digv2.1 Pixel Read Out Chips designed by the Paul Scherrer Institute and the Token Bit Manager designed by Rutgers.
* Provide for the ability to control and read out the TBM.
* Provide the ability to bias (≤600V) the Pixel Sensor.
* Distribute low-voltage power to the Read Out Chips and TBM.

The FPix HDI performs the same functions as the HDI designed and used by the CMS Barrel Pixel collaboration. The pixel sensor and read out chips used in both detectors are identical and the TBMs used in both are nearly so. The two groups have collaborated; sharing observations, concerns and solutions.

The HDI is laminated to the top of a Pixel Sensor, which in turn has been bump-bonded to the top of 16 Read Out Chips to form a Module. A Module will be attached to two sides of a Blade. Some number of Blades (depending on radial position) will be connected in a turbine like structure to form a Half-Disk. A representation of a Module can be seen in Figure 1. Some of features of the HDI can be seen in Figure 2.

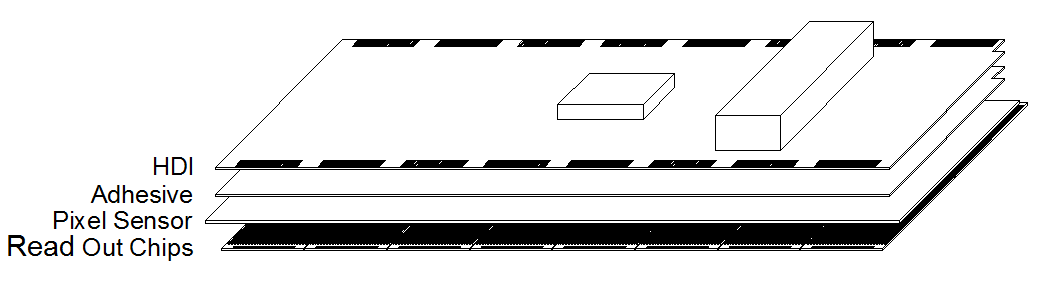
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Figure 1. FPix Module.

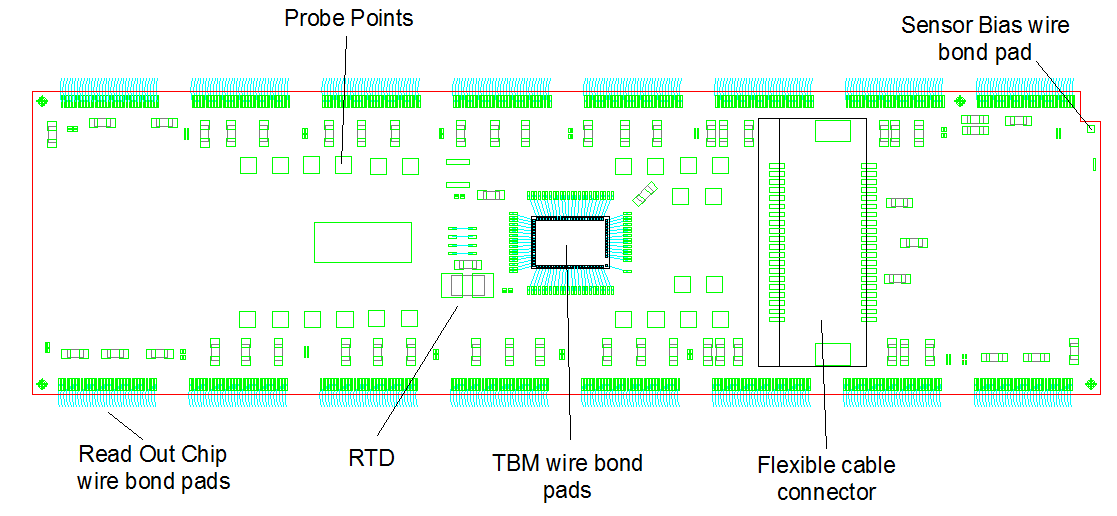


Figure . Some HDI features.

**Initial Design Decisions:**

Why flex?

Connections between the HDI and both the bare-die TBM mounted on the HDI and the bare-die Read Out Chips bump bonded to the bottom of the sensor are realized using ultrasonic aluminum wedge wire bonds. The wire bond pad feature size, as well as the desired via diameter and trace width and spacing, are readily realizable in flexible printed circuits. Additionally, the thickness of a flexible printed circuit for a 4 layer design is less than a comparable rigid epoxy-resin printed circuit board. The flexible printed circuit board solution is also less expensive than ceramic based circuits.

Why not the same as the BPix HDI?

The BPix HDI is also a flexible printed circuit. The vendor chosen by CERN to fabricate the BPix HDIs utilizes a method which can be described as being additive, contrasted to the subtractive method utilized by traditional printed circuit board fabricators (rigid or flex). At the time the decision was made to pursue traditional printed circuit board fabrication methods, we received budgetary quotes that indicated the cost of the FPix HDI to be ~10% that of the BPix solution. With ~1000 circuits to be purchased this suggested a significant savings. Recent budgetary quotes for the production circuits, presumably more accurate after delivering Prototype and Rev. C circuits, have not indicated a significant increase in cost.

Interface to Read Out Chips

The digital Serial Data stream from any Read Out Chip to the TBM runs at 160Mb/s NRZ and requires the greatest bandwidth of any signals to / from a Read Out Chip. Each bit position is 6.25ns wide. Assuming the HDI needs to support a 1.6ns transition time for each pulse position (25% bit width), the required bandwidth for the trace connecting a Read Out Chip to the TBM can be estimated to be 219MHz. The velocity of propagation in polyimide circuits is approximately 0.58c resulting in a wavelength estimate of 0.8m.

The TBM has been located on the HDI to equalize the distances of the two longest Serial Data connections. The longest connection is 35.6mm. As a fraction of the wavelength in polyimide circuits this distance is λ/22. Falling between the two generally accepted guidelines of λ/20 and λ/40, transmission line aspects of these traces were ignored – the impedance of the traces were not specified and terminating networks were not implemented.

Though differential, the signals between Read Out Chips and the TBM were considered as two independent voltage signals 180° out of phase in the design of the HDI. The routing of the traces associated with these signals was preferentially on the third copper layer, immediately above the ground plane to minimize noise emissivity and sensitivity. The pairs of traces were routed to be in parallel, closer to each other than to other traces. Figure 3 shows a representation of the Serial Data output driver on a PSI46digV2.1 Read Out Chip. Pull down resistors (37Ω) located on the TBM receivers terminate the traces connecting the two chips. The estimated impedance of any single trace associated with the Read Out Chip / TBM interface is 38Ω.

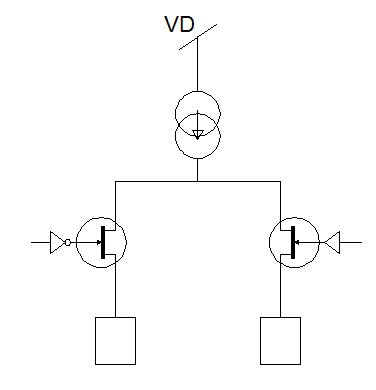


Figure . PSI46digV2.1 Differential Output Driver

Interface to TBM

Besides connections to the four groups of Read Out Chips, the TBM requires a communication path to a control and data acquisition hardware interface located approximately 0.76m away. An aluminum flexible printed circuit cable that inserts into a flex circuit connector mounted on the HDI is the path that these signals traverse. To simplify the layout of the HDI, any terminating networks required by this long connection are to be located at the far end of the flex cable. Additionally, all corresponding HDI traces are very short (~9mm) and located on the upper copper layer (routed without vias) to minimize impedance changes.

Bias Voltage Routing

The bias voltage network on the HDI consists of a single series current limiting resistor. A single trace runs from the four contacts on the flex cable connector to the resistor, then from the resistor on to the wire bond pad in the corner of the HDI that will be used to make a connection to the pixel sensor itself. IPC-2221 guidelines have been consulted to determine minimum same-layer conductor separation appropriate for 750V.

Low-Voltage Power Distribution

Each Read Out Chip requires two low-voltage power connections to operate. The maximum current draw for a PSI46digV2.1 chip from the VA supply (~3V) is 25mA. The expected maximum current draw from the VD supply (~2.5V) is expected to occur at the chips located nearest the beam pipe after significant irradiation. Even though the chip pitch is small (8.1mm) the expected maximum current draw for each chip further away from the beam pipe is less than it’s predecessor. The anticipated initial Read Out Chip current draw from the VD net for all chips is 25mA. After irradiation in CMS, the chips on the blade closest to the beam pipe are expected to draw between 33 and 58mA. To save mass, and to be able to properly route traces between Read Out Chips and the TBM, the VA and VD nets were not implemented as HDI wide planes. Instead, power is delivered to the Read Out Chips over wide traces on inner layers. These traces arranged to minimize the number of Read Out Chip connections in a given length.

To gauge the effect of parallel connections of Read Out Chips to each power bus, we calculate the anticipated resistance associated with one Read Out Chip pitch worth of the trace. We can then sum the currents flowing through that segment to calculate a voltage drop for that segment. Each next segment will see less current, equal to that drawn by a Read Out Chip. The anticipated copper thickness for each inner layer is 18μm.

The layout of the inner layer VA power trace is such that the current to a maximum of 5 chips needs to pass through the first chip segment in that string. The width of the VA trace is 1.7mm. Using 1.71x10-8 Ωm as the resistivity of copper we calculated the resistance per Read Out Chip segment (8100μm) to be 4.5mΩ. Summing the voltage drops, the Read Out Chip at the end of the power trace can expect to be 1.7mV less than the VA voltage at the connector.

The layout of the inner layer VD power trace is such that the current to a maximum of 8 chips needs to pass through the first segment in that string. The width of the VD power trace varies from the region under the TBM, were its very wide to the first Read Out Chip in the string. We don’t count the current drawn by the TBM against this calculated voltage drop seen by the last Read Out Chip in the string because this area is wide and close to the connector. The width of the trace making up the first segment is 2.2mm and its length is 34mm. The calculated resistance for this segment is 14.7mΩ. The width of the power trace at the Read Out Chips is 1.8mm with a calculated resistance of 4.3mΩ for each 8100μm length. The Read Out Chip at the end of this trace can be expected to be 9.7mV less than the VD voltage at the connector using the anticipated current drawn by irradiated Read Out Chips in specific positions on the HDI.

**Circuit History:**

The vendor fabricating these circuits is the same one that made all of the FPix flexible printed circuits currently installed in CMS. The vendor has been very responsive to our requests for; information, explanations, modifications and suggestions in all of our dealings with them. The features that make the current HDI circuits difficult to fabricate are the via hole diameter (100µm) and the via pad diameter (250µm). These features are precisely those that allowed the FPix collaboration to pursue an alternative to the BPix solution. The vendor making these pre-production circuits has been the only one to respond to our requests for quotation.

We have received three deliveries of HDI circuits: Approximately 50 Prototype circuits and two deliveries of Revision C circuits (approximately 50 in each). There was an approximate 18 month gap between the delivery of the Prototype circuits and the first batch of the Rev. C circuits. There was a 5 month delay between the two deliveries of Rev. C circuits. These delays allowed the FPix Collaboration opportunities to evaluate the design and implementation of the HDI circuits.

Modules assembled and tested with the Prototype version of the HDI revealed one major functional issue. The collaboration generated a number of desired features that were added to the design as the revision level (referring to the schematic) changed from Prototype to C. All of these features, and a correction for the major issue, were realized in the current revision.

Evaluation of the first batch of Rev. C circuits revealed a number of issues which were brought to the attention of the vendor. To complete the order of ~50 Rev. C circuits, the fabricator produced three panels of 50 circuits each. To allow us to investigate a number of fabrication options, the fabricator agreed to process each of these panels slightly differently and to deliver all circuits for our inspection. We were able to note improvements in the second batch of circuits. However, we noted other issues in the second batch that, after consulting the fabricator, were determined to be mainly related to lack of attention in the fabrication process. These issues resulted in circuits that would be rejected during our incoming inspection process and returned for replacement were we receiving only good circuits.

Bias voltage short:

One major functional issue was discovered soon after the first of the Prototype circuits were assembled into modules - we were unable to apply bias voltage to the pixel sensor. The construction of a module has an HDI laminated to the upper surface of the pixel sensor, where the bias voltage is distributed. The lamination layer is very thin. The Prototype HDIs were fabricated with a bottom layer flexible solder mask. We specified that the circuits should be button plated instead of panel plated when plating the via barrels to save mass in the circuit (less copper). The plated buttons should have been sanded by the fabricator after plating to reduce their profile, but this process step was skipped. This resulted in bumps on the buttons surrounding the vias. These bumps pressed through the bottom layer solder mask and then again through the thin lamination layer. This resulted in shorts to the pixel sensor upper surface, which is conductive. The bottom layer of the HDI is where the ground plane is located. There are many connections to the ground net, all require vias. While there were undoubtedly other nets shorted to the sensor, it was most noticeable in ground and resulted in the inability to bias the sensor beyond a volt or two due to current limiting in the high voltage supply.

To combat the problem of via buttons exposed through the bottom layer solder mask two corrections were implemented in the first batch of delivered Revision C circuits: The bottom layer solder mask had been replaced by a polyimide cover coat and attention was paid by the fabricator to sanding the plated via button to reduce their profile. The initial high voltage testing of these circuits produced satisfactory results, but examination of the data sheet for this cover coat product suggested the potential for bias voltage break-through of the 12.5μm thick polyimide layer in the long-term. Retesting at significantly greater voltages (in excess of ~1000V) resulted in breakdown of the polyimide.

In concert with the circuit fabricator, we arrived at a circuit construction modification that we intend to specify for the production order. As previously noted the receipt of Revision C circuits was split into two widely delayed deliveries. We took advantage of this delay to ask the fabricator to supply circuits that were processed differently where the bottom side covering was concerned to allow us to evaluate more than one solution.

One third of the latest received circuits were laminated with a polyimide cover coat that was twice as thick (both in the polyimide and adhesive layers) than the initially received Rev. C circuits. This type of circuit was tested for high voltage standoff (@1800V) and found to be completely acceptable. These circuits exhibit a feature that presents concern about the ability to properly wire bond to them – they aren’t flat. The speculation is that the unbalanced construction (solder mask on top, cover coat below) results in the cupping of the circuit. While the cupping can be overcome by vacuum during the TBM attach and wire bonding process, there was concern that the cupping may pull the edges of the circuit away from the sensor after lamination and affect the HDI to Read Out Chip wire bonds.

One of the approaches we took to mitigate the problem with plating associated with vias punching through the bottom layer solder mask of the Prototype circuits was to cover the bottom surface with polyimide tape, which worked when tested with high voltage. The circuit fabricator offered, and we accepted, to laminate a small number of mechanical circuits (electrically bad) with a bottom layer polyimide cover coat. The existing solder mask on these circuits was not removed. These circuits passed our high voltage tests as well. The remaining two-thirds of the final shipment of Rev. C circuits were finished in a similar manner, but processed differently. Both had a bottom layer polyimide cover coat laminated over the solder mask. One third had the cover coat applied while the circuits were still part of the processing panel then singulated, the other third had the cover coat applied after the circuits were routed from the panel –as the fabricator had processed the mechanically bad Prototype circuits for us earlier. Both of these batches of circuits were fabricated with same thicker polyimide cover coat product used in the circuit with no solder mask. Neither batch of these circuits exhibited the cupping to the extent that the circuits without the solder mask did.

High voltage testing of the circuits with bottom layer polyimide cover coat over solder mask will likely not be performed – the cover coat is the same as that placed on the bare circuits and the solder mask offers some additional thickness. Our intent is to order production circuits with bottom layer cover coat applied over solder mask while the circuits are still in the panel, which is a more efficient process for the vendor.

Wire bonding issues:

Wire bonding to HDI circuits will be performed at three locations – Fermilab, Nebraska and Purdue. Each site performed studies on the Production HDI circuits and found them to be acceptable. The first shipment of Rev. C HDIs did not perform well in this regard. Through much investigation by members of the collaboration we determined, and shared with the circuit fabricator, the following information:

* The copper in the upper copper layer (where wire bond pads are located) was too thin. Ultrasonic bonding forms a metal-to-metal connection between the aluminum wire and the gold / nickel plated copper pad by pressing the wire into the pad and providing ultrasonic energy to form the weld. The thin copper layer was judged to not provide sufficient resistance to the pressure imparted by the wire bonder, resulting in tenuous connections. This speculation was confirmed when we sectioned some of these circuits and examined them for wire bond pad metal thickness. Those from the first batch of Rev. C circuits were significantly thinner than similar pads from Prototype circuits.
  + We shared our findings with the circuit fabricator. Looking through production records, they determined that the circuits were sanded to reduce the profile of the button plated vias, but the resist layer used to expose the vias for plating had been removed prior to sanding. This resist layer could be thought of as a buffer to protect the remaining outer layer copper from the sanding process. Effectively, some of the copper on the wire bond pads (as well as some traces) was sanded away. The wire bond and surface mount component pads exhibited evidence of this sanding, showing scratches.
  + By comparison with the Prototype circuits, we determined that a minimum copper thickness that we expect to result in acceptable wire bond pull strengths. We will include this requirement in the specification for production circuits. The fabricator has demonstrated in the second batch of Rev. C circuits that they are capable of meeting this requirement.

Issues found in the second delivery of Rev. C circuits:

All Revision C circuits were fabricated using the same gerber data. As previously mentioned, the circuit vendor agreed to process the three panels of circuits in the second delivery differently to allow the FPix collaboration the opportunity to determine a circuit lay-up that provided both high-voltage breakdown protection and circuits that could exhibit acceptable wire bondability. To facilitate this process, we agreed to accept all circuits, good and bad. Inspection of the circuits determined that we could specify circuits that would meet both the high voltage and wire bond requirements. The same inspection process also revealed features that suggested lack of attention during the fabrication process, though if we were to have received only good circuits it’s not clear that we would have made these observations:

* The widths of exposed wire bond pads were significantly less (20%) than expected. We suspect, but did not verify through the upper layer solder mask, that the traces were narrower as well.
  + We suspect that the gerber data (for at least the upper copper layer) was not properly compensated to account for feature narrowing during the copper etching process. We presented data indicating the narrow pads and our speculation to the vendor. They concurred with our hypothesis and will take steps in the Production order to ensure it doesn’t recur. We have also included this requirement in our HDI Circuit Specification document.
* Circuits from one of the three panels were routed incorrectly. The circuit outline of the HDI is not symmetric. The circuits exhibited evidence that there were two routing passes with the outline rotated 180° between the two. This resulted in a corner of the circuit nearly removed.
  + This type of issue is clearly not acceptable and would be rejected for replacement on inspection. We shared this observation and assertion with the vendor who agreed completely.
* There were examples of mis-registration of the upper layer solder mask with respect to upper copper layer features. We had worked with the vendor to increase the upper layer solder mask openings to compensate for expected mis-registration in the Rev. C gerber data so were surprised to make this observation.
  + While the assembly of surface mount components to the HDI is not so sensitive to this issue, partial covering of a wire bond pad is not acceptable and would be rejected for replacement on inspection. We shared this observation and assertion with the vendor who agreed completely.
* Visual inspection revealed one circuit that had an apparent short between adjacent Read Out Chip wire bond pads. Using a probe station, measurements with an ohmmeter verified the presence of a short. In and of itself, this is not remarkable. That the circuit was stamped as electrically good is bothersome. All HDIs that we’ve received have been electrically tested prior to delivery. This is the only example we’ve seen with this issue in any delivery of HDIs so far received.
  + This observation was shared with the circuit vendor. They have been sub-contracting their circuit testing to an outside firm. This process will be performed in-house for subsequent fabrications.
  + Visual inspection will be performed on all HDIs as they are received. A subset will undergo electrical testing performed by FPix collaborators. Circuits that look suspicious will be subject to greater scrutiny. Circuits that do not pass our inspection will be returned to the circuit fabricator for replacement. The vendor has agreed to this proposal.
* Visual inspection reveals a number of circuits that exhibited vias breaking out of (not wholly enclosed by) their upper layer pads.
  + This is a clear violation of IPC standards. We suspect that the only reason that we found circuits with this feature is that we agreed to accept all circuits.
  + Circuits that do not meet IPC standards will be returned to the fabricator for replacement.

**Additional information:**

HDI Revision C1 schematics are available as document 12341 in the cms docdb. Note that component (capacitor and resistor) values are not finalized and thus not indicated in the schematic.

Design change history

Prototype to Rev.C:

* A surface mount DIP switch used to set the address of the TBM was removed to reduce mass and replaced with an array of wire bond pads. Change the address by removing wire bonds.
* Added 24 “bed of nails” type probe points for verifying operation of TBM while operating.
* Added 4 fiducials used by visual recognition equipment used in the module assembly process.
* Added a location that can be used to place wire bonds. These bonds can be used to optimize semi-automatic wire bonder settings.
* Devices were moved to realize space for vacuum chucks used in the module assembly process.
* Added a grounded wire bond pad that could be used to make contact to the sensor guard ring if deemed necessary in the future.
* Minimized the number of resistors in the sensor bias voltage network.
* Increased size of upper layer solder mask openings to accommodate expected location tolerances.
* Increased the size of TBM wire bond pads.
* Provided space for serial number information in the silk screen. The vendor uniquely identifies each circuit by run, panel number in the run, and circuit location in the panel. This information is used to track the HDI through testing and assembly.

First Rev. C delivery to the second:

* Requested thicker copper on upper layer.
* Asked for thicker nickel layer on wire bond pads. The nickel thickness on the pads of the first delivery met IPC requirements for pads used for aluminum wedge bonds. CERN colleagues recommended making this request.
* Request different bottom layer treatment for each of the three panels in process.
  + Bottom layer polyimide cover coat over bottom layer copper.
  + Bottom layer flexible solder mask over bottom layer copper, polyimide cover coat over solder mask. Circuits routed from panel before application of cover coat.
  + Bottom layer flexible solder mask over bottom layer copper, polyimide cover coat over solder mask. Circuits routed from panel after application of cover coat.
* Use thicker polyimide cover coat for all three panels.