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**PPD / EED / Infrastructure and Support Group**

Technical Note: IG\_ 20160002

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**INFN RPix Flexible Printed Circuit**

**Design Review**

**Overview:**

A review of the RPix Flexible Printed Circuit was requested 26-Jan-2016. Documentation supplied with the request consisted of a schematic diagram, gerber data and various Excel workbooks.

The RPIx Flexible Printed Circuit utilizes 6 CMS PSI46dig Read Out Chips and one TBM08c Token Bit Manager to provide communication and control for the Read Out Chips. The RPix Flexible Printed Circuit appears to be a 4-layer copper / polyimide circuit.

The electrical safety aspects of the design of the RPix Flexible Printed Circuit were evaluated using “Electrical Design Standards for Electronics to be used in Experimental Apparatus at Fermilab” (Fermilab ESH&Q docdb document #[2781](https://esh-docdb.fnal.gov:440/cgi-bin/RetrieveFile?docid=2781&filename=FNAL_Electrical_Design_Standard_7.2.pdf&version=5)) and generally accepted practices for electrical utilization equipment as described in the National Electrical Code.

A functional review of the design utilized the datasheets was performed. The gerber data was also examined. Consistency in connections to / from the Flexible Printed Circuit was examined in an attempt to discover missing connections. Where such data was available, the proper layout / orientation of components on the printed circuit board was also investigated.

**Scope of the Review:**

Notes made during this review were entered into the Observations section of this Findings Report as the review progressed. Areas that require additional attention are noted in the Recommendations section. The Recommendations section is listed early in this review to make it easy to find. Entries in the Observations section serve as an accurate history of the progress of the review and are used to illustrate which aspects of the design were examined. They should not necessarily be construed to illuminate areas of concern. Entries found in the Recommendations section will necessarily have corresponding entries, with additional detail, in the Observations section. The opposite in not necessarily true. Entries in the Observations section that provide additional details for entries in the Recommendations section are highlighted in red.

**Recommendations:**

* Consider increasing the called out thickness for the Inner1 copper layer to 18µm to yield a balanced construction.
* Consider means to reduce the overall thickness of the circuit to maximize the likelihood of realizing reliable wire bonds.
* Consider modifying the layer stack up for the vias used in the design. The current openings may be too small to be counted on to allow vias to be probed for diagnostic purposes. Exposed copper in the region of surface mount soldered components is at a greater risk of contamination and unwanted electrical connections if adequate post-soldering cleaning is not performed.
* Based on IPC-2221 guidelines, the detector bias voltage should not exceed 740V.
* Consider removing the upper silk screen features that enclosed TBM wire bond pads.
* Consider removing the upper silk screen features that enclose Read Out Chip wire bond pads.
* Consider modifying the trace widths for the TBM\_OUT\_A(+/-) nets on the upper and third copper layers to realize more uniform characteristic impedance. Changes in the dielectric thickness will modify impedance values.
* Consider methods to reduce the impedance and / or the effect of the impedance of the bottom copper layer VD+ trace. Increasing the cross sectional area of the trace by making it wider would help reduce the impedance. Locating an additional bypass capacitor from VD+ to ground near the TBM end of the circuit may provide some mitigation of the effect of the impedance. Note that this capacitor may or may not be needed once the circuit it put in operation, but having the footprint available but not necessary is better than the reverse.
* Add individual vias to the bottom layer copper pour for the VD+ net found on Samtec connector (J1) for pins 15 and 17 to reduce the effects of via impedance. Consider adding redundant vias for each VD+ pin on the Samtec connector.
* Add a connection to the VD+ net for pin 11 of each Read Out Chip.
* Add an individual via to the bottom layer copper pour for the VA+ net found on Samtec connector (J1) for pin 13. Consider adding redundant vias for both VA+ pins on the Samtec connector.
* Consider methods to reduce the impedance and / or the effect of the impedance of the bottom copper layer VA+ trace. Increasing the cross sectional area of the trace by making it wider would help reduce the impedance. Locating an additional bypass capacitor from VA+ to ground near the TBM end of the circuit may provide some mitigation of the effect of the impedance. Note that this capacitor may or may not be needed once the circuit it put in operation, but having the footprint available but not necessary is better than the reverse.
* Consider relocating capacitors C10, C12, C13, C14 and C15, or increasing the width, to reduce the impedance of the traces to them.
* Consider modifying the trace widths for the SD\_IN\_0(+/-) nets on the third and bottom copper layers to realize more uniform characteristic impedance. Changes in the dielectric thickness will modify impedance values.
* Consider reducing the length of the connections from the serial data outputs of ROC1 to the SD\_IN\_0(+/-) nets to maximize signal fidelity of these nets.
* Consider modifying the trace widths for the SD\_IN\_2(+/-) nets on the third and bottom copper layers to realize more uniform characteristic impedance. Changes in the dielectric thickness will modify impedance values.
* Consider examining at least the Clk\_0(+/-), Clk\_1(+/-), Clk\_2(+/-) and Clk\_3(+/-) nets for excess length, stubs and non-uniform trace impedance.
* Correct the inconsistency between the schematic and the layout for connections to / from the RTD.

**Observations:**

 Circuit Construction:

Based on the Cross Section.xlsx spreadsheet the layer stack up is assumed to be; upper copper, ground plane copper, Inner1 copper, bottom copper. The copper thicknesses indicated in the spreadsheet are 10µm for all but the ground plane layer which is indicated to be 18µm.

* In general, balanced construction is preferred for printed circuit fabrication, particularly for flexible printed circuits where one attempts to place the neutral bend axis in the middle of the circuit.

Three polyimide layers are shown in the spreadsheet, the center one is indicated to be 150µm while the outer two are indicated to be 50µm. No specific indication of the adhesive layers used to hold the circuit together are indicated. For trace impedance calculations the thickness of the adhesive layers are assumed to be included in the thickness listed for the polyimide layers.

* The ability to create reliable ultrasonic aluminum wedge wire bonds to flexible printed circuits is inversely related to the thickness of the circuit. Summing the known thicknesses this circuit appear to be at least 300µm thick, not including the additional thickness of upper and lower solder masks or cover coats which are not listed. It is assumed that the polyimide thicknesses were chosen in an attempt to control trace impedance on the Inner1 and bottom copper layers.

Vias:

Small openings in the upper and lower solder mask layers are present for all vias. The openings are not as large as the via capture pad and may not be always open sufficiently for probing, if that was the intent.

Samtec Connector:

Connections on / off the flexible printed circuit are found on a 50-pin surface mount Samtec QSS-025-RA connector (J1). Eight additional contacts are found under the connector body. These contacts require through hole pads and are used to connect the reference planes in the connector to the ground net on circuit.

* No attempt was made to verify the connections on the connector, this will be the responsibility of a review of the cable / mating connector.
* The footprint found in the upper copper layer gerber data is consistent with the recommendations made by the manufacturer.

Detector Bias Voltage:

Four contacts on the Samtec connector are shown to be associated with detector high voltage. As a common net, they are connected to one side of resistor R5. The other side of R5 is shown connected to two bias pads. IPC-2221 guidelines suggest minimum spacing for conductors on a common layer as a function of difference in potential. The routing of the bias voltage nets will be examined on all layers on which they are found. The minimum spacing between the bias voltage net(s) and adjacent copper (assumed to be at ground potential) will be listed, along with the suggested IPC voltage associated with that distance.

* The Samtec connector is found on the upper copper layer. Two contacts on either side of the 2 row by 25 contact connector are routed to a via. Contacts immediately adjacent to the bias voltage contacts are left un-connected. This practice is consistent with that taken by the design of the US CMS Forward Pixel HDI. The surface mount series resistor is found on the upper copper layer. After routing on lower layers, the two bias voltage pads are also located on the upper copper layer.
	+ The minimum distance, found between the HV\_R net and a via associated with the TBM\_RDa\_Out- net near the Samtec connector, is 0.858mm. This distance is consistent with an IPC-2221 recommendation for 740V.
* The two vias are connected to a single copper pour found on the bottom copper layer. This copper pour is also connected to a via that is connected to the series resistor on the upper copper layer. The other side of the series resistor is connected to a via that’s connected to another copper pour on the bottom copper layer. That copper pour routes the bias voltage to 4 vias.
	+ The minimum distance, found between either of the copper pours and adjacent copper, is 1mm. This distance is consistent with an IPC-2221 recommendation for 800V.
* The four vias are connected to a long copper pour on the Inner 1 copper layer. This copper pour delivers the bias voltage to vias associated with the bias pads in the region that the detector will be located.
	+ The minimum distance, found between the copper pour and adjacent copper, is 1mm. . This distance is consistent with an IPC-2221 recommendation for 800V.

TBM:

The symbol for the TBM found in the schematic is consistent with documentation found for the TBM08c. The wire bond footprint and orientation found in the upper copper layer gerber data is consistent with the layout of the bare die pads.

* An upper layer pad connected to the ground net is located underneath the TBM08c, but not exposed through the upper layer solder mask.
	+ The bottom side of the TBM08c is not believed to be conductive so the opening in the solder mask is not believed to be required.
* The upper silk screen gerber data indicates a box surrounding the TBM wire bond pads. This feature is within the upper solder mask opening for these pads. There is concern that the solder mask, or mis-registration of the solder mask, may contaminate the wire bond pads to the extent that reliable wire bonds are not possible.
* The high-speed output data pair from the TBM transfer data at rates up to 400Mb/s. These nets are the most sensitive to bandwidth requirements and thus warrant attention.
	+ TBM08c documentation indicates that these nets should be terminated with external 37Ω resistors to ground at their destination. We’ve interpreted this information to design the long cable that connects the Forward Pixel HDI to downstream electronics to exhibit single-ended trace characteristic impedance of about 37Ω as well.
	+ The high-speed output pair from the TBM08c in this design is found primarily on the upper copper layer. The traces on this layer are 0.160mm wide and approximately 175mm long.
	+ Third copper layer traces transition these nets to vias located immediately adjacent to the Samtec connector. These traces are 0.333mm wide and approximately 25mm long.
		- Using data from the provided spreadsheet, the characteristic impedance of the upper copper layer traces, located directly above the ground plane, can be estimated to be about 28Ω.
		- Using data from the provided spreadsheet, the characteristic impedance of the third copper layer traces, located directly below the ground plane, can be estimated to be about 41Ω.
			* Ideally these two values would be the same and approximately 37Ω.
* Power for the TBM08c consists of 4 wire bond connections to the VD+ net. The VD+ net originates with 6 connections to the 50-contact Samtec connector. A wide (~5mm) copper pour runs the length of the circuit, approximately 250mm to deliver power to the TBM as well as the Read Out Chips. The anticipated thickness of the bottom layer copper is 10µm, yielding a connection with a cross-sectional area of 0.05mm2.
	+ The length of the copper pour to the TBM is approximately 200mm. The resistance of this connection is estimated to be 68mΩ. The inductance of this connection is estimated to be about 250nH.
		- The impedance of this trace at various frequencies can be estimated to be;
			* 15Ω at 10MHz.
			* 150Ω at 10MHz.
		- This estimate does not include the impedance of the cable connected to the Samtec connector. A bypass capacitor for the VD+ net to ground is show in the schematic and found near the Samtec connector on the circuit. TBM08c documentation suggests none of the capacitors associated with the device actually are connected to the VD+ net.
		- Three of the Samtec connector connections share a common via connection to the copper pour on the bottom layer. The impedance of this single via is a hindrance to good power connections.

Read Out Chip:

The symbol for the PSI46 Read Out Chip found in the schematic is consistent with documentation found for the PSI46dig. The wire bond footprint and orientation found in the upper copper layer gerber data is consistent with the layout of the bare die pads.

* Two power connections are required for each Read Out Chip; VA+ (power for analog operations) and VD+ (power for digital operations).
	+ Members of the Barrel Pixel Detector Group noted that the operation of the PSI46dig Read Out Chip was enhanced by making an explicit connection of the Cap\_VD+ input to the VD+ net as well as the bypass capacitor. It’s not clear that this change in connection was ever reflected in subsequent documentation, but acting on the recommendation of our colleagues the Forward Pixel Detector Group implemented this change on the most recent version of their HDI.
	+ The VA+ net originates with two connections to the Samtec connector. A single via connects to a small copper pour on the bottom copper layer which then transitions to a wide trace on the third copper layer. Multiple vias are used to make this layer to layer transition. The VA+ trace is approximately 8.2mm wide and 135mm before it narrows for distribution to the Read Out Chips. The copper thickness of this layer is listed to be 10um yielding a cross sectional area of 0.082mm2.
		- The estimated resistance of this trace is estimated to be 28mΩ. The inductance of this trace is estimated to be 50nH.
			* The impedance of this trace at various frequencies can be estimated to be;
				+ 3Ω at 10MHz.
				+ 30Ω at 100MHz.
			* This estimate does not include the impedance of the cable connected to the Samtec connector. A bypass capacitor for the VA+ net to ground is show in the schematic and found near the Samtec connector on the circuit.
			* This trace is located directly below the solid ground plane on the second copper layer so form an integrated bypass capacitor.
	+ Each Read Out Chip requires 3 ancillary capacitors. One is a local bypass for the VD+ net, the other two bypass internal nets. The functionality of capacitors depends on the connections to / from the devices. Increasing inductance, and to a lesser extent the resistance, of the traces degrades the intended performance. In general, the closer a capacitor is to the Read Out Chip it’s associated with the better, wider traces better than narrow.
		- Most of the Read Out Chip capacitors are located reasonably close to their associated Read Out Chips. Capacitors C10, C12, C13, C14 and C15 are the outliers and might benefit from some relocating.
* The chip address bits on the six Read Out Chips are as follows:
	+ ROC0: 0000
	+ ROC1: 0001
	+ ROC2: 0010
	+ ROC3: 0011
	+ ROC4: 0100
	+ ROC5: 0101
* The token paths from and back to the TBM are as follows:
	+ The token pair from TBM port 0 is routed to ROC0. In the event that ROC0 is not passing the token, resistors R10 and R11 can be installed to bypass the token to ROC1.
	+ The token output from ROC0 is routed to ROC1. In the event that ROC 1 is not passing the token, resistor R6 and R7can be installed to bypass the token to ROC2.
	+ The token output from ROC1 is routed to ROC2. In the event that ROC2 is not passing the token, resistors R8 and R9 can be installed to bypass the token back to the TBM port 1 input.
	+ The token output from ROC2 is routed to the TBM port 1 input.
	+ The token pair from TBM port 2 is routed to ROC3. In the event that ROC3 is not passing the token, resistors R16 and R17 can be installed to bypass the token to ROC4.
	+ The token output from ROC3 is routed to ROC4. In the event that ROC4 is not passing the token, resistors R12 and R13 can be installed to bypass the token to ROC5.
	+ The token output from ROC4 is routed to ROC5. In the event that ROC5 is not passing the token, resistor R14 and R15 can be installed to bypass the token to the TBM port 3 input.
	+ The token output from ROC5 is routed to the TBM port 3 input.
* The upper silk screen gerber data indicates a box surrounding the Read Out Chip wire bond pads. This feature is within the upper solder mask opening for these pads. There is concern that the solder mask, or mis-registration of the solder mask, may contaminate the wire bond pads to the extent that reliable wire bonds are not possible.
* ROC0 and ROC1 receive their clock, trigger and serial data from port 0 on the TBM08c. They return their serial data to port 0.
* ROC2 receives it’s clock, trigger and serial data from port 1 on the TBM08c. It returns it’s serial data to port 1.
* ROC3 and ROC4 receive their clock, trigger and serial data from port 2 on the TBM08c. They return their serial data to port 2.
* ROC5 receives it’s clock, trigger and serial data from port 3 on the TBM08c. It returns it’s serial data to port 3.
* In general, these traces are routed on three different copper layers with different trace widths resulting in some concerns about impedance mismatches. Of these signals, the serial data from the Read Out Chips back to the TBM08c have the greatest bandwidth requirement and thus are the most sensitive to trace characteristic impedance. It’s tempting to look at the clock, control and data signals associated with the Read Out Chips and TBM08c and assume that they are differential. As we have built circuits and cables to allow communication to / from the TBM both from on the circuit and off, we have been advised to treat these pairs of signals as two single-ended signals that are operating 180° out of phase. When trace characteristic impedance is deemed important, we’ve been advised to aim for 37Ω.
	+ Each serial data input on the TBM has an internal 37 Ohm resistor to ground.
* The data rate on the traces from the Read Out Chip(s) to the TBM is 160Mb/s. This corresponds to a bit changing every 6.25ns. Assuming that a 2ns rise /fall time is sufficient to resolve individual bits we can estimated the required trace bandwidth by BW ≈ 0.34 / tr = 170MHz. This is the highest frequency component we would be interested in and will be used to establish the critical length of traces between Read Out Chips and the TBM08c. A generally held rule of thumb states that if a trace is longer than one 20th or one 40th (depending on how conservative one wants to be) of the wavelength associated with the highest frequency component the impedance characteristics of the trace need to be considered. We assume that the speed of propagation in flexible printed circuits is about 0.6c so the wavelength for a 170MHz sin wave is about 1m. In this case, λ/20 = 53mm and λ/40 = 26mm. If 1ns rise / fall times are required, the critical lengths become 26mm and 13mm respectively.
* There are 4 high-speed data signal pairs from the 6 Read Out Chips back to the TBM08c. They will be examined independently.

SD\_IN\_0(+/-):

The serial data pair to TBM port 0 originates from wire bond pads 6 and 7 on ROC0. The upper copper layer traces from the wire bond pads to vias are short and deemed inconsequential in terms of estimating characteristic impedance.

These vias connect to a pair of traces found on the third copper layer. These 0.333mm wide traces are about 34mm in length. These traces terminate in vias and transition to traces on the bottom copper layer. These 0.6mm wide traces are about 72mm in length. These traces terminate in vias that transition to the upper copper layer and short traces to the wire bond pads for the TBM.

* Using data from the provided spreadsheet, the characteristic impedance of the third copper layer traces, located directly below the ground plane, can be estimated to be about 41Ω.
* Using data from the provided spreadsheet, the characteristic impedance of the bottom layer traces, using the ground plane as the reference, can be estimated to be about 31Ω.
	+ Ideally these two values would be the same and approximately 37Ω.

The serial data pair from ROC1 are also connected to this net. This arrangement necessitates a stub of some length. For this design, the stub appears as a pair of 15mm long traces from wire bond pads for ROC1 to the vias that allow the nets to transition from the third copper layer to the bottom. In reality, these traces are combinations of two different widths, narrower near the Read Out Chip then expanding a short distance away. For simplicity we will use only the wide, 160µm wide trace for impedance estimation.

* Using data from the provided spreadsheet, the characteristic impedance of the upper copper layer traces, located directly above the ground plane, can be estimated to be about 28Ω.
	+ The introduction of a relatively long stub will likely have a detrimental effect on the quality of the net(s) irrespective of the characteristic impedance of the traces that make up the stub.

SD\_IN\_1(+/-):

The serial data pair to TBM port 1 originates from wire bond pads 6 and 7 on ROC2. The upper copper layer traces from the wire bond pads to vias are approximately 10mm long.

* Using data from the provided spreadsheet, the characteristic impedance of the upper copper layer traces, located directly above the ground plane, can be estimated to be about 28Ω.

These vias are connected to bottom layer traces. These 0.6mm wide are approximately 16mm long and terminate into vias.

* Using data from the provided spreadsheet, the characteristic impedance of the bottom layer traces, using the ground plane as the reference, can be estimated to be about 31Ω.

These vias are connected to upper copper layer traces. These traces are short and are deemed inconsequential in terms of estimating characteristic impedance.

* The length of these traces and lack of stubs do not warrant any special recommendations.

SD\_IN\_2(+/-):

The serial data pair to TBM port 2 originates from wire bond pads 6 and 7 on ROC4. The upper copper layer traces from the wire bond pads to vias are short and deemed inconsequential in terms of estimating characteristic impedance.

These vias connect to a pair of traces found on the bottom copper layer. These 0.6mm wide traces are about 10mm in length. These traces terminate in vias that transition to the third copper layer.

The third copper layer traces are 0.333mm wide and approximately 30mm long and terminate at vias that transition to bottom layer traces.

The bottom layer traces are approximately 6mm long and transition the nets to the upper copper layer where very short traces connect to TBM08c wire bond pads

* Using data from the provided spreadsheet, the characteristic impedance of the bottom layer traces, using the ground plane as the reference, can be estimated to be about 31Ω.
* Using data from the provided spreadsheet, the characteristic impedance of the third copper layer traces, located directly below the ground plane, can be estimated to be about 41Ω.
	+ Ideally these two values would be the same and approximately 37Ω.

The serial data pair from ROC3 are also connected to this net. This arrangement necessitates a stub of some length. For this design, the stub appears as a pair of short traces from wire bond pads for ROC3 to the vias that allow the nets to transition from the third copper layer to the bottom. The length of these traces is judged to be inconsequential in terms of estimating characteristic impedance.

SD\_IN\_3(+/-):

The serial data pair to TBM port 3 originates from wire bond pads 6 and 7 on ROC5. The upper copper layer traces from the wire bond pads to vias are approximately 10mm long.

These vias transition the nets to 0.333mm wide traces on the third copper layer. These traces are approximately 74mm long and terminate into vias that transitions the nets back to the upper copper layer where short traces make the connections to TBM08c wire bond pads.

* Using data from the provided spreadsheet, the characteristic impedance of the third copper layer traces, located directly below the ground plane, can be estimated to be about 41Ω.
* The remaining Read Out Chip input nets were cursorily examined. Wire bond pads for these Read Chip Pads, and their corresponding pads for the TBM08c, are all on the upper copper layer. In general these pads are connected to upper copper layer traces that transition the nets to the third copper layer or the bottom copper layer, or combinations of the two in establishing the connections between chips. These signals have less bandwidth requirements than the serial data nets from the Read Out Chips and thus are a bit more tolerant of trace lengths and impedance mismatches. Nonetheless, routing and impedance matching investigations for at least the Clk\_0(+/-), Clk\_1(+/-), Clk\_2(+/-) and Clk\_3(+/-) nets might be helpful.

RTD:

A provision for a temperature sensing device is indicated in the schematic. Two connections are shown, from pins 44 and 46 of the Samtec connector to either side of a device indicated to be a 10k RTD.

* The layout of the circuit does not match what’s indicated in the schematic. Four traces are found connecting the Samtec connector to the RTD, pins 44 and 46 to one side, pins 48 and 50 to the other. The lack of agreement between the schematic and the layout indicates a possible breach in the integrity of the design. If this inconsistency had been found near the beginning of the review it would have been halted immediately. That it was found this late is still worrisome, but probably not an indication of disaster.

**Gerber Data:**

Gerber data (7 files dated 01/26/2016 2:37PM) was imported into GerbTool, a gerber data viewer, for inspection. The format of the files is RS274X, 2,5, absolute, leading, ASCII, metric. The files include upper, inner and lower copper layers, upper and lower solder mask layers and an upper layer silk screen. NC Drill data was also imported into GerbTool. Format for the file is Excellon, 2,5, absolute, none, metric, ASCII, plated.

The four copper layers can be described as follows:

* The upper copper layer contains all surface mount and bare die attach components. Surface mount solder and wire bond pads are located on this layer. Traces are located on this layer.
* The second layer is a circuit wide copper pour, solid except for relief around vias not associated with the Ground net.
* The third layer contains wide power and detector bias traces and signal traces.
* The bottom copper layer contains a wide power trace, some copper pours and signal traces.

Inspection of the upper solder mask revealed nothing more that the partially covered vias.

Inspection of the lower solder mask revealed nothing more that the partially covered vias.

A DRC inspection was run in GerbTool for the 4 copper layers. The results of this inspection are listed below:

* The minimum distance between unrelated copper is;
	+ 75µm for the upper copper layer
	+ 150µm for the second copper layer
	+ 90µm for the third copper layer
	+ 100µm for the bottom copper layer
* The minimum trace width for the top layer is 95µm, for all others it’s 100µm.