

# RTF User's Manual

Donna Kubik

July 21, 2000

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## 1 Introduction to the RTF module

The RTF (Receive Trigger Filter) module provides an interface between the ZIP (Z-sensitive Ionization and Phonon) module and the DAQ (Data AcQuisition) system. The RTF module's multifunctionality is reflected in its name.

## 2 Receive

Six signals are received from the ZIP module; four phonon signals and two charge signals. Each of these signals is received differentially, via a 25 pin "D" connector located at the rear of the module, by an INA103K instrumentation amplifier.

The amplifier receives differential signals from the backplane, via the 25 pin connector, and converts them to a single ended signals referenced to analog ground as shown in FIG. 2.1.

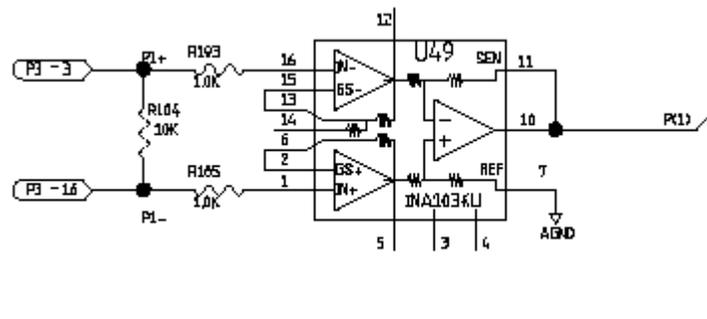


FIG. 2.1 Circuit used by the RTF module to receive the input signal from the ZIP module

These signals include QI, QO, and P1-P4. The purpose of this circuit is to eliminate voltage differences between input signal grounds and output signal grounds, as well as provide a low output impedance.

The INA103 amplifier's input range is  $\pm 11V$ . This will easily accommodate the expected  $\leq 4V$  input from the ZIP. This expected range is a result of two things. The digitizers in the data acquisition system have a range of  $\pm 2V$ , resulting in a full range of 4V. However, there is an auto zeroing circuit on the ZIP module, prior to the driver. During tuning the SQUID offset is adjusted. The auto zeroing eases the detector tuning procedure by eliminating the need to constantly compensate for an adjustment of the SQUID offset by manually changing the driver offset. The bipolar range of the digitizers will be matched by applying an offset to the signal on the RTF module (see section 4.1), prior to digitization.

The resistors across the input to each INA103 differential amplifier are selected to match the impedance of the input cable.

Certain source impedances can cause the INA103 to oscillate. This depends on circuit layout and source or cable characteristics connected to the input. The 1.0K

resistor in series with the positive and negative inputs of the differential amplifier are used to reduce the tendency to oscillate.

The outputs of the INA103Ks are bussed to both the *Summer and Trigger* and the *500 kHz / 5 MHz Filter* circuits.

### 3 Trigger

Each of the signals from the INA103Ks also goes to the Summer and Trigger circuits which produce additional signals for the charge information and for phonon information (P LO Filter, P LO Trigger, P HI Filter, and P HI Trigger).

Either or both of the charge signals may be added via a summing amplifier circuit to form the charge sum, and any number of the four phonon signals may be added to form the phonon sum.

The summed signals are filtered by both high pass and low pass filters and are sent through a buffer to front panel connectors (Q LO filter, Q HI filter, P LO filter, P HI filter). The output of the filter is also sent to a discriminator, where it is compared to an adjustable threshold set by a DAC on the RTF board. The output of the discriminator drives a 22ms oneshot, the output of which is referred to as the trigger. This output is available via front panel connectors (Q LO trigger, Q HI trigger, P LO trigger, P HI trigger). The trigger is also output to the DAQ via connector P1. The state of each trigger is also indicated by an LED on the front panel. The threshold voltages are buffered and are also available for viewing via a front panel connectors (Q LO threshold, Q HI threshold, P LO threshold, P HI threshold).

#### 3.1 Summer

The charge summing circuit and its inputs are shown in FIG. 3.1. The phonon summing circuit and its inputs are shown in FIG. 3.2.

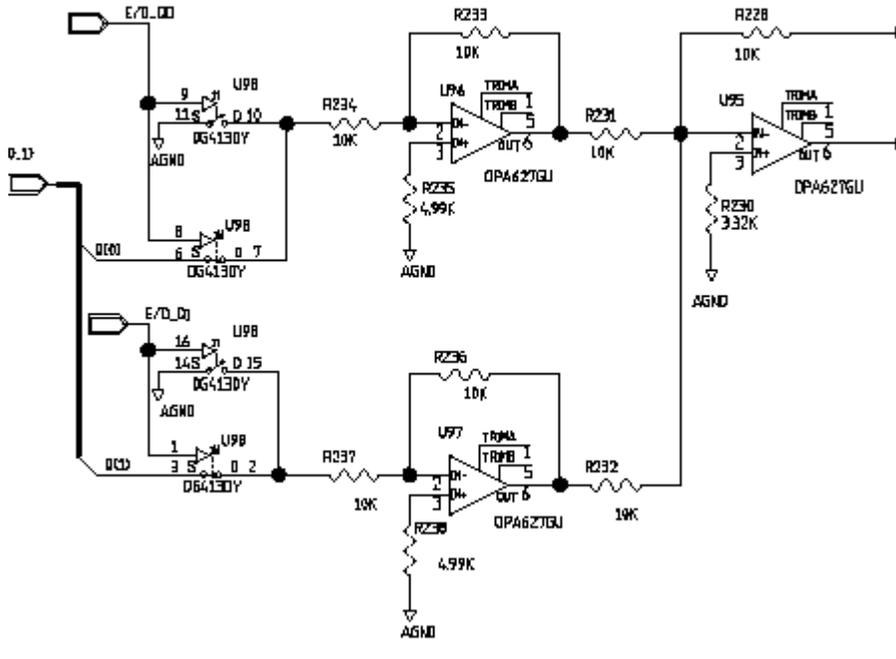


FIG. 3.1 Summing circuit for the charge signals showing the input selection switches, input buffer, and summing amplifier circuit

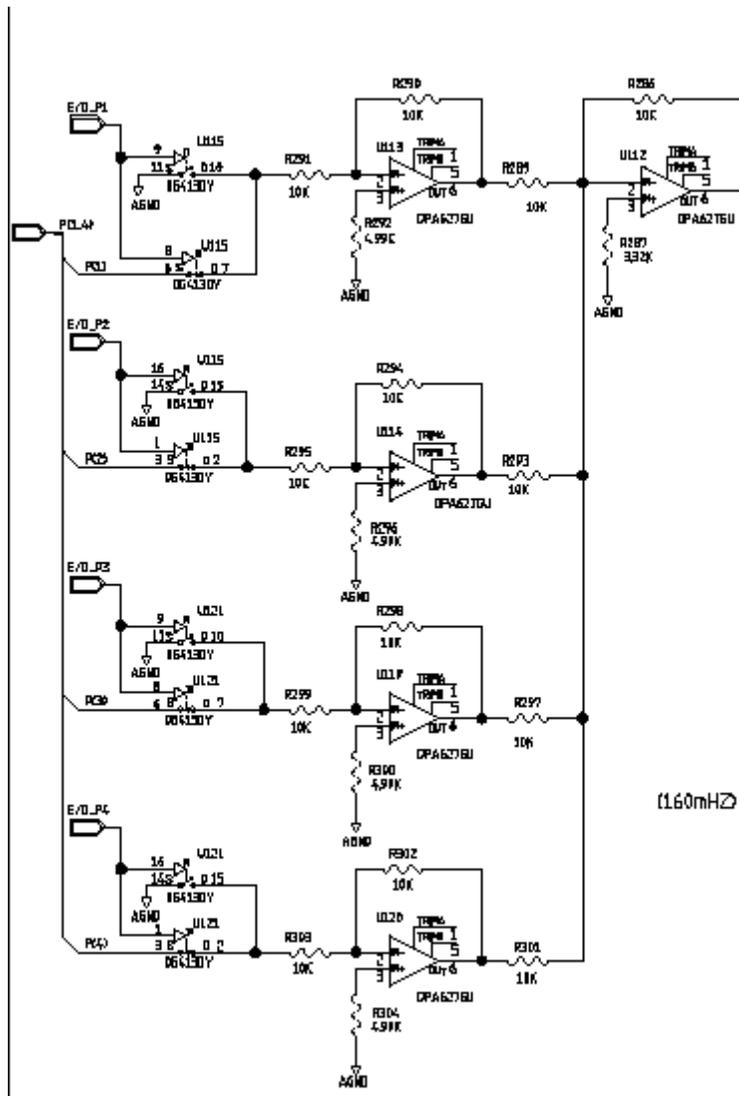


FIG. 3.2 Summing circuit for the phonon signals showing the input selection switches, input buffer, and summing amplifier circuit

The channels input to the summers are selected via DG130 SPST analog switches. If the signal is to be part of the sum, it passes to the summing amplifier circuit via an input buffer. If it is not selected to be part of the sum, it is shunted to ground. This is shown in FIG. 3.1 and 3.2.

Each signal to be summed then passes through an OPA627GU unity gain inverting amplifier. Since the output of a summing amplifier is an inverted sum of the voltages applied to the input of the amplifier, by first inverting the signal with the OPA627's, the output from the summing amp will be of the same polarity as the signal input from the ZIP module.

The series and feedback resistors,  $R_s$  and  $R_f$ , respectively, and the resistor-to-ground in combination with the input capacitance of these OPA627's (10pF) and parasitic capacitance from board layout (~10pF) form "parasitic" filters. It is desirable to make the  $f_{3dB}$  of these parasitic filters much higher than the  $f_{3dB}$  of the OPA627 to avoid phase shifts of 45 deg or greater (with respect to the input) which can result in undesirable oscillations. The lower these resistances are, the higher  $f_{3dB}$  of the resultant (parasitic) filters will be and the farther away it will be from the  $f_{3dB}$  of the input signal.  $R_f$  and  $R_s$  are  $1k\Omega$  and the resistor to ground is  $499\Omega$ .

The  $1k\Omega$   $R_f$  and  $R_s$  and the  $3.32k\Omega$  resistor to ground for the OPA627 summing amp circuits were similarly chosen to be low.

An additional consideration is that of errors that can result due to input bias currents. The inverting amplifier will produce a non-zero output voltage when its input terminal is connected to ground. This is because the input bias current,  $I_B$ , produces a voltage drop across the resistors, which is then amplified by the circuit's voltage gain. The inverting input of these two OPA627 inverting amp configurations (unity gain inverting amplifiers and the summers) sees an impedance of  $R_s \parallel R_f$ , so the bias current produces a

voltage  $V_{in} = I_B (R_s \parallel R_f)$ , which is then amplified by the gain at dc,  $-\frac{R_f}{R_s}$ .

One solution to minimize this error is to ensure that both inputs see the same dc impedance. It is also a good idea to keep the resistance of the feedback network small enough so that the bias current doesn't produce large offsets.

In the case of the unity gain inverting amplifiers, the input bias current resistors (R235, R238, R292, R296, R300, R304) are  $499\Omega$ , which is equal to  $R_s \parallel R_f$ .

In the case of the summing circuits, the input bias current resistor for the charge circuit, R230, should be equal to the equivalent resistance of three  $1k\Omega$  resistors in parallel (R228, R231, R232), which equals  $333\Omega$ . The input bias current resistor for the phonon circuit, R287, should be equal to the equivalent resistance of five  $1k\Omega$  resistors in parallel (R286, R289, R293, R297, R301), which equals  $200\Omega$ . It should be noted that these are not in fact the values of these input bias current resistors, likely due to oversights during circuit revisions. Although this is not ideal, it probably doesn't cause obvious problems due to the fact that these circuits are followed by the capacitors of the high pass filters (C59, C64, C69, C74) which serve to block the dc voltage created by the input bias current.

## 3.2 Filters

The signals from the summers are used to generate a trigger.

First the signals are filtered. The purpose of filters is to create a single pole, bandpass filter, comprised of a high pass and low pass filter, which will attenuate all frequencies except those contained in the rising edge of the detector pulse. This filtering will thereby increase the usable trigger sensitivity for the next stage, which is called the trigger comparator.

The outputs from both the charge and phonon summing circuits are split to form a HI and LO trigger, where HI and LO refer to the expected amplitude of the input signal. Since the amplitude is unknown, the input signal from the detector is fed into both the HI and LO circuits which will generate a Q HI and a Q LO trigger and a P HI and P LO trigger, for the charge and phonon circuits, respectively.

The P HI and Q HI channels are designed for large signals. The high pass filters are necessary to remove any DC offset from the front end. In this case noise is not as big a problem and the low pass filters do not limit the bandwidth as much as they do for the P LO and Q LO channels. The P HI and Q HI channels have a gain of 0.5.

The P LO and Q LO channel, the signals are assumed to be smaller, hence require amplification ( $\sim 100x$ ). Again, the high pass filter removes any DC offset from the front end. The combination of the high pass and low pass filters admit only frequencies in the rising edge of the pulse, minimizing the bandwidth, and hence, minimizing noise in these lower-amplitude signals. There is no need to preserve the trigger shape of the pulse, for once an event is identified as a good one to look at, one can go back in time, offline, and examine the corresponding event output from the 500 kHz and/or 5 MHz filter circuit, which carefully preserved the pulse shape.

Via the configuration of the inputs to the DAQ, the experimenters many choose to trigger only on the trigger output from the HI circuits, only from the LO circuit, or on a combination of both PHI and PLO (or QHI and QLO). A combination is used if it is desirable to detect events in a particular energy window.

The calculated values of each filter are shown in TABLE 3.1.

Filter	$\tau_r$ L.P. filter	$\tau_f$ H.P. filter
$Q_{LO}$	$7.3\mu s(47.9kHz)$	$22\mu s(15.9kHz)$
$Q_{HI}$	$730ns(479kHz)$	$2.2ms(159Hz)$
$P_{LO}$	$7.3\mu s(47.9kHz)$	$22\mu s(15.9kHz)$
$P_{HI}$	$732ns(479kHz)$	$2.2s(159mHz)$

TABLE 3.2  $f_{3dB}$  for the filters in the *Summer and Trigger* circuit

### 3.1.1 P LO and Q LO filter

One side of the teed charge summer output goes to Q LO circuitry (the other side goes to Q HI). Similarly, one side of the teed phonon summer output goes to P LO circuitry (the other side goes to P HI). The outputs are sent through a high pass, RC filter having a 15.9 kHz 3dB point for both Q LO and P LO to the input of a unity gain, high speed OPA627 amplifiers (U94 and U111) which provide the necessary high impedance load for the filters. Each filter is formed by a  $10k\Omega$  resistor (R227 and R285) and a  $0.001\mu F$  capacitor (C59 and C69).

The Q LO and P LO channels experience a gain of 101 from the non-inverting OPA627GU op amps (U93 and U110, respectively). The signal is modified by an additional factor of  $\sim 0.5$ . This may be due to the unintentional filtering by a filter formed by the  $10k\Omega$  resistor at the input of the noninverting amplifiers and the parasitic capacitance of the 1N4448 clipping diodes plus the input capacitance of the OPA637AU op amps (R225, D4, D5, and U93 for Q LO; R283, D6, D7, and U110 for P LO). Additionally, the signal may be attenuated due to overlapping filter characteristics of the high and low pass filters whose poles are quite close together.

Along with these factors, the Q LO (but not P LO) channel also experiences a gain which will vary depending on the amplitude and polarity of the input signal as shown in FIG. 3.1 below. Please note that these features are not included in P LO's circuitry. The output of U94 is clipped by the  $10k\Omega$  resistor and two diodes to ground, limiting the signal going into U93 to  $\pm 0.8V$ . Amplifier (U93) has three parallel branches in its feedback network. The first is a  $10k\Omega$  resistor in the feedback along with a  $100\Omega$  resistor to ground resulting in a gain of 101. The second is a branch with a 10V zener diode, which has the purpose of limiting the positive output swings to 10V. The third is a  $100\Omega$  resistor and diode in series, which provides an output, for negative input signals, of twice the input voltage plus 0.8 volts.

Both Q LO and P LO circuits have a  $100K\Omega$  nulling pot from pin 1 to pin 5, allowing for setting the output voltage to zero for a zero volt input. The outputs of U93 and U110 are passed through low pass filters having a  $-3dB$  point of 48 kHz. Each filter is formed by a  $33.2k\Omega$  resistor (R220 and R279) and a  $100pF$  capacitor (C58 and C68). The outputs from the low pass filters are then teed to a front panel connector a high input impedance amplifier to and to the discriminator circuit.

Case	Input Voltage	Output Voltage	Diagram
Case I	$V_{in} < \frac{10^* + 0.7^*}{101}$ <p>*values necessary to turn on diodes of interest (circled on diagram)</p>	$V_{out} = \left(1 + \frac{10,000\Omega}{100\Omega}\right) V_{in}$ $V_{out} = 101 * V_{in}$	
Case II	$V_{in} > \frac{10^* + 0.7^*}{101}$ <p>*values necessary to turn on diodes of interest (circled on diagram)</p>	$V_{out} = V_{diode} + V_{zener-diode}$ $V_{out} \approx 10.8 \text{ Volts}$	
Case III	$V_{in} > \frac{-0.7^*}{101}$ <p>*value necessary to turn on diode of interest (circled on diagram)</p>	$V_{out} = \left(1 + \frac{10,000\Omega}{100\Omega}\right) V_{in}$ $V_{out} = 101 * V_{in}$	
Case IV	$V_{in} < \frac{-0.7^*}{101}$ <p>*value necessary to turn on diode of interest (circled on diagram)</p>	$V_{out} = 2V_{in} + V_{diode}$ $V_{out} \approx 2V_{in} + 0.7 \text{ Volts}$ <p><i>Note:</i> <math>2V_{in}</math> is derived from the following op-amp relationship:  <math display="block">\frac{V_{in}}{100\Omega} + \frac{V_{out} - V_{in}}{100\Omega} = 0</math></p>	

FIG. 3.1 Q LO channel gain

### 3.1.2 Q HI filter and P HI filter

The P HI filter consists of U124 (OP627), C74, and R326. The Q HI filter consists of U104 (OP627), C64, and R260. The input to the filters is provided by the output of the 2 and 4 channel summers after passing through their respective buffers. The output of the P HI filter goes to the P HI driver and discriminator. Likewise the output of the Q HI filter goes to the Q HI driver and discriminator.

The input values were chosen to accommodate the  $\frac{1}{2}$  gain and the  $101 * \frac{1}{2}$  gain as seen in the high and low channels respectively.

In the high channels, the gain of  $\frac{1}{2}$  is due to a simple voltage division (formed by R257 and R258 for Q HI and R323 and R324 for P HI )

The input values were chosen to accommodate the  $\frac{1}{2}$  gain and the  $101 * \frac{1}{2}$  gain as seen in the high and low channels respectively.

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### 3.1.3 Filter output buffers

Note that the filter formed by the 1.0kohm and 100pF near the output of the QLO and PLO circuits has an  $f_{3db} = 159\text{MHz}$ , much higher than the other filters in that circuit. Note: This filter is only applied *after* the signal is teed off to the comparator, so will *not* affect the trigger. The evolution of the circuit involving the OPA627 and LM6321 is as follows: There was concern about shorting the output of the LM6321, so the 1:2 voltage divider was added (2 1000k resistors) to protect the LM6321. The LM6321 has a fairly high bias current that can cause a voltage drop through the 1kohm resistors causing an offset. The 6327 was added to remove this offset.

## 3.3 Trigger

The trigger circuit is designed to create a trigger signal via comparison of a user defined level and the input signal. The threshold level is initially set by the user via a DAC. The DAC voltage is compared to the signal from the P HI, P LO, Q HI of Q LO filter circuits. The DAC voltage may be monitored via a front panel connector.

The output of the comparator determines the state of the trigger. The trigger signal is available in three ways: It is sent via connector P1 (on pin pairs 1-18, 2-19, 2-26, 10-27 for Q LO, Q HI, P LO and P HI respectively), it may be viewed via a front panel connector, and it is indicated by a front panel LED.

If the input signal reaches the threshold level, the threshold level is decreased to prevent multiple triggering on a noisy signal.



### 3.3.2 Discriminator

The DAC voltage is compared to the signal from the P HI, P LO, Q HI of Q LO filter circuits by a LM311D voltage comparator. The discriminator circuit which generates the trigger signal is shown in FIG. 3.3.2 below.

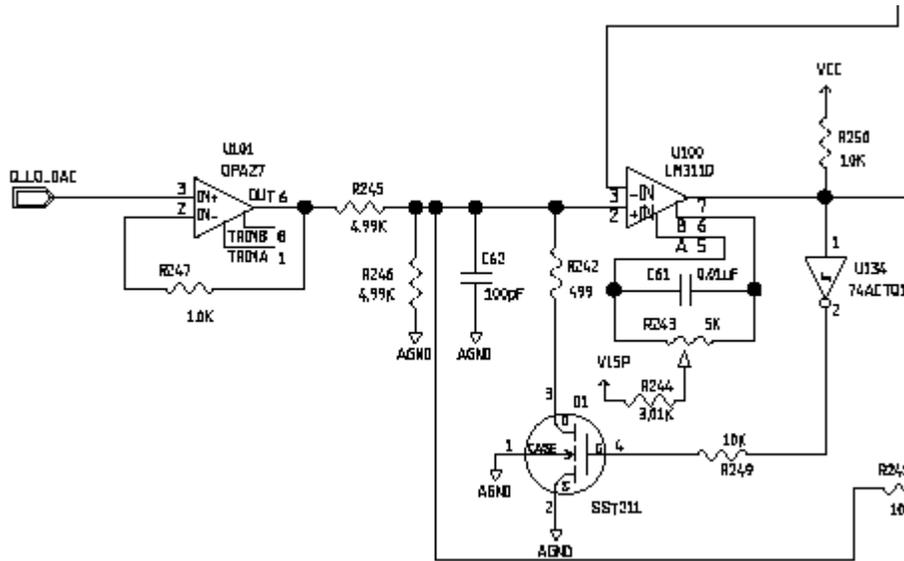
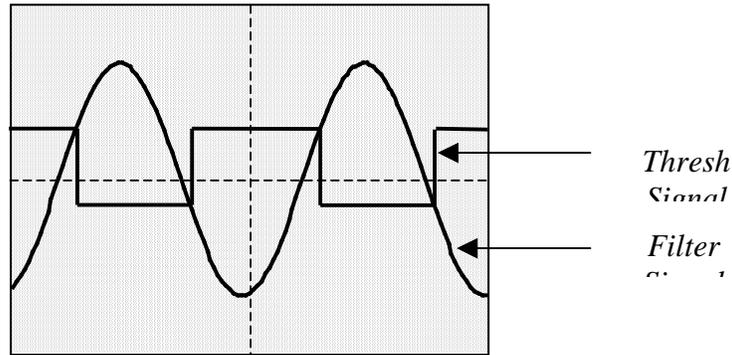


FIG. 3.3.2 Comparator inputs and trigger output

The DAC value used to set the user-determined threshold level is connected in series to a 4.99 kOhm resistor, which in turn is in parallel with another 4.99 kOhm resistor. A voltage division occurs and thus the circuit uses one half the value of the DAC to determine whether or not to set itself in a triggered state. This value is compared to the input signal. If the signal is found to be greater than one half the DAC level, then the circuit is assumed to enter the triggered state. The output of the comparator, which is then low, is inverted by a 74ACTQ14SC inverter. The high output from the inverter turns on an SST211 transistor which connects a 499Ω resistor to ground, thus putting it in parallel with the 4.99kΩ resistor mentioned above. This results in a larger division of the DAC voltage thus lowering the threshold voltage when the circuit is in the triggered state.

Once the signal falls to the lower threshold, the output of the comparator is high, and the threshold is reset to one half the DAC setting.

The thresh signal intersects the filter signal as shown in FIG. 3.2 below.



Note the sharp angle in the thresh signal occurring anywhere other than precisely at those intersection points indicates an error. For example:



Such an error can occur if the internal offset associated with the LM311D is not properly compensated for. A variable resistor is provided to adjust this offset

### 3.3.3 Trigger outputs

The trigger signal is split two ways as shown in FIG. 3.3.3. One leg connects it to a connector which provides the interface to the DAQ. The other leg of the tee provides an indication of the state of the trigger via an LED and also via a front panel connector. On each leg of the tee the output from the discriminator is first inverted, therefore 5V indicates a triggered state.

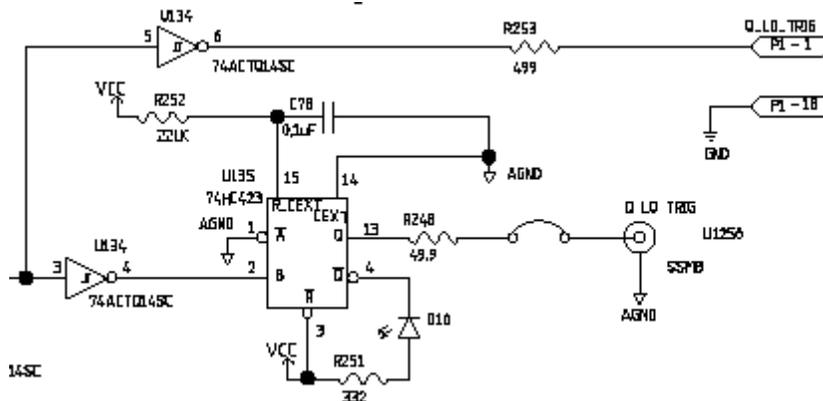


FIG. 3.3.3 Trigger outputs

### Trigger output via P1

One leg of the tee connects the trigger signal to 25-pin connector, P1, on pin pairs 1-18, 2-19, 2-26, 10-27 for Q LO, Q HI, P LO and P HI respective, via a 499Ω resistor. P1 provides an interface to the DAC.

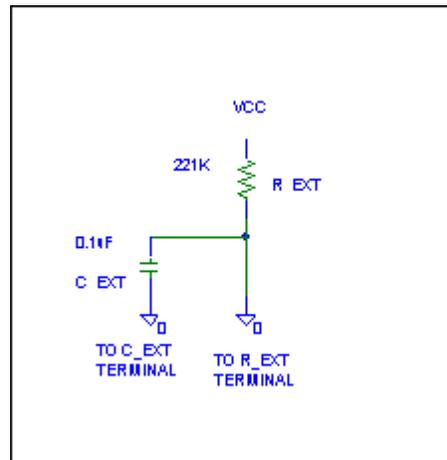
Note: The output from the discriminator is inverted, therefore 5V indicates a triggered state.

### Front panel connector and LED trigger signals

Similarly, on the other leg of the tee, the output from the discriminator is inverted, therefore 5V indicates a triggered state. This provides the input to pin B on the 74HC423 one shot. The output pulse width, PW, of this one shot is simply:

$$PW = (R_{EXT})(C_{EXT}),$$

where  $R_{EXT}$  and  $C_{EXT}$  are connected according to:



With  $R_{EXT} = 221K\Omega$  and  $C_{EXT} = 0.1\mu F$ ,

$$PW = (221K)(0.1\mu F),$$

$$PW = 22.1ms.$$

When Input B is high and Input A, which is tied to GND, is low, the output Q is a high 22.1ms pulse and the output  $\bar{Q}$  is a low 22.1ms pulse. Q is output to the front panel connector. A front panel mounted LED is biased by VCC and a 332Ω resistor such that it turns on when the signal at  $\bar{Q}$  is low. This results in the LED is on when the circuit is in the triggered state.

## 4 500 kHz and 5 MHz filters buffered outputs

### 4.1 Offset

The signals entering the RTF Board have negligible offset. This is a result of the zero-offset circuit at the input of the driver on the ZIP Board. However, it should be noted that, because the zero-offset circuit is located prior to the driver at the end of the ZIP Board, the driver amplifiers may introduce some offset into the system. The RTF board is designed to provide the option of offsetting the signal by 1.48 V. An offset might be desirable in order to take full advantage of the bipolar range of the digitizers, thus improving resolution.

### 4.2 Offset Control System

The offset is implemented through a difference amp circuit (Sheet 4-10) where the V+ input is the signal to be modified and the V- input is the fixed offset value of 1.48 V (labeled VPC on Sheet 4-10). This offset value is provided by the reference voltage source circuit shown on sheet ?-?.

Two switches (DG411's) are in place such that the user has the option of allowing the signal to pass through the op-amp (allowing for the offset) or to bypass it (see Sheet 4-10).

Addresses are set by the user and compared by comparator MC74HC688 (U1) LA(0-4). The lower 4 bits of the address select the output (pin 17) of the 74HC154 (U2). This output is connected to the enable pins (CP) of the 74HC574's (U10, U11), which then allow the 16 bit data string through to the 74HC139 decoders (U26, U27, U28). The decoders determine which switches of the DG411's (U43, U44, U54, U64, U74, U84) will be closed. Only two (of four) switches on each DG411 pack are used for each channel. One is used for letting the signal pass straight through with no offset added (switch 1 selected with data = 00) and the other is used to guide the signal through the difference amplifier (switch 2 selected with data = 01) which results in an offset being added to the signal (see Sheet 2-10).

### 4.2 500 kHz and 5 MHz filters

The signal is then put through a 5 MHz filter followed by a unity gain buffer. The signal is then teed. One leg of the tee goes through a unity gain buffer to a front panel coaxial connector via a 51 ohm resistor. The other leg of the tee goes through a 500 kHz low pass filter followed by a unity gain buffer on to a front panel coaxial connector, via a 51 ohm resistor. Each pair of signals is labeled 500 kHz and 5 MHz. Thus, two filtered signals per channel are provided for output to the experiment digitizers as is shown in FIG. 3.2.

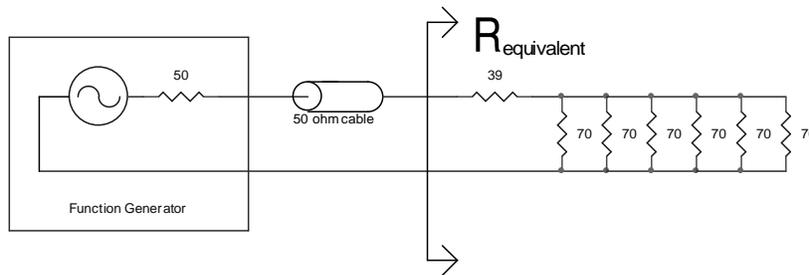


## 5 RTF breakout box

It is desirable to match the output circuit to the  $50\ \Omega$  output impedance of the function generator. The matching was achieved as follows:

The input to each of the four phonon and two charge channels is across a  $70\ \Omega$  resistor ( $70\ \Omega$  was chosen to match the impedance of the cable that connects the RTF breakout box to the RTF board). These six  $70\ \Omega$  resistors are in parallel. A  $39\ \Omega$  resistor placed in series with the  $70\ \Omega$  resistors will create an equivalent resistance,  $R_{equivalent}$ , of about  $50\ \Omega$ :

$$R_{equivalent} = 39\ \Omega + \frac{70\ \Omega}{6 \text{ resistors}} \cong 50\ \Omega$$



Note that to avoid reflections, the  $39\ \Omega$  resistor should be placed as close as possible to the RTF breakout box BNC input connectors.

As a result of the 39 ohm resistor the input voltage from the function generator is modified by a factor of 0.2303. The calculations for this factor are as follows:

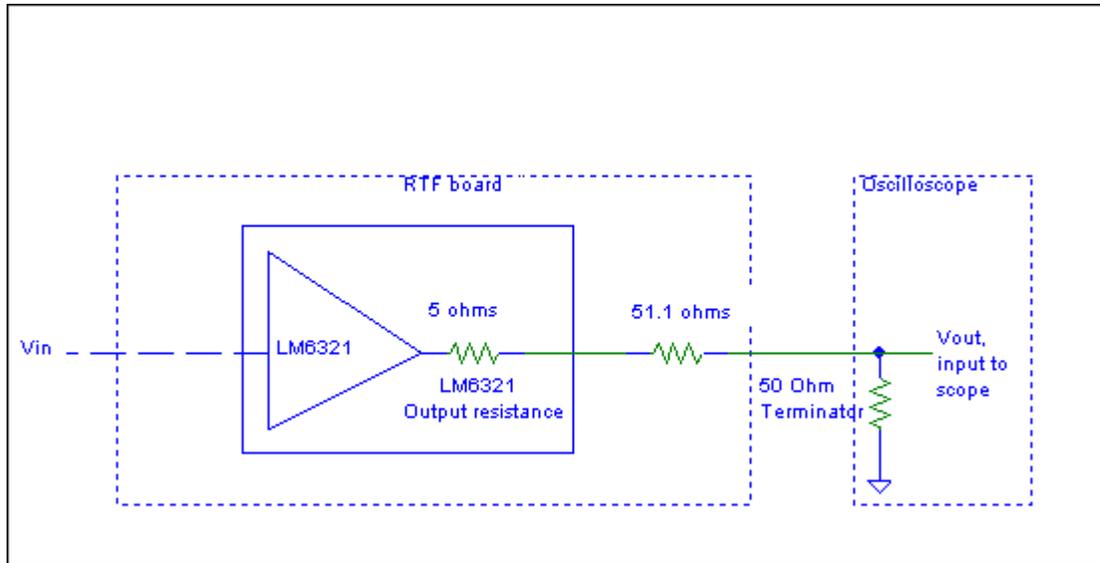
$$V_{out} = \left( \frac{R_{6 \text{ parallel } 70\ \Omega}}{R_{39\ \Omega} + R_{6 \text{ parallel } 70\ \Omega}} \right) V_{in},$$

$$V_{out} = \left( \frac{11.67\ \Omega}{39\ \Omega + 11.67\ \Omega} \right) V_{in},$$

$$V_{out} = (0.2303)V_{in}.$$

## 6 Output characteristics

The following information will become pertinent if the output probe line should be terminated by  $50\Omega$  at the scope. The observed amplitude and offset of the output signal will be modified by a factor of .47 with respect to the input signal amplitude and the 1.48 V offset. This voltage division is a function of the output resistance associated with the op-amp (LM6321 buffer), as well as a  $51.1\Omega$  resistor placed in series with it. Because the measurement is taken across a  $50\Omega$  terminator, the final output voltage is reduced by a factor of .47 (see diagram below).



$$V_{out} = \left( \frac{50}{5+51.1+50} \right) V_{in} ,$$

$$V_{out} = 0.47 V_{in} .$$

# Appendix

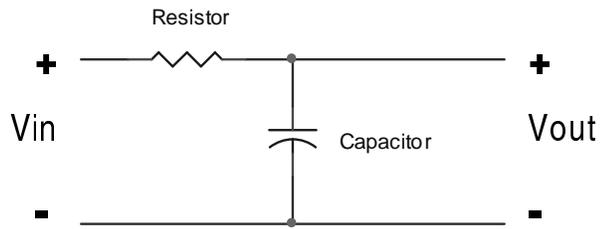


Figure 1 - Low Pass Filter

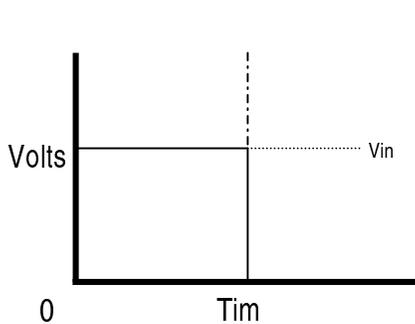


Figure 2 – Input Signal

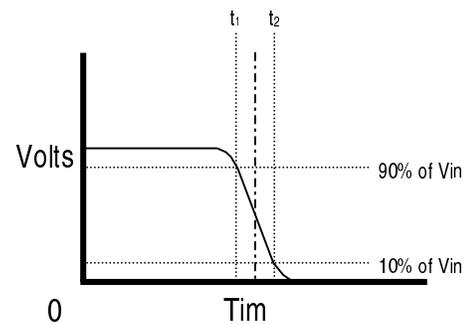


Figure 3 – Output Signal

Throughout documentation the following equation was referred to on numerous occasions:

$$f_{3dB} = \frac{0.35}{\tau_f} \quad (\text{eq 1})$$

Where a relationship exists between the bandwidth ( $f_{3dB}$ ) of a filter and the rise-time( $\tau_f$ ) associated with it. The following is a derivation of this relationship.

Simple circuit theory gives us the following equations:

$$V_{out} = V_{in} e^{-\frac{t}{RC}} \quad (\text{eq 2})$$

$$RC = \frac{1}{2\pi f_{3dB}} \quad (\text{eq 3})$$

The fall-time( $\tau_f$ ) of a signal is defined as the amount of time necessary for the signal to drop from 90% of its initial value to 10% of its initial value. As denoted on figure 3, we shall refer to the fall-time( $\tau_f$ ) as  $(t_2-t_1)$ .

Solving for  $t_1$  and  $t_2$  using equation 2(eq 2), the following is obtained:

$$V_{out} = V_{in} e^{\frac{-t}{RC}} \quad (\text{eq 2})$$

$$0.9V_{in} = V_{in} e^{\frac{-t_1}{RC}}$$

$$0.1V_{in} = V_{in} e^{\frac{-t_2}{RC}}$$

$$0.9 = e^{\frac{-t_1}{RC}}$$

$$0.1 = e^{\frac{-t_2}{RC}}$$

$$\ln(0.9) = \frac{-t_1}{RC}$$

$$\ln(0.1) = \frac{-t_2}{RC}$$

$$t_1 = -RC \ln(0.9)$$

$$t_2 = -RC \ln(0.1)$$

Therefore the fall-time( $\tau_f$ ) is equal to:

$$\tau_f = (t_2 - t_1)$$

$$\tau_f = -RC \ln(0.1) + RC \ln(0.9)$$

$$\tau_f = -RC \ln\left(\frac{0.1}{0.9}\right) \quad (\text{eq 4})$$

Solving equation 4 (eq 4) for RC the following is obtained:

$$RC = -\frac{\tau_f}{\ln\left(\frac{0.1}{0.9}\right)} \quad (\text{eq 5})$$

Solving equations 3 (eq 3) and 5 (eq 5) for bandwidth result in the desired equation (eq 1):

$$RC = \frac{1}{2\pi f_{3dB}} \quad (\text{eq 3})$$

$$RC = -\frac{\tau_f}{\ln\left(\frac{0.1}{0.9}\right)} \quad (\text{eq 5})$$

$$RC = \frac{1}{2\pi f_{3dB}} \quad (\text{eq 3})$$

$$f_{3dB} = \frac{1}{2\pi RC}$$

$$f_{3dB} = \frac{1}{2\pi \left( -\frac{\tau_f}{\ln\left(\frac{0.1}{0.9}\right)} \right)}$$

$$f_{3dB} = \frac{0.35}{\tau_f} \quad (\text{eq 1})$$

