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This file is located on the Lab PC, at D:\users\haldeman\cdms\Stanford Driver.doc

Supplied Voltages

General Operation

The Driver is a module which has 6 independent analog amplifier channels, each of which have controllable gain, and DC input offset voltage. The Gain choices are 1, 2, 5, 10, 20 and 50. The bandwidth of each channel is approximately 10 MHz wide. Offset is done at the input, and as a result, is unaffected by gain and visa-versa. The input signals are referred to Front-end ground, (FEGND) and the output signals are referred to Analog ground (AGND).

The input impedance to each channel is approximately 500 ohms and the output impedance is approximately 50 ohms and is designed to drive a 50 ohm load; AC or DC coupled. When driving a 50 ohm load, the maximum output voltage swing is approximately plus or minus 2 volts.

This module may be plugged into a powered connector; there is no need to turn off power during insertion or extraction into the backplane connector. When the module is first powered up, the 15 Volt LEDs on the front panel should light up, followed in approximately 1/4 second by the 5 Volt LED.

Power Control Circuitry

This module utilizes the following voltages available at the backplane:

+15, -15 and +5D.

When the Driver Module is plugged in, the circuitry voltages remain off for a period of approximately 1.3 seconds, after which IC23, pin 5 goes high, turning Q2 on, causing both, Q3 and Q4 to turn on. Turning Q3 and Q4 on, connects the + & - 15 volt supplies to the rest of the module circuitry. Approximately 300 milliseconds after application of the 15 volts to the rest of the circuitry, IC 25 turns on Q1 connecting the 5 Volts to the module.

Board generated voltages.

Four very precise, and stable, voltages are generated for powering the two, four channel DAC's. These voltages consist of the +10 and -10 for powering the DAC's, and the +5 and -5 volts for the high and low references.

Digital Interface

In order to appear as a single gate load to the crate backplane, all of the lines are buffered. The data lines are buffered by IC34, whereas the address, read and write lines are buffered by IC29. IC29 is operated in a unidirectional mode; always passing the backplane signals to this module. The data lines (IC34), on the other hand, have the direction controlled by the write line, but only if this particular module is being addressed. The address this module responds to is determined by the address set up by switch SW4, and IC35. IC35 compares the bit pattern of A08, A09, A10 and A12 with that of SW4; if they match, the outputs of IC34 are enabled(active).

Digital to Analog Converter (DAC).

These quad devices, allow the user to set the output voltage anywhere in the range of plus or minus five volts. A system reset sets the 4 outputs to zero volts. The 4 outputs control the following devices.

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Module Addressing

This module utilizes the following address lines: A12, A10, A09, A08, to select this module, and we call this the “**Module Address**”. Lines A2, A1, A0 are used to select an item on this module to read from or write to.

Module Address + 0; DAC0;	Reads or writes the DRIVER, Channel 00 OFFSET.
Module Address + 1; DAC1;	Reads or writes the DRIVER, Channel 01 OFFSET
Module Address + 2; DAC2;	Reads or writes the DRIVER, Channel 02 OFFSET
Module Address + 3; CSR0 ;	Reads or writes the DRIVER, CSR0
Module Address + 4; DAC4;	Reads or writes the DRIVER, Channel 03 OFFSET
Module Address + 5; DAC5 ;	Reads or writes the DRIVER, Channel 04 OFFSET
Module Address + 6; DAC6 ;	Reads or writes the DRIVER, Channel 05 OFFSET
Module Address + 7; CSR1 ;	Reads or writes the DRIVER, CSR1

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Control and Status Register (CSR0), Bit assignments

The address of CSR0 is **Module Address + 3**. **CSR0** consists of IC20. It is a 16 bit register which can be both, read from and written to, and have the following control functions.

Bit 2	Bit 1	Bit 0	Meaning
0	0	0	Driver Channel 0, Amplifier OFF
0	0	1	Driver Channel 0, Amplifier OFF
0	1	0	Driver Channel 0, Gain = 1
0	1	1	Driver Channel 0, Gain = 10
1	0	0	Driver Channel 0, Gain = 2
1	0	1	Driver Channel 0, Gain = 20
1	1	0	Driver Channel 0, Gain = 5
1	1	1	Driver Channel 0, Gain = 50

Bit 5	Bit 4	Bit 3	Meaning
0	0	0	Driver Channel 1, Amplifier OFF
0	0	1	Driver Channel 1, Amplifier OFF
0	1	0	Driver Channel 1, Gain = 1
0	1	1	Driver Channel 1, Gain = 10
1	0	0	Driver Channel 1, Gain = 2
1	0	1	Driver Channel 1, Gain = 20
1	1	0	Driver Channel 1, Gain = 5
1	1	1	Driver Channel 1, Gain = 50

Bit 8	Bit 7	Bit 6	Meaning
0	0	0	Driver Channel 2, Amplifier OFF
0	0	1	Driver Channel 2, Amplifier OFF
0	1	0	Driver Channel 2, Gain = 1
0	1	1	Driver Channel 2, Gain = 10
1	0	0	Driver Channel 2, Gain = 2
1	0	1	Driver Channel 2, Gain = 20
1	1	0	Driver Channel 2, Gain = 5
1	1	1	Driver Channel 2, Gain = 50

Bit 11	Bit 10	Bit 9	Meaning
0	0	0	Driver Channel 3, Amplifier OFF
0	0	1	Driver Channel 3, Amplifier OFF
0	1	0	Driver Channel 3, Gain = 1
0	1	1	Driver Channel 3, Gain = 10
1	0	0	Driver Channel 3, Gain = 2
1	0	1	Driver Channel 3, Gain = 20
1	1	0	Driver Channel 3, Gain = 5
1	1	1	Driver Channel 3, Gain = 50

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Bit 14	Bit 13	Bit 12	Meaning
0	0	0	Driver Channel 4, Amplifier OFF
0	0	1	Driver Channel 4, Amplifier OFF
0	1	0	Driver Channel 4, Gain =1
0	1	1	Driver Channel 4, Gain = 10
1	0	0	Driver Channel 4, Gain = 2
1	0	1	Driver Channel 4, Gain = 20
1	1	0	Driver Channel 4, Gain = 5
1	1	1	Driver Channel 4, Gain = 50

Bit 15 **Module Reset.** Writing a "1" to CSR0, Bit 15, produces a module reset.

Control and Status Register (CSR1), Bit assignments

The address of CSR1 is **Module Address + 7**. **CSR1** consists of IC46. It is a 16 bit register which can be both, read from and written to, and has the following control functions.

Bit 2	Bit 1	Bit 0	Meaning
0	0	0	Driver Channel 5, Amplifier OFF
0	0	1	Driver Channel 5, Amplifier OFF
0	1	0	Driver Channel 5, Gain =1
0	1	1	Driver Channel 5, Gain = 10
1	0	0	Driver Channel 5, Gain = 2
1	0	1	Driver Channel 5, Gain = 20
1	1	0	Driver Channel 5, Gain = 5
1	1	1	Driver Channel 5, Gain = 50

Bits 3 through 15 unused.