

This file is located on the Lab PC, at D:\users\haldeman\cdms\Stanford QET.doc

## **General Module Description**

This module was designed for the Cryogenic Dark Matter Search(CDMS), experiment(E891), and has the primary purpose of supplying the DC bias to each of the four Transition Edge Sensors located on each semiconductor crystal in the detector. Each sensor, is used in conjunction with a SQUID(Superconducting, QUantum, Interference Device) for the detection of phonons caused by the interaction of Weakly Interacting Massive Particles (WIMPs), within the Silicon and/or Germanium crystals in the CDMS detector. There are four outputs, each having an adjustable voltage range of -5 to +5 volts, with 12 bit resolution. The output impedance of each channel is approximately 25 kilo-ohms.

Power is supplied to the QET Module via the 96 Pin connector which plugs into the subrack backplane. Over-current and over-voltage protection is provided by a combination of 0.5 ampere fuses, and transient voltage suppressers(TVS). Also, large surge currents during hot plug-ins are avoided, minimizing damage to the connector pins, because a delay of about 1.3 seconds exists between plugging the board in, and application of +/- 15 volts to the module circuits. Approximately ¼ second later, the 5 volt circuitry is energized, followed by a ½ second “power on reset”.

The heater pulse width is adjustable between 10 milliseconds and 1,600 milliseconds in either, 10 millisecond steps between 10 and 160 milliseconds, or 100 millisecond steps between 100 and 1,600 milliseconds ( depending on which capacitor is selected during insertion ). During the heater pulse width, the output impedance is reduced from approximately 25 kilohms to approximately 5.2 kilohms.

## **Backplane Supplied Voltages**

This module utilizes the following voltages available at the backplane:

FE+15, FE-15, and +5D.

When the QET Module is plugged in, the circuitry voltages remain off for a period of approximately 1.3 second, after which the two FE15 volt supplies are connected to the circuitry. Approximately 300 milliseconds after application of the 15 volts, the 5D voltage is applied.

## **Board Generated Voltages.**

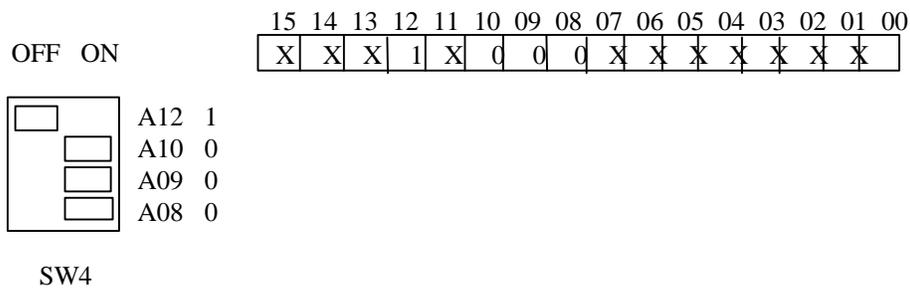
Four very precise and stable, voltages are generated for the 4 channel DAC. These voltages consist of the +10 and -10 for powering the DAC, and the +5 and -5 volts for the high and low references, respectively.

A -5 Volt level is produced by IC50(page 1), for supplying the negative supply voltage to IC's 15 & 25, on page 1 of the schematic diagram.

## Digital Interface

In order for this module to appear as a single gate load to the crate backplane, all of the backplane lines are buffered near the backplane connector. The data lines are buffered by IC34, whereas the address, read and write lines are buffered by IC29. IC29 is operated in a unidirectional mode; always passing the backplane signals to other circuitry in this module. The data lines (IC34), on the other hand, have the direction controlled by the write line, but only if this particular module is being addressed.

The address, this module responds to, is determined by the address set up by switch SW4, and IC35. IC35 compares the bit pattern of A12, A10, A09 and A08 with that of SW4, as illustrated below; if they match, the outputs of IC34 are enabled(active). In the below illustration, switch (SW4) is set for a module address of XXX1X000XXXXXXXXX, where X means “don’t care”. When the switch is set as illustrated at the lower left, this module will only respond to the address illustrated on Address lines A12, A10, A09 and A08.

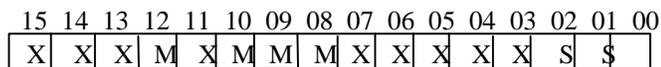


**Digital to Analog Converter (DAC).** This quad device allows the user to set the DAC output voltage anywhere in the range of plus or minus five volts. A system reset, or writing an 0800(HEX.) to the DAC, sets the 4 outputs to zero volts.

### Module Subaddressing.

In the addressing scheme illustrated below, the bit locations designated “M”, are decoded as the module address. The settings of the four switches on SW4 determines the bit pattern this module responds to.

The bit locations designated “S”, are for addressing up to eight devices in this module. These addresses are listed below. For example, a read or write to address 010 ( in the three “S” locations) is a read or write to the DAC that produces the “C SENSOR BIAS”.



**Module Address + 0; DAC0;** Reads or writes “A SENSOR BIAS” voltage.

**Module Address + 1; DAC1;** Reads or writes “B SENSOR BIAS” voltage.

**Module Address + 2; DAC2;** Reads or writes “C SENSOR BIAS” voltage.

**Module Address + 3; DAC3;** Reads or writes “D SENSOR BIAS” voltage.

**Module Address + 4; CSRO;** Reads or writes the Control and status register Zero (CSRO).

|                           |  |
|---------------------------|--|
| <b>Module Address + 5</b> | Not used.  |
| <b>Module Address + 6</b> | A write to this address, generates a module <b>RESET</b> . |
| <b>Module Address + 7</b> | A write to this address causes the heater to be pulsed.    |

### Control And Status Register (CSRO), Bit Assignments

The address of CSRO is **Module Address + 4**. The control and Status Register consists of IC41. It's a 16 bit register that can be both, read from and written to, and have the following control functions.

|        |                                       |
|--------|---------------------------------------|
| Bit 0  | calibrate/measure A                   |
| Bit 1  | calibrate/measure B                   |
| Bit 2  | calibrate/measure C                   |
| Bit 3  | calibrate/measure D                   |
| Bit 4  | Heater Pulse width = ???milliseconds. |
| Bit 5  | Heater Pulse width = ???milliseconds. |
| Bit 6  | Heater Pulse width = ???milliseconds. |
| Bit 7  | Heater Pulse width = ???milliseconds. |
| Bit 8  | Enable Heater A                       |
| Bit 9  | Enable Heater B                       |
| Bit 10 | Enable Heater C                       |
| Bit 11 | Enable Heater D                       |
| Bit 12 | CSRO-12                               |
| Bit 13 | CSRO-13                               |
| Bit 14 | CSRO-14                               |
| Bit 15 | CSRO-15                               |

**Bit 0 calibrate/measure A:** A “High” value on this bit, puts channel A, in the “**Calibrate**” mode. In the calibrate mode, an external signal, named “**Variable**”, is selected by IC15, and sent to the “A Bias” output. If bit 0 is “Low”, channel A is in the “**Measure**” mode, and the output voltage of channel A is controlled by DAC 0. In the measure mode, it's also possible to pulse the output with a larger magnitude voltage for a period determined by CSRO bits 4 through 7.

**Bit 1 calibrate/measure B:** A “High” value on this bit, puts channel B, in the “**Calibrate**” mode. In the calibrate mode, an external signal, named “**Variable**”, is selected by IC15, and sent to the “B Bias” output. If bit 1 is “Low”, channel B is in the “**Measure**” mode, and the output voltage of channel B is controlled by DAC 1. In the measure mode, it's also possible to pulse the output with a larger magnitude voltage for a period determined by CSRO bits 4 through 7.

**Bit 2 calibrate/measure C:** A “High” value on this bit, puts channel C, in the “**Calibrate**” mode. In the calibrate mode, an external signal, named “**Variable**”, is selected by IC15, and sent to the “C Bias” output. If bit 2 is “Low”, channel C is in the “**Measure**” mode, and the output voltage of channel C is controlled by DAC 2. In the measure mode, it's also possible to pulse the output with a larger magnitude voltage for a period determined by CSRO bits 4 through 7.

**Bit 3 calibrate/measure D:** A “High” value on this bit, puts channel D, in the “**Calibrate**” mode. In the calibrate mode, an external signal, named “**Variable**”, is selected by IC15, and sent to the “D Bias” output. If bit 3 is “Low”, channel D is in the “**Measure**” mode, and the output voltage of channel D is

controlled by DAC 3. In the measure mode, it's also possible to pulse the output with a larger magnitude voltage for a period determined by CSR0 bits 4 through 7.

**Bits 4, 5, 6, & 7: Heater Pulse Width:** These four bits allow the pulse width to be set for 32 different widths ( depending on which capacitor was selected during insertion ) in either 10 or 100 millisecond increments; bit 4 is the LSB. The minimum width available is 10 milliseconds and the maximum width is 1.7 seconds.

**Bits 8 through 11: Heater Pulse Enable:**These bits select the channels that will generate a heater pulse when the heater is pulsed ( see **Module Addressing** above ).

Bit 8 High, enables heater pulsing for channel A.

Bit 9 High, enables heater pulsing for channel B.

Bit 10 High, enables heater pulsing for channel C.

Bit 11 High, enables heater pulsing for channel D.

**Bits 12 through 15:** inclusive, are unused.