

QAMP - DISCRETE USERS MANUAL

This file is located on the CO-OP PC (Merle-co-op)\\ D:\Cdms\Qamps\Qamp – Discrete\
qampD_usr_man.doc

GENERAL MODULE DESCRIPTION

Supplied Voltages

Power Control Circuitry

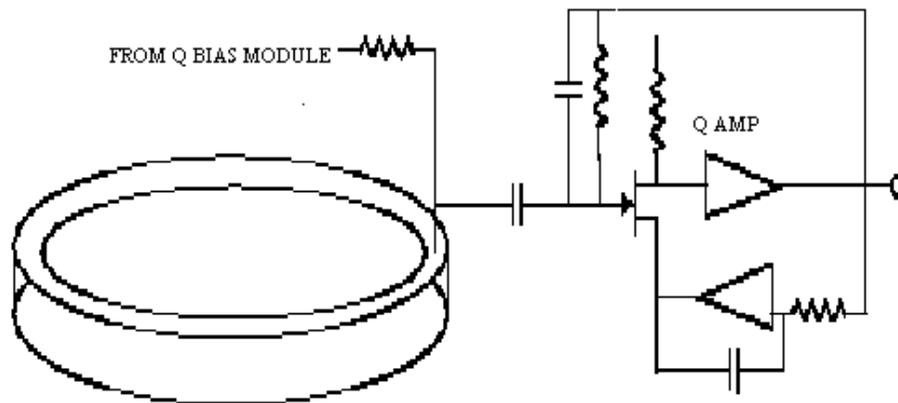
This module utilizes the following voltages available at the backplane:

FE+15, and FE-15.

When the Qamp Module is plugged in, the +15 and –15 volt supplies from the backplane are supplied via fuses to their respective location on the Qamp module.

Qamp Description:

The Qamp module is used in conjunction with the front-end FET to convert charge collected from the detector to a voltage which ultimately gets sent to the data acquisition system, via the Driver, for digitization. The detector has a disk shape, approximately 7.5 cm in diameter, and 1 cm thick. The charge collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.



A separate, individually controlled, DC bias voltage is provided for each of these two charge-collecting electrodes, on the detector, by the Qbias module. The detector charge from each of these two charge-collecting electrodes, is AC coupled to the two JFET-Gates through DC Bias blocking capacitors. Because the JFET-Gate is very sensitive to charge, it is important to minimize the noise charge at this node. Charge on a capacitor is proportional to both capacitance and voltage; $Q = C * V$. The stray capacitance at the JFET-Gate to it's surroundings is difficult to control. Mechanical vibrations (microphonics), cause variations in stray capacitance which produce corresponding variations in charge in the stray capacitance. The smaller we make the stray capacitance voltage, the smaller will be the variations in Q for a given variation in Cstray. Reducing V to zero would obviously make Q zero, and thus independent of variations in Cstray.

The simplified theory of operation of the Q Amp is as follows. There are two feedback loops at work in this module, as illustrated above; a fast one (the upper path in the illustration) and a slow one, each having an individual separate purpose. The slow loop, which drives the JFET-Source, serves the purpose of

keeping the DC output of the Q Amp (AD840 pin 10) at zero volts. This is important because the Q Amp output has a DC connection to the JFET-Gate. The slow loop also keeps the JFET at the correct operating point when the JFET-Gate is at essentially zero volts with respect to ground. There may be other reasons for keeping the JFET-Gate at zero volts, but the most important fundamental reason is to prevent charge from coupling into the input due to the physical motions of grounded portions of the detector enclosure, as mentioned above. If the JFET-Gate is at the same voltage as the enclosure, the voltage across the stray capacity is zero, and changes in the stray capacity will not result in a flow of charge through the stray capacitance.

The operation of the slow loop is as follows; lets assume the JFET-Gate is at ground voltage and the JFET-Source is at some positive voltage with respect to (wrt) the JFET-Gate, say $\frac{3}{4}$ of a volt, and the drain is at about 3 volts. The Q Amp has a zero voltage output when the JFET-Drain (connected to the input of the AD840) via Q1(common base amp) and Q2(emitter follower amp) is at about 3 volts. Since the AD840 is a non-inverting amplifier, an increase in the JFET-Drain voltage produces a positive voltage at the output of the Q Amp. This positive output at the input of the, long time-constant, inverting integrator(OP627), begins driving the JFET-Source in a more negative direction, causing a larger current flow in the JFET and thus a decrease in the JFET-Drain voltage, opposing the original increase. Thus the integrator's task is to keep the DC output of the Q Amp at zero volts.

The fast loop also keeps the JFET-Gate near zero volts by neutralizing the charge injected into the gate node by the detector through the JFET-Gate, DC blocking capacitor, situated between the Detector and the JFET-Gate. This neutralizing charge is supplied from the output of the Q Amp through a parallel combination of resistance and capacitance which we call the "**Feedback Network**". The amplitude of the Q Amp output pulse is determined by the capacitance in the feedback network and the quantity of charge from the detector.

So both loops essentially function to keep the JFET-Gate near zero volts.