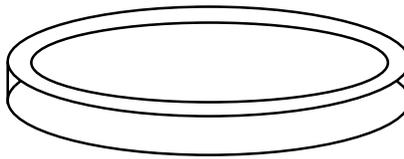

This file is located on the Lab PC, at D:\users\haldeman\cdms\Stanford Q Bias.doc

General Module Description

The **Q Bias Module** provides two DC voltage outputs for supplying bias voltage to the detector charge collection segments, and two current outputs for flashing the trapped-charge-neutralizing LED's. All four outputs are bipolar and have their magnitudes controlled via individual 12-bit DAC's. The detector is either Silicon or Germanium, and has a disk shape, approximately 7.5 centimeters(cm) in diameter, and 1cm thick. The Charge-collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.



One of the voltage outputs is connected to each of these two Charge-collecting electrodes. Each bias voltage has an output range of -5 volts to +5 volts, with 2.44 millivolt resolution. Bits 8 and 9 in CSR0 cause these detector electrodes to be either connected to their respective outputs, or connected to FEGND.

Another function of the **Q Bias Module**, is to provide bias current for energizing two LED's. For this purpose, the **Q Bias module** has two current sources which are able to source, or sink, up to 5 milliamps, with 2.44 microamp resolution. These two current sources are controlled independently, and can be turned on continuously, or operated in a pulsed mode. In the pulsed mode, the sources can be put in the single pulse mode, (requiring a write to this module for each pulse generated), or repetitive mode. In the single pulse mode, the pulse width is adjustable, via digital control. In the repetitive mode, both the pulse width and the pulse rate are adjustable, via digital control.

Supplied Voltages

Power Control Circuitry

This module utilizes the following voltages available at the backplane:

+15, -15, FE+15, FE-15 and +5D.

When the Driver Module is plugged in, the circuitry voltages remain off for a period of approximately 1.3 seconds, after which IC24, pin 5 goes high, turning Q3, Q4, Q5, and Q6, on, connecting the + & - 15 volt supplies to the rest of the module circuitry. Simultaneous with IC24, pin 5 going high, is pin 6 going low, which turns Q1 on, connecting the 5 Volt supply to the rest of the Module. Approximately 300 milliseconds after application of the 5 volts to the rest of the circuitry, IC 25 terminates it's "power-on" reset level.

Board generated voltages.

Four very precise, and stable, voltages are generated for powering the four channel DAC. These voltages consist of the +10 and -10 for powering the DAC, and the +5 and -5 volts for the high and low DAC references.

Digital Interface

In order to appear as a single gate load to the crate backplane, all of the lines are buffered. The data lines are buffered by IC2, whereas the address, read and write lines are buffered by IC1. IC1 is operated in a unidirectional mode; always passing the backplane signals to this module. The data lines (IC2), on the other hand, have the direction controlled by an addressed read, or selected read (SREAD) line. The address this module responds to is determined by the address set up by switch SW1, and IC5. IC5 compares the bit pattern of A08, A09, A10 and A12 with that of SW1; if they match, the outputs of IC2 are enabled(active), and the data is placed on the internal bus going to the two Control and Status Registers(CSR0 and CSR1), as well as to the four channel DAC. This internal bus has a 10 kilohm pull-down resistor on each line to prevent excessive input stage power supply current draw in the CSR's.

Digital to Analog Converter (DAC).

This quad output device, allows the user to set the output voltage anywhere in the range of minus five volts, to plus 4.9975V , in 2.44mV steps. A system reset sets the 4 outputs to zero volts. The actual output voltage is determined by:

$$V_{out} = -5Volts + \left(\frac{10N}{4096} \right)$$

Where N is the binary code loaded into the DAC.

The 4 DAC outputs control the following devices.

DAC0=Q inner Bias Voltage ; Supplies the bias voltage to the detector inner disk.

DAC1=Q outer Bias Voltage ; Supplies the bias voltage to the detector outer ring.

DAC2=LED1 Bias Current ; Sets the bias current for LED1(1mA/V, in 2.44 uA steps).

DAC3=LED2 Bias Current ; Sets the bias current for LED2(1mA/V, in 2.44 uA steps).

Module Addressing

This module utilizes the following address lines: A12, A10, A09, A08, to select this module, which we call this the “**Module Address**”. Lines A2, A1, A0 are used to select an item on this module to read from or write to.

Module Address + 0; (DAC0); Reads or writes the **Q inner Bias**.

Module Address + 1; (DAC1); Reads or writes the **Q outer Bias**.

Module Address + 2; (DAC2); Reads or writes the **LED1 Bias**.

Module Address + 3; (DAC3); Reads or writes the **LED2 Bias**.

Module Address + 4; Reads or writes CSR0

Module Address + 5; Reads or writes CSR1

Module Address + 6; Not used.

Module Address + 7; Not used.

Control and Status Register (CSR0), Bit assignments

The address of CSR0 is **Module Address + 4**. **CSR0** consists of IC3. It is a 16 bit register which can be both, read from and written to, and has the following control functions. The indications are “**high/low**”.

Bit	Meaning	Indication
0	LED1 Bias	ON/OFF
1	LED1 Bias(If Bit0 is high)	Continuous/Pulse
2	LED1 Bias(If Bit1 is low)	Repetitive/Single
3	LED1 Bias(If Bit1 is low)	Long/Short
4	LED2 Bias	ON/OFF
5	LED2 Bias(If Bit4 is high)	Continuous/Pulse
6	LED2 Bias(If Bit5 is low)	Repetitive/Single
7	LED2 Bias(If Bit5 is low)	Long/Short
8	Q inner bias/ground	Output at V_{ibias} /Output grounded
9	Q outer bias/ground	Output at V_{obias} /Output grounded
10	Q inner monitor	Available on 9U Module only
11	Q outer monitor	Available on 9U Module only
12	not used	
13	not used	
14	not used	
15	Module Reset	Sets all 16 bits in both CSR's to

“0”

Control and Status Register (CSR1), Bit assignments

The address of CSR1 is **Module Address + 5**. **CSR1** consists of IC4. It is a 16 bit register which can be both, read from and written to, and controls the pulse width of the pulse width generators, as well as the pulse rate of the two pulse rate generators.

The width controls both the short and long pulse widths. The short pulse generator has a minimum width of 5 microseconds and the width can be incremented to 80 microseconds in 16, 5 microsecond steps. The long pulse generator has a minimum width of 200 microseconds and the width can be incremented to 3200 in 16, 200 microsecond steps.

The rate controls the respective pulse rate generators. The period has a minimum setting of 100 milliseconds and can be varied up to 1600 milliseconds in 16, 100 millisecond steps. In order to determine the width or rate, add the weight of the individual bits to the respective minimums.

Bit	Meaning	Rate Period	Narrow Pulse	Long Pulse
0	LED1 Pulse Width 0		5 uS	200 uS
1	LED1 Pulse Width 1		10 uS	400 uS
2	LED1 Pulse Width 2		20 uS	800 uS
3	LED1 Pulse Width 3		40 uS	1600 uS
4	LED1 Rate0 (Period)	100mS		
5	LED1 Rate1 (Period)	200mS		
6	LED1 Rate2 (Period)	400mS		
7	LED1 Rate3 (Period)	800mS		
8	LED2 Pulse Width 0		5 uS	200 uS
9	LED2 Pulse Width 1		10 uS	400 uS
10	LED2 Pulse Width 2		20 uS	800 uS
11	LED2 Pulse Width 3		40 uS	1600 uS
12	LED2 Rate0 (Period)	100mS		
13	LED2 Rate1 (Period)	200mS		
14	LED2 Rate2 (Period)	400mS		
15	LED2 Rate3 (Period)	800mS		