ORIGINAL

VERSION # 1

DATE REVISED

01/10/00

ZIP MODULE INDEX
(1/8/99)

SCHEMATIC (SECTION - PAGE #)	QNTY BRD	PDF SCH. PAGE	Certified Circuit Number	LAST PDF WRT DATE	BOM	LAST REV DATE
LEGEND **(COVER PAGE)**		6	N/A	3/25/99		
MISC. CONNECTORS **(1-1)**	1	7	N/A	9/24/99		
P2 CONNECTOR BLOCK **(1-2)**	1	8	N/A	7/27/99		
P4 CONNECTOR BLOCK **(1-3)**	1	9	N/A	7/27/99		
ZIP BLOCK DIAGRAM **(2-1)**	1	10	N/A	9/23/99		
SQUID BLOCK DIAGRAM **(3-1)**	4	11	N/A	9/9/99		
SQUID FRONT END **(3-2)**	1	15	CCM005	10/5/99		
SQUID VAR. GAIN AMP **(3-3)**	1	16	CCM006	7/14/99		
SQUID FEEDBACK CONTROL BLOCK **(3-4)**	4	17	N/A	9/9/99		
SQUID FEEDBACK INTEGRATOR **(3-5)**	1	21	CCM008	9/28/99		
SQUID FEEDBACK POLARITY **(3-6)**	1	22	CCM009	5/14/99		
SQUID FEEDBACK MONITOR **(3-7)**	1	23	CCM010	9/9/99		
SQUID FEEDBACK LOGIC **(3-8)**	1	24	CCM011	9/9/99		
SQUID ZAP CONTROLL **(4-1)**	1	25	CCM012	10/6/99		
QET BLOCK DIAGRAM **(5-1)**	1	26	N/A	9/9/99		
QET NOISE BUFFER FRONT END **(5-2)V1**	1	27	CCM030	9/29/99		
QET FILTER **(5-3)**	N/A	N/A	CCM014			
QET SELECTOR **(5-4) V1**	1	28	CCM031	9/29/99		
QAMP BLOCK DIAGRAM **(6-1)**	2	29	N/A	9/9/99		
DISCRETE Q AMPLIFIER **(6-2)**	1	31	CCM001	9/27/99		
QAMP 14V **(6-3)**	1	32	CCM003	9/9/99		
QBIAS FRONT END **(7-1)**	1	33	CCM016	5/14/99		
LED BLOCK DIAGRAM **(8-1)**	1	34	N/A	5/14/99		
(8-2)			N/A			
LED PULSE CONTROL **(8-3)**	1	35	CCM028	5/14/99		
LED CURRENTCONTROL **(8-4)**	1	36	CCM020	4/6/99		
LED CURRENT SOURCE **(8-5)**	1	37	CCM019	5/14/99		
FETTEMP **(9-1)**	1	38	N/A	10/1/99		
DRIVER **(10-1)**	1	39	CCM002	9/9/99		
EXTERNAL TEST RECEIVER **(11-1)**	1	40	CCM022	9/28/99		
DAC&BUFFERS BLOCK DIAGRAM **(12-1)**	1	41	N/A	9/9/99		
DAC REFERENCES **(12-2)**	1	42	N/A	3/25/99		
DAC PRECISION REFERENCE **(12-3)**	1	43	CCM023	1/25/99		
DAC 10 VOLT REFERENCE **(12-4)**	1	44	CCM024	9/9/99		
DAC 5 VOLT REFERENCE **(12-5)**	XXXXX	XXXX	CCM025	XXXX	XXX	XXX
DAC'S 1 TO 7 **(12-6)**	7	45	N/A	9/9/99		
DUAL NON-INVERT BUFFER BLOCK **(12-7)**	9	52	N/A	9/9/99		
DUAL NON-INVERT. BUFFERS **(12-8)**	1	61	CCM007	4/6/99		
BUFFER FILTER **(12-9)**	1	62	CCM017	1/25/99		
LOGIC BLOCK DIAGRAM **(13-1)**	1	63	N/A	9/23/99		
(13-2)			N/A			
CONTROL LOGIC **(13-3)**	1	64	N/A	10/1/99		
CSR LOGIC **(13-4)**	1	65	N/A	10/1/99		
POLARITY CONTROL BLOCK**(13-5)**	1	66	N/A	9/9/99		
POLARITY CONTROL **(13-6)**	1	67	CCM018	9/23/99		
(13-7)			N/A			
POWER CONTROL BLOCK DIAGRAM**(14-1)**	1	68	N/A	9/23/99		
5 VOLT SECTION **(14-2)**	1	69	CCM026	9/9/99		
15 VOLT SECTION **(14-3_)**	1	70	CCM027	10/1/99		
Q AMP REFERENCE **(14-4)**	1	71	CCM004	1/25/99		

PART 1: SECTION, SUBSECTION DECODING

SECTION DAC/CSR name	SUBSECTION DAC/CSR	SUBSECTION NAME	section/subsection address	section decoding
Module Info	ID		xx00	zip logic
section 0	RESET		xx0F	zip logic
Sense Bias DAC	DAC 0	Sensor Bias A	xx1A	zip logic
section 1	DAC 1	Sensor Bias B	xx1B	zip logic
	DAC 2	Sensor Bias C	xx1C	zip logic
	DAC 3	Sensor Bias D	xx1D	zip logic
Squid Bias DAC	DAC 0	Squid Bias A	xx2A	zip logic
section 2	DAC 1	Squid Bias B	xx2B	zip logic
	DAC 2	Squid Bias C	xx2C	zip logic
	DAC 3	Squid Bias D	xx2D	zip logic
Squid Lock DAC	DAC 0	Squid Lock A	xx3A	zip logic
section 3	DAC 1	Squid Lock B	xx3B	zip logic
	DAC 2	Squid Lock C	xx3C	zip logic
	DAC 3	Squid Lock D	xx3D	zip logic
Squid Gain DAC	DAC 0	Squid Gain A	xx4A	zip logic
section 4	DAC 1	Squid Gain B	xx4B	zip logic
	DAC 2	Squid Gain C	xx4C	zip logic
	DAC 3	Squid Gain D	xx4D	zip logic
Squid Driver DAC	DAC 0	Squid Driver A	xx5A	zip logic
section 5	DAC 1	Squid Driver B	xx5B	zip logic
	DAC 2	Squid Driver C	xx5C	zip logic
	DAC 3	Squid Driver D	xx5D	zip logic
Q Driver DAC	DAC 0	Q O Driver	xx60	zip logic
section 6	DAC 1	Q I Driver	xx61	zip logic
	DAC 2	Test Voltage	xx62	zip logic
	DAC 3			zip logic
Q Bias DAC	DAC 0	Q O Bias	xx70	zip logic
section 7	DAC 1	Q I Bias	xx71	zip logic
	DAC 2	LED Bias	xx72	zip logic
	DAC 3	Zap Voltage	xx73	zip logic
unused				
section 8 to D				
CSR	CSR0	Sense Bias CSR	xxE0	zip logic
section E	CSR1	Squid CSR	xxE1	zip logic
	CSR2	Squid Driver CSR	xxE2	zip logic
	CSR3	LED CSR	xxE3	zip logic
	CSR4	Q CSR	xxE4	zip logic
	CSR5	CSR5	xxE5	zip logic
Test		FetHeater	xxFE	zip logic
section F		Test Pulse	xxFF	zip logic

The Module is decoded from bits 8 to12 of the address bus

The SECTIONS are decoded from bits 4 to 7 of the address bus

The SUBSECTIONS are decoded from bits 0 to 3 of the address bus

Outputs are from logic #1: zip_logic3.vhd

PART 2: CSR SUBSECTION OUTPUTS vs DATA BUSS BITS

Data Bit	Sense Bias CSR	Squid CSR	Squid Driver CSR	LED CSR	Q CSR	CSR5	Module ID	Data Bit
BD0	EXT_ENA_A	FB_C/O_SQ_A	**CHA_GAIN0**	WIDTH_0	***Q_O_GAIN0***	TRIG_ENA	Serial Number bit 0	BD0
BD1	EXT_ENA_B	FB_C/O_SQ_B	**CHA_GAIN1**	WIDTH_1	***Q_O_GAIN1***		Serial Number bit 1	BD1
BD2	EXT_ENA_C	FB_C/O_SQ_C	**CHA_GAIN2**	WIDTH_2	***Q_O_GAIN2***		Serial Number bit 2	BD2
BD3	EXT_ENA_D	FB_C/O_SQ_D	**CHA_POLARITY**	WIDTH_3	***Q_O_POLARITY***		Serial Number bit 3	BD3
BD4	***HEAT_PULSE_A***	***SQ_POL_A_-***	**CHB_GAIN0**	WIDTH_4	***Q_I_GAIN0***		Serial Number bit 4	BD4
BD5	***HEAT_PULSE_B***	***SQ_POL_B_-***	**CHB_GAIN1**	WIDTH_5	***Q_I_GAIN1***		Serial Number bit 5	BD5
BD6	***HEAT_PULSE_C***	***SQ_POL_C_-***	**CHB_GAIN2**	WIDTH_6	***Q_I_GAIN2***		Serial Number bit 6	BD6
BD7	***HEAT_PULSE_D***	***SQ_POL_D_-***	**CHB_POLARITY**	WIDTH_7	***Q_I_POLARITY***		Serial Number bit 7	BD7
BD8		TEST_ENA_A	**CHC_GAIN0**	RATE_0	Q_O_ENA		Board Version bit 0	BD8
BD9		TEST_ENA_B	**CHC_GAIN1**	RATE_1	Q_I_ENA		Board Version bit 1	BD9
BD10		TEST_ENA_C	**CHC_GAIN2**	RATE_2			Board Version bit 2	BD10
BD11		TEST_ENA_D	**CHC_POLARITY**	RATE_3			Board Version bit 3	BD11
BD12	***ZAP_ENA_A***	PRE_INT_MON_A	**CHD_GAIN0**	RATE_4	LED_1_ENA		Board Type bit 0	BD12
BD13	***ZAP_ENA_B***	PRE_INT_MON_B	**CHD_GAIN1**	RATE_5	LED_2_ENA		Board Type bit 1	BD13
BD14	***ZAP_ENA_C***	PRE_INT_MON_C	**CHD_GAIN2**	RATE_6	LED_CTRL_0		Board Type bit 2	BD14
BD15	***ZAP_ENA_D***	PRE_INT_MON_D	**CHD_POLARITY**	RATE_7	LED_CTRL_1		Board Type bit 3	BD15

Register outputs that are PLAIN text are outputs of the latching register: logic #2: csr_logic3.vhd

Register outputs that are BOLD text are outputs that are pulses from logic #3: ziprelay2.vhd

Register outputs that are bold and italized text are outputs that are pulses from logic #4: chargeamps.vhd

Module Info ID bits are read only. These are shorts to +VCC or GND to set the condition

PART 3: GAIN AND POLARITY DECODING MATRIZ

Data bits to the DACs set the output voltage level

DAC output voltage calculation:
Vout=Vrefl +((Vrefh-Vrefl) * N)/4096
N= is digital code in decimal

POLARITY	2	1	0	GAIN
0	0	0	0	1
0	0	0	1	1.43
0	0	1	0	2
0	0	1	1	5
0	1	0	0	10
0	1	0	1	14.3
0	1	1	0	20
0	1	1	1	50
1	0	0	0	-1
1	0	0	1	-1.43
1	0	1	0	-2
1	0	1	1	-5
1	1	0	0	-10
1	1	0	1	-14.3
1	1	1	0	-20
1	1	1	1	-50

NOTE:
ALL SIGNAL NAMES ARE HIGH TRUE

LED_CTRL_1	LED_CTRL_0	
0	0	OFF
0	1	SINGLE
1	0	MULTI
1	1	ON

PART 5: Module Address decode vs. slot number

Address		Slot Number
xxx0 0000 xxxx xxxx	00xx	0
xxx0 0001 xxxx xxxx	01xx	1
xxx0 0010 xxxx xxxx	02xx	2
xxx0 0011 xxxx xxxx	03xx	3
xxx0 0100 xxxx xxxx	04xx	4
xxx0 0101 xxxx xxxx	05xx	5
xxx0 0110 xxxx xxxx	06xx	6
xxx0 0111 xxxx xxxx	07xx	7
xxx0 1000 xxxx xxxx	08xx	8
xxx0 1001 xxxx xxxx	09xx	9
xxx0 1010 xxxx xxxx	0Axx	10
xxx0 1011 xxxx xxxx	0Bxx	11
xxx0 1100 xxxx xxxx	0Cxx	12
xxx0 1101 xxxx xxxx	0Dxx	13
xxx0 1110 xxxx xxxx	0Exx	14
xxx0 1111 xxxx xxxx	0Fxx	15
xxx1 0000 xxxx xxxx	10xx	16
xxx1 0001 xxxx xxxx	11xx	17
xxx1 0020 xxxx xxxx	12xx	18
xxx1 0011 xxxx xxxx	13xx	19
xxx1 0100 xxxx xxxx	14xx	20
xxx1 0101 xxxx xxxx	15xx	21

FetHeater creates a 30 second pulse

PART 4: CHIPS AND DECODED OUTPUTS TO ZIP BOARD CIRCUITS

These are the names of the chips, the project name that the code is found in and the outputs by name that they decode for the ZIP board

project name:chargeamps	project name: zipchips	project name:ziprelay2	project name: addrlogic
CHARGE AMP	CSR_LOGIC3	ZIPRELAY2	ZIP_LOGIC3
qo_gain_1	qo_ena	chA_gain_1	moduleid
qo_gain_10	qi_ena	chA_gain_10	sense_bias_dac
qo_gain_1_143	led_1_ena	chA_gain_1_143	squid_bias_dac
qo_gain_2_5	led_2_ena	chA_gain_2_5	squid_lock_dac
qo_gain_1_2	ext_ena_A	chA_gain_1_2	squid_gain_dac
qo_gain_143_5	ext_ena_B	chA_gain_143_5	squid_driver_dac
qo_pol_pos	ext_ena_C	chA_pol_pos	q_driver_dac
qo_pol_neg	ext_ena_D	chA_pol_neg	q_bias_dac
qi_gain_1	fb_c/o_sq_A	chB_gain_1	subdac
qi_gain_10	fb_c/o_sq_B	chB_gain_10	sense_bias_csr
qi_gain_1_143	fb_c/o_sq_C	chB_gain_1_143	squid_csr
qi_gain_2_5	fb_c/o_sq_D	chB_gain_2_5	squid_driver_csr
qi_gain_1_2	test_ena_A	chB_gain_1_2	led_csr
qi_gain_143_5	test_ena_B	chB_gain_143_5	q_csr
qi_pol_pos	test_ena_C	chB_pol_pos	csr5
qi_pol_neg	test_ena_D	chB_pol_neg	rw
zap_ena_A	pre_int_mon_A	chC_gain_1	rst
zap_ena_B	pre_int_mon_B	chC_gain_10	testpulse
zap_ena_C	pre_int_mon_C	chC_gain_1_143	buffer_ena
zap_ena_D	pre_int_mon_D	chC_gain_2_5	buffer_write
heat_pulse_A	trig_ena	chC_gain_1_2	moduleselect
heat_pulse_B	led_pulse_out	chC_gain_143_5	ps1_on
heat_pulse_C	clockena	chC_pol_pos	ps2_on
heat_pulse_D		chC_pol_neg	ps3_on
sq_pol_A_pos	READ ONLY INFO	chD_gain_1	heat_fet
sq_pol_A_neg	module configuration	chD_gain_10	poweron
sq_pol_B_pos		chD_gain_1_143	clock_ena
sq_pol_B_neg		chD_gain_2_5	
sq_pol_C_pos		chD_gain_1_2	
sq_pol_C_neg		chD_gain_143_5	
sq_pol_D_pos		chD_pol_pos	
sq_pol_D_neg		chD_pol_neg	
clockena		moduleaddr	
chipselect	chipselect	clockena	
		chipselect	

CONTROL INPUTS FROM ZIP_LOGIC

sense_bias_csr	sense_bias_csr	squid_driver_csr	
squid_csr	squid_csr	moduleselect	
q_csr	q_csr		
	csr5		
	led_csr		
	moduleid		
testpulse	testpulse		
poweron	poweron	poweron	

CONTROL INPUTS FROM CSR_LOGIC3

trig_ena			

CONTROL INPUTS FROM OTHER SOURCES

read	read	read	read
write	write	write	write
bd(15 dowto 0)	bd(15 dowto 0)	bd(15 dowto 0)	slot(4 downto 0)
trigplus_minus	trigplus_minus		addr(15 downto 0)
powerup	powerup	powerup	powerup
			pwr_monitor
clock	clock	clock	clock
			heat_fet_init

This file is named Backplane Pinout.xls
and can be found at
Network Neighborhood\Entire Network\Microsoft Windows Network\Fnal\Ppdserver1\ETT.PPD\PROJECTS\Ett_ES\CDMS\crates\backplane\user manual

50 Pin D Connector
Detector I/O
Slots 1 thru 9, and
12 thru 20
[Crate Front View]
P/J1

Pin #		Pin #		Pin #	
50	Qi Feedback			17	FEGND
		33	FEGND		
49	FET Temp+			16	Qi Drain
		32	FEGND		
48	FEGND			15	Qi Bias
		31	Qi Source		
47	FEGND			14	FEGND
		30	Qo Feedback		
46	FET Heater-			13	FEGND
		29	FEGND		
45	FET Heater +			12	Qo Drain
		28	FEGND		
44	FEGND			11	Qo Bias
		27	Qo Source		
43	FEGND			10	FEGND
		26	LED 2		
42	LED 1			9	FEGND
		25	FEGND		
41	FBout C			8	SQUID Bias C
		24	FEGND		
40	FEGND			7	QET Bias C
		23	SQUID Bias D		
39	FEGND			6	FEGND
		22	FBoutD		
38	QET Bias D			5	FEGND
		21	FEGND		
37	FBout A			4	SQUID Bias A
		20	FEGND		
36	FEGND			3	QET Bias A
		19	SQUID Bias B		
35	QET Bias B			2	FBout B
		18	FEGND		
34	FEGND			1	FEGND

The backplane connector is
part # AMP 205211-2

The mating connector on the
module is part # AMP 745355-4

48 Pin DIN Connector
Crate Power
Slots 1 thru 21
[Crate Front View]
P/J2

Pin #	Row A	Row B	Row C
1	FEGND	Aux Heater Power+	FEGND
2	FEGND	Aux Heater Power-	FEGND
3	FE +15	FE +15	FE +15
4	FEGND	FEGND	FEGND
5	FE -15	FE -15	FE -15
6	FEGND	FEGND	FEGND
7	FEGND	FEGND	FEGND
8	AGND	AGND	AGND
9	A15+	A15+	A15+
10	AGND	AGND	AGND
11	A15-	A15-	A15-
12	AGND	AGND	AGND
13	10Hz+	AGND	VARIABLE+
14	10Hz-	AGND	VARIABLE-
15	1kHz+	**Spare**	Trig+
16	1kHz-	**Spare**	Trig-

NOTES;

1	Revision 10/23/97 changed 48 pin contacts C13,C14,C15 and C16
2	Revised view of 50 Pin and 25 Pin connectors to show proper 0rientation on 4/7/99
3	10 Layer Backplane

The backplane connector is
part # AMP 535034-4

The mating connector on the
module is part # AMP 650948-5

25 Pin D Connector
Detector Output
Slots 1 thru 9, and
12 thru 20
[Crate Front View]
P/J3

Pin #			Pin #
			13
25			
			12
24			
			11
23			
			10
22	AGND		
		FET T SENSE	9
21	AGND		
		LED Vmon	8
20	AGND		
		LED Imon	7
19	AGND		
		SQUID D	6
18	AGND		
		SQUID C	5
17	AGND		
		SQUID B	4
16	AGND		
		SQUID A	3
15	AGND		
		Qo Out	2
14	AGND		
		Qi Out	1

The backplane connector is
part # AMP 207463-1

The mating connector on the
module is part # AMP 745353-4

Slots 1 thru 20
Detector n
(n = 1 through 18)
[Crate Front View]
P/J4

Pin #	Row A	Row B	Row C
1	5 Volts	5 Volts	5 Volts
2	5 Volts	5 Volts	5 Volts
3	5 Volts	5 Volts	5 Volts
4	5 Volts	5 Volts	5 Volts
5	DGND	DGND	DGND
6	D0	DGND	D8
7	D1	DGND	D9
8	D2	DGND	D10
9	D3	DGND	D11
10	D4	DGND	D12
11	D5	DGND	D13
12	D6	DGND	D14
13	D7	DGND	D15
14	DGND	DGND	DGND
15	A 0	DGND	A 8
16	A 1	DGND	A 9
17	A 2	DGND	A 10
18	A 3	DGND	A 11
19	A 4	DGND	A 12
20	A 5	DGND	A 13
21	A 6	DGND	A 14
22	A 7	DGND	A 15
23	DGND	DGND	DGND
24	Read	DGND	Write
25	DGND	DGND	DGND
26	5 Volts	5 Volts	5 Volts
27	5 Volts	5 Volts	5 Volts
28	5 Volts	5 Volts	5 Volts
29	Local Address A4	Local Address A3	5 Volts
30	Local Address A2	Local Address A1	Local Address A0
31	DGND	DGND	DGND
32	Bussed Spare 1	Bussed Spare 2	Sync out

The backplane connector is
part # AMP 535032-4

The mating connector on the
module is part # AMP 650947-5

Slot 21
GPIB Controller
[Crate Front View]
P/J4

Row A	Row B	Row C
spare	5 Volts	Trig1-
spare	5 Volts	Trig1+
5 Volts	5 Volts	spare
5 Volts	5 Volts	spare
DGND	DGND	DGND
D0	DGND	D8
D1	DGND	D9
D2	DGND	D10
D3	DGND	D11
D4	DGND	D12
D5	DGND	D13
D6	DGND	D14
D7	DGND	D15
DGND	DGND	DGND
A 0	DGND	A 8
A 1	DGND	A 9
A 2	DGND	A 10
A 3	DGND	A 11
A 4	DGND	A 12
A 5	DGND	A 13
A 6	DGND	A 14
A 7	DGND	A 15
DGND	DGND	DGND
Read	DGND	Write
DGND	DGND	DGND
5 Volts	5 Volts	5 Volts
5 Volts	5 Volts	5 Volts
5 Volts	5 Volts	5 Volts
5 Volts	5 Volts	5 Volts
DGND	DGND	DGND
Bussed Spare 1	Bussed Spare 2	Sync out

SYMBOL LEDGEND

AGND — ANALOG GROUND PLANE

FEGND — FRONT END GROUND PLANE

GND — DIGITAL GROUND PLANE

V15P V15PFE +10R +5REF +5QD +5Q VCC

CONNECTIONS TO POWER PLANES

V15N V15NFE -10R -5REF -5QD -5Q

INTRA PAGE CONNECTION

EXTERNAL PAGE CONNECTION OUTPUT

EXTERNAL PAGE CONNECTION INPUT

BACKPLANE CONNECTOR PIN

BLOCK — INPUT PIN — OUTPUT PIN

SYMBOL

PAGE CONNECTOR DESIGNATIONS:

ANALOG CONTROL INPUT — ANALOG CONTROL OUTPUT

ANALOG SIGNAL INPUT — ANALOG SIGNAL OUTPUT

3-3(2C)

SECTION PAGE COORDINATES

REVISIONS

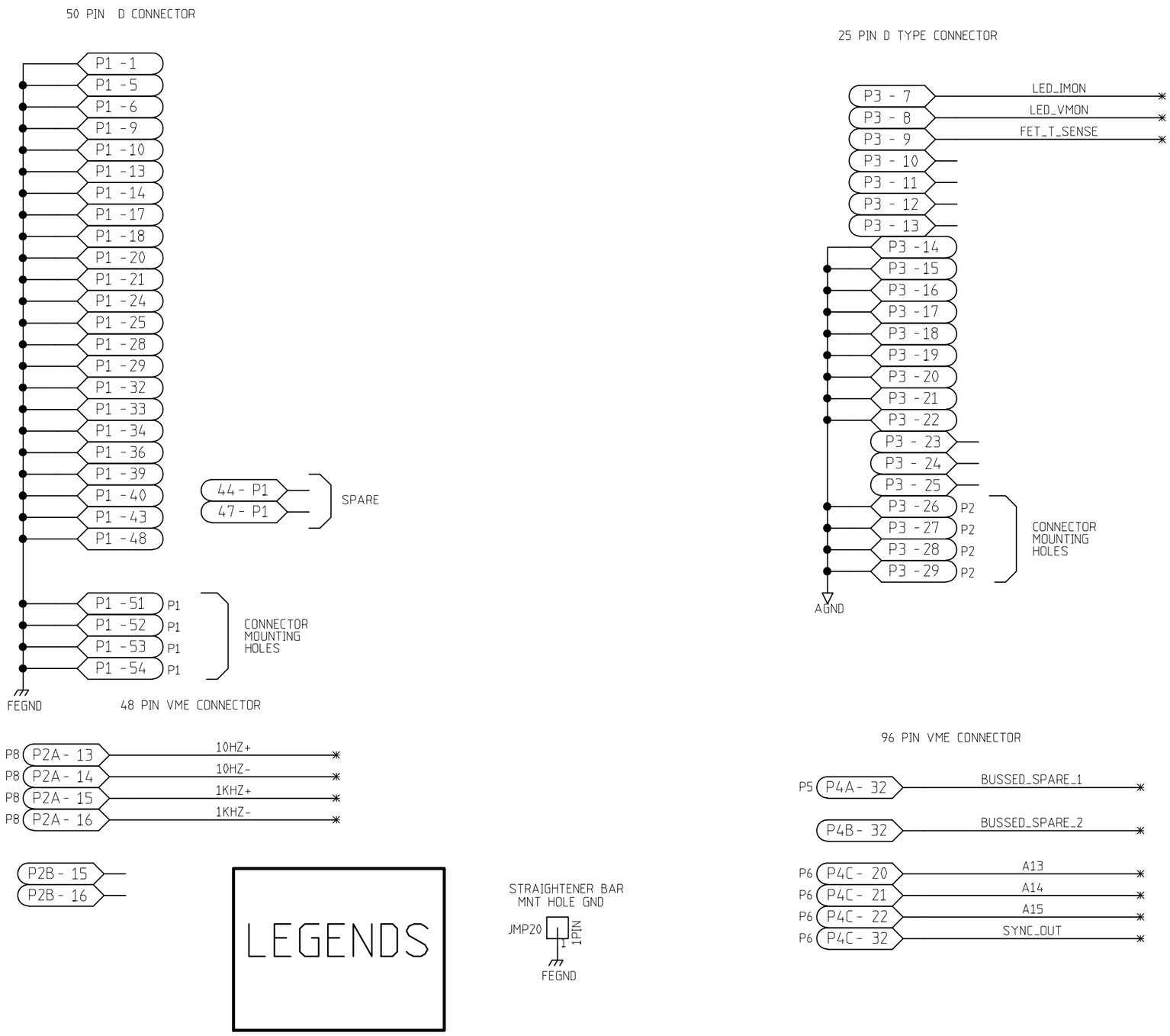
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/21/98
DRAWN	BRUCE MERKEL	12/21/98
CHECKED	TOM CRENNA	12/21/98
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE DRAWING
SYMBOL LEGEND

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE | SHEET COVER PAGE



REVISIONS

REV	DESCRIPTION	DATE	APPROVED

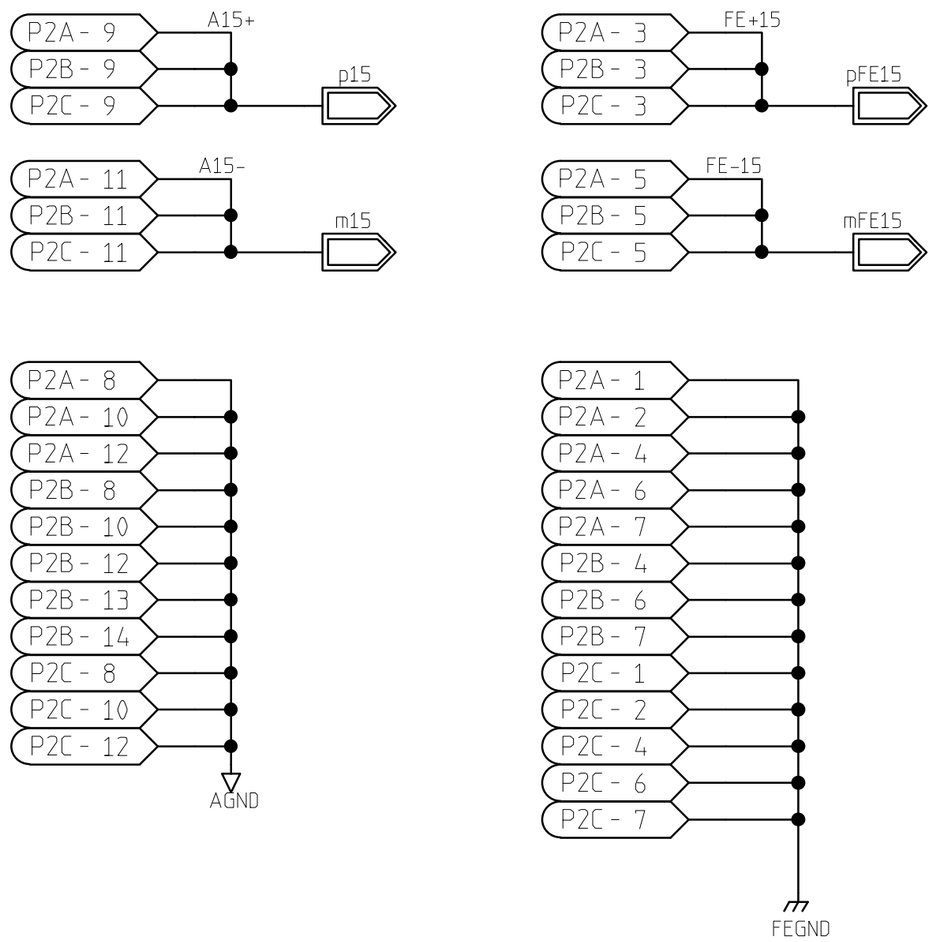
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	12/9/98
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
MISC. CONNECTORS

SIZE	FSCM NO.	DWG. NO.	REV
B			1

SCALE | SHEET 1-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	NAME CHANGE TO MATCH BACKPLANE	7/27/99	BDM



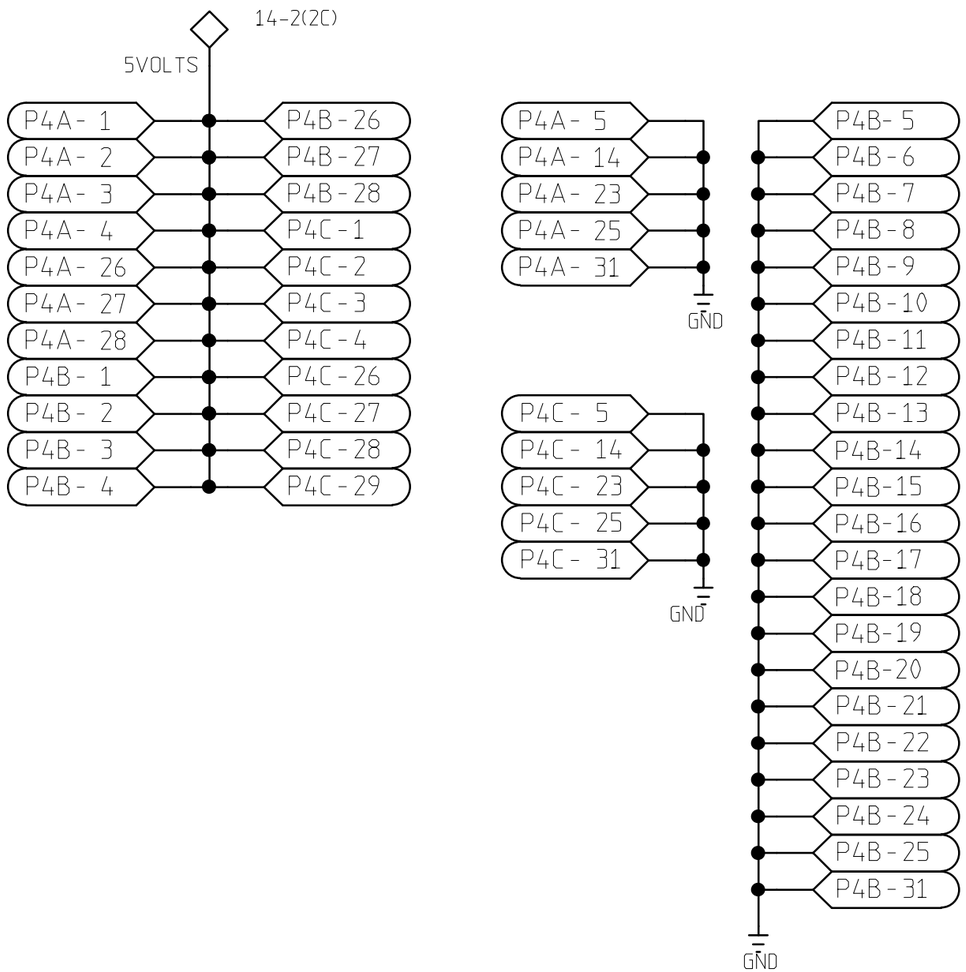
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	10/8/98
DRAWN	BRUCE MERKEL	10/8/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
P2 BACKPLANE POWER CONNECTION

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE		SHEET 1-2

P4
(96 PIN CONNECTOR)



REVISIONS

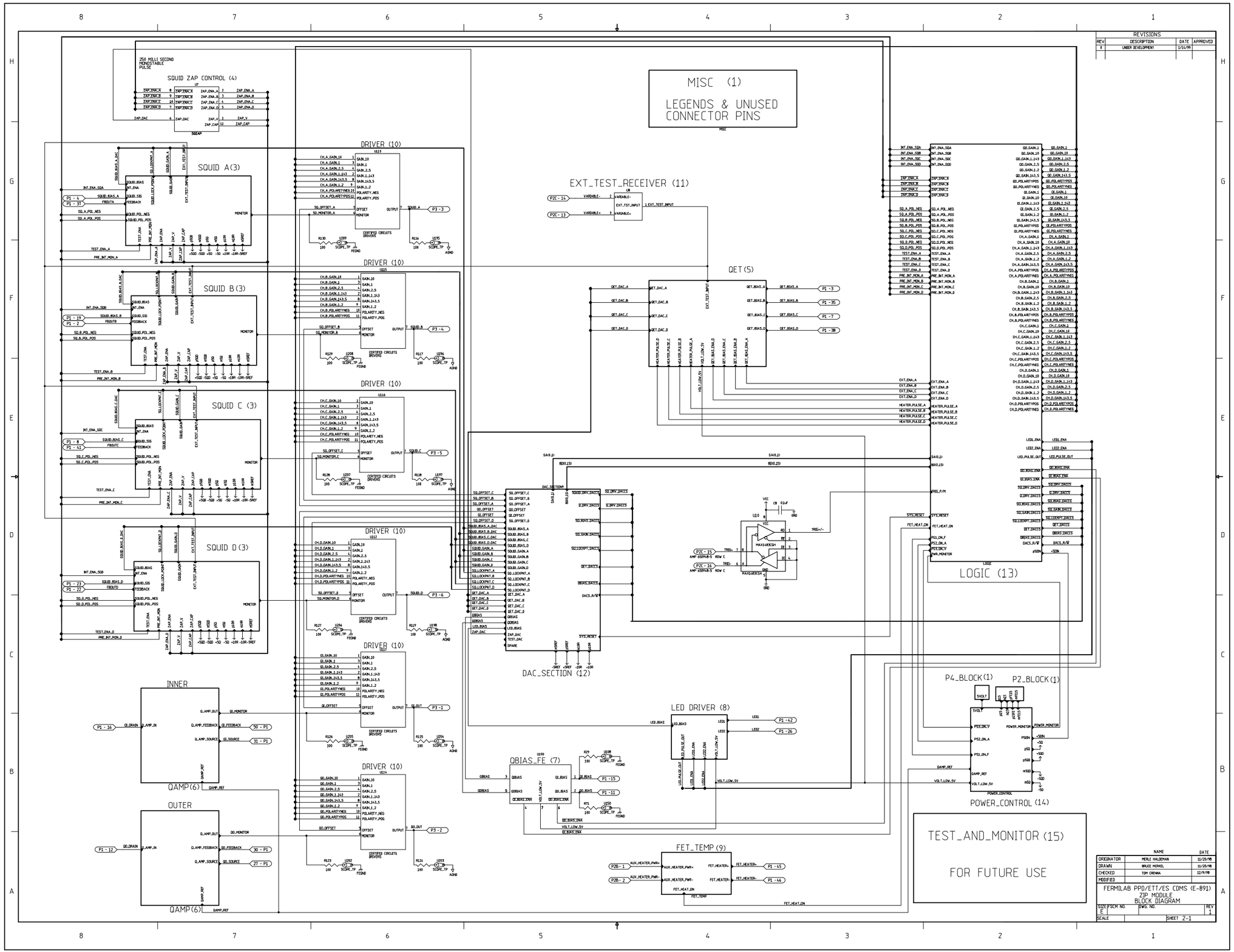
REV	DESCRIPTION	DATE	APPROVED
0	NAME CHANGED TO MATCH BACKPLANE	7/27/99	BDM

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	10/8/98
DRAWN	BRUCE MERKEL	10/8/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

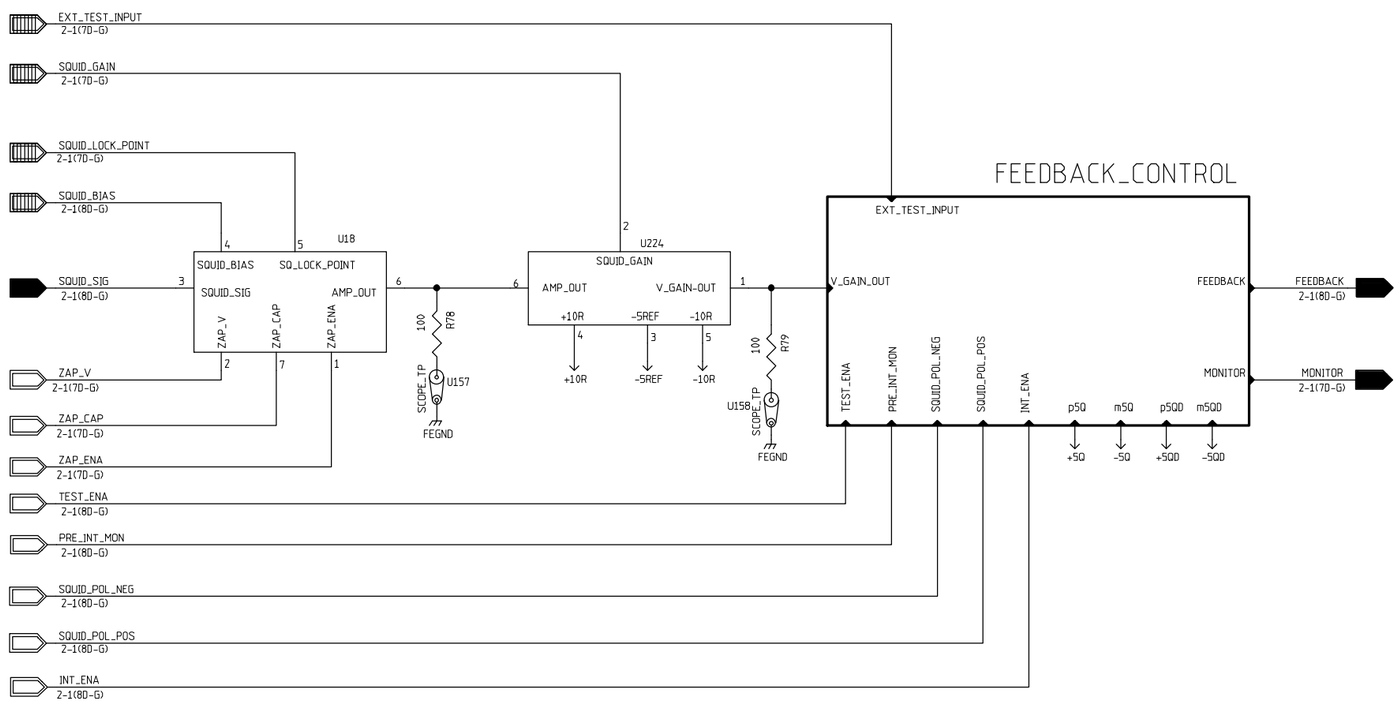
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
P4 BACKPLANE POWER CONNECTION

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE | SHEET 1-3


MISC (1)
LEGENDS & UNUSED CONNECTOR PINS
SQUID ZAP CONTROL (4)
250 MILLI SECOND MONOSTABLE PULSE
SQUID A(3)
SQUID B(3)
SQUID C (3)
SQUID D(3)
DRIVER (10)
EXT_TEST_RECEIVER (11)
QET(5)
LOGIC (13)
DAC_SECTION (12)
INNER
OUTER
QAMP(6)
LED DRIVER (8)
QBIAS_FE (7)
FET_TEMP (9)
P4_BLOCK(1)
P2_BLOCK(1)
POWER_CONTROL (14)
TEST_AND_MONITOR (15)
FOR FUTURE USE
REVISIONS
REV | DESCRIPTION | DATE | APPROVED
1 | UNDER DEVELOPMENT | 1/16/99
NAME | DATE
ORIGINATOR | MERLE HALDEMAN | 11/20/98
DRAWN | BRUCE MERKEL | 11/20/98
CHECKED | TOM CHERNA | 12/9/98
MODIFIED
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
BLOCK DIAGRAM
SIZE | FSCM NO. | DWG. NO. | REV
E | 1
SCALE | SHEET 2-1

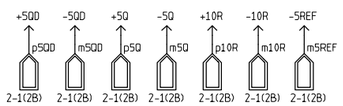
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SQUID FRONT END

SQUID VARIABLE GAIN AMPLIFIER

SQUID FEEDBACK CONTROL

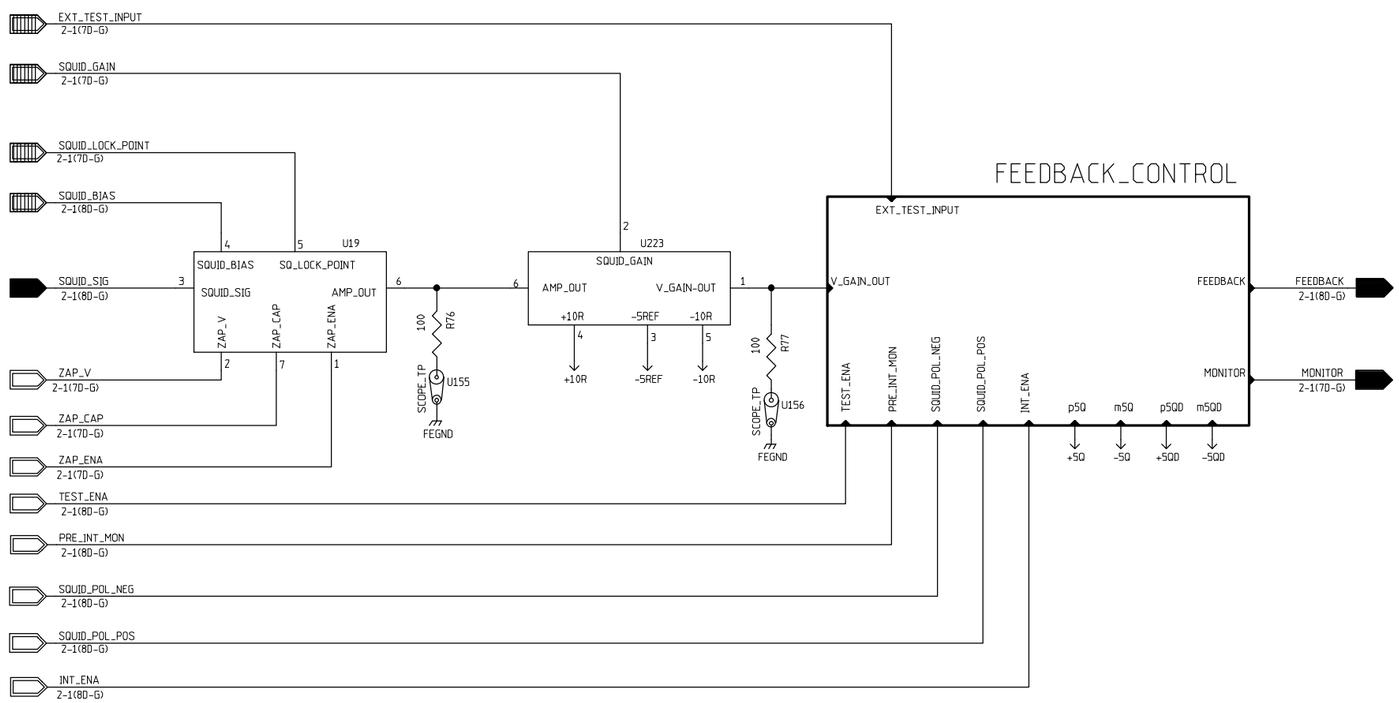


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-1	

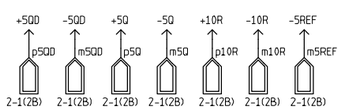
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SQUID FRONT END

SQUID VARIABLE GAIN AMPLIFIER

SQUID FEEDBACK CONTROL

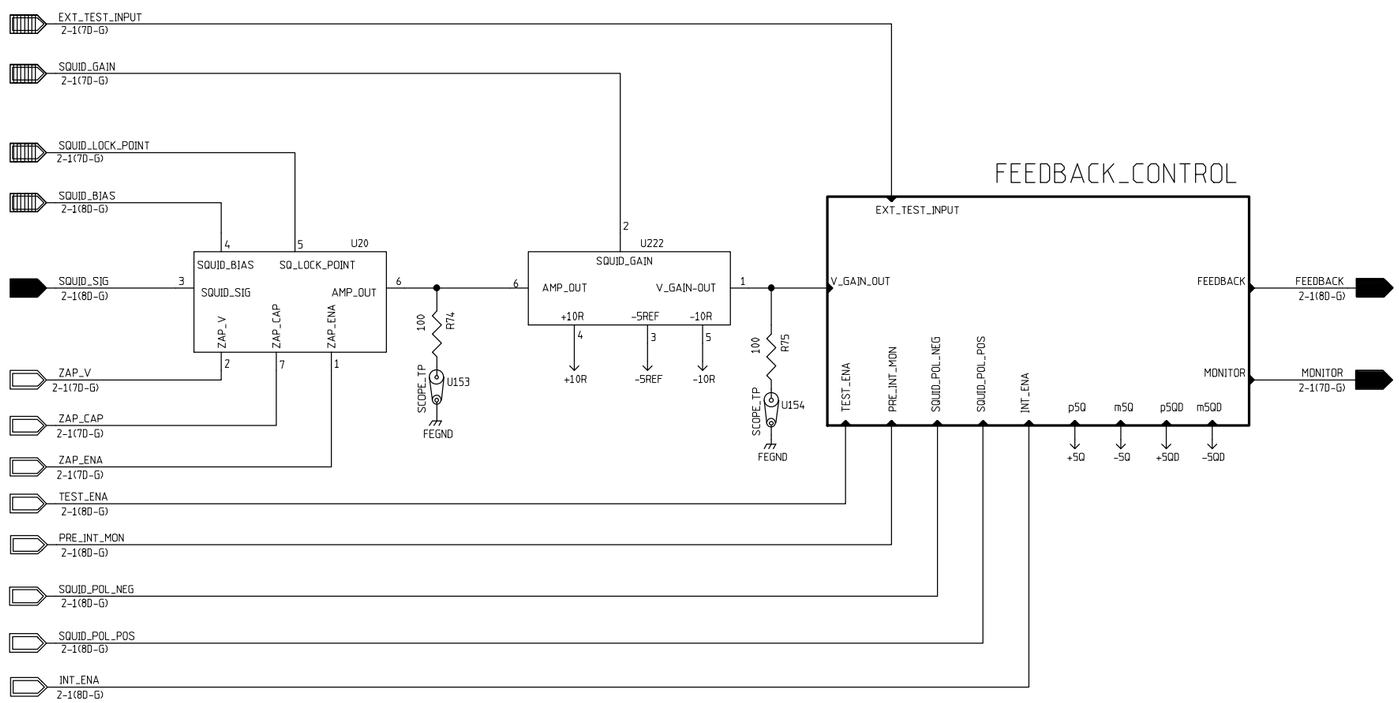


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-1	

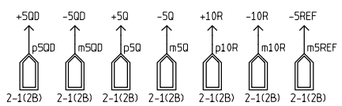
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SQUID FRONT END

SQUID VARIABLE GAIN AMPLIFIER

SQUID FEEDBACK CONTROL

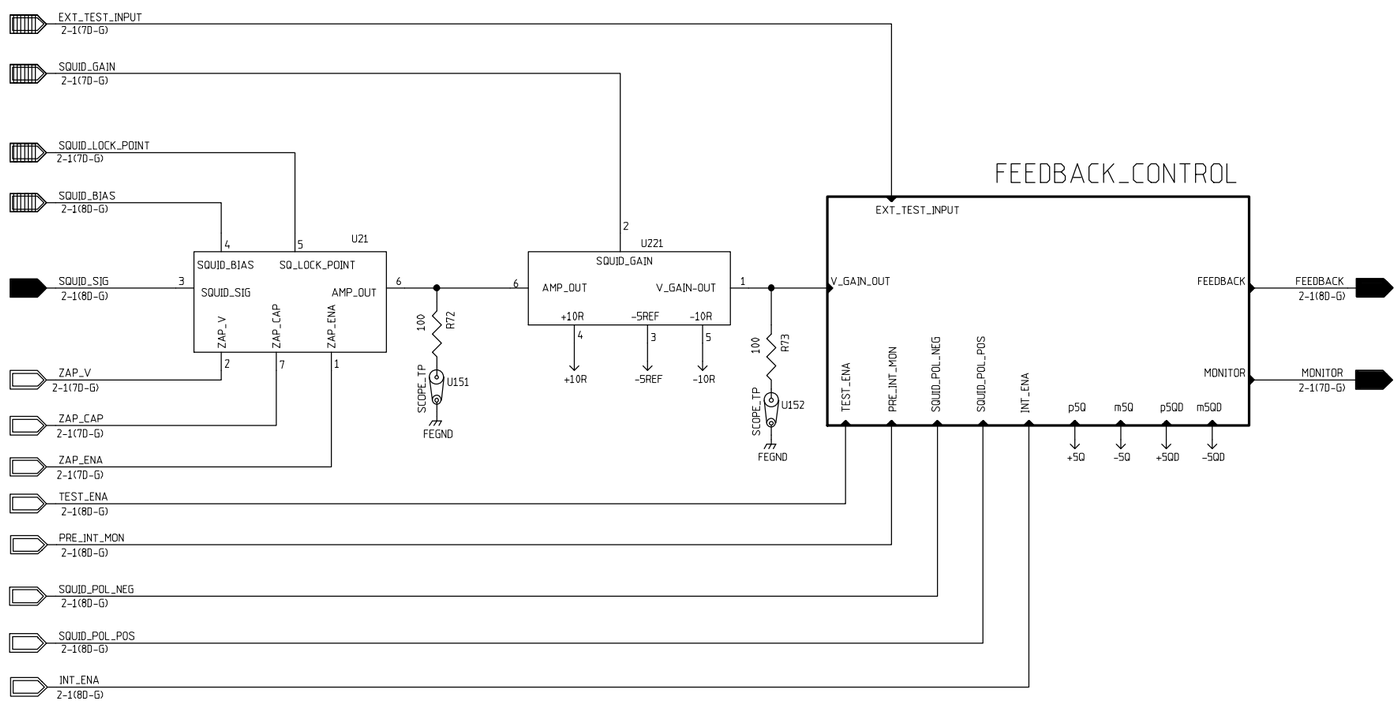


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-1	

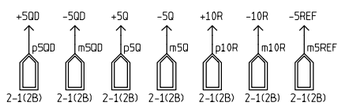
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SQUID FRONT END

SQUID VARIABLE GAIN AMPLIFIER

SQUID FEEDBACK CONTROL



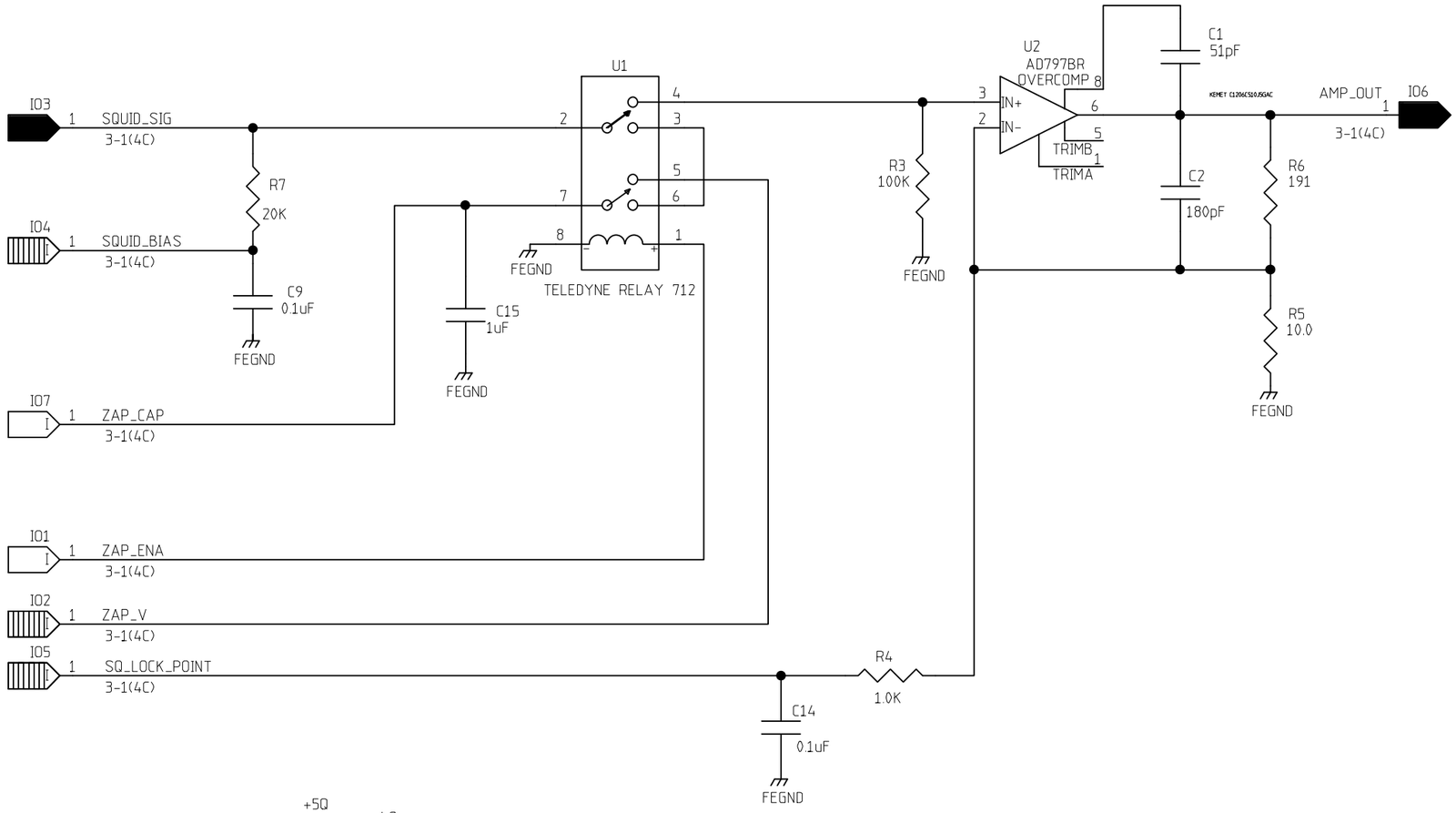
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

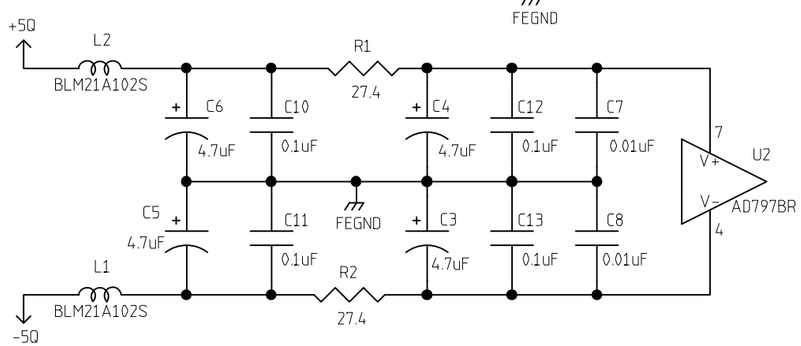
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

RELAY SHOWN IN
DEENERGIZED STATE



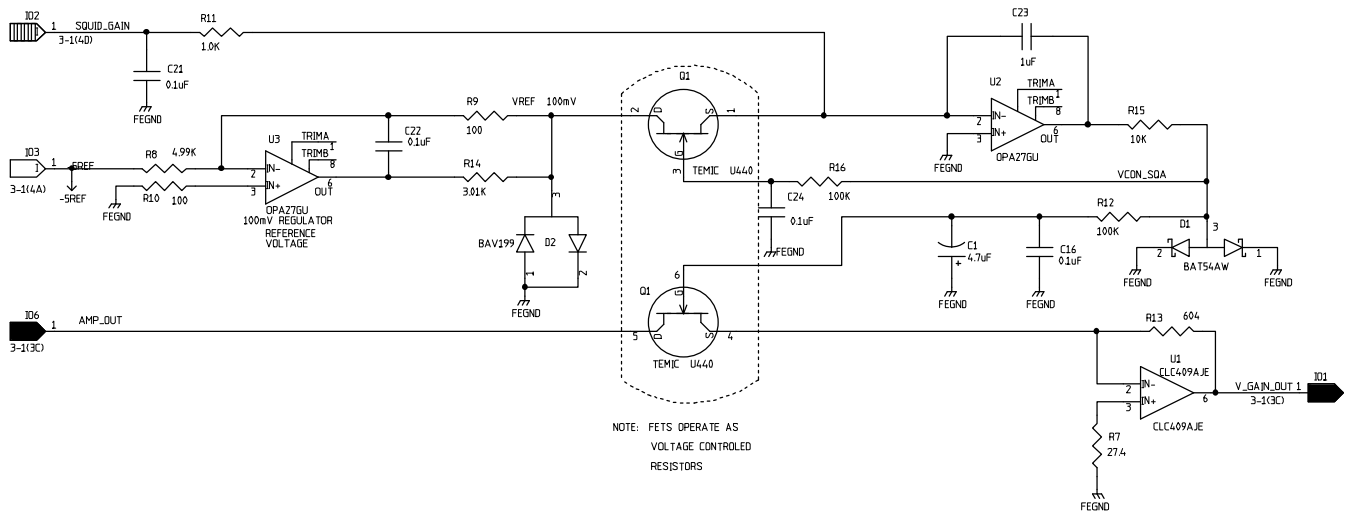


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/11/98
DRAWN	BRUCE MERKEL	11/11/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 3-2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	MODIFIED TO REMOVE OSCILLATIONS	5/19/99	BDM



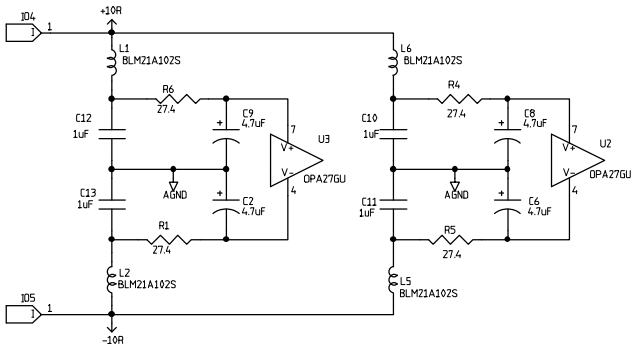
NOTE: FETS OPERATE AS VOLTAGE CONTROLED RESISTORS

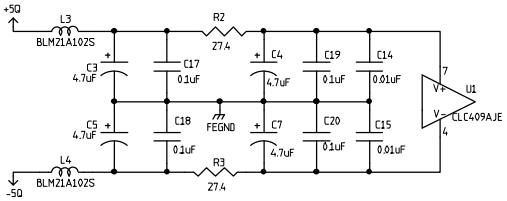
VARIABLE GAIN AMPLIFIER

$GAIN = R13 \times \frac{GVC}{100}$

GCV = GAIN_CONTROL_VOLTAGE IN VOLTS

R13 IN OHMS

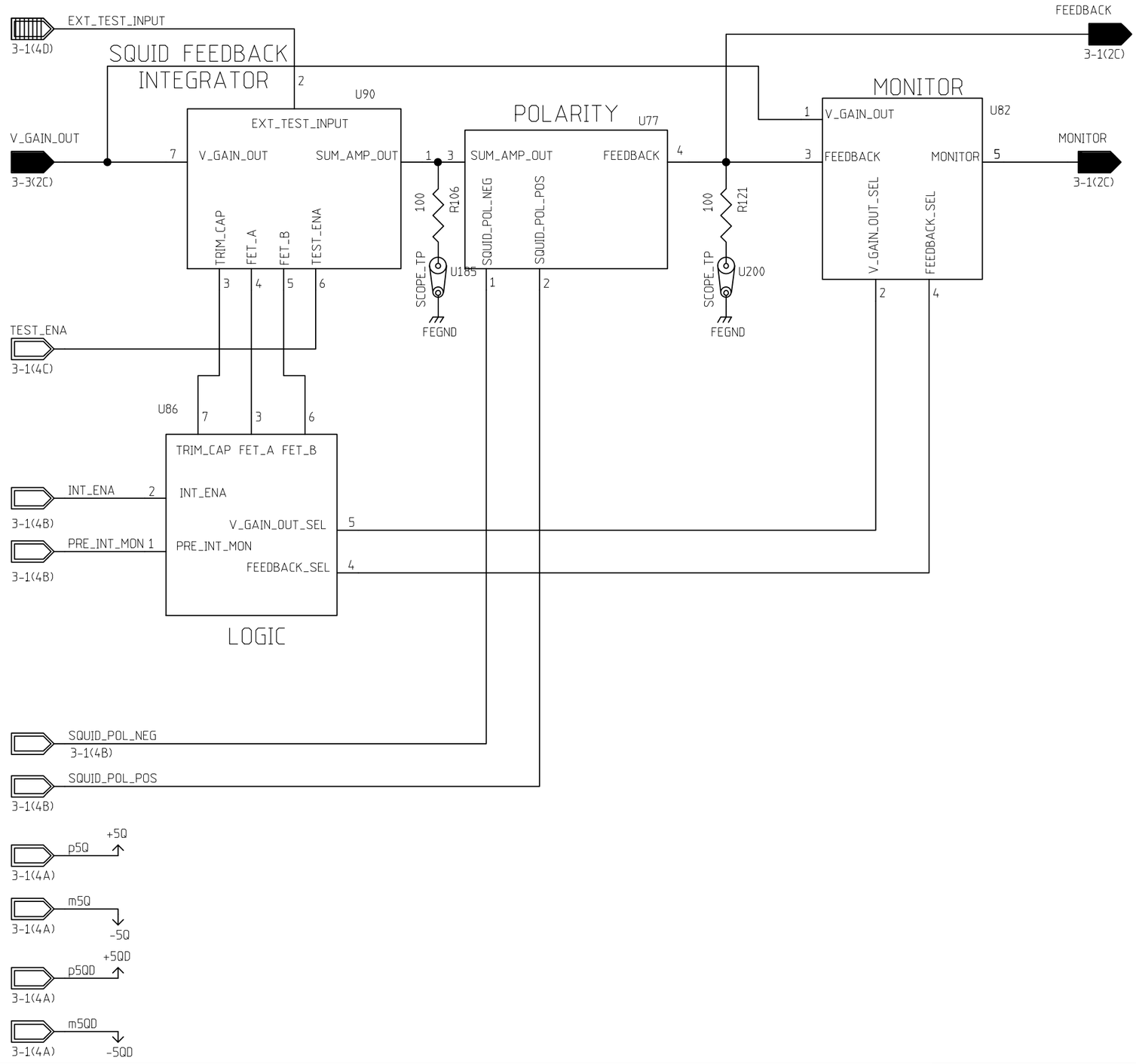




	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID VARIABLE GAIN AMP

SIZE	FSCM NO.	DWG. NO.	REV
C			
SCALE		SHEET 3-3	

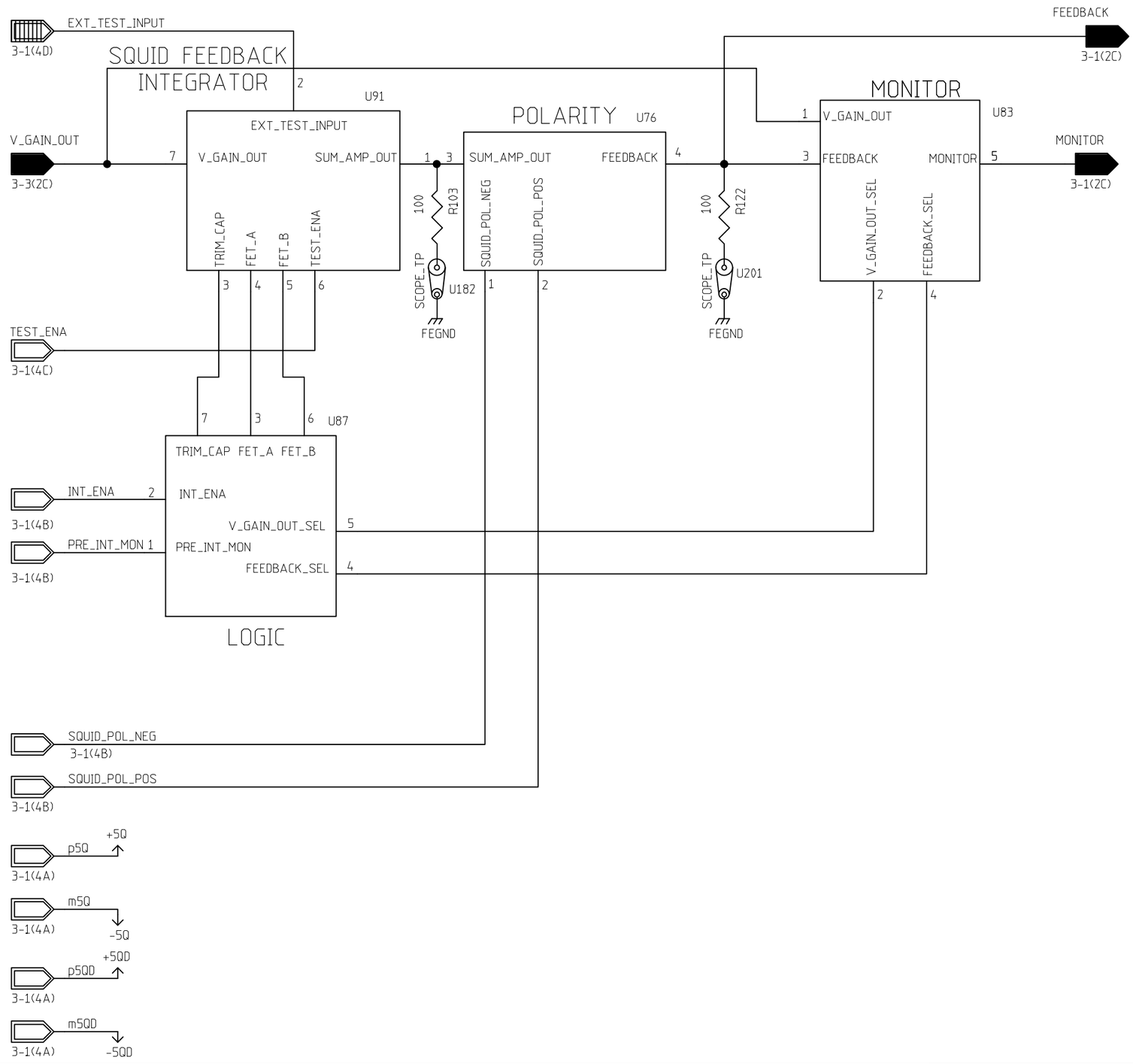


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-4	

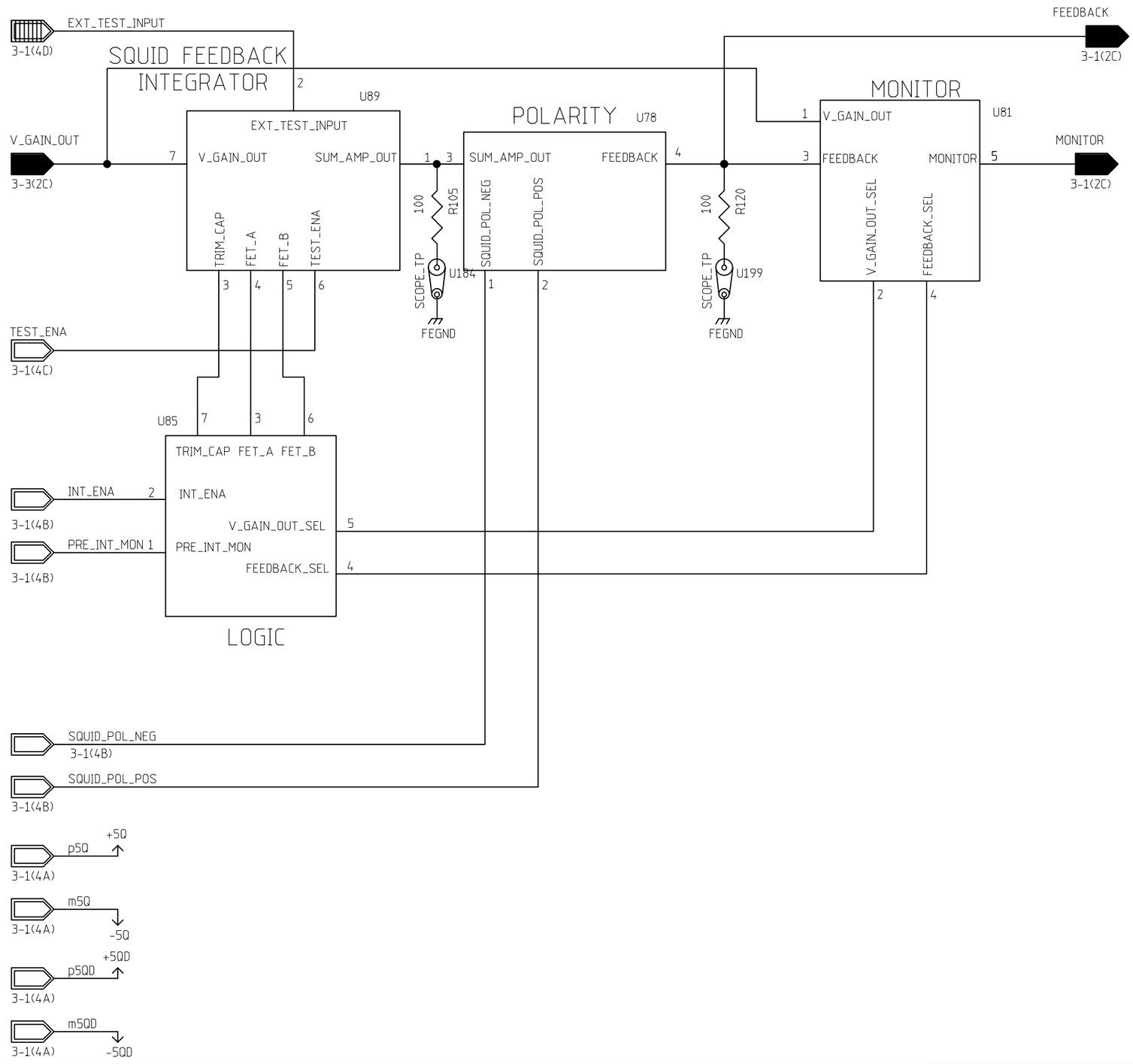


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-4	

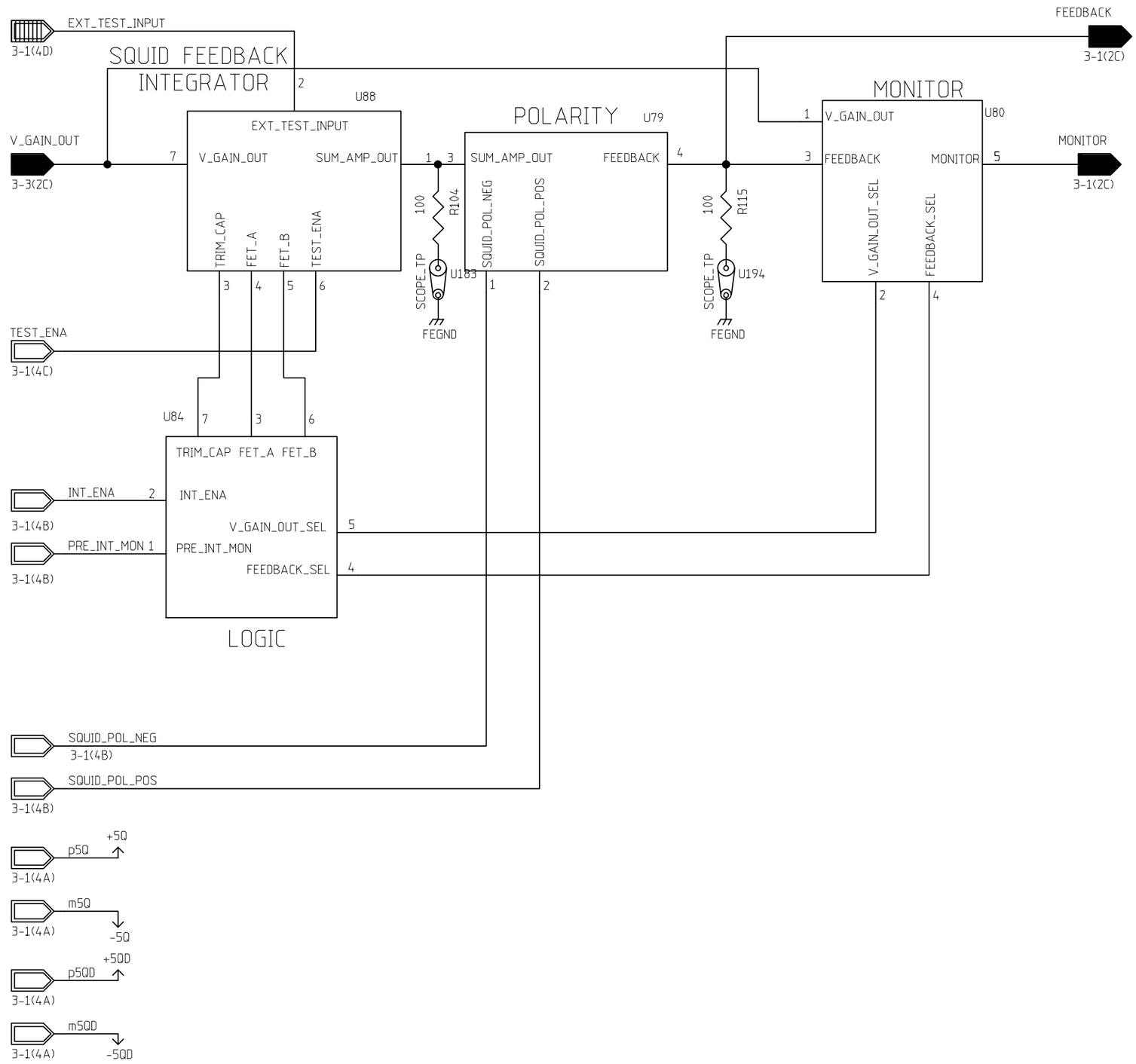


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-4	



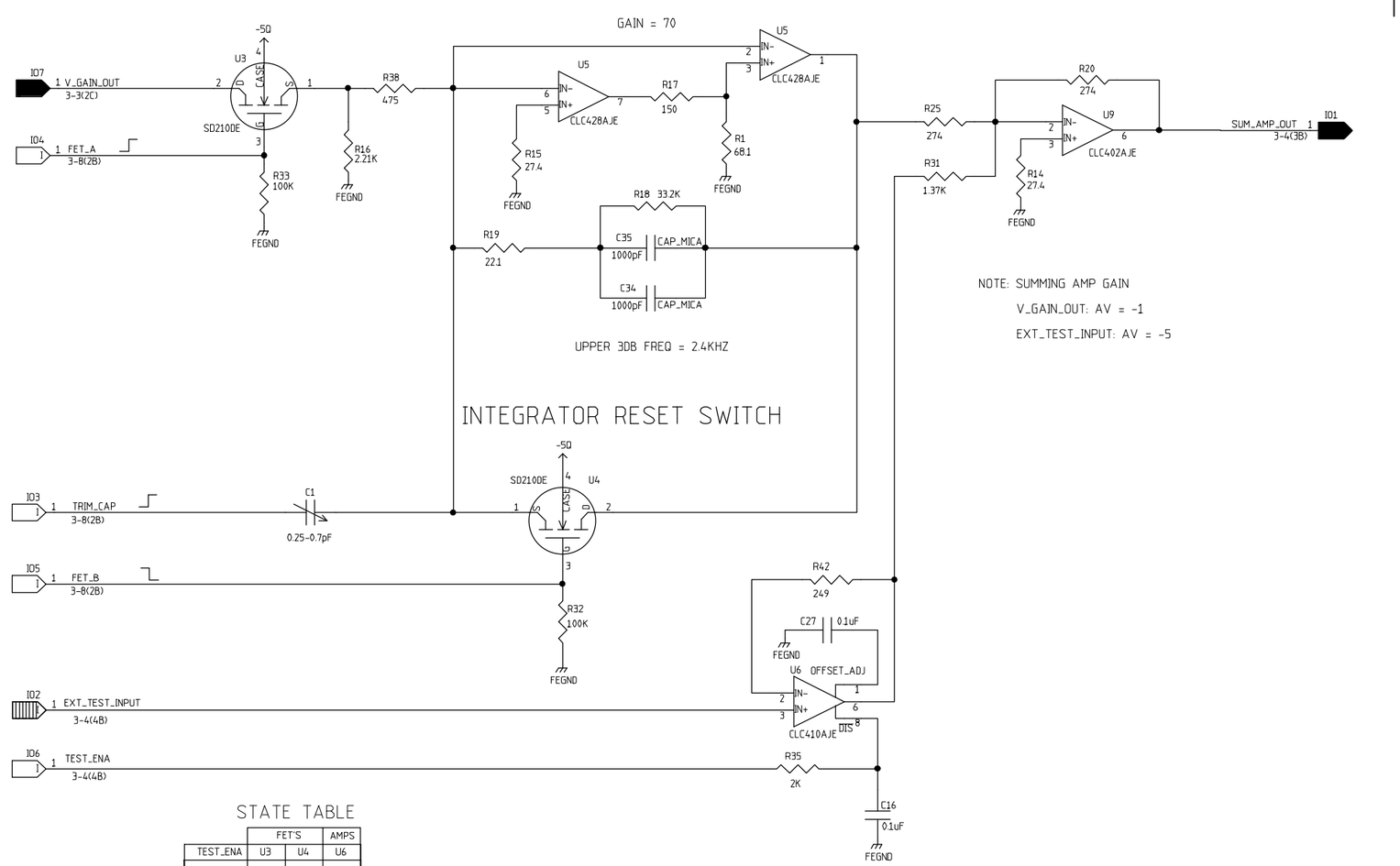
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-4	

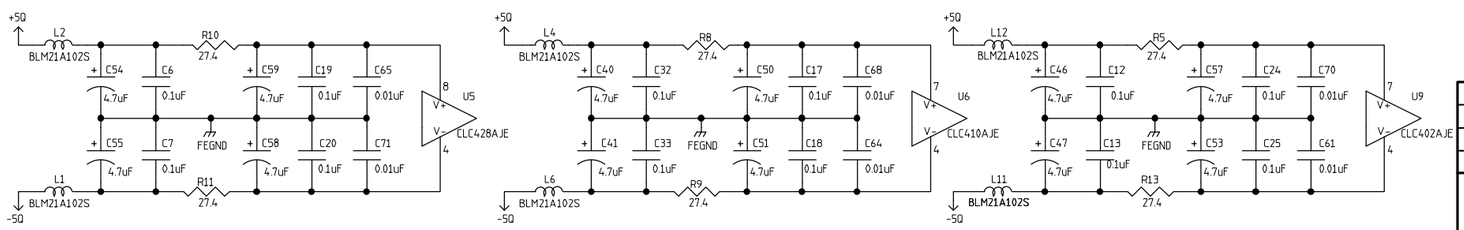
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	UPDATED FOR VERSION 1	9/17/99	



STATE TABLE

	FET'S		AMPS
TEST_ENA	U3	U4	U6
LOW	O	C	E
HI	C	O	D

O = OPEN C = CLOSED
E = ENABLE D = DISABLE



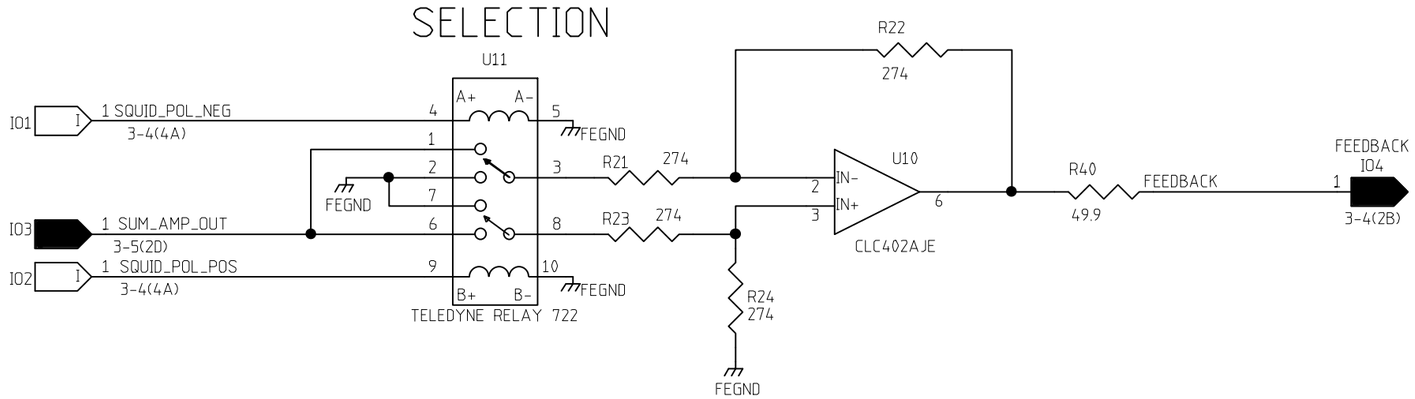
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

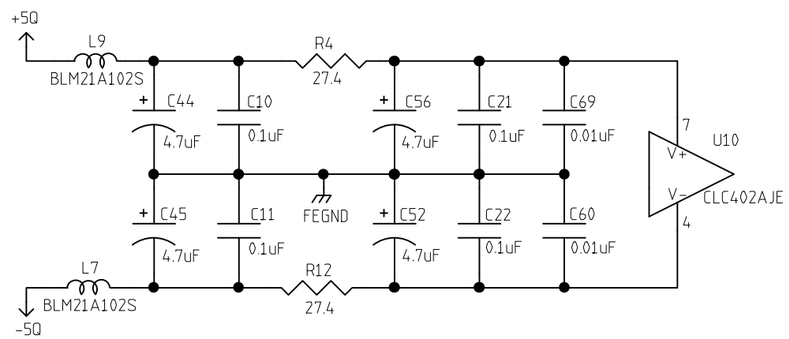
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK INTEGRATOR

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 3-5	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POLARITY SELECTION





	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

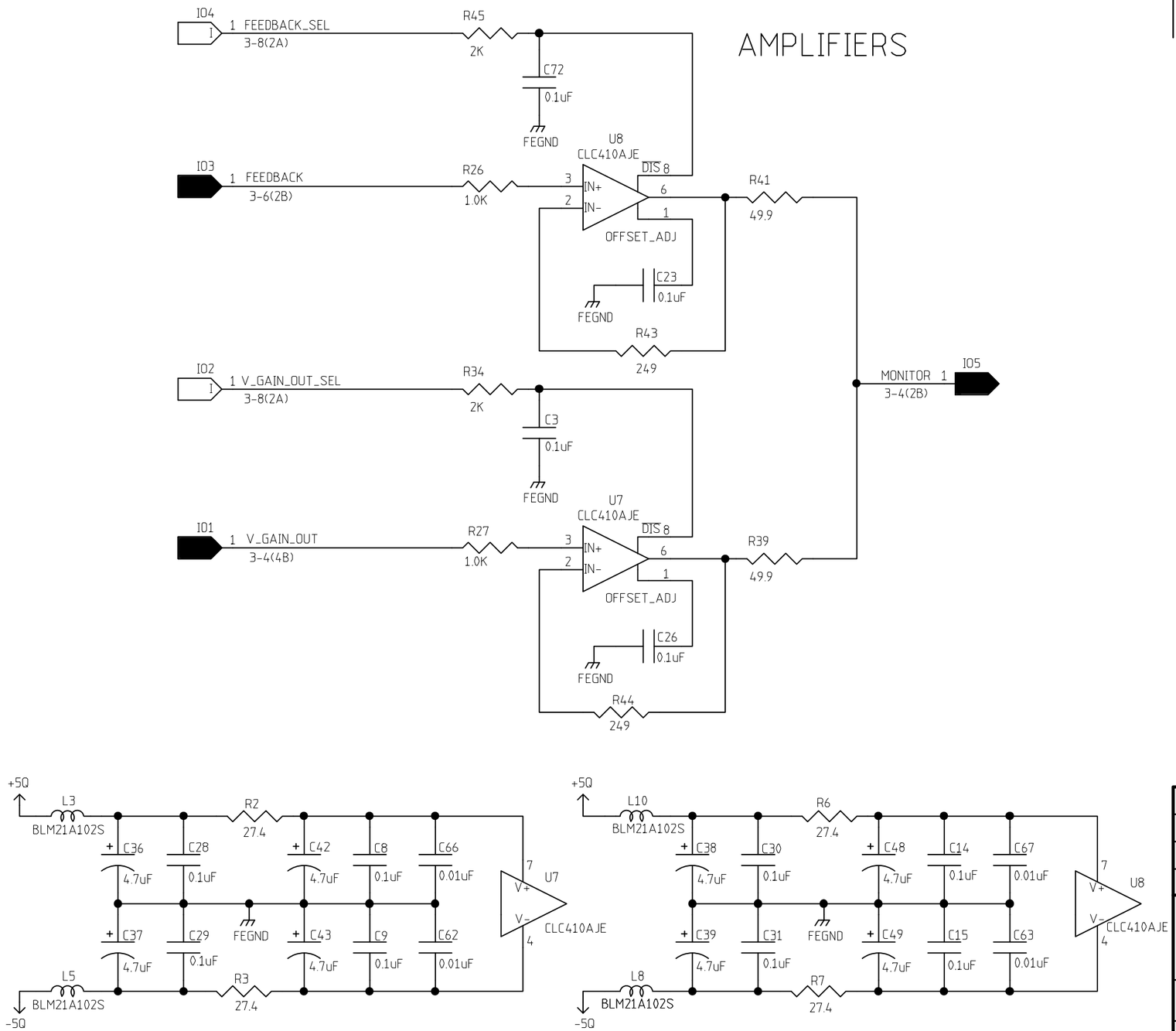
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK POLARITY

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 3-6

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

MONITOR SELECTION AMPLIFIERS

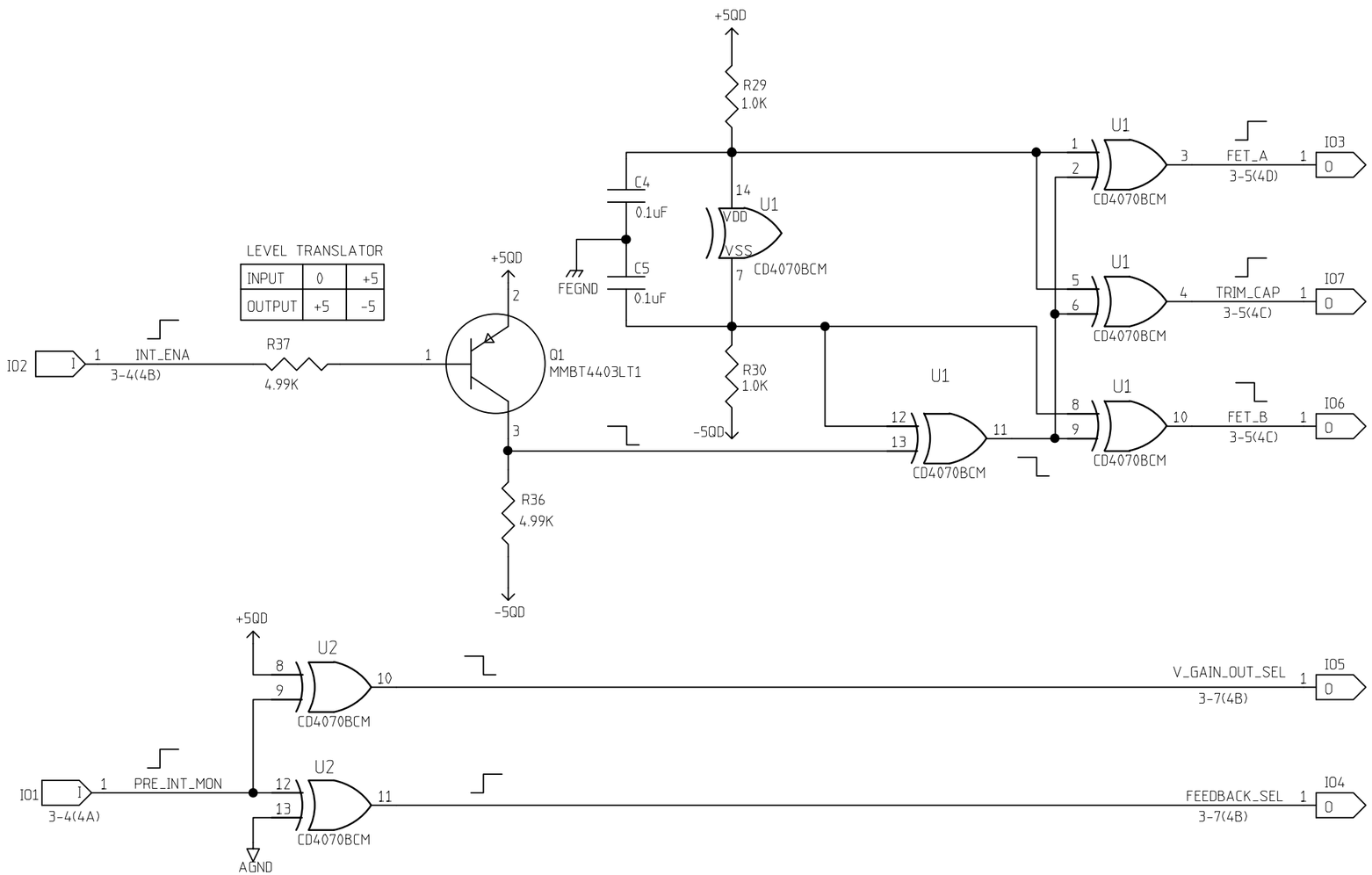


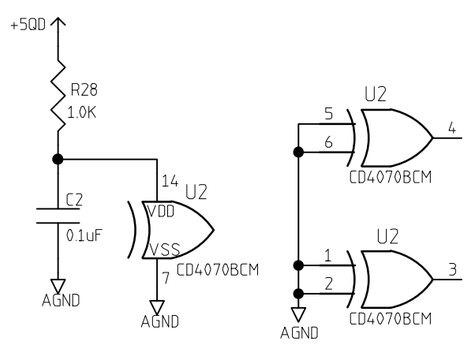
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/13/98
DRAWN	BRUCE MERKEL	11/13/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK MONITOR

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-7	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





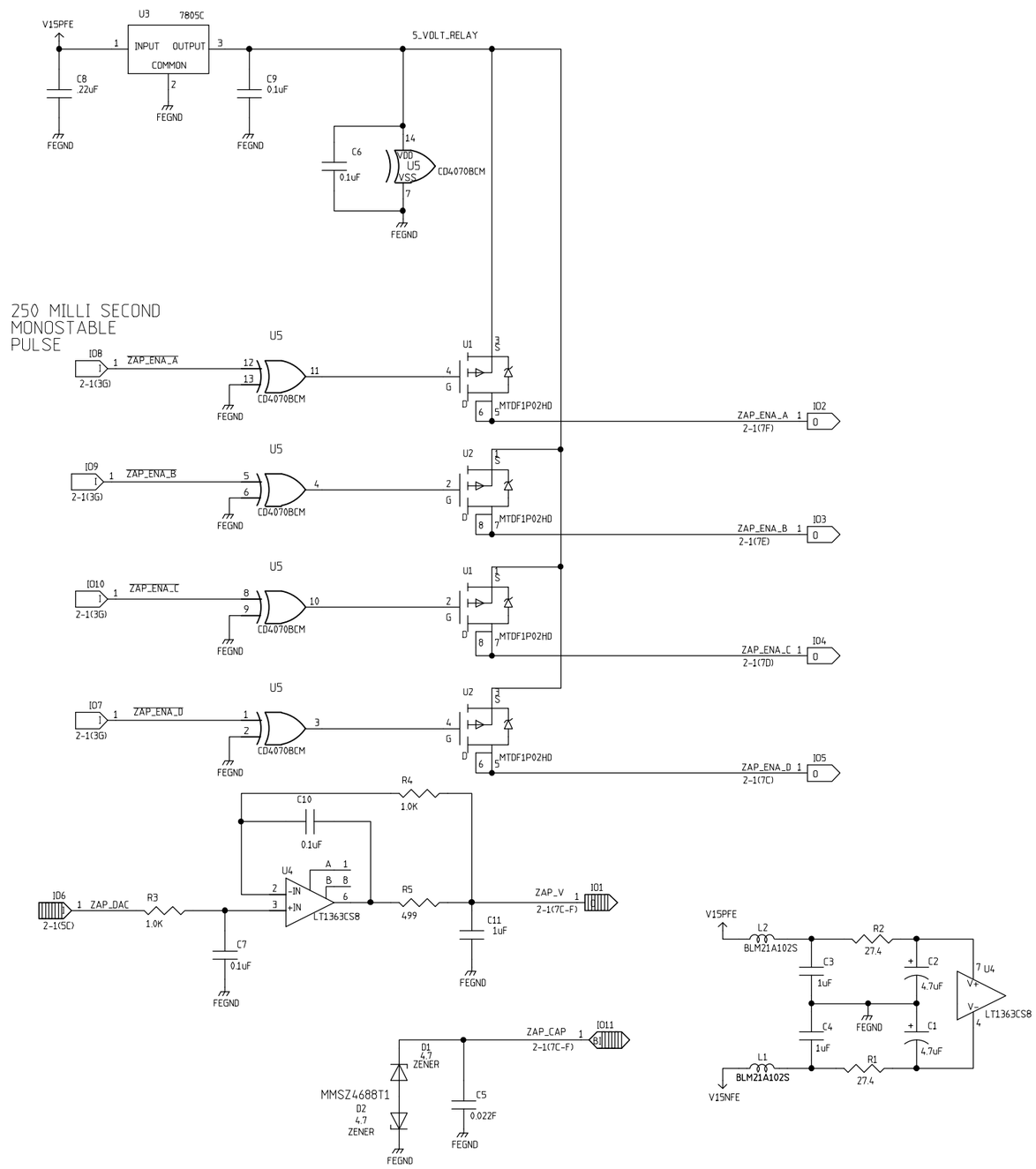
NOTE: U1 POWER SHOWN ABOVE

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID FEEDBACK LOGIC

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 3-8	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



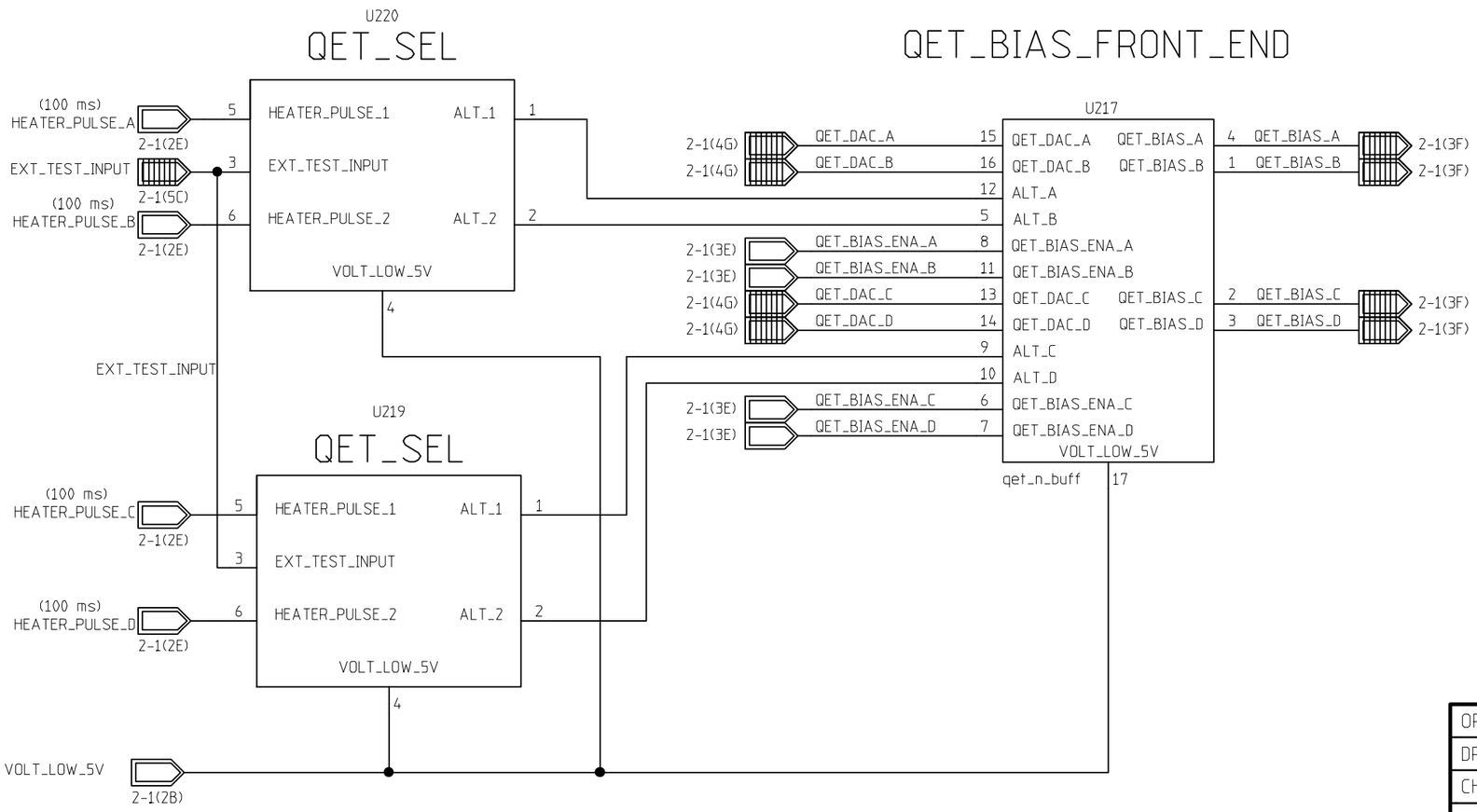
REVISED 9/21/99 BRUCE MERKEL

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
SQUID ZAP CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 4-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

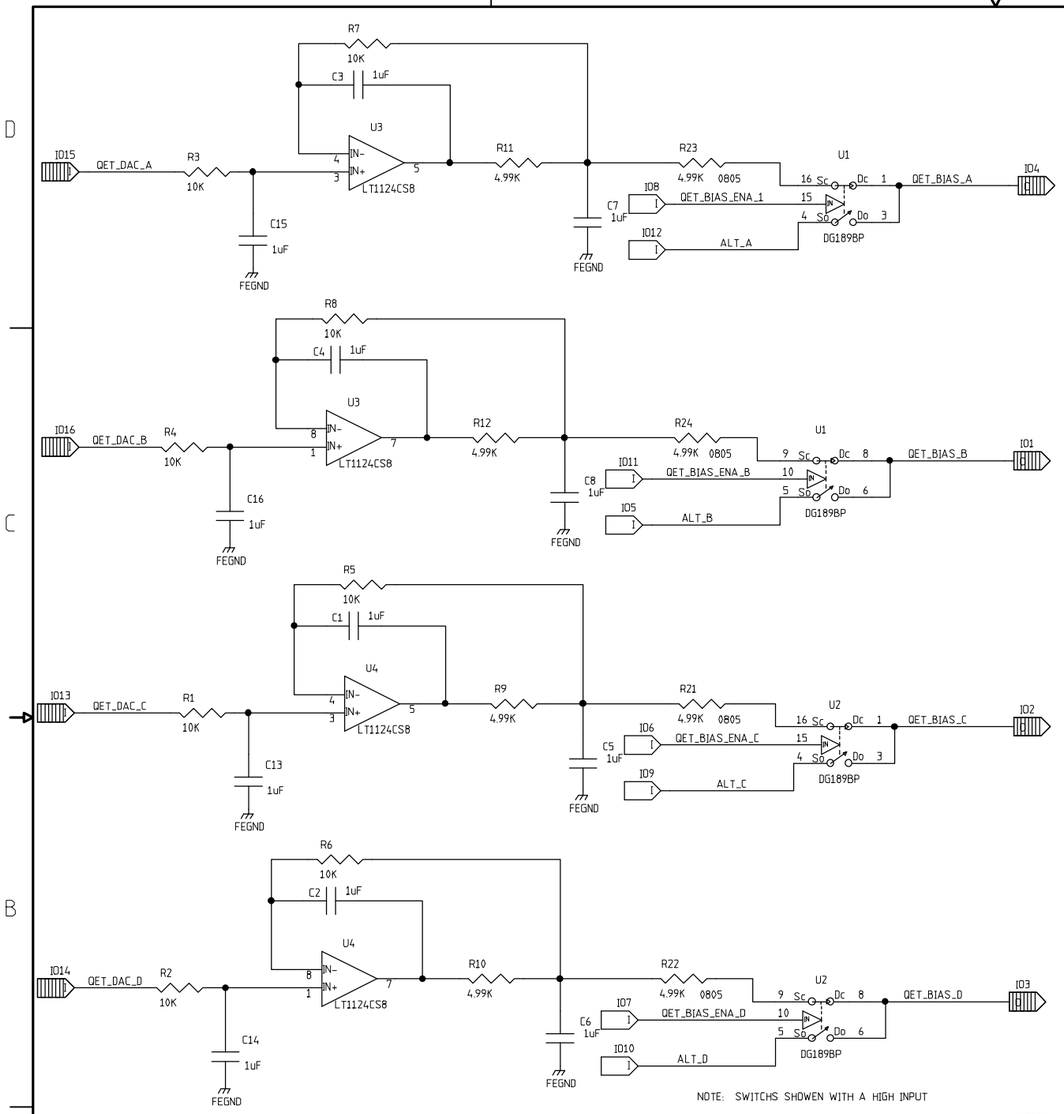


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 5-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



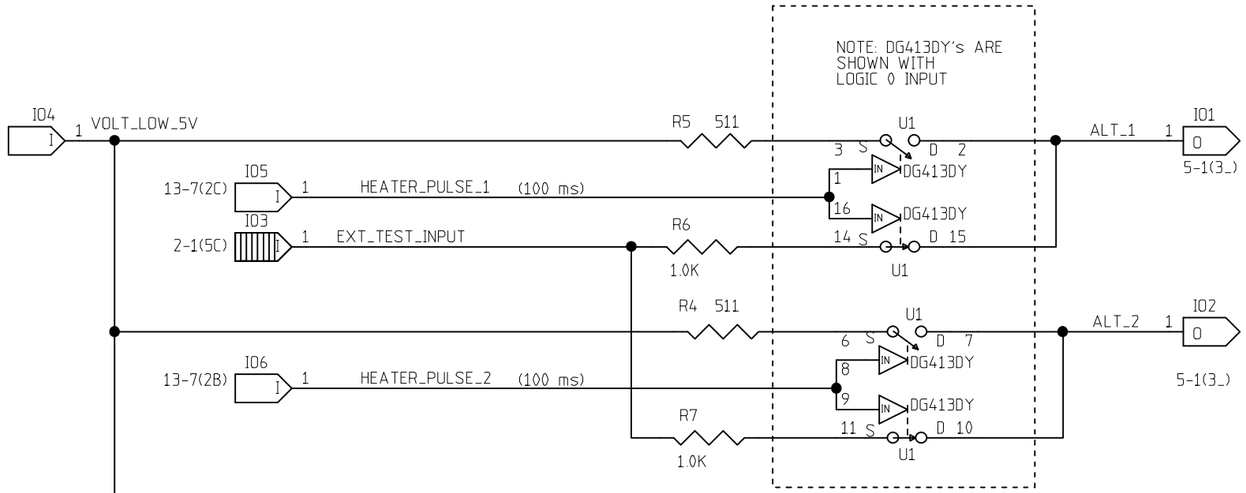
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	06/17/99
DRAWN	BRUCE MERKEL	07/16/99
CHECKED		
APPROVED		

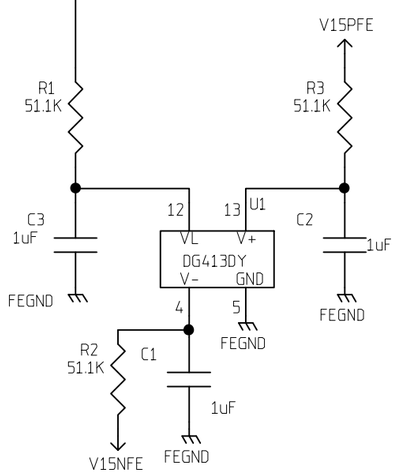
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 5-2	

DWG. NO.
SH.
REV

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





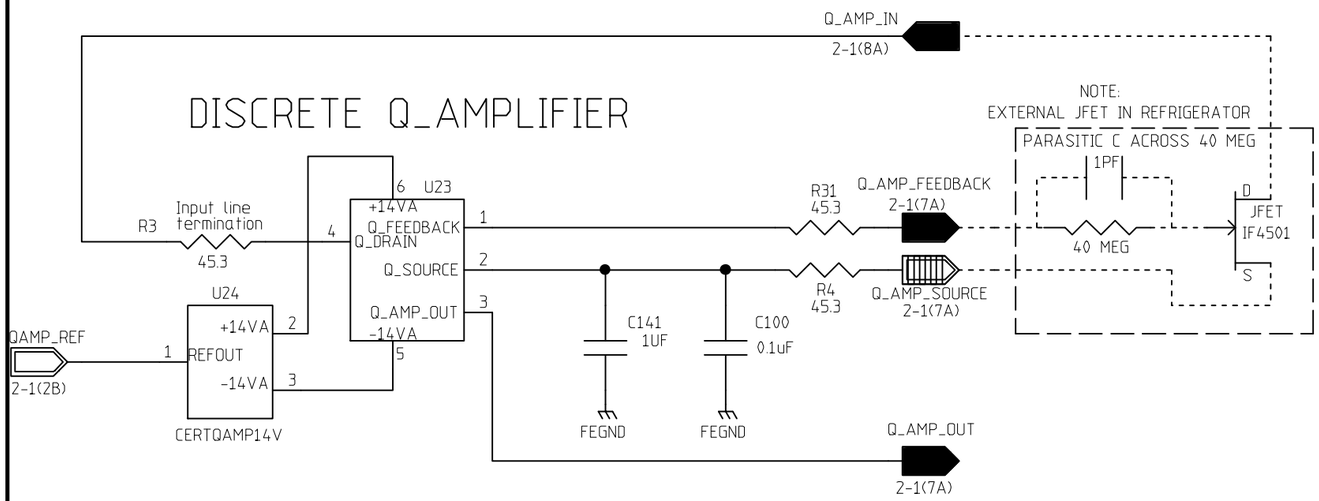
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	07/16/99
CHECKED		
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QET_SEL

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 5-4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

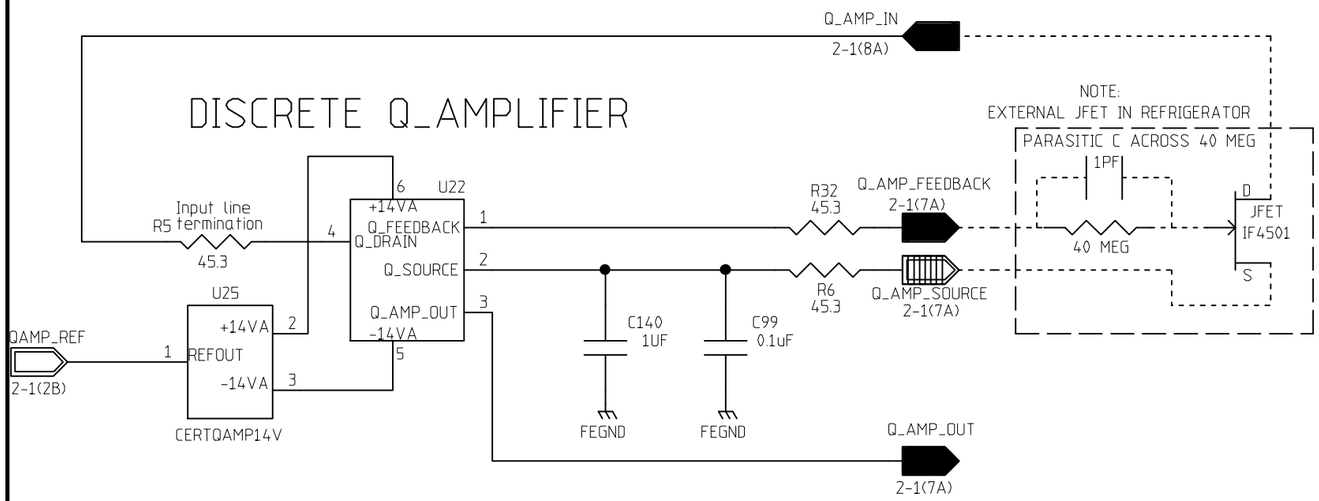


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QAMP BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 6-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



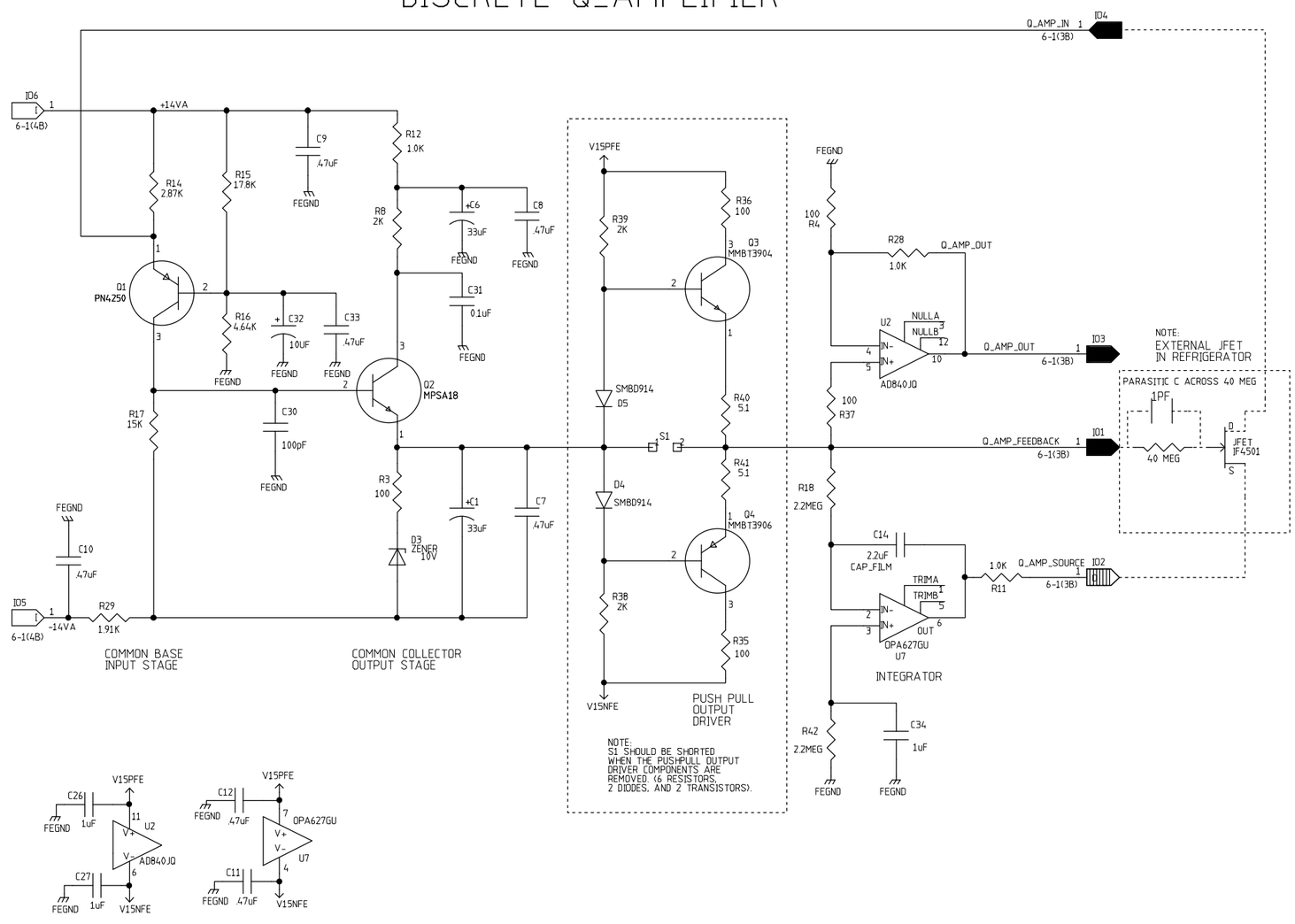
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QAMP BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 6-1	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	GENERAL MODIFICATIONS	9/27/99	B.MERKEL

DISCRETE Q_AMPLIFIER

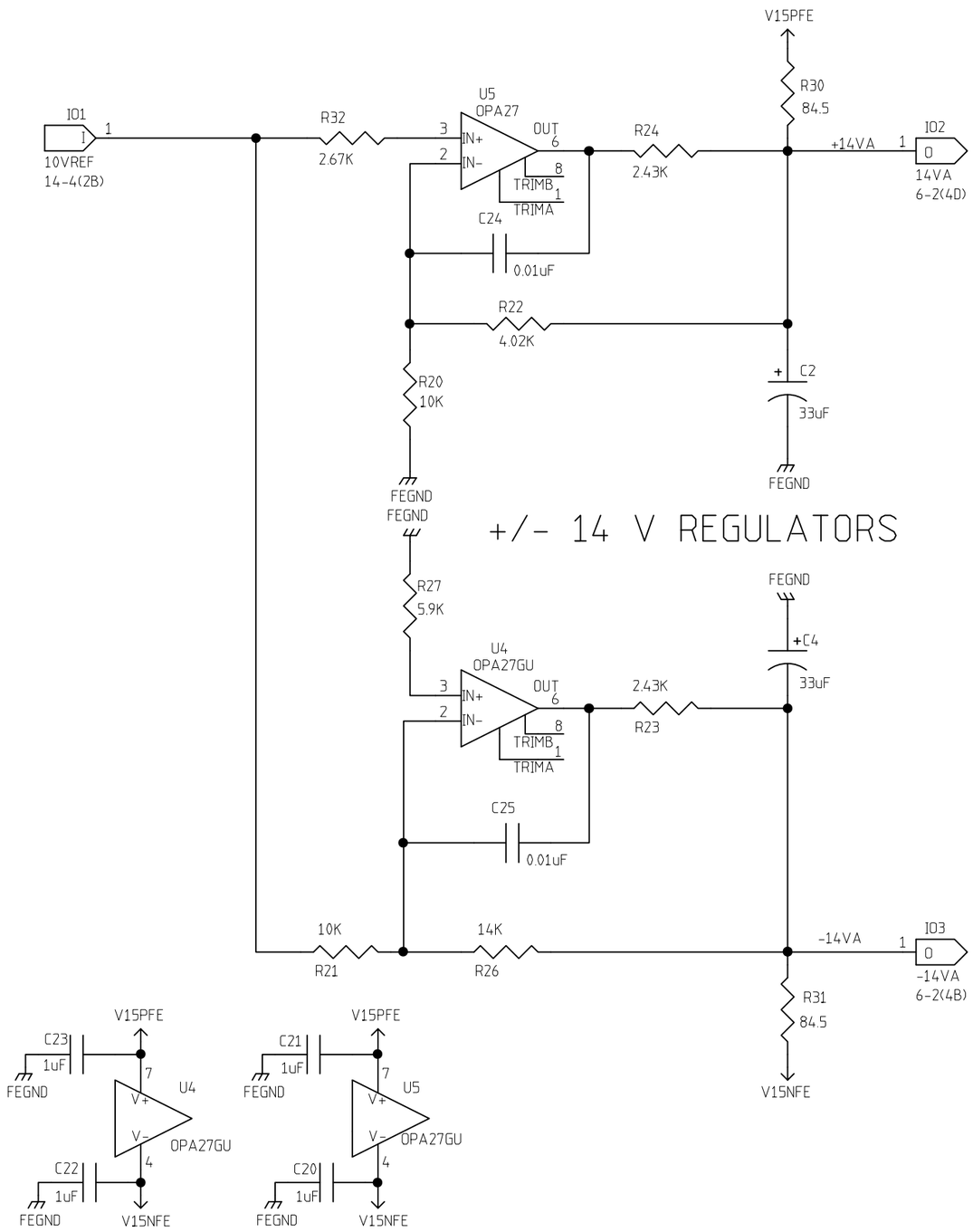


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
DISCRETE Q AMPLIFIER

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 6-2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

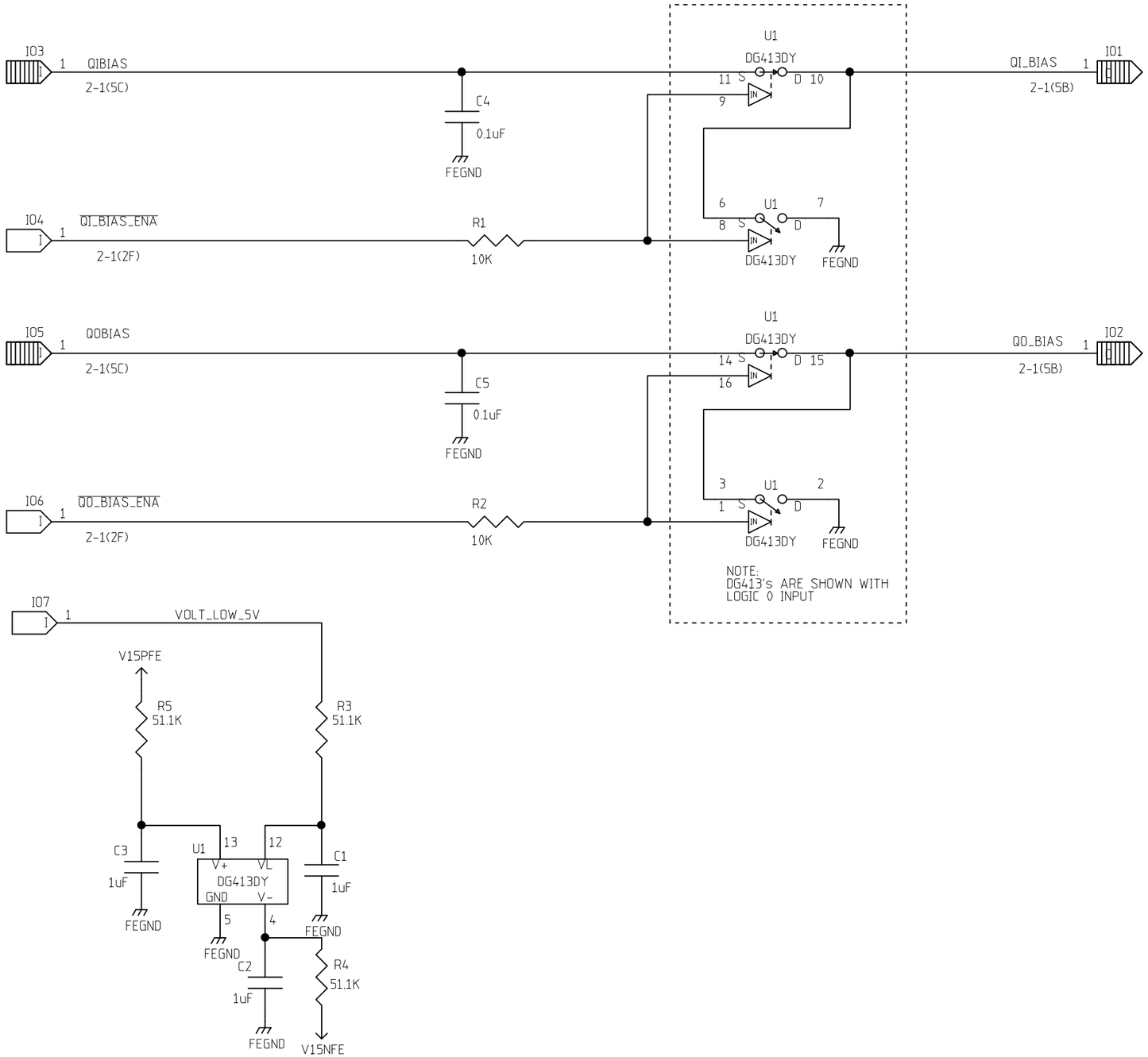
FERMILAB PPD/ ETT/ ES CDMS (E-891)

ZIP MODULE

Q AMP 14V

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 6-3



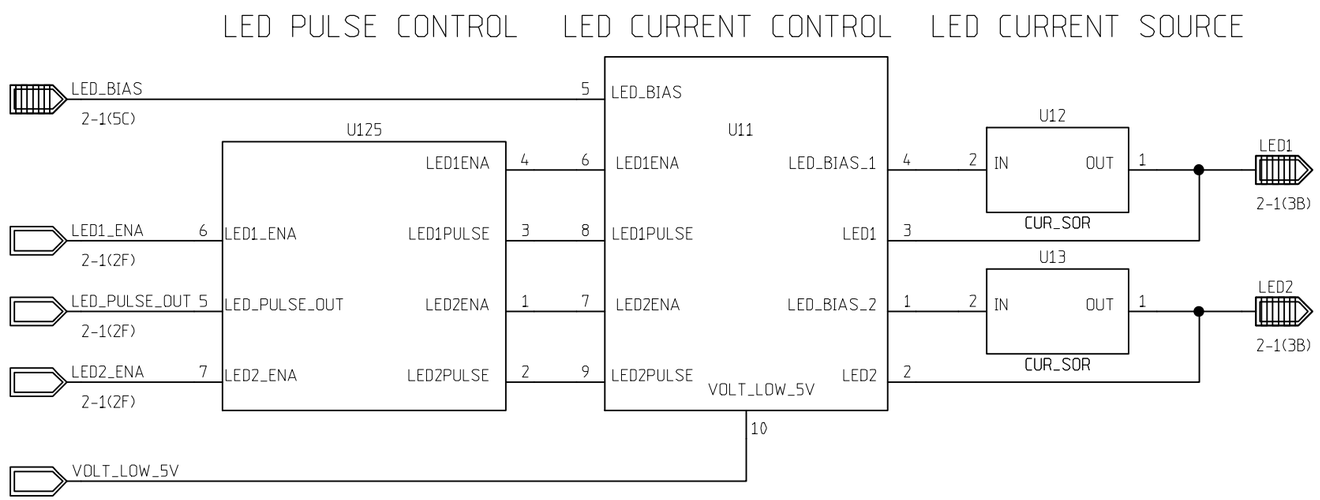
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/08/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
QBIAS FRONT END

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 7-1	

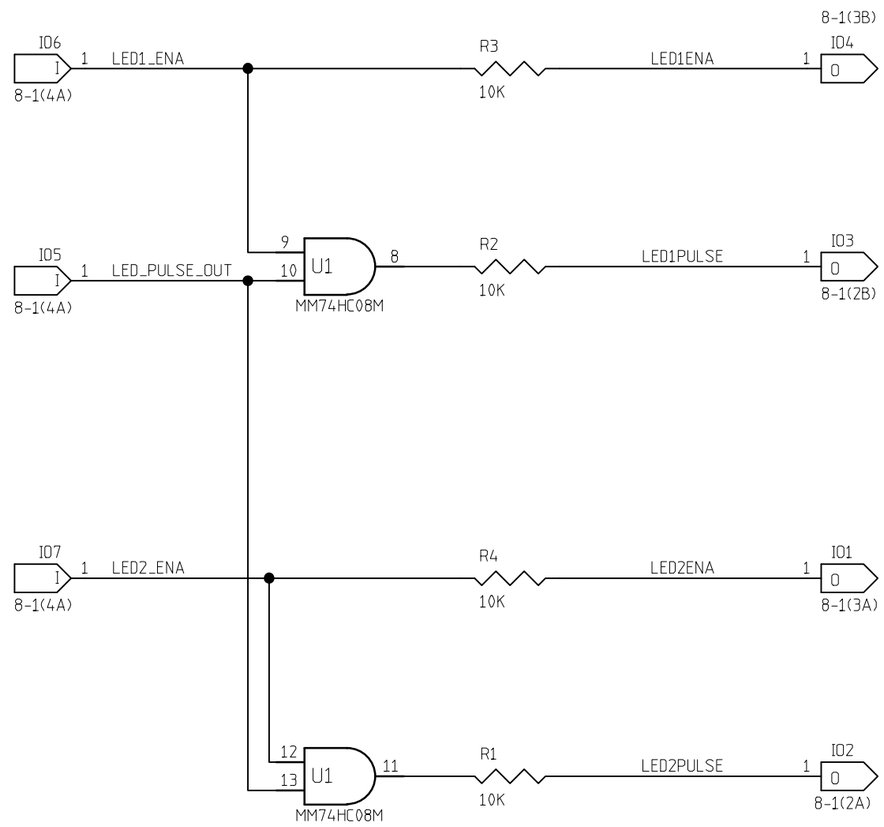
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	MOVED DIGITAL OUT OF ANALOG AREA	3/24/99	B MERKEL

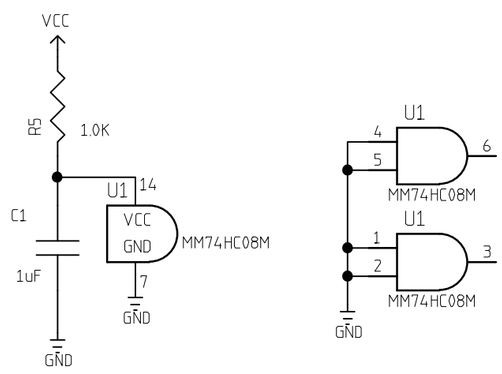


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	3/24/99
CHECKED		
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
LED BLOCK DIAGRAM

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 8-1	





REVISIONS

REV	DESCRIPTION	DATE	APPROVED

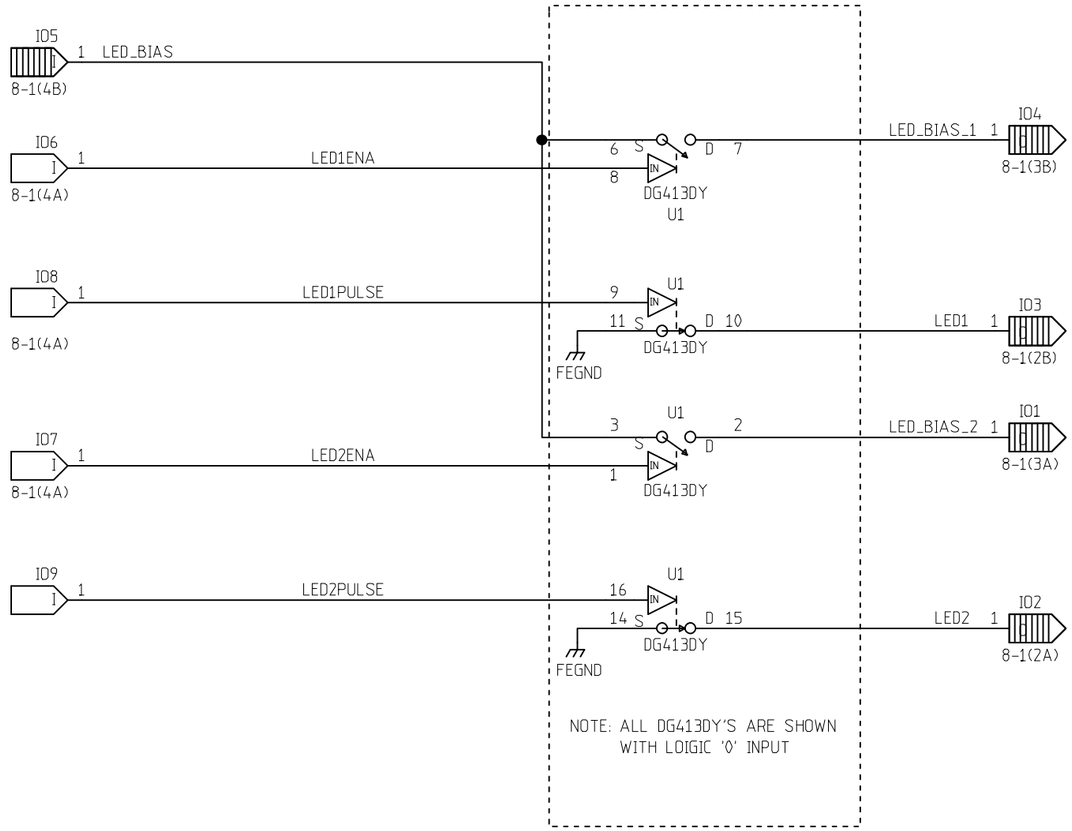
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	3/24/99
DRAWN	BRUCE MERKEL	3/24/99
CHECKED		
APPROVED		

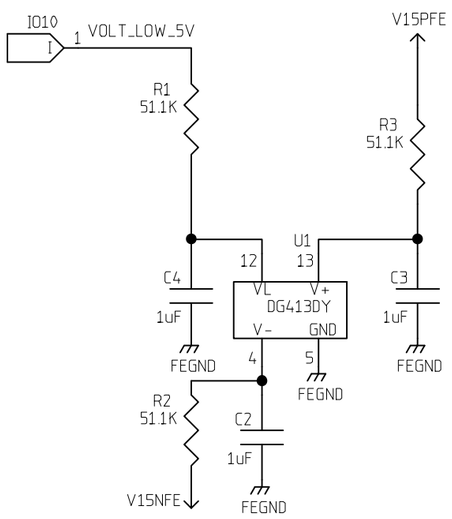
FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED PULSE CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 8-3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	ADDED A 5V OUTSIDE SOURCE AND REMOVED THE DIGITAL LOGIC TO THE DIGITAL SECTION	3/24/99	B MERKEL



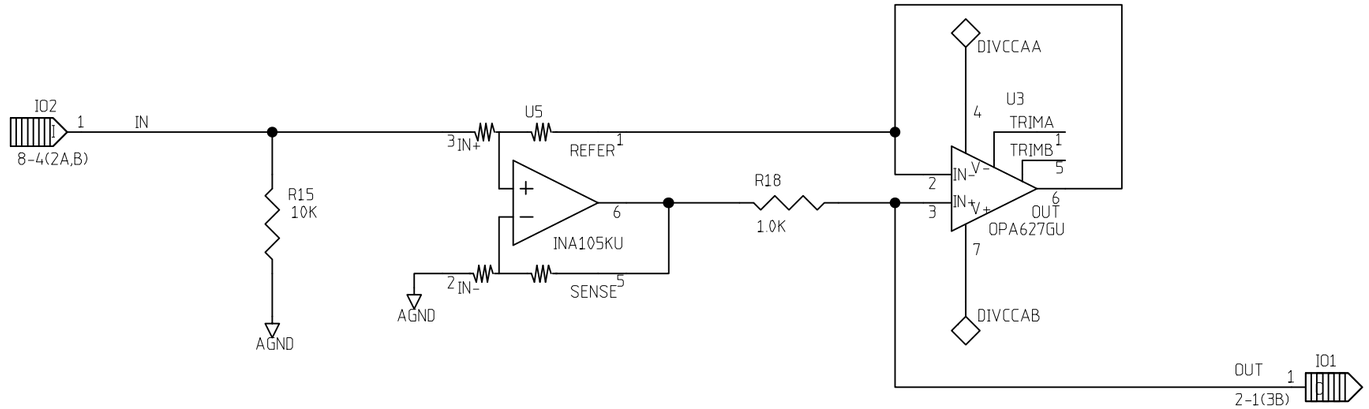


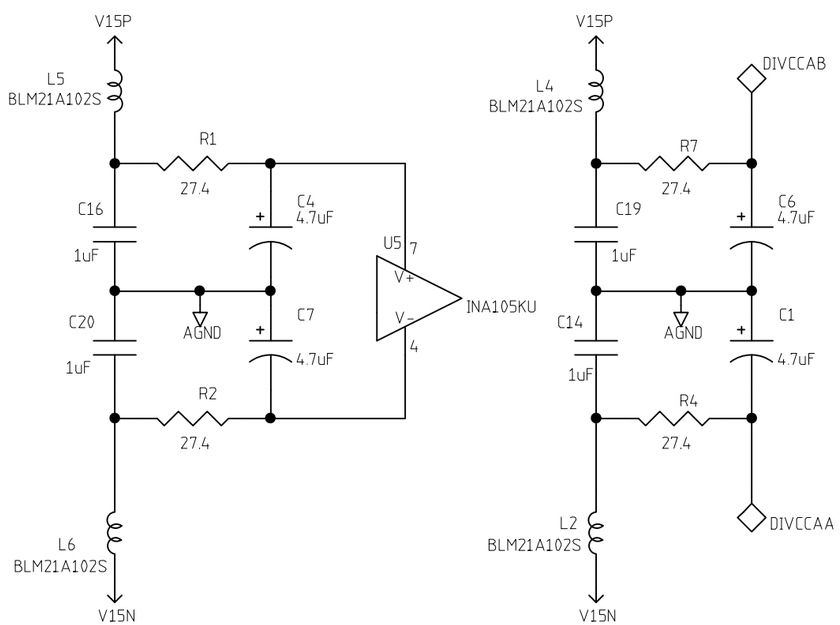
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/17/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED CURRENT CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 8-4	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





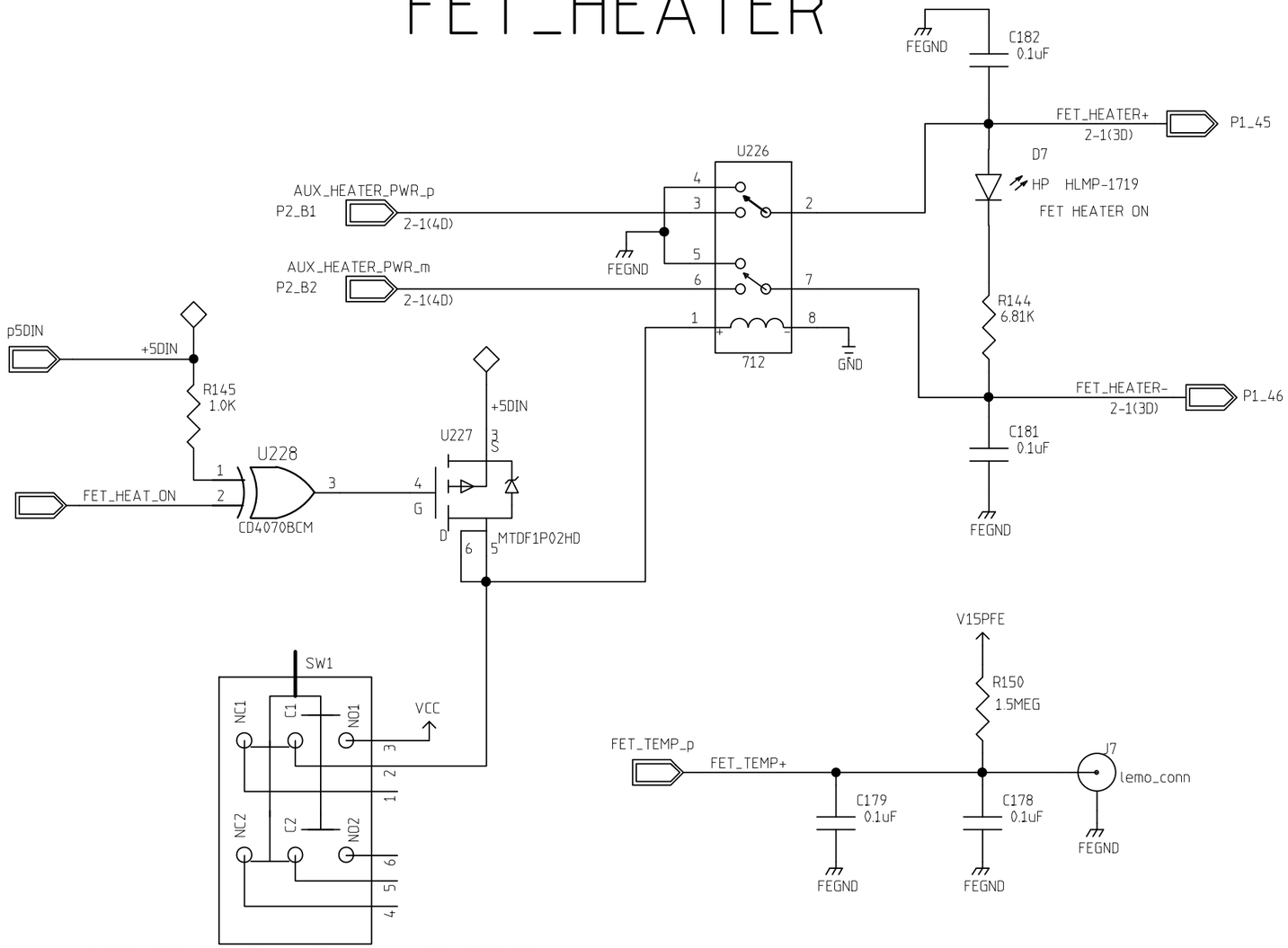
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	12/09/98
CHECKED	TOM CRENNA	1/6/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
LED CURRENT SOURCE

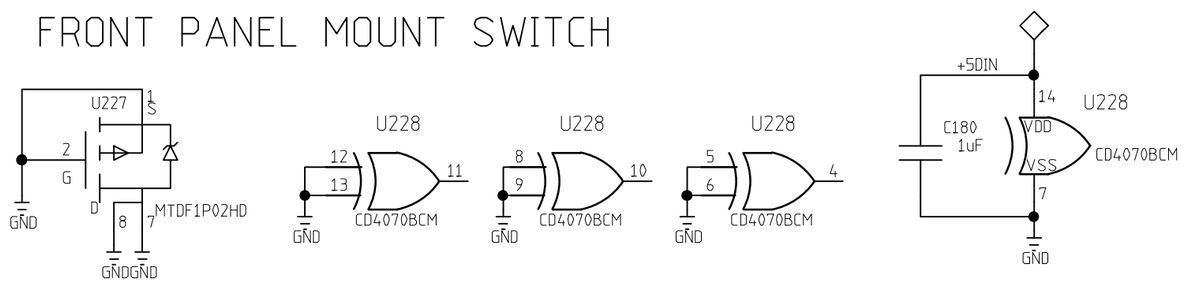
SIZE	FSCM NO.	DWG. NO.	REV
B			
SCALE		SHEET 8-5	

FET_HEATER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	SCHEMATIC UPDATED FOR VERSION 1	10/18/99	BDM



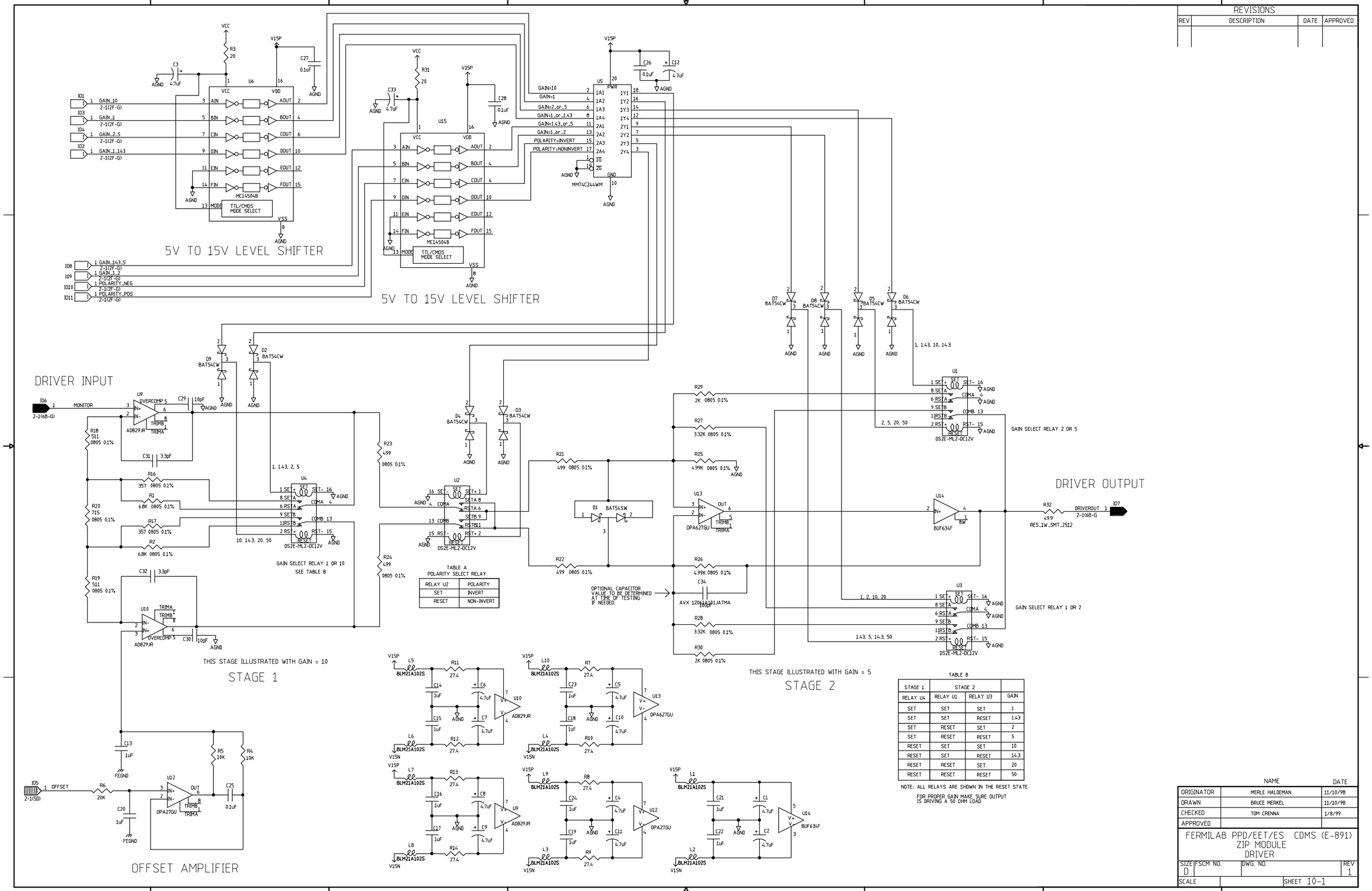
MONENTARY PUSH BUTTON
FRONT PANEL MOUNT SWITCH



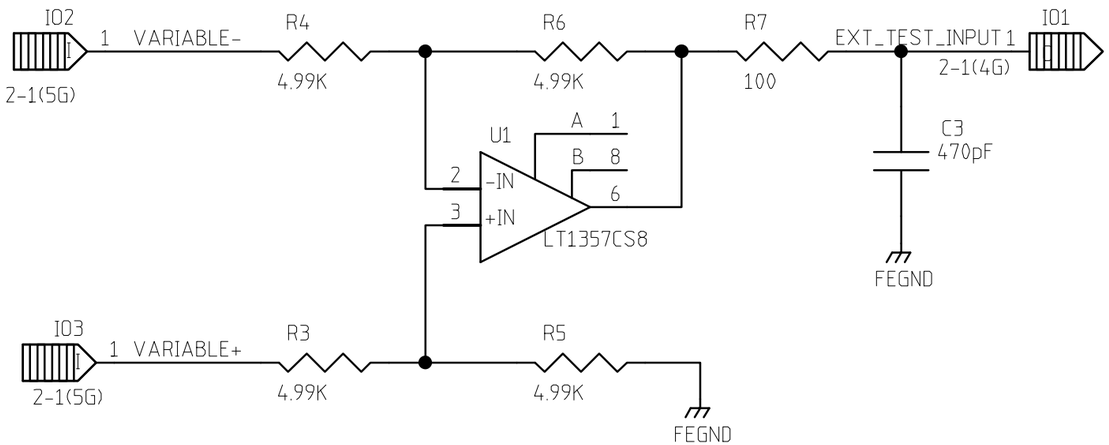
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	9/23/99
DRAWN	BRUCE MERKEL	9/23/99
CHECKED		
APPROVED		

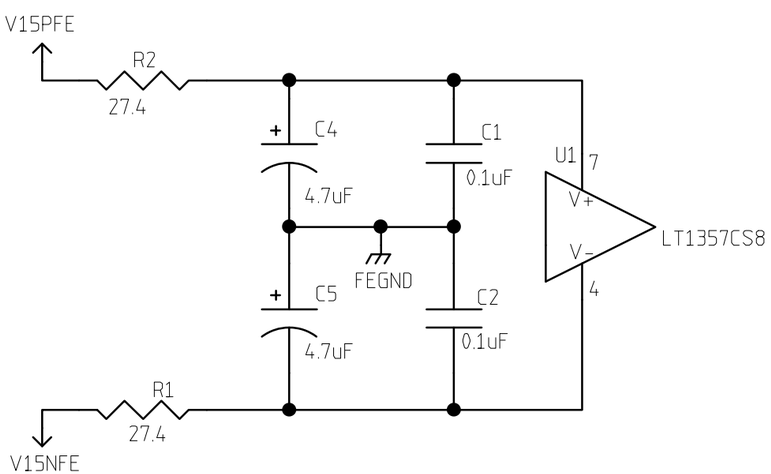
FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
FET_HEATER

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 9-1	


5V TO 15V LEVEL SHIFTER
5V TO 15V LEVEL SHIFTER
DRIVER INPUT
DRIVER OUTPUT
GAIN SELECT RELAY 2 OR 5
GAIN SELECT RELAY 1 OR 2
GAIN SELECT RELAY 1 OR 10
SEE TABLE B
THIS STAGE ILLUSTRATED WITH GAIN = 10
STAGE 1
THIS STAGE ILLUSTRATED WITH GAIN = 5
STAGE 2
OFFSET AMPLIFIER
OPTIONAL CAPACITOR VALUE TO BE DETERMINED AT TIME OF TESTING IF NEEDED.
TABLE A
POLARITY SELECT RELAY
RELAY U2 | POLARITY
SET | INVERT
RESET | NON-INVERT
TABLE B
STAGE 1 | STAGE 2 | |
RELAY U4 | RELAY U1 | RELAY U3 | GAIN
SET | SET | SET | 1
SET | SET | RESET | 1.43
SET | RESET | SET | 2
SET | RESET | RESET | 5
RESET | SET | SET | 10
RESET | SET | RESET | 14.3
RESET | RESET | SET | 20
RESET | RESET | RESET | 50
NOTE: ALL RELAYS ARE SHOWN IN THE RESET STATE
FOR PROPER GAIN MAKE SURE OUTPUT IS DRIVING A 50 OHM LOAD
REVISIONS
REV | DESCRIPTION | DATE | APPROVED
NAME | DATE
ORIGINATOR | MERLE HALDEMAN | 11/10/98
DRAWN | BRUCE MERKEL | 11/10/98
CHECKED | TOM CRENNA | 1/8/99
APPROVED
FERMILAB PPD/EET/ES CDMS (E-891)
ZIP MODULE
DRIVER
SIZE D | FSCM NO. | DWG. NO. | REV 1
SCALE | SHEET 10-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CHANGED U1 FROM ANALOG DEVUCES SSM2141S TO LINEAR TECHNOLOGY LT1357CS8 FOR FASTER RESPONSE ALSO ADDED TWO 4.7uF CAPS TO BYPASS	4/28/99	M.HALDEMAN





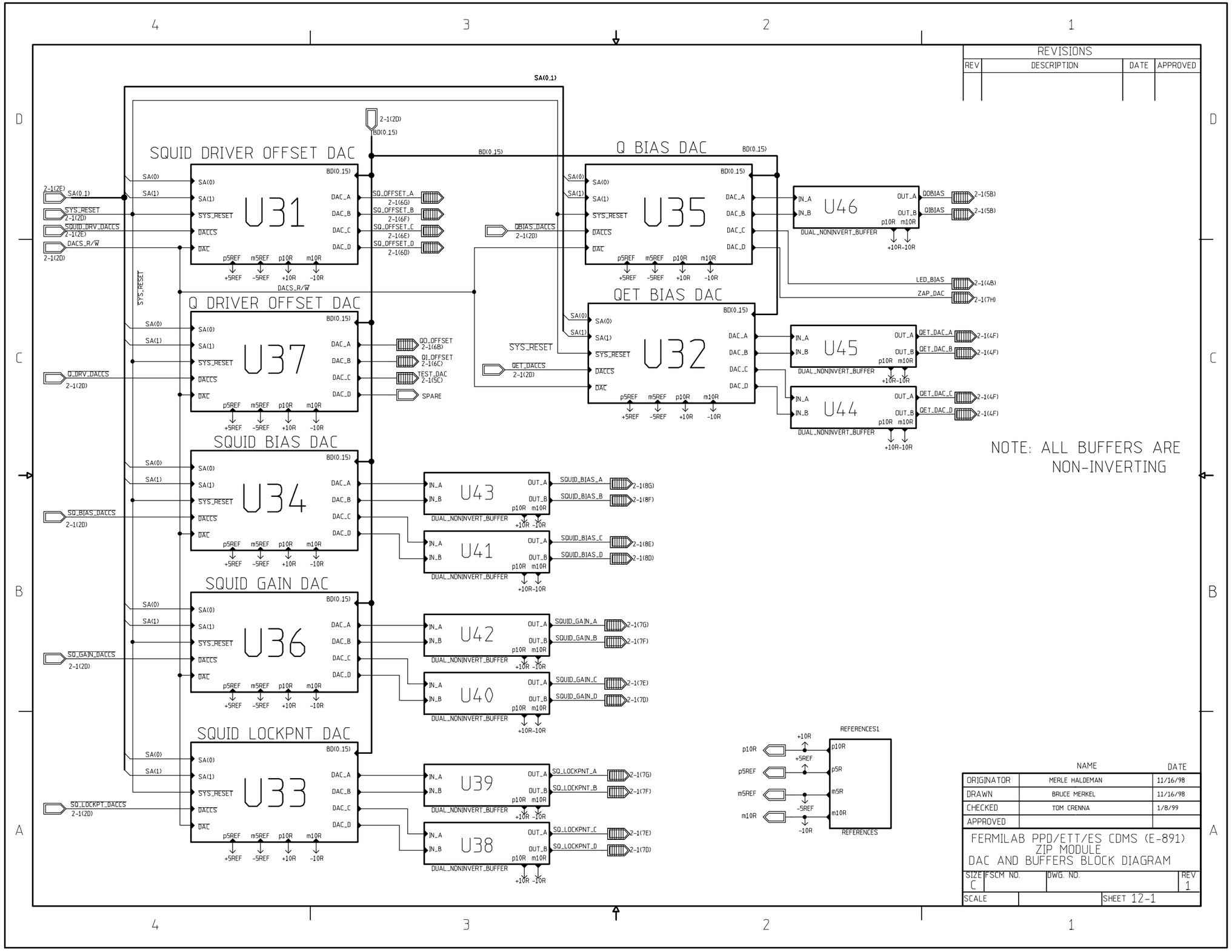
NOTE: FOR HIGHER SPEED USE A LT1363CS8

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
EXTERNAL TEST RECEIVER

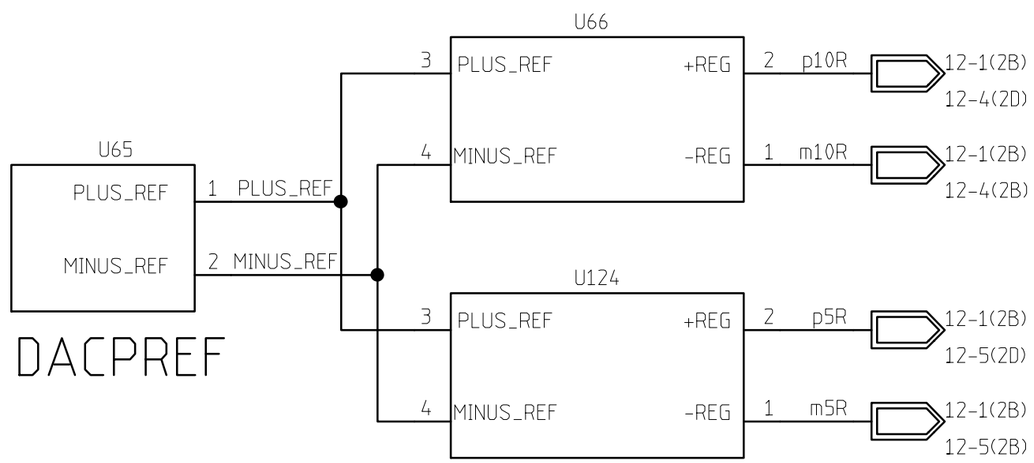
SIZE	FSCM NO.	DWG. NO.	REV
A			A

SCALE | SHEET 11-1


SQUID DRIVER OFFSET DAC
U31
Q DRIVER OFFSET DAC
U37
SQUID BIAS DAC
U34
SQUID GAIN DAC
U36
SQUID LOCKPNT DAC
U33
Q BIAS DAC
U35
QET BIAS DAC
U32
U46
U45
U44
U43
U41
U42
U40
U39
U38
DUAL_NONINVERT_BUFFER
REFERENCES1
REFERENCES
SQ_OFFSET_A
SQ_OFFSET_B
SQ_OFFSET_C
SQ_OFFSET_D
Q0_OFFSET
Q1_OFFSET
TEST_DAC
SPARE
QOBIAS
QIBIAS
LED_BIAS
ZAP_DAC
QET_DAC_A
QET_DAC_B
QET_DAC_C
QET_DAC_D
SQUID_BIAS_A
SQUID_BIAS_B
SQUID_BIAS_C
SQUID_BIAS_D
SQUID_GAIN_A
SQUID_GAIN_B
SQUID_GAIN_C
SQUID_GAIN_D
SQ_LOCKPNT_A
SQ_LOCKPNT_B
SQ_LOCKPNT_C
SQ_LOCKPNT_D
SQ_BIAS_DACCS
SQ_GAIN_DACCS
SQ_LOCKPT_DACCS
Q_DRV_DACCS
QET_DACCS
QBIAS_DACCS
SQUID_DRV_DACCS
DACS_R/W
SYS_RESET
SA(0_1)
BD(0_15)
NOTE: ALL BUFFERS ARE NON-INVERTING
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
NAME
DATE
ORIGINATOR
MERLE HALDEMAN
11/16/98
DRAWN
BRUCE MERKEL
11/16/98
CHECKED
TOM CRENNA
1/8/99
APPROVED
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
DAC AND BUFFERS BLOCK DIAGRAM
SIZE
C
FSCM NO.
DWG. NO.
REV
1
SCALE
SHEET 12-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-19-99	

DAC 10 VOLT REGULATOR



DAC 5 VOLT REGULATOR

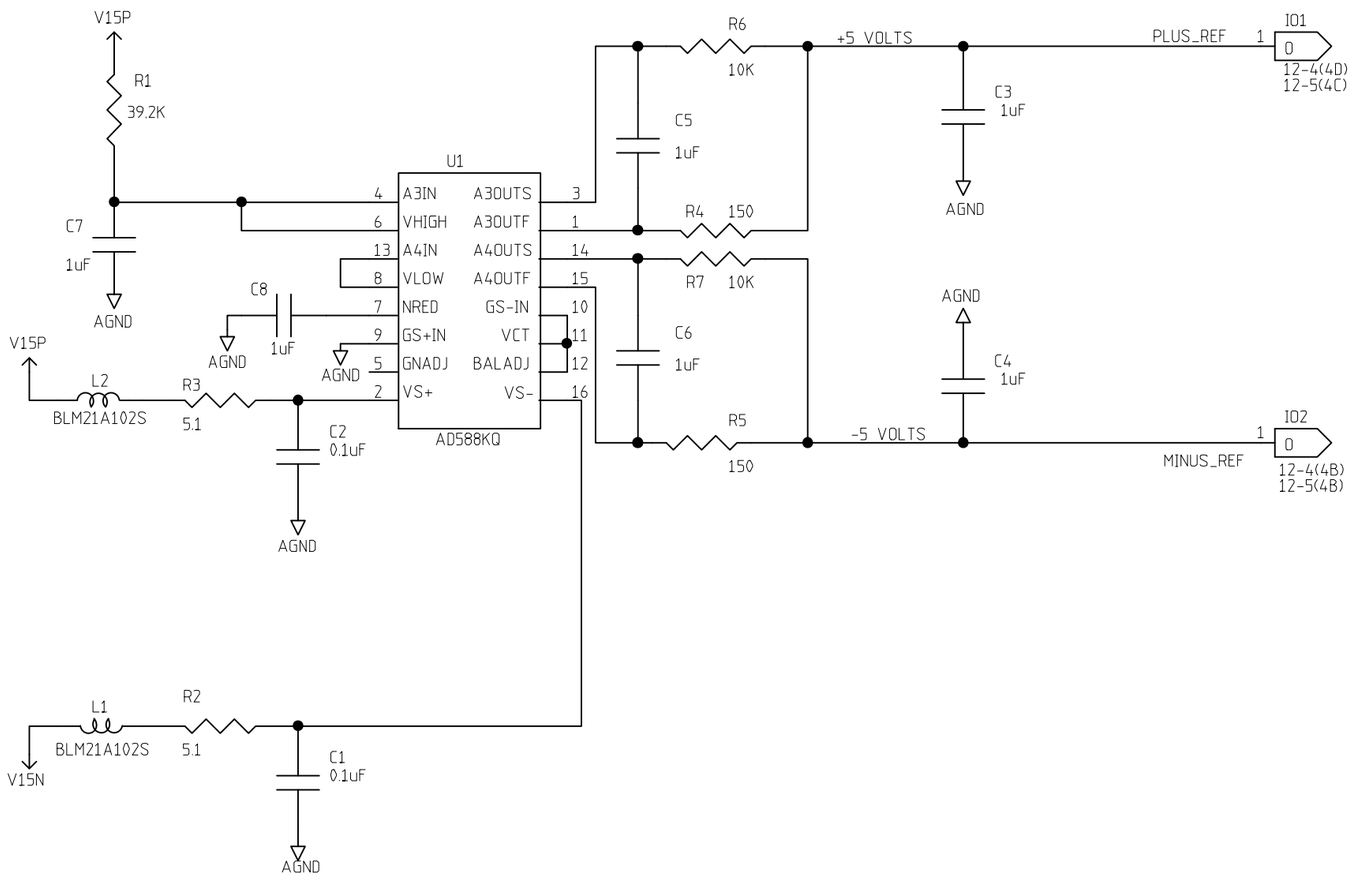
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/16/98
DRAWN	BRUCE MERKEL	11/16/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC REFERENCES

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE | SHEET 12-2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



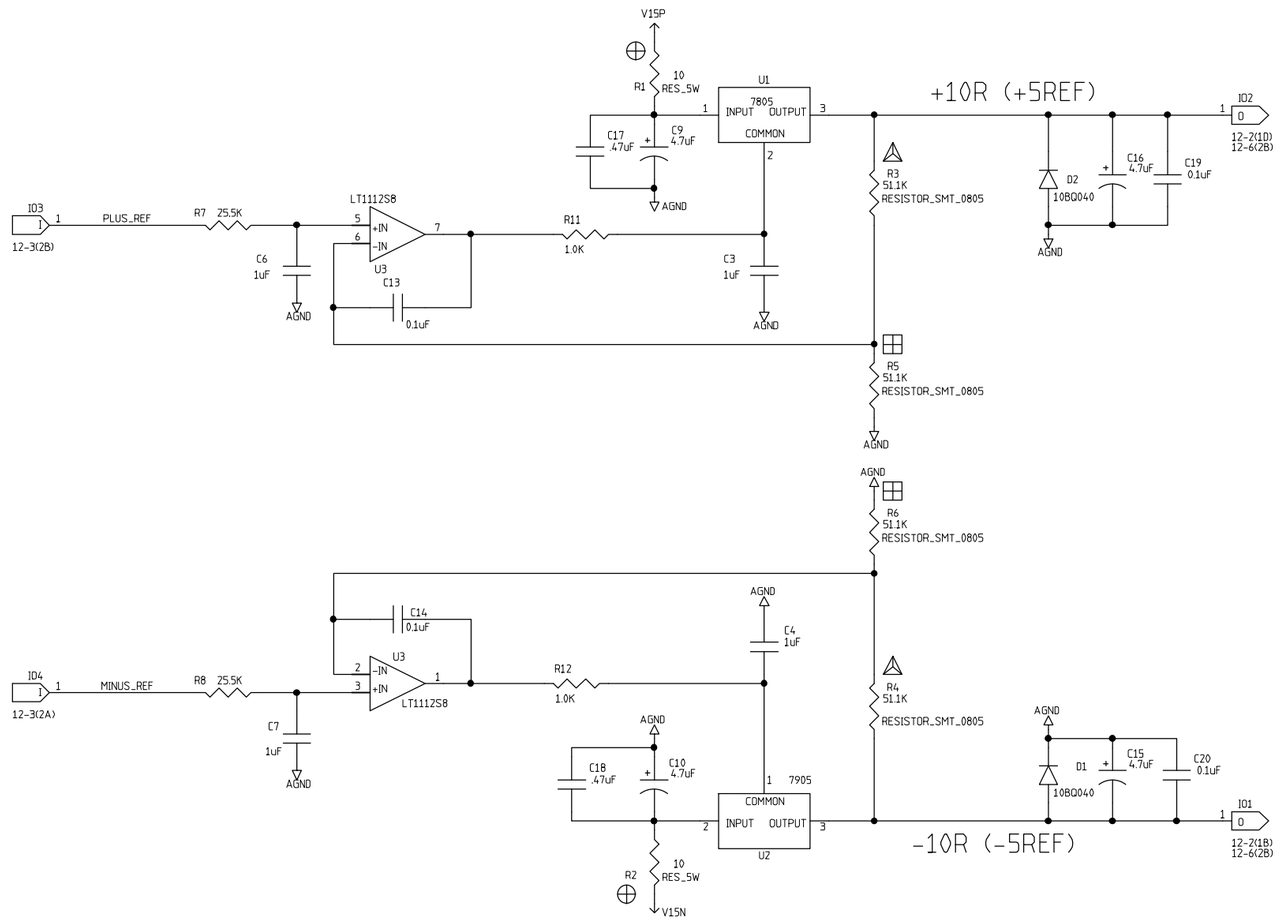
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/01/98
DRAWN	BRUCE MERKEL	12/01/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

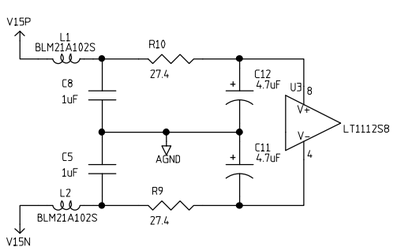
FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC PRECISION REFERENCE

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 12-3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	USE FOR BOTH 10 & 5 VOLT REFERENCE	3/23/99	B. MERKEL





ALL VALUES SHOWN FOR

10 VOLT REFERENCE

USE VALUES BELOW FOR

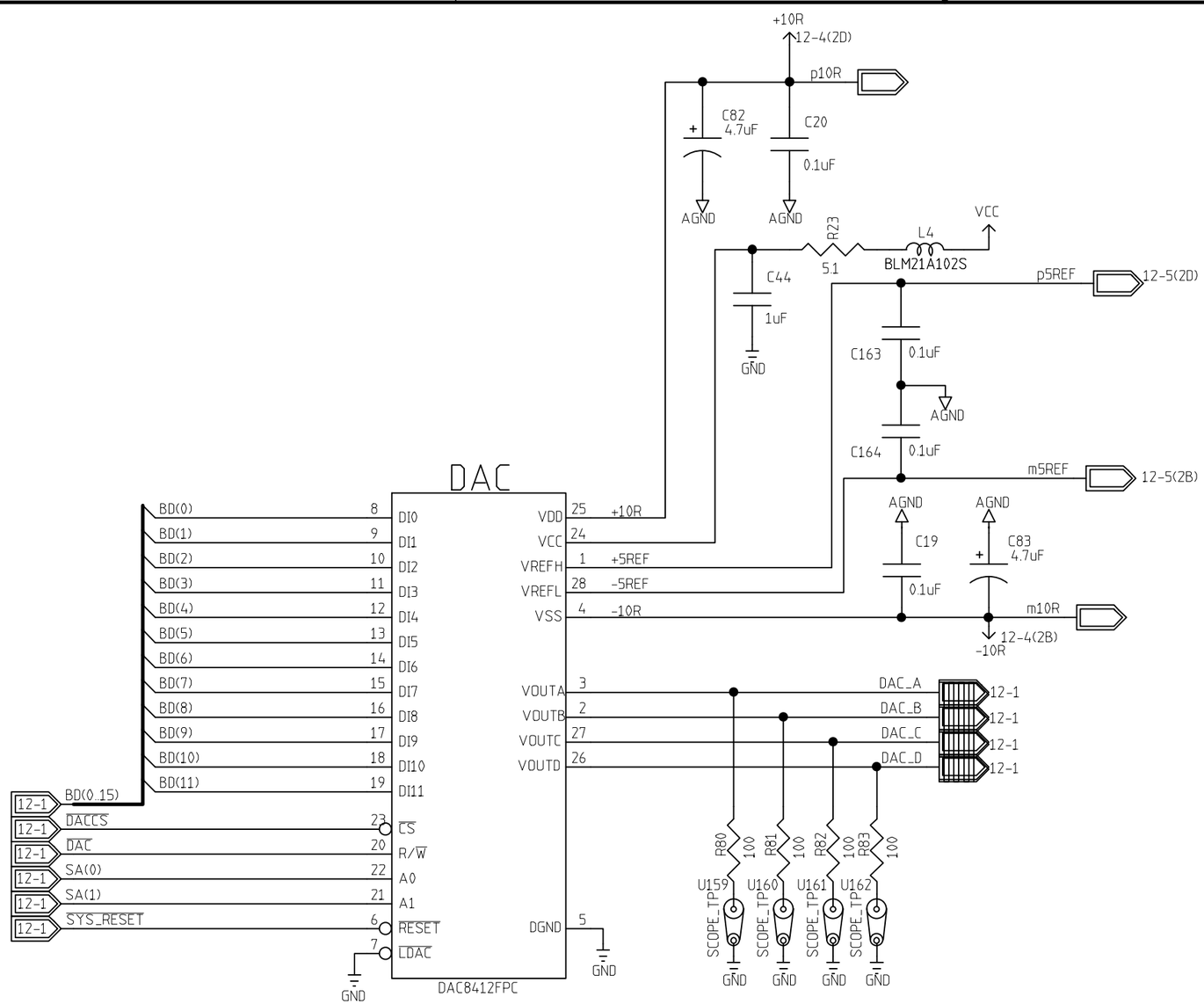
5 VOLT REFERENCE

⊕ 240 OHM 5W RESISTOR
△ 25.5K OHM RESISTOR
⊞ RESISTOR NOT INSTALLED

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/01/98
DRAWN	BRUCE MERKEL	12/01/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC +/- VOLTAGE REFERENCES

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 12-4	

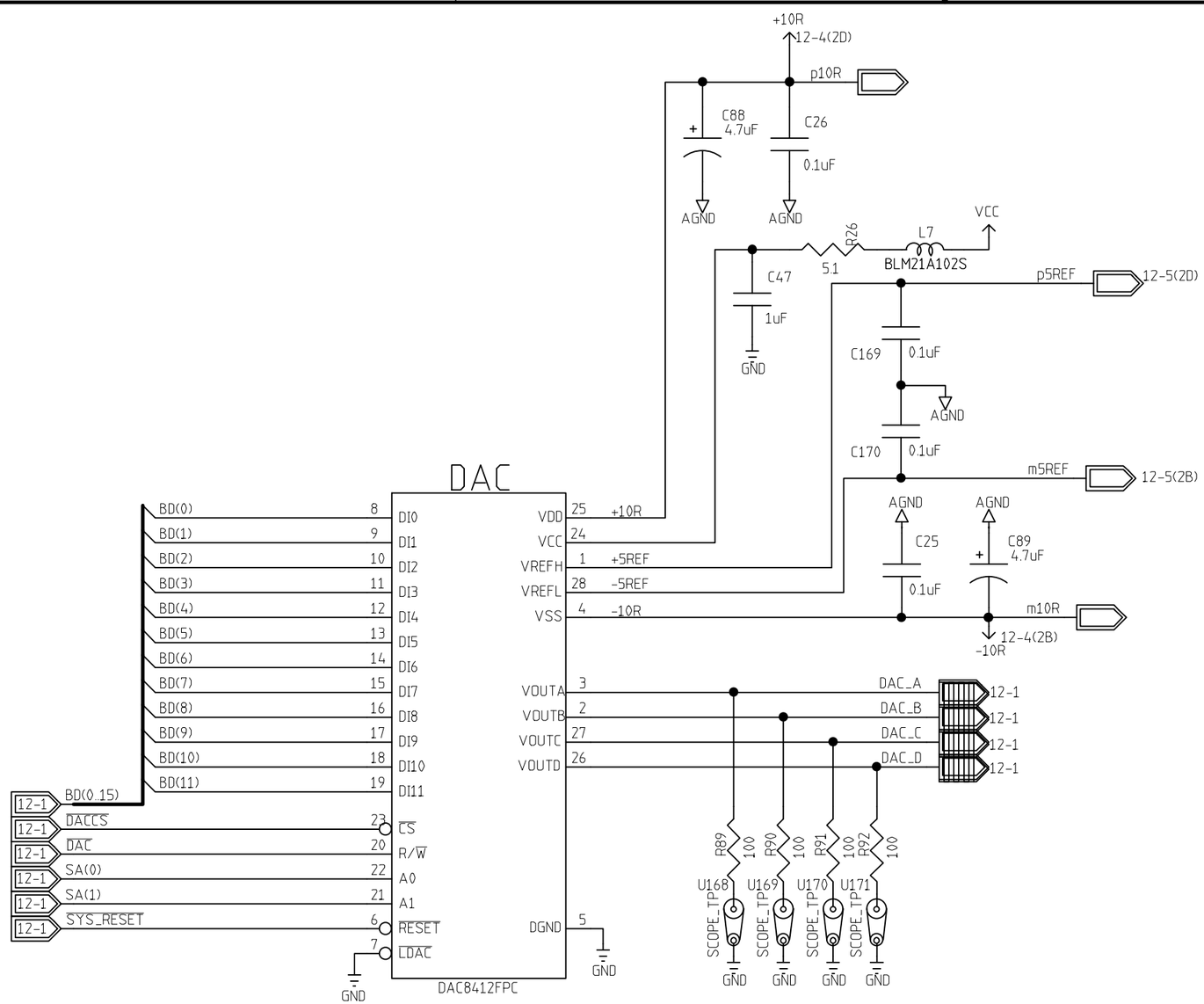


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	



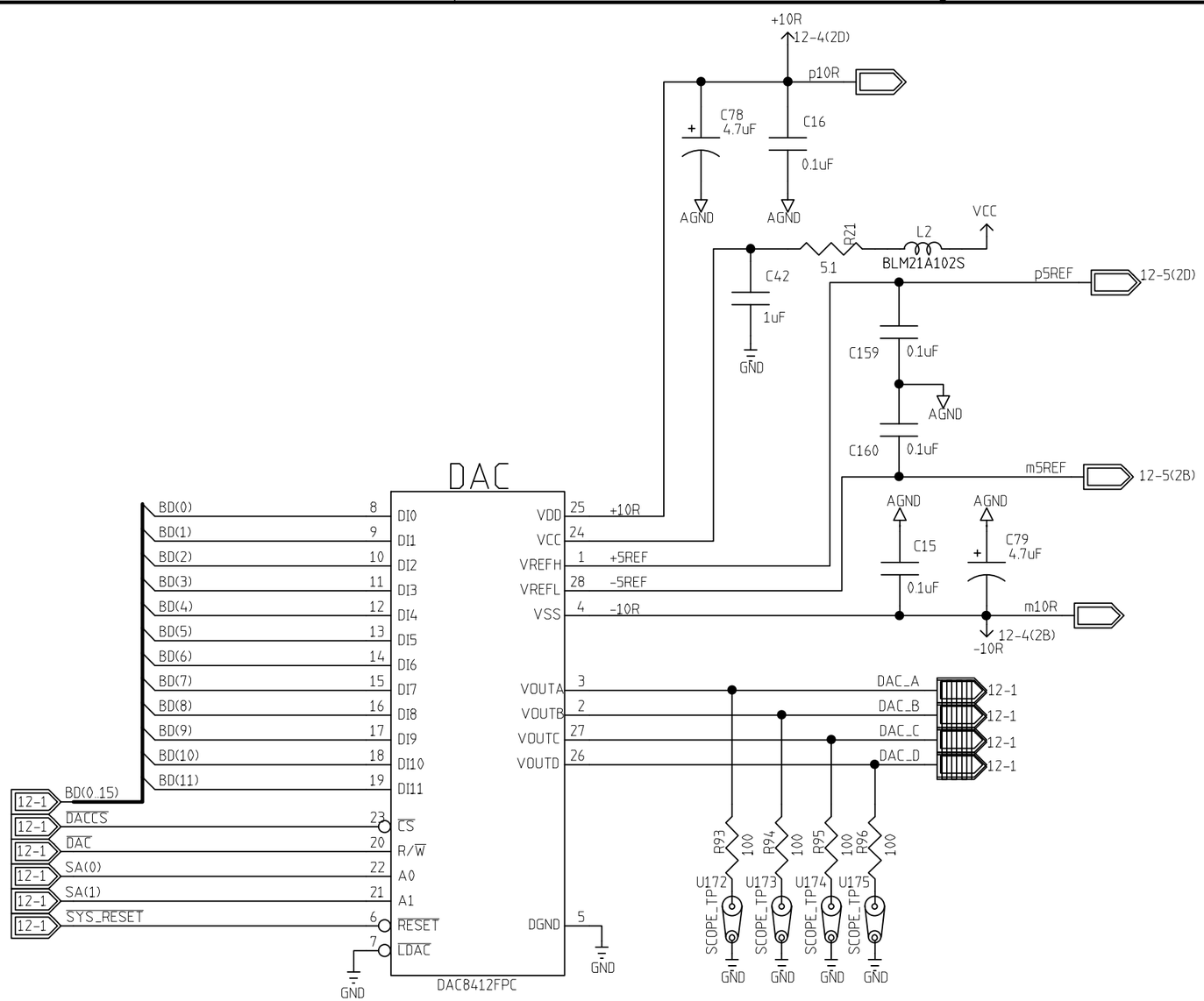
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	

U32

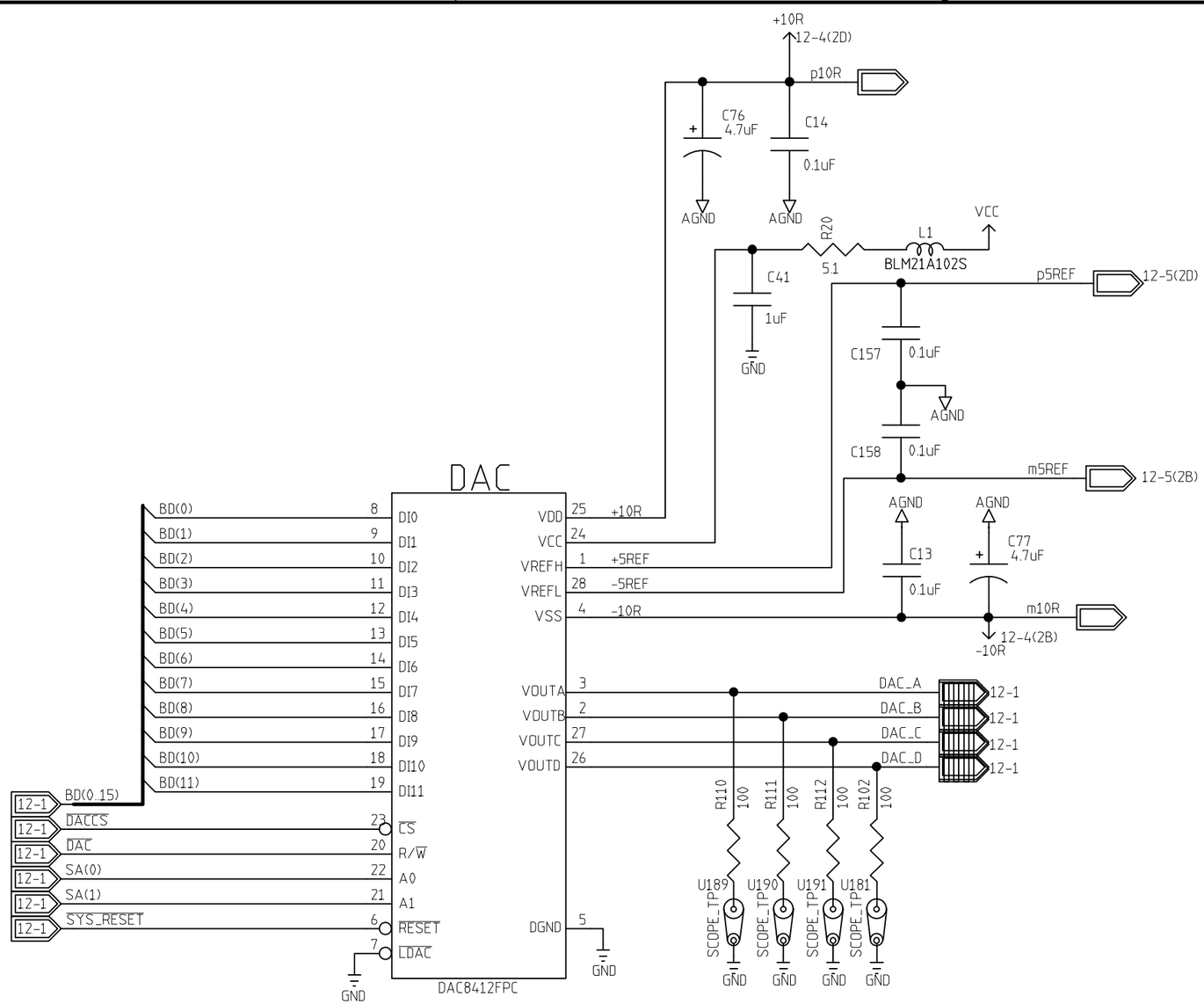


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	



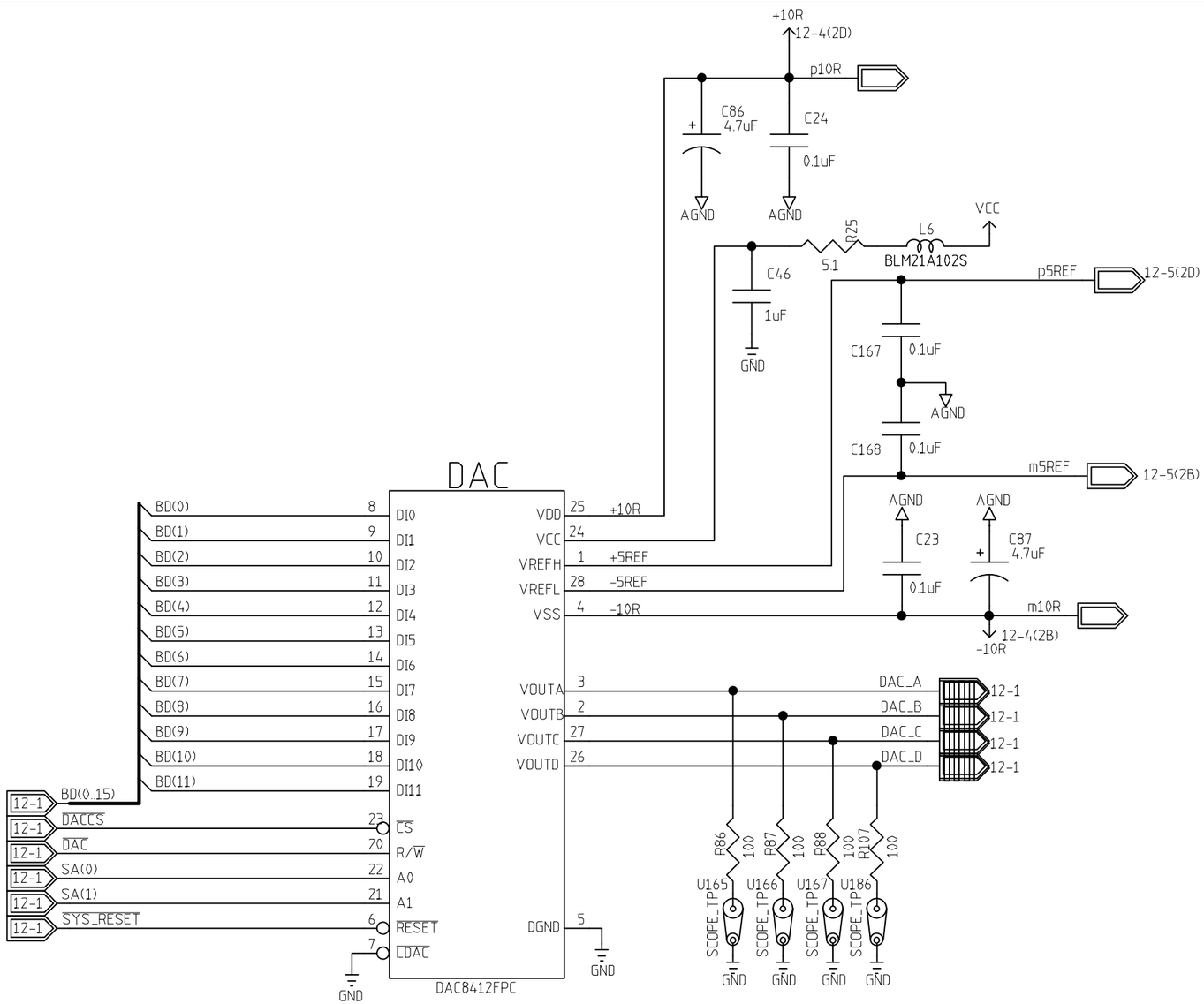
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	

U31

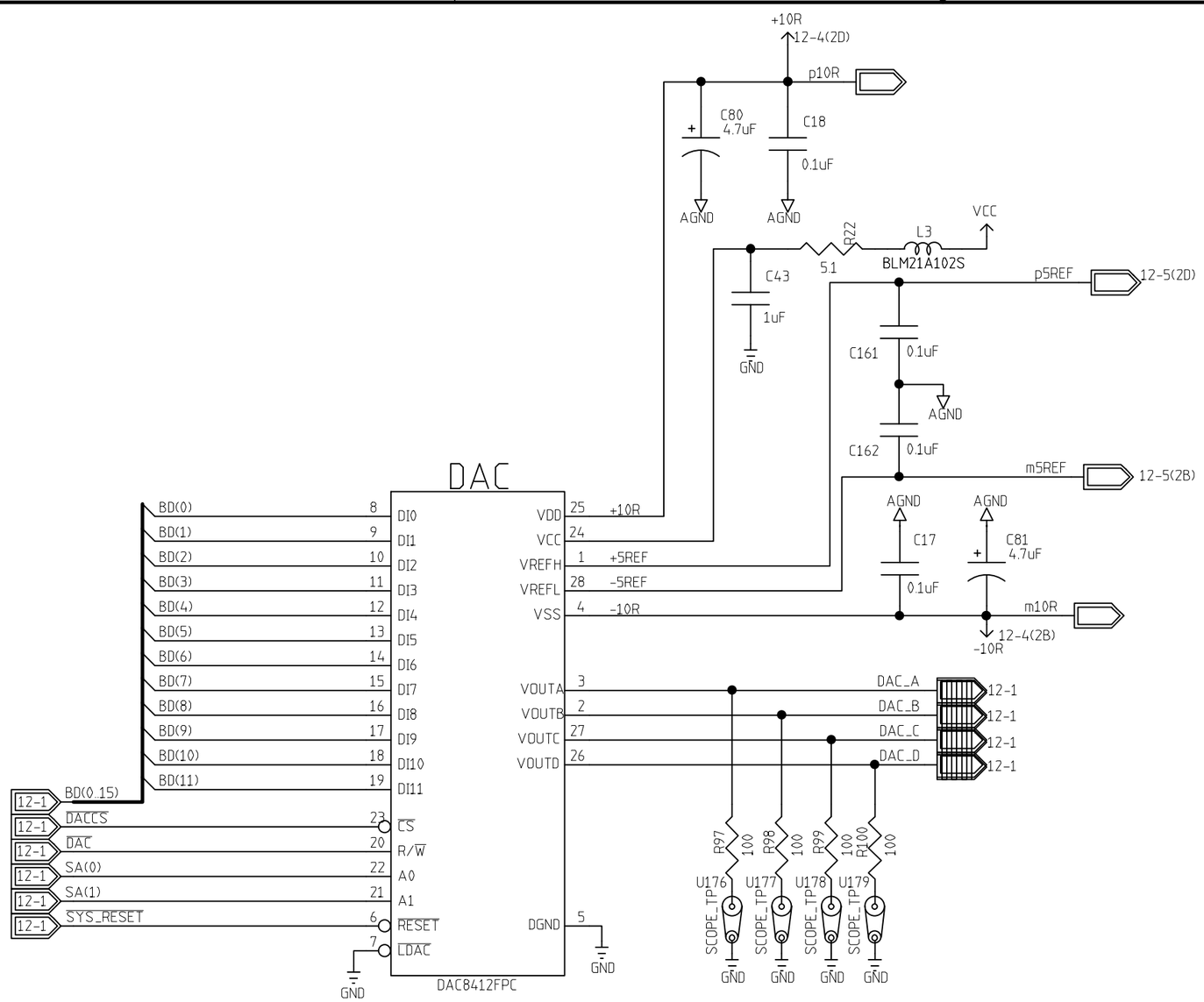


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	

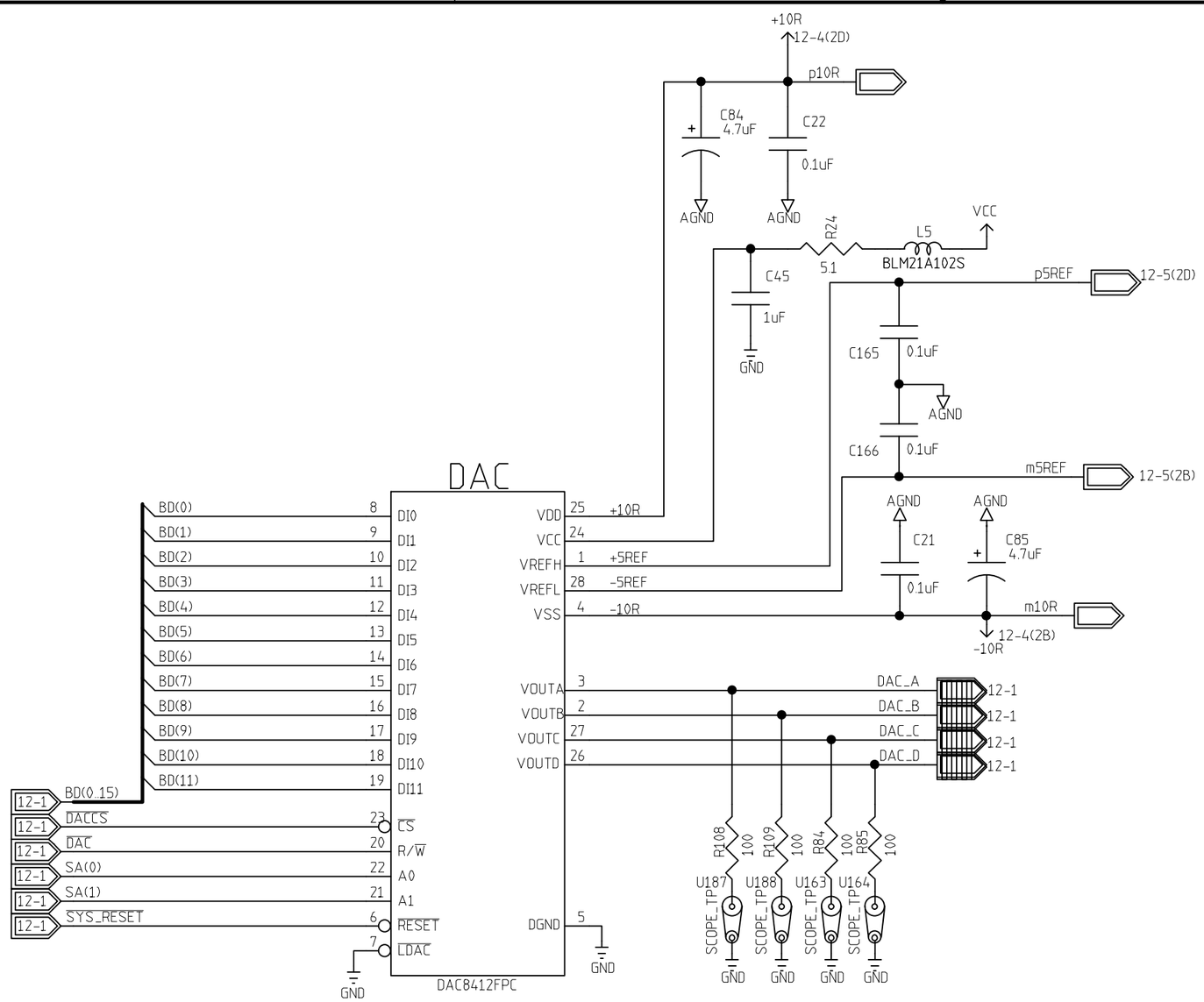


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	



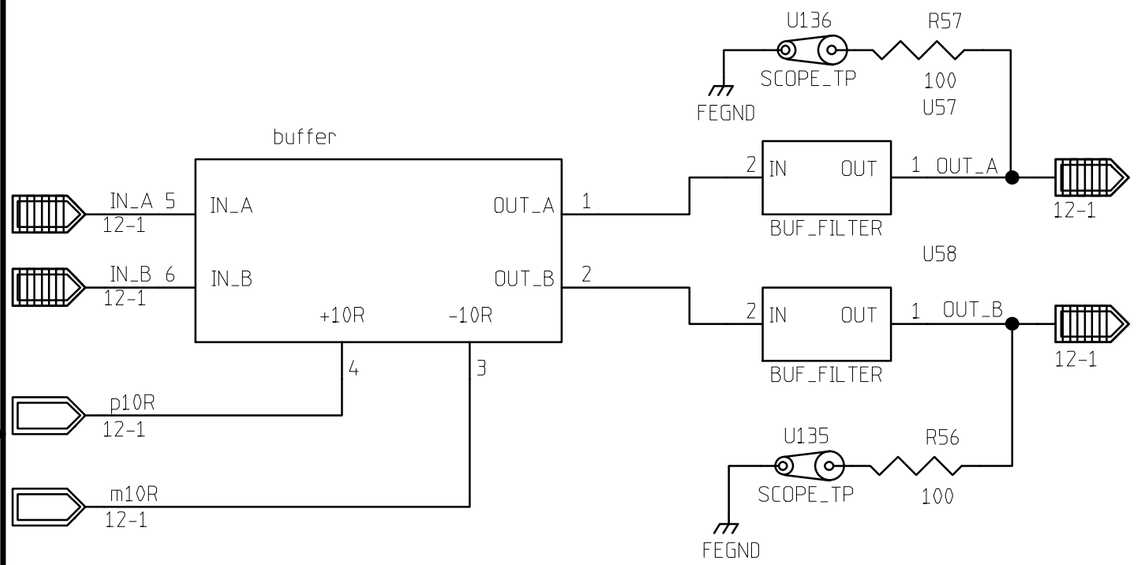
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	UNDER DEVELOPMENT	1-19-99	

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ ETT/ ES CDMS(E-891)
ZIP MODULE
DAC'S_1_TO_7

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 12-6	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



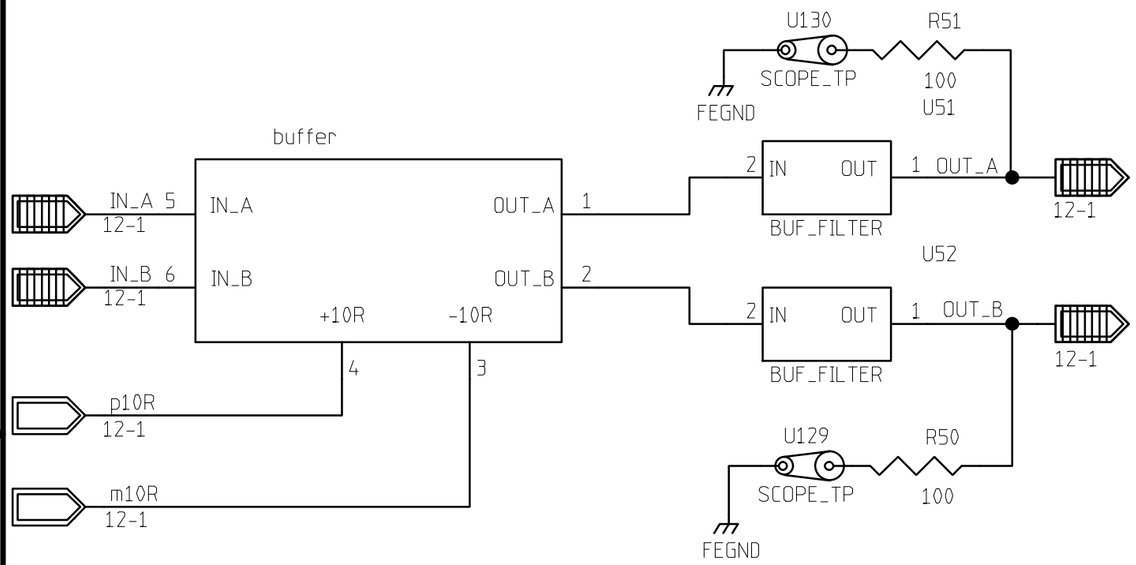
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U42 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



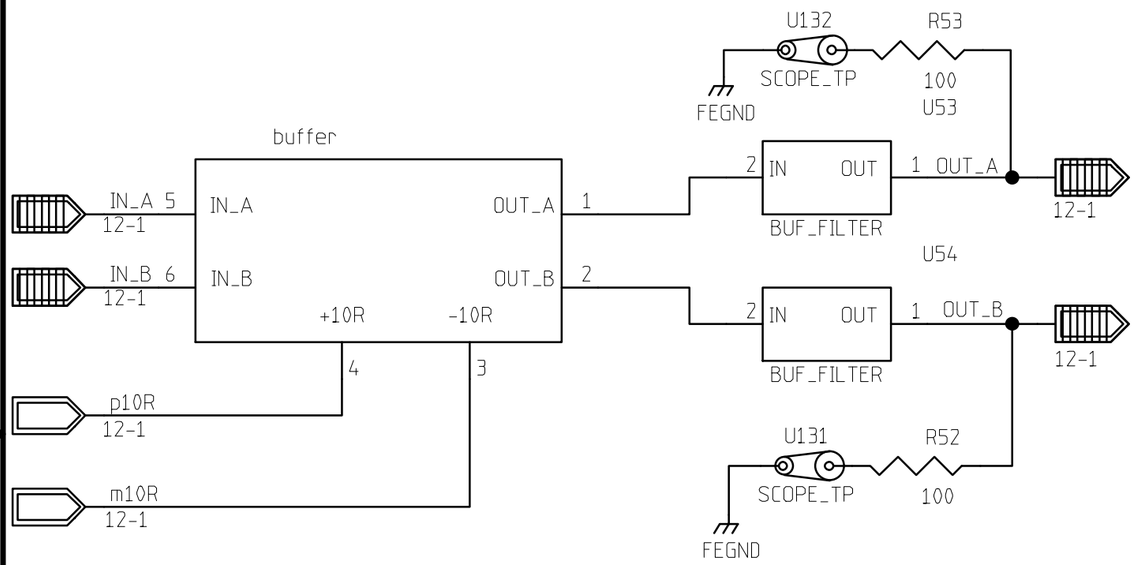
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U39 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



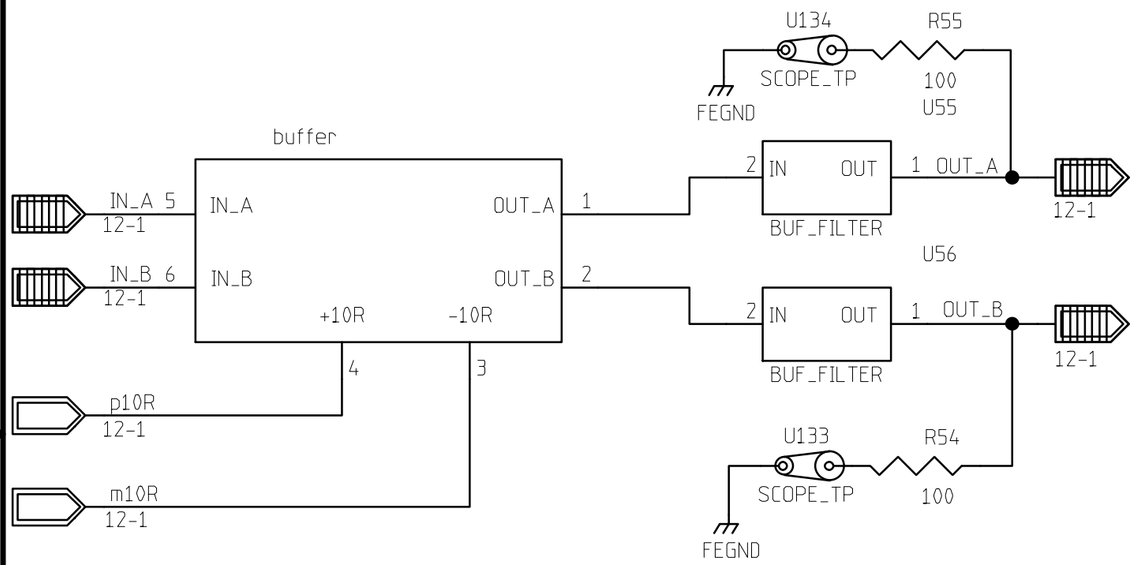
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U40 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



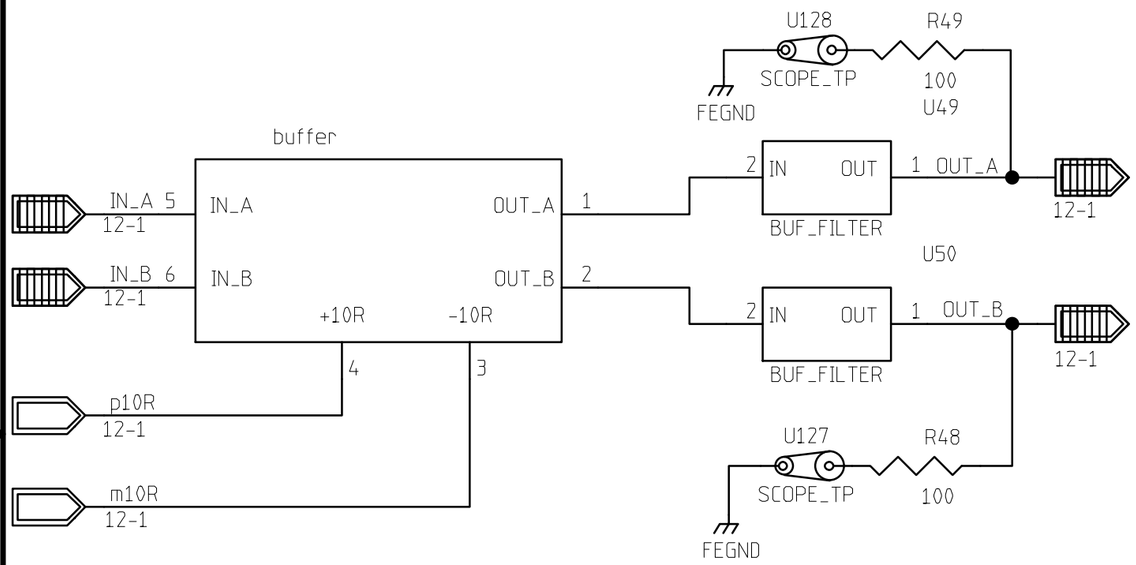
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U41 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



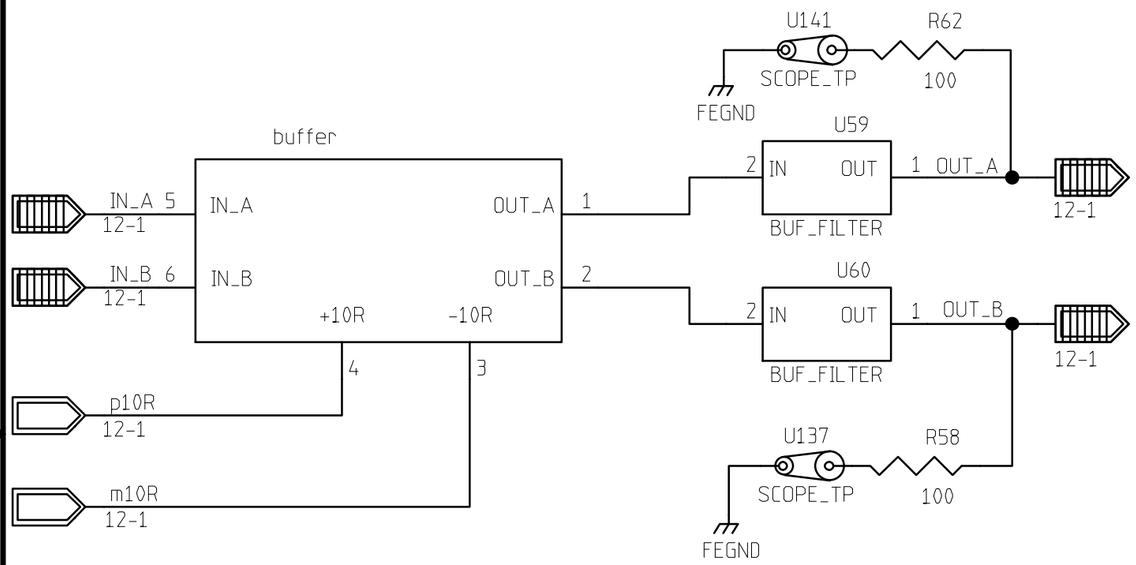
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U38 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



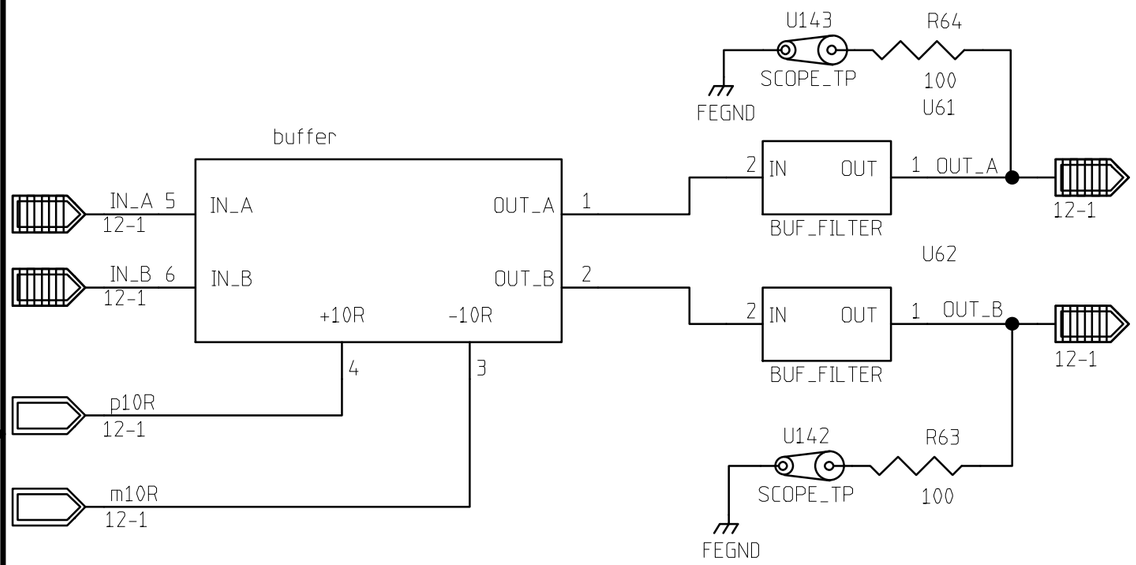
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U43 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE		SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



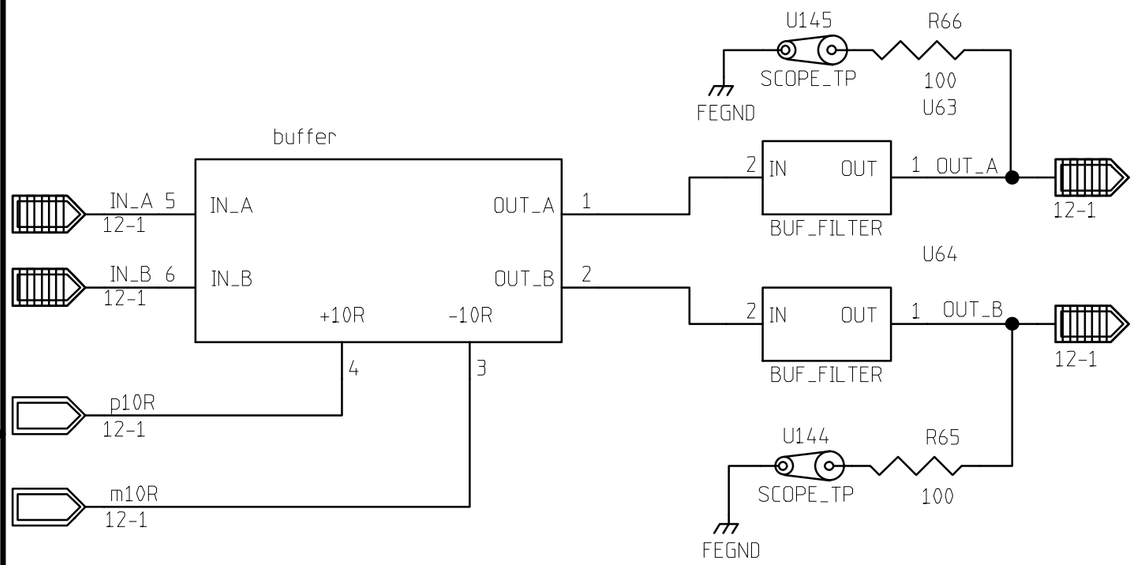
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U44 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



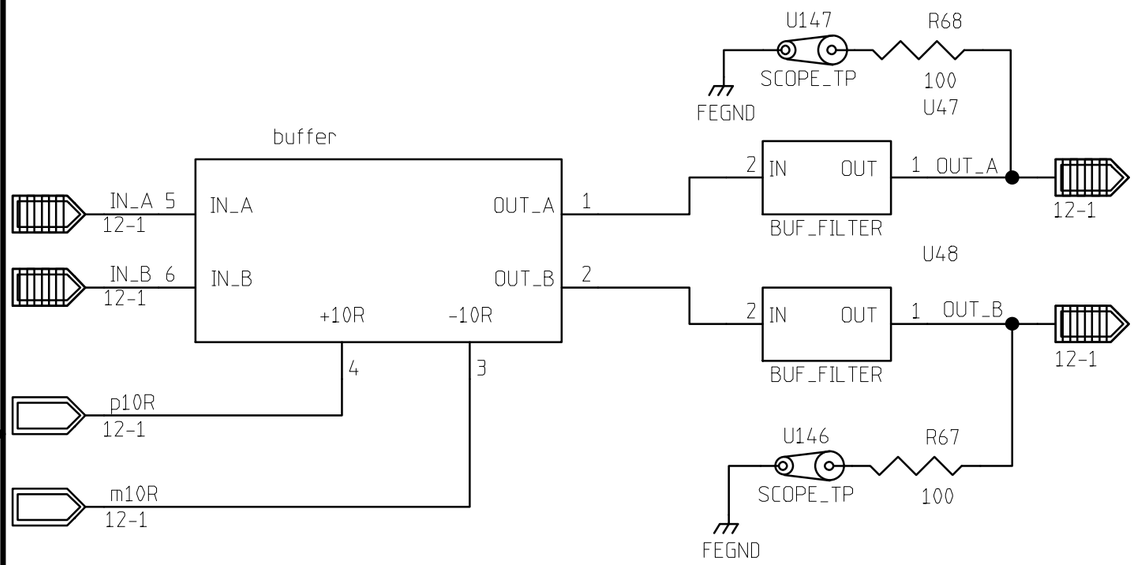
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U45 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



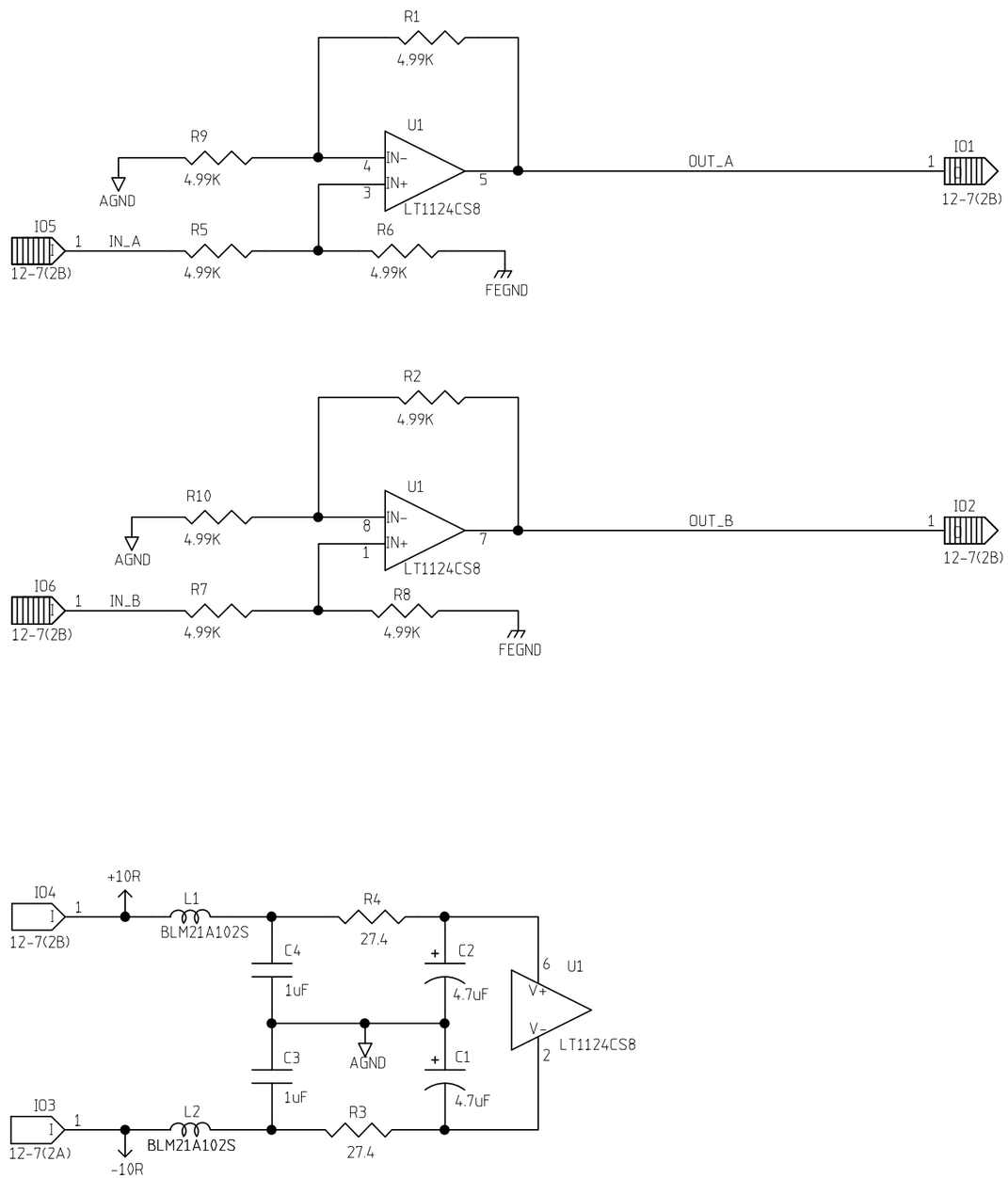
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	12/10/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
U46 DUAL NON_INVERTING BUFFER BLOCK

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 12-7

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



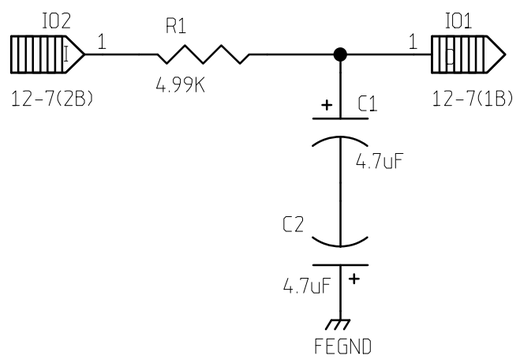
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/17/98
DRAWN	BRUCE MERKEL	11/17/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
DUAL NON-INVERTING BUFFERS

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 12-8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

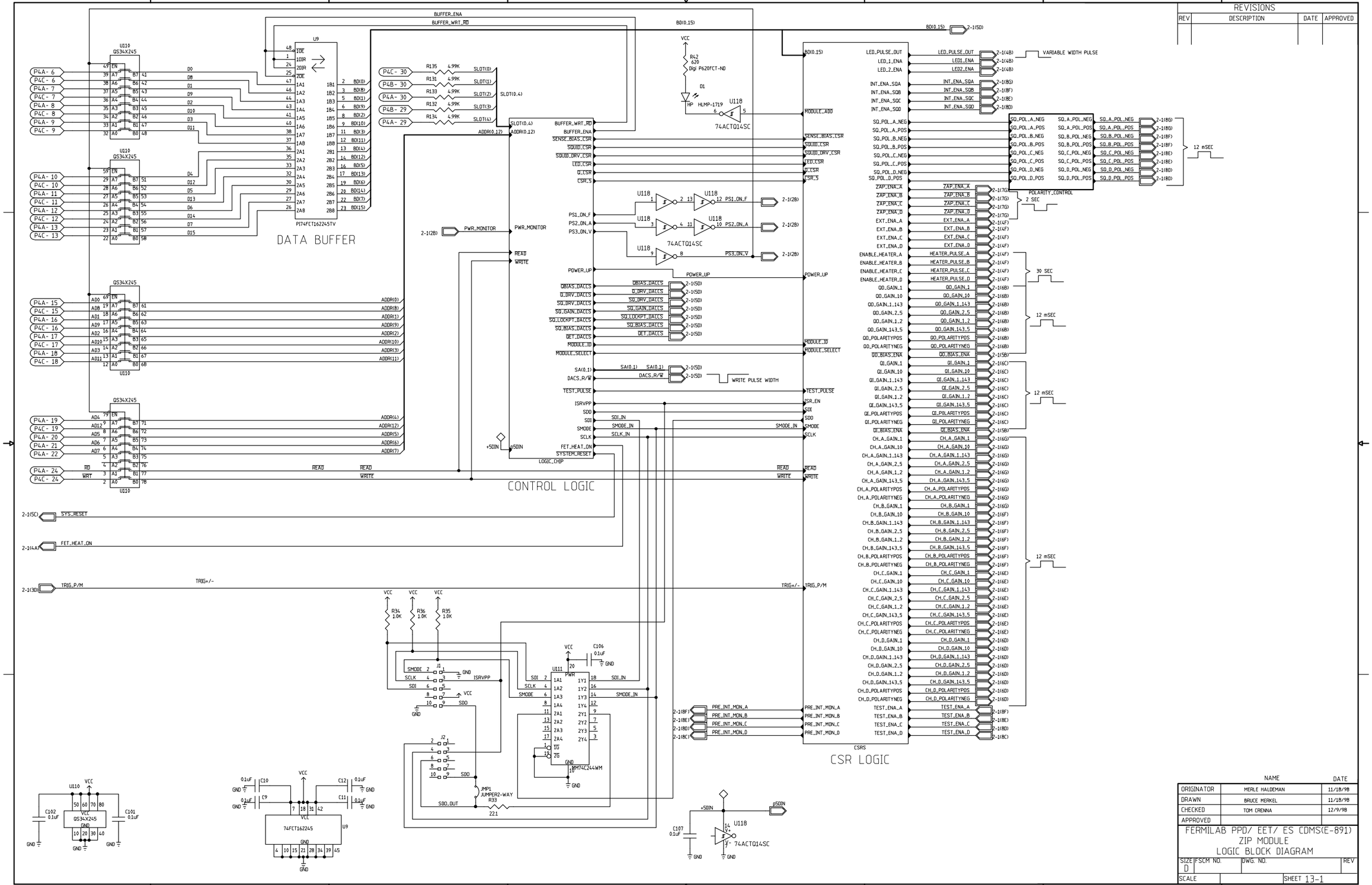


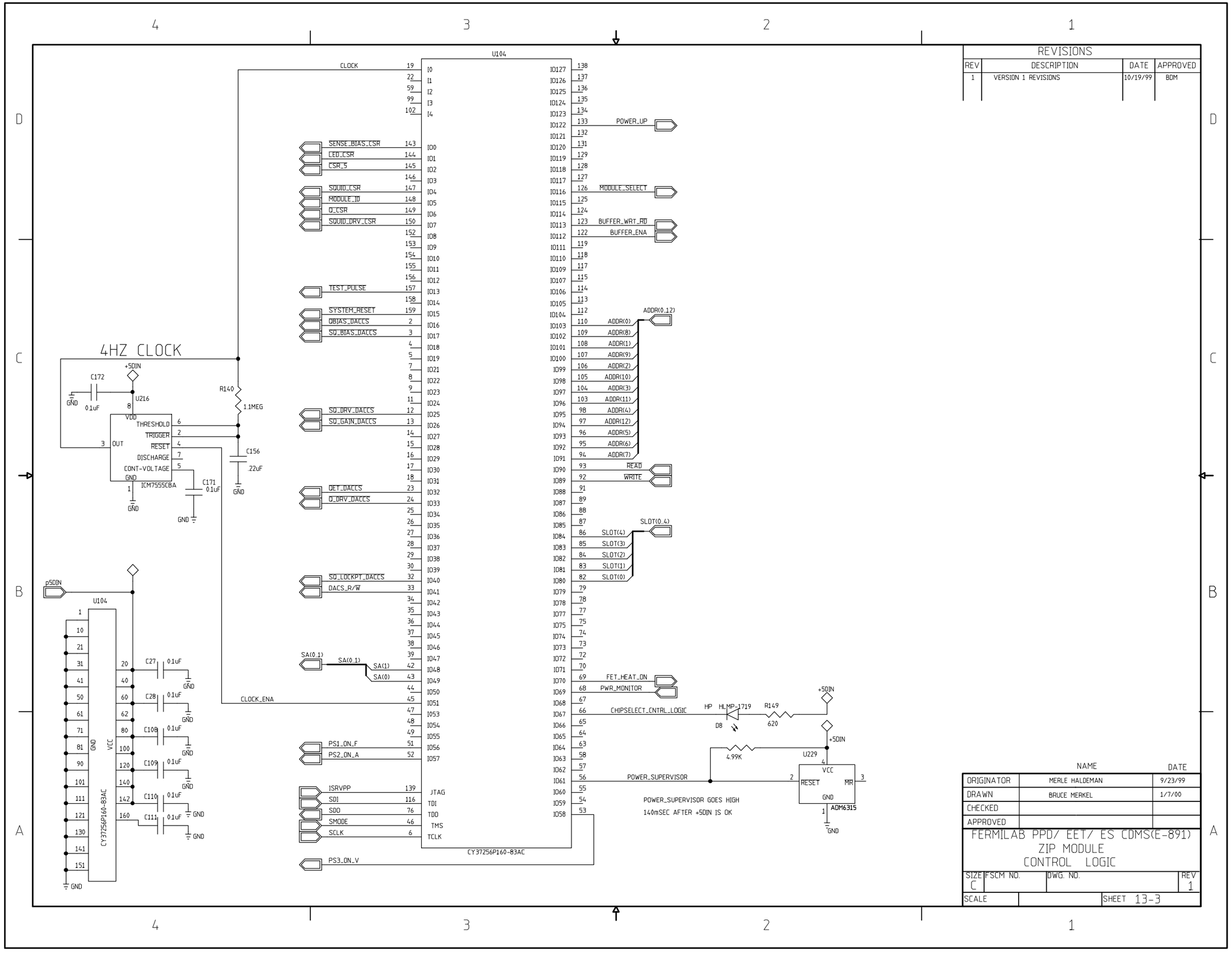
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	12/09/98
DRAWN	BRUCE MERKEL	12/09/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
BUFFER FILTER

SIZE	FSCM NO.	DWG. NO.	REV
A			

SCALE		SHEET 12-9


DATA BUFFER
CONTROL LOGIC
CSR LOGIC
U110 QS34X245
U9 PI74FCT162245TV
U118 74ACTQ14SC
U111 MM74C244WM
BUFFER_ENA
BUFFER_WRT_RD
PWR_MONITOR
SYS_RESET
FET_HEAT_ON
TRIG_P/M
VARIABLE WIDTH PULSE
POLARITY_CONTROL
12 mSEC
2 SEC
30 SEC
WRITE PULSE WIDTH
LOGIC_CHIP
JUMPER2-WAY
R33 221
R42 620 Digi P620FCT-ND
D1 HP HLMP-1719
R34 1.0K
R36 1.0K
R35 1.0K
R135 4.99K
R131 4.99K
R133 4.99K
R132 4.99K
R134 4.99K
C101 0.1uF
C102 0.1uF
C106 0.1uF
C107 0.1uF
C10 0.1uF
C9 0.1uF
C12 0.1uF
C11 0.1uF
REVISIONS
REV DESCRIPTION DATE APPROVED
ORIGINATOR MERLE HALDEMAN 11/18/98
DRAWN BRUCE MERKEL 11/18/98
CHECKED TOM CRENNA 12/9/98
APPROVED
FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
LOGIC BLOCK DIAGRAM
SIZE D
SCALE
SHEET 13-1

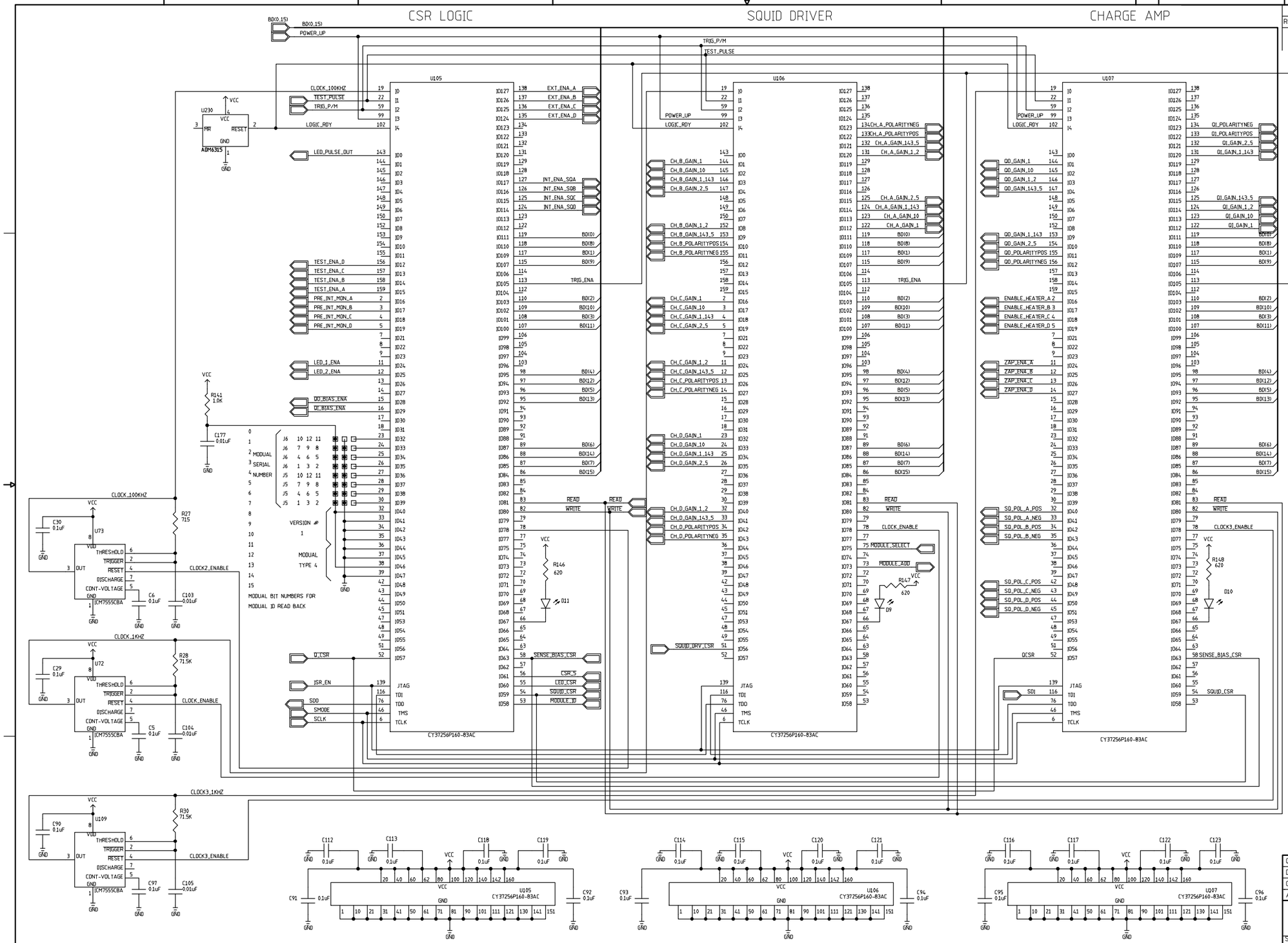


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	VERSION 1 REVISIONS	10/19/99	BDM

	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	9/23/99
DRAWN	BRUCE MERKEL	1/7/00
CHECKED		
APPROVED		

FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
CONTROL LOGIC

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 13-3	



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

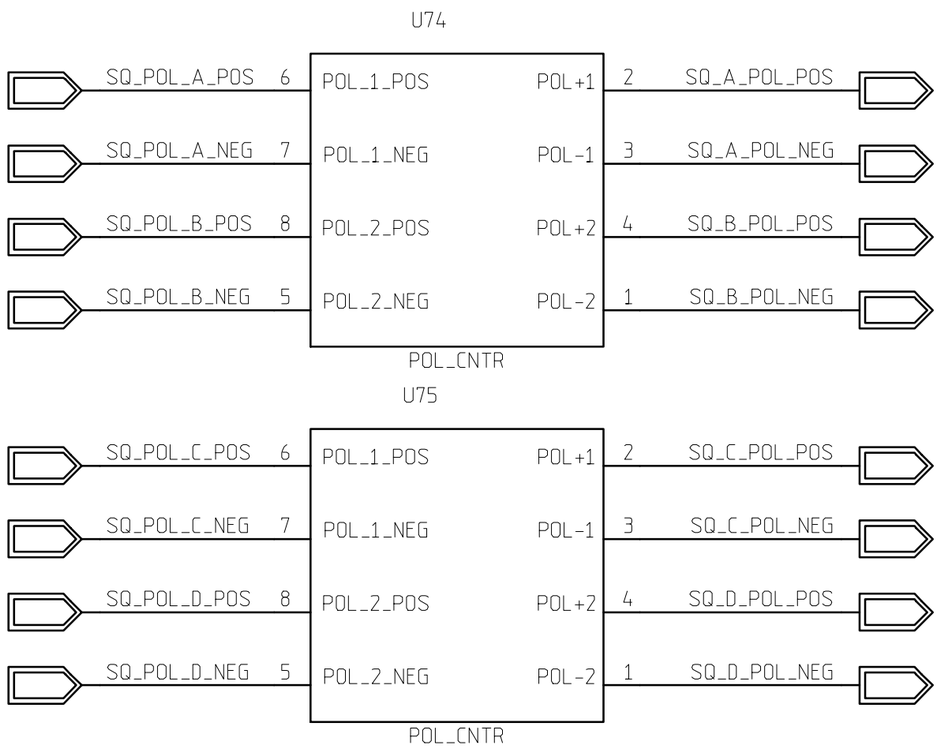
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	12/9/98
APPROVED		

FERMILAB PPD/ EET/ ES CDMS(E-891)
ZIP MODULE
CSR LOGIC

SIZE D | FSCM NO. | DWG. NO. | REV 1
SCALE | SHEET 13-4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

11mSEC ONE SHOT



	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

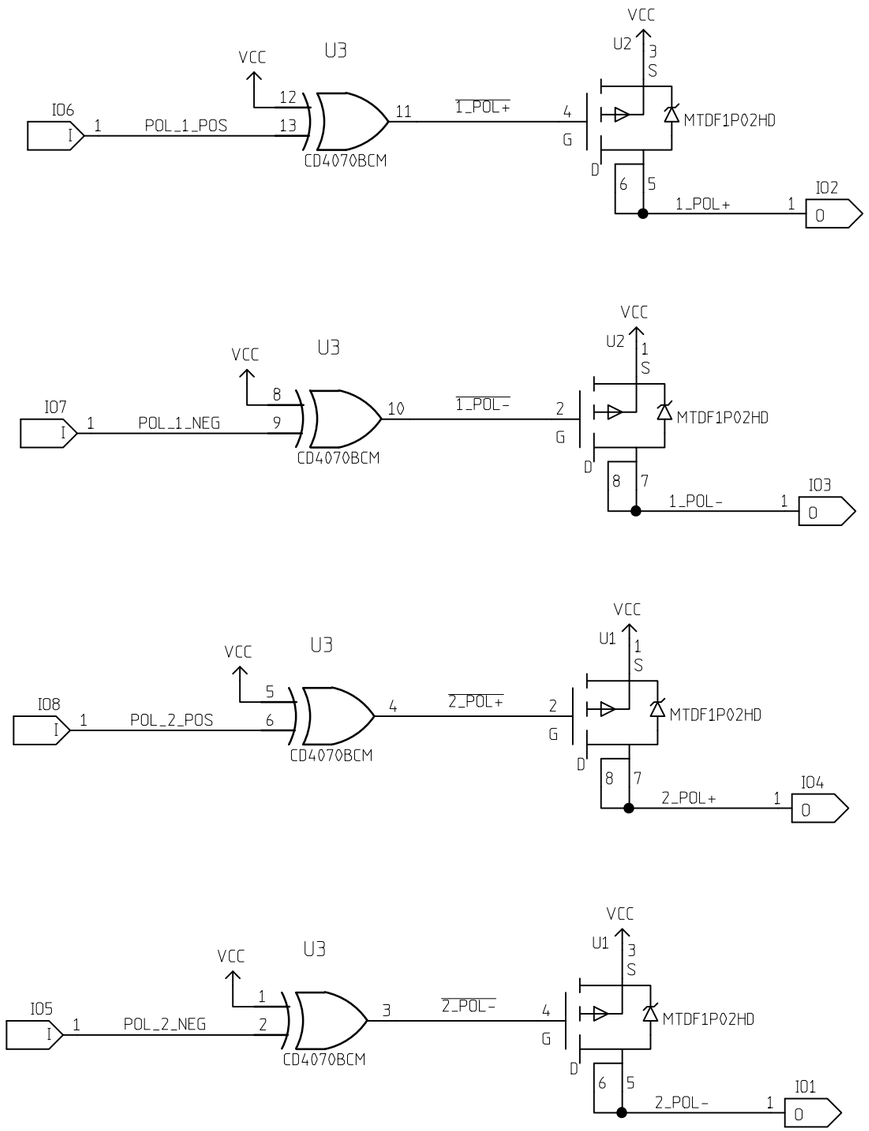
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POLARITY CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
A			1

SCALE | SHEET 13-5

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDER DEVELOPMENT	1-20-99	

11mSEC PULSE

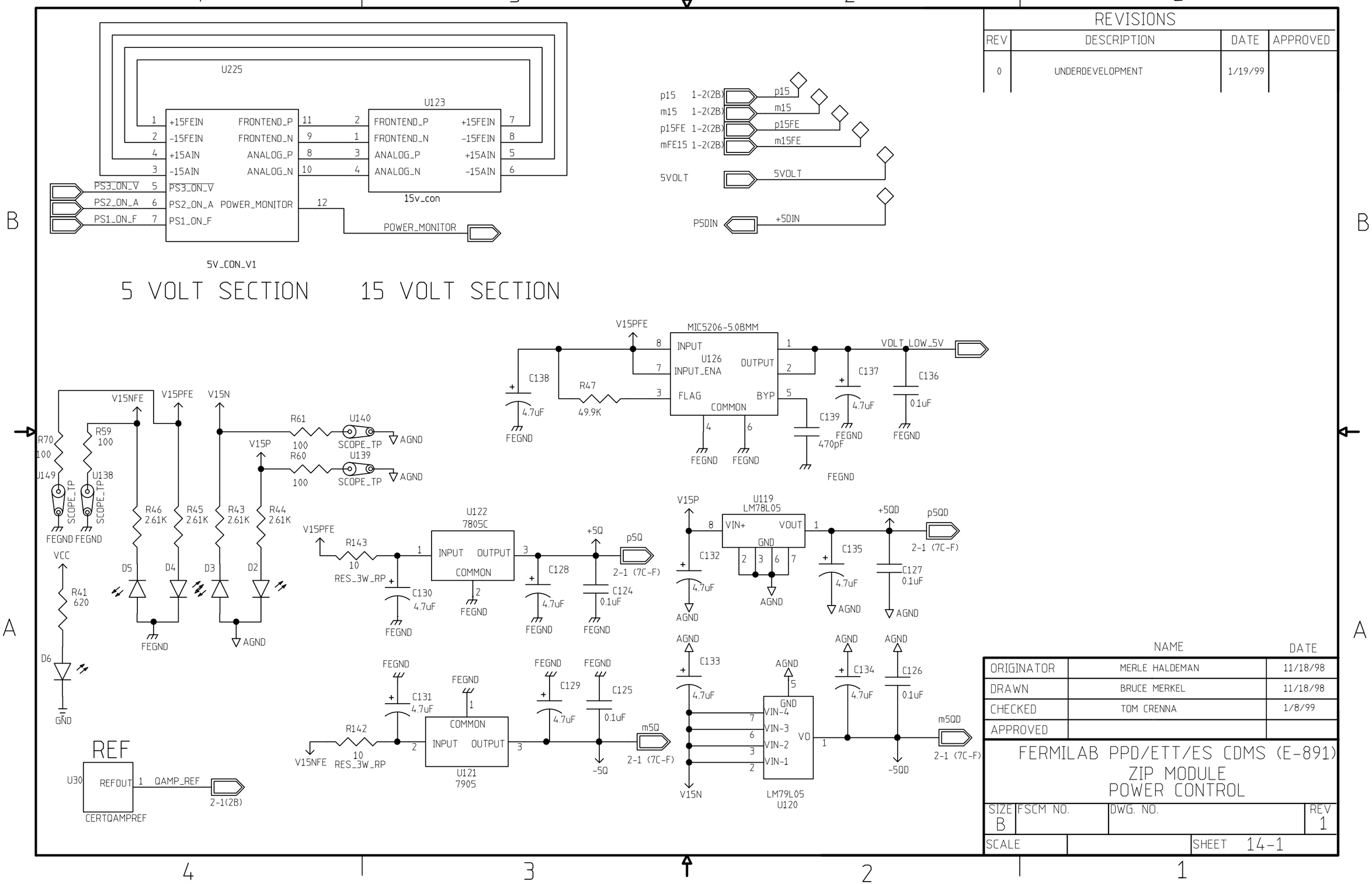


	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POLARITY CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 13-6	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	UNDERDEVELOPMENT	1/19/99	

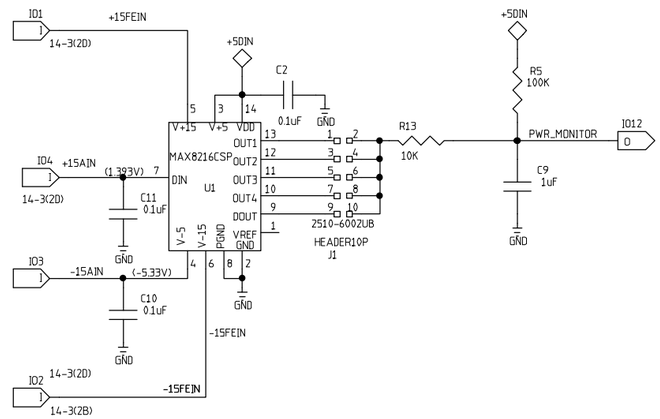


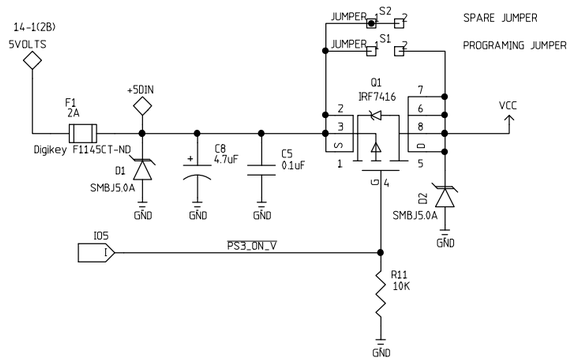
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

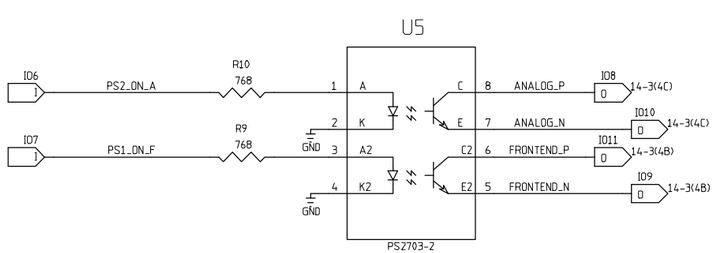
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
POWER CONTROL

SIZE	FSCM NO.	DWG. NO.	REV
B			1
SCALE		SHEET 14-1	

POWER ON SEQUENCER







REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

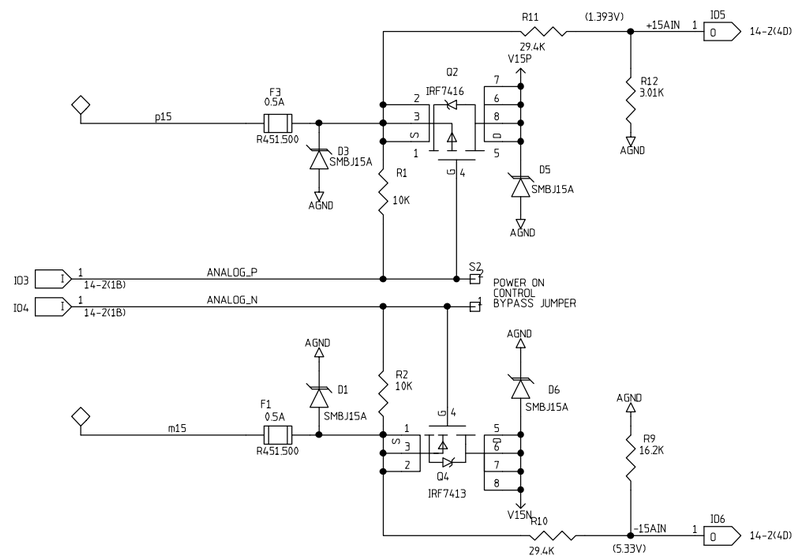
	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

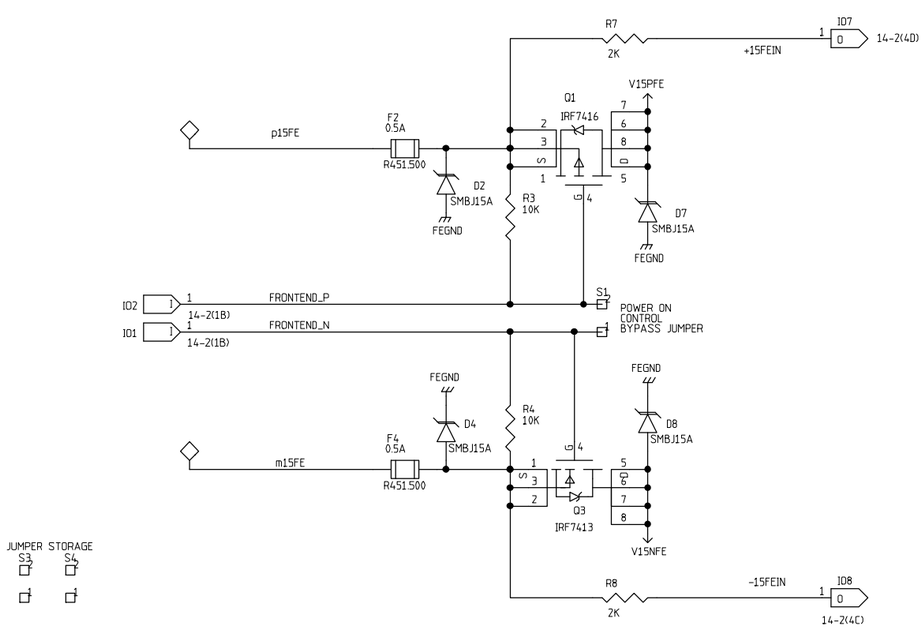
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
5 VOLT SECTION

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 14-2	

POWER ON SEQUENCER CONTINUED

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

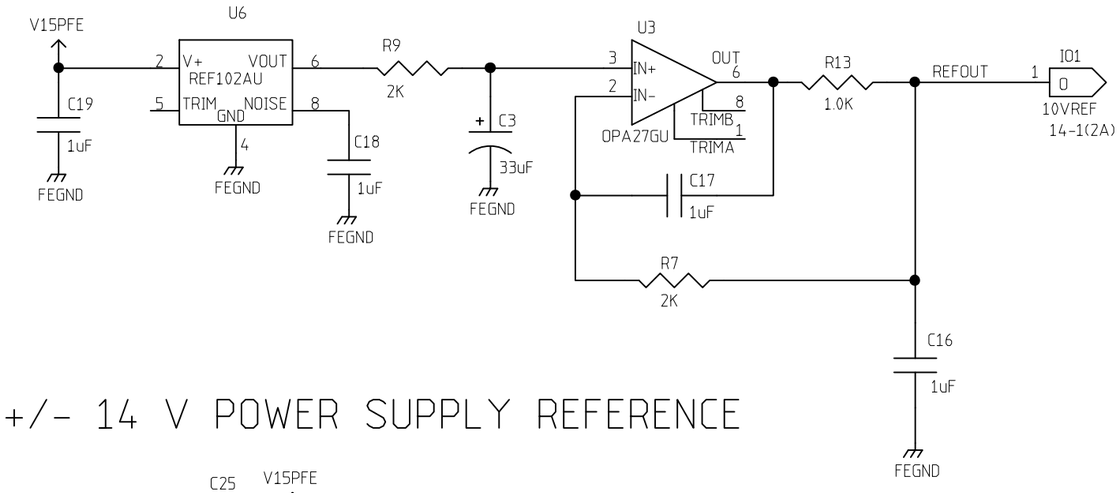
FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
15 VOLT SECTION

SIZE	FSCM NO.	DWG. NO.	REV
C			1
SCALE		SHEET 14-3	

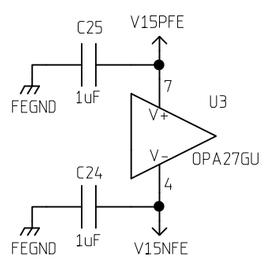
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

10 VOLT REFERENCE

10 VOLT BUFFER & NOISE FILTER



+/- 14 V POWER SUPPLY REFERENCE



	NAME	DATE
ORIGINATOR	MERLE HALDEMAN	11/18/98
DRAWN	BRUCE MERKEL	11/18/98
CHECKED	TOM CRENNA	1/8/99
APPROVED		

FERMILAB PPD/ETT/ES CDMS (E-891)
ZIP MODULE
Q AMP REFERENCE

SIZE	FSCM NO.	DWG. NO.	REV
B			

SCALE | SHEET 14-4