

ZIP Module V1 Users Manual: DRAFT Version

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General Module Description(Merle Haldeman)

The ZIP module is being designed for experiment E891, the Cold Dark Matter Search(CDMS). It's primary purpose is to control, and process signals received as a result of the detection of Weakly Interactive Massive Particles(WIMP's), and pass them on to the data acquisition system. The received signals enter the ZIP Module via a fifty-pin D-connector located at the top of the ZIP Module, and leave via a similar twenty-five-pin connector. The ZIP is a 9U module, the design of which essentially consists of the circuitry of ten, 3U modules. 9U and 3U are the respective sizes of the circuit boards. The ten 3U modules which were used to design the 9U Zip are as follows; one QET module, four SQUID modules, one DRIVER module, one Qbias module, two Qamp modules, and one FET TEMP module. . Below is a diagram(see fig. 1) of the ZIP module consisting of the connections between the individual 3U modules, in addition to the connections between the ZIP board and the detector. Following the diagram is a description of how each 3U module operates. While reading these descriptions please refer to the diagram(fig. 1), or for a more detailed understanding of how each individual circuit operates please refer to the 9U schematics located on the FERMILAB home page under experiment E891.

QET Bias Description:(Mark VanDrunen, revised 5/14/99)

QET stands for "Quasiparticle trapping assisted Electrothermal feedback Transition edge sensor"; also referred to as the "Sensor". The QET circuitry has the primary purpose of supplying the DC voltage bias to each of the four Transition Edge Sensors located on each semiconductor crystal in the detector. This sensor is a superconductor which is presently operating in the critical point, which is right at the temperature where a small change in temperature results in a large change in resistance. A WIMP colliding with the nucleus of the Silicon or Germanium detector loses some energy, which appears as a phonon. This phonon travels to the QET causing a small change in temperature, which results in a large change in resistance of the QET. The QET is operated in an essentially constant voltage mode. When the resistance makes a large change, the current through it makes a corresponding large change. The QET is placed in series with a coil, which produces a magnetic field in proportion to the current in the QET. A large change in QET resistance thus results in a large change in the magnetic field produced by the coil, which we'll call the sensor coil. In order to detect this current change, we use a device which is extremely sensitive to magnetic fields, known as a SQUID(Super-conducting Quantum Interference Device).

The QET module has four outputs, as can be seen on schematic sheet 5-1. Any output, QET_BIAS_x(where x can be A, B, C or D) can be connected to either, the "EXT_TEST_INPUT", or the appropriate input, BIAS_x. BIAS_x receives it's input from QET_x(where x is 1 or 2), which receives it's input from either QET_DAC_x(where x is A, B, C or D), or +5 volts. The QET_DAC output range is -5 volts to +5 volts, with a 12 bit resolution, and has a source impedance of approximately 5kohms. The QET_FILTER adds another 5kohm resistance for a total output impedance of approximately 10.2 kilo-ohms, for each QET_BIAS_x output. The +5 volts is applied as a pulse of power to heat the QET, and is controlled by the "HEATER-PULSE".

The function of the heater pulse is to bring the QET to the critical operating point, should it become completely superconducting. When completely superconducting, the QET has no resistance and dissipates no power, as a result, the Electrothermal Feedback mechanism ceases to function. Applying the excessive voltage(5 Volts through approximately 5.7kohm) to the QET, forces it out of the completely

superconducting mode. The heater pulse has an adjustable width between 10 milliseconds and 160 milliseconds in 10 millisecond steps, or between 100 and 1600 milliseconds in 100 millisecond steps. During the heater pulse width the output impedance is reduced from approximately 10.2 kilo-ohms to approximately 5.1 kilo-ohms.

The QET BIAS section has one output called QET_BIAS. The user can choose to let through one of three different inputs (EXT_TEST_INPUT, VOLT_LOW_5V, or QET_DAC). If HEATER_PULSE_1 (CSR Logic Section) sends a high to the input of two gates on U1 (DG413) the gate restricting the signal VOLT_LOW_5V (Power Section) closes and passes it through. It also opens the other gate in series with signal QET_DAC_1 (DAC Section) not allowing it to pass. If a low is sent then QET_DAC_1 is passed through. The signal that is passed through is called BIAS_A.

BIAS_A then goes into another gate. The user now decides to let BIAS_A signal or EXT_TEST_INPUT signal (EXT_TEST_RECEIVER Section) to pass through. This choice is made by sending a high or low signal from the CSR called EXT_ENA_A. If the signal is high it allows EXT_TEST_INPUT to pass through the QET BIAS section. Also, the gate restricting BIAS_A is opened. This is because the signal EXT_ENA_A is passed through an inverter before it reaches this gate. If the signal EXT_ENA_A is low BIAS_A is passed through and EXT_TEST_INPUT is not. The signal that makes it through is called QET_BIAS_A and it is sent out a backplane connector. A truth table is shown below telling which signal is outputted for the different gate sequences.

| EXT_ENA_A | HEATER_PULSE | OUTPUT |
|---------------------|---------------------|----------------|
| 0 | 0 | QET_DAC_1 |
| 0 | 1 | VOLT_LOW_5V |
| 1 | X | EXT_TEST_INPUT |
| | | |
| Note: X= Don't Care | | |

SQUID Description:(Merle Haldeman Revised 5/7/99)

The SQUID Module was designed to receive signals from the SQUID(Superconducting Quantum Interference Device) near the detectors. SQUIDs consist of an arrangement of super-conducting, josephson junctions that can quite easily measure a single quantum of magnetic flux (200 nanogauss-cm²), and voltages as small as 10 fempto volts.

The SQUID circuitry consists of several subcircuits which are described below.

SQUID Front End:(Tom Crenna Revised 5/11/99):

The squid front does two things; it sends a bias to the SQUID for proper operation and receives the signal(SQUID_SIG) from the Squid. The SQUID bias voltage is sent directly to the SQUID via a 20k resistor(R7). The signal from the SQUID passes relay U1 (Teledyne,712 DPDT relay), then on to U2 (AD797) for amplification, and finally to the output (AMP_OUT). U2 is an ultralow distortion, ultralow noise op-amp, which is being used here as a preamplifier to provide a gain of approximately 16.4. The SQUID bias voltage is present at the amplifier input with the SQUID signal superimposed on it. The SQUID_BIAS voltage is controlled by the SQUID BIAS DAC. In order to compensate for this bias voltage at the input of the amplifier, there is another input (LOCK_POINT_ADJ), coming from the SQUID LOCKPNT DAC, and going to the negative input of the AD797 amplifier (U2), via R4. This input creates the proper offset to compensate for the SQUID_BIAS voltage. During the time the relay (U1) is passing the SQUID signal to amplifier U2, the ZAP circuitry capacitor is being charged or being held in a charged state. For an explanation of the ZAP circuitry, see SQUID ZAP control.

SQUID Variable Gain Amplifier(Tom Crenna)**SQUID Feedback Integrator(Andy Paullin)****SQUID Feedback Polarity Selection (Tom Jankovsky Revised 5/10/99)**

The SQUID polarity section changes the polarity of the SQUID feedback Summing Amplifier output signal. Activating either the *SQUID_POL-* or *SQUID_POL+* line changes the corresponding polarity to inverting or non-inverting. The polarity reversal is accomplished by utilization of a latching a relay that reroutes the signal. The signal is routed to the inverting input of the op-amp for negative polarity, or to the non-inverting input for positive polarity. The *FEEDBACK* signal leaving the polarity selection stage, is sent to both, the feedback monitor amplifiers and out the backplane, to the detector.

Squid Feedback Monitor : (Mark Van Drunen, Revised 5/12/99)

The squid feedback monitor selection circuitry, acts as a two-pole-single-throw switch which allows either the *FEEDBACK* signal (from the polarity section) to pass through U8, or the *V_GAIN_OUT* signal (from the squid variable gain amplifier section) to pass through U7. The CLC410AJE is a low noise, current feedback amplifier which has a fast disable/enable control, enabling the amplifier output when the control is high, and disabling the amplifier output when the control is low. The signal coming from the enabled amplifier is called the *MONITOR* signal, and is sent to the appropriate SQUID driver section.

The *FEEDBACK* signal is passed through op-amp(U8) to the driver section only when *FEEDBACK_SEL* is sent a high from the Squid Feedback Logic Section. This is controlled by the *MONITOR_SEL* signal from the CSR(control status register), which is housed in U105. Pins 2,3,4, and 5 of U105 are the four *MONITOR_SEL* lines for the four squids. The U105 is a surface mountable, programable logic device manufactured by Cypress Semiconductor, which was programmed using VHDL.

The *V_GAIN_OUT* signal is passed through the op-amp(U7) to the driver section only when *V_GAIN_OUT_SEL* is sent a high from the Squid Feedback Logic Section. This is controlled indirectly by the same pins on the CSR that control *FEEDBACK_SEL*. When *FEEDBACK_SEL* is sent a high from the *MONITOR_SEL* line the *V_GAIN_OUT_SEL* is at ground and visa versa. Thus the *MONITOR* signal will come from *FEEDBACK* or *V_GAIN_OUT*.

SQUID Feedback Logic(Mark Van Drunen, Revised 5/18/99)

The Squid Feedback Logic (schematic sheet 3-8) allows the user to choose whether or not, the V_GAIN_OUT signal (schematic sheet 3-4) will pass through the integrator. This is accomplished turning the FET SWITCHs on or off. Plus 5 volts on the gate turns the FET SWITCH on and -5 volts on the gate turns the FET SWITCH off. If the user chooses not to let signal pass through, FET SWITCH U3 is turned off and FET SWITCH U4 is turned on. The circuitry on schematic sheet 3-8, provides the level shifting required between the CSR (control status register) LOGIC SECTION, and the FET SWITCH gates. These procedures are controlled by setting the appropriate bits in the CSR.

The Squid Feedback Logic is controlled by one signal FB_CLOSE sent from pins 124, 125, 126, and 127 of U105 in the CSR Logic Section. If FB_CLOSE arrives at the base (pin 1) of Q1 a Level Translator as a high level, Q1 is off and the collector(pin 3) should be at -5 volts. On the other hand, a low at the base of Q1 results in Q1 being turned on hard, and the collector will be approximately +5 volts. The high or low then goes into a CMOS Quad, Dual input, Exclusive-OR Gate. If the inputs are equal it outputs a low level and if they are different it outputs a high level. Three of the four gate outputs are signals that continue to more circuitry (FET_A, TRIM_CAP, and FET_B). If FB_CLOSE is high, FET_A output and TRIM_CAP output are high, while FET_B output is low. When this happens the integrator is not used. The capacitance in the feedback of the integrator is discharged by turning on FET SWITCH U4, and V_GAIN_OUT signal to the integrator is blocked by turning off FET SWITCH U3. When FB_CLOSE is low, the two FET SWITCHES change state and the integrator, integrates the V_GAIN_OUT signal.

SQUID ZAP Control(Tom Jankovsky, Revised 5/11/99)

The purpose of the SQUID ZAP control is to issue a voltage, the level of which, is determined by the ZAP Voltage DAC. This voltage is sent to the SQUID portion of the detector causing it to heat up. Heating pushes the SQUID out of the super conductive region making the Josephson Junctions resistive. This resistance dissipates trapped flux lines as heat. Discharging a 0.022F capacitor which has been charged to a voltage determined by the ZAP Voltage DAC, provides the needed ZAP voltage.

The SQUID Zap control uses a fixed width, 250-millisecond mono-stable input pulse to control the discharge time of the Zap Capacitor (C5) onto the SQUID. The 250ms input pulse arrives from one or more of the CSR logic section via control lines: ZAP_ENA_CSR_A, ZAP_ENA_CSR_B, ZAP_ENA_CSR_C, ZAP_ENA_CSR_D. When a LOW arrives on these lines, it is exclusively ORed with front end ground, producing a LOW at the output of (U5). This LOW signal turns the FET (U1 & U2) on, energizing the relay in the SQUID front-end section. While the relay is energized, the zap capacitor discharges into the SQUID portion of the detector, removing the trapped flux lines. When the relay is not energized, the zap capacitor is being charged via the ZAP_V line. The ZAP_V line is supplied by a special op-amp (U4) capable of driving highly capacitive loads. The input of the op-amp is supplied by a DAC along the ZAP_DAC line.

The SQUID module can be operated in either calibrate, measure, or zap mode. In the calibrate mode the integrator has its input opened and the integrator is placed in the reset mode. In the measure mode the integrator has its input connected, and the integrator is placed in the integrate mode. The zap mode puts the SQUID module either in the "Synchronous" or "Asynchronous" zapping mode. In the asynchronous mode writing to a specified address will zap the circuit. In the synchronous mode writing to a specified address will arm the zapping circuitry, causing the circuit to get zapped by a subsequent "TRIG" signal received from the backplane. After a synchronous zap, the zapping circuit is automatically disarmed. A

zap voltage is provided in values of 0, 1.25, 2.5, or 3.75 volts. The width of the zap can be set between 100 milliseconds and 1,600 milliseconds in 100 millisecond increments. The SQUID module also has the capability of reading back the status of the arming circuitry with the zapper armed bit via the CSR. Once signals have been received and processed through the SQUID module they are sent to the SQUID feedback coil near the detector and to the Driver module.

Driver Description:(Andy Paullin)

The Driver module has six independent analog amplifier channels, each of which has a selectable gain and polarity, as well as controllable DC input offset voltage. The gain choices are 1, 1.43, 2, 5, 10, 14.3, 20, and 50, and the polarity can be inverting or non-inverting for any gain setting. The 3dB bandwidth of each channel is approximately 1 MHz wide. Offset is done at the input, and as a result, is unaffected by the gain and visa-versa. The input offset is adjustable over a range of -5 to +5 volts, in approximately 2.44 millivolt steps. Each channel is designed to drive a 50 ohm impedance with shunt capacitance of up to 1000pf. The Driver receives four of its inputs from the four SQUID channels, and the other two drivers get their input signals from the two Qamp channels. The SQUID and Qamp signals are processed via the Driver and sent to the data acquisition system for analysis.

Gain and polarity of each driver channel is controlled by latching relays. This type of relay requires power only during the change of state (approximately 12 milliseconds); the remainder of the time the relay coil is disconnected from power with one end of the coil grounded. The input of each driver channel consists of a pseudo instrumentation amplifier made up of U9, U10 and U13. U9 and U10 make up the input stage, which has a full differential input and differential output U9 accepts the input signal, and U10 accepts the offset to be subtracted from the input signal. The offset voltage is provided by a 12 bit DAC capable of being adjusted over an approximate range of -5 Volts to +4.9975 Volts , in 2.5millivolt steps. The outputs of U9 and U10 are converted to a single ended output by U13. U13 however is incapable of driving a 50 ohm load, and is thus buffered by U14. The feedback for U13 includes U14 in order to minimize additional gain and offset errors introduced by U14.

The gain of the first stage is 20 when the two 6.8k ohm resistors are switched in by U4, or a gain of 2 when the two 357 ohm resistors are switched in by U4. The gain of the second stage is 5, when only the 5k ohm resistors are in the feedback circuitry. When the 3.32k ohm resistors are placed in parallel (by U3) with the 5k ohm resistors, the second stage gain is 2. The gain is 1.43 when the 2k ohm resistors are placed in parallel with the 5k ohm resistors by U1. When all three resistors, 5k, 3.32k and 2k, are placed in parallel, the second stage gain is 1. It is one half of the combination of the first and second stage gains which determine the actual driver gain. The one half comes from the 49.9 ohm resistor in series with the U14 output, driving a 50 ohm load.

Qbias Description: (Tom Jankovsky Revised 5/10/99)

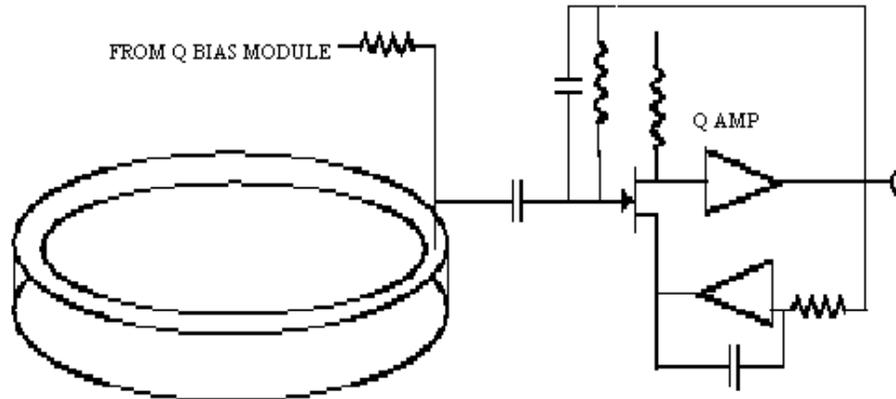
The Qbias module provides two DC voltage outputs for supplying bias voltage to the detector charge collection segments, and two currents for flashing the trapped-charge-neutralizing LED's. All four outputs are bipolar and have their magnitudes controlled via individual 12-bit DACs. The detector is either silicon or germanium, and has dimensions of approximately 7.5 cm in diameter, and 1 cm thick. The charge-collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.



One of the voltage outputs is connected to each of these two charge-collecting electrodes. Each bias voltage has an output range of -5 to +5 volts, with 2.44-millivolt resolution. The data entered into the CSR can cause these detector electrodes to be connected to their respective outputs, or connected to FEGND. Another function of the Qbias module is to provide bias current for energizing two LED's. For this purpose, the Qbias module has two current sources that are able to source, or sink, up to 5 milliamps, with 2.44-microamp resolution. These two current sources are controlled independently, and can be turned off or on. When on, they can be turned on continuously, or operated in a pulsed mode. In the pulsed mode, the sources can be put in the single pulse mode (requiring a write to this module for each pulse generated), or repetitive mode. In the single pulse mode, the pulse width is adjustable via digital control. In the repetitive mode, both the pulse width and the pulse rate are adjustable via digital control.

Qamp Description:(Merle Haldeman, Revised 5/7/99)

The Qamp module is used in conjunction with the front-end FET to convert charge collected from the detector to a voltage which ultimately gets sent to the data acquisition system, via the Driver, for digitization. The detector has a disk shape, approximately 7.5 cm in diameter, and 1 cm thick. The charge collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.



A separate, individually controlled, DC bias voltage is provided for each of these two charge-collecting electrodes on the detector, by the Q_{bias} module, described above. The charge from each of these two charge-collecting electrodes, is AC coupled to the two JFET-Gates through DC Bias blocking capacitors. Because the JFET is a voltage controlled device, it is very important to minimize extraneous voltages at this node. Voltage on a capacitor is proportional to both capacitance and charge; $V = Q/C$; a change in either one results in a change in voltage. The stray capacitance (C_{stray}) between the JFET-Gate and it's surroundings is difficult to control and variations in this stray capacitance, due to mechanical vibrations(microphonics) is extremely difficult to remove. If Q on C_{stray} is zero, then changes in C_{stray} due to mechanical variations such as vibrations, will not produce corresponding changes in the voltage on the FET Gate. Reducing V to zero would obviously make Q zero, and thus independent of variations in C_{stray} . The simplified theory of operation of the Q Amp is as follows. There are two feedback loops at work in this module, as illustrated above; a fast one (the upper path in the illustration) and a slow one (the lower path in the illustration), each having an individual separate purpose. The slow loop, which drives the JFET-Source, serves the purpose of keeping the DC output of the Q Amp (AD840 pin 10) at zero volts. This is important because the Q Amp output has a DC connection to the JFET-Gate. This DC connection is via resistor having a resistance in the vicinity of 4×10^7 ohms. The slow loop also keeps the JFET at the correct operating point when the JFET-Gate is essentially at zero volts with respect to ground, by forcing the JFET-source positive, keeping the Gate-Source junction back-biased .

The operation of the slow loop is as follows; lets assume the JFET-Gate is at ground voltage and the JFET-Source is at some positive voltage with respect to (wrt) the JFET-Gate, say $\frac{3}{4}$ of a volt, and the drain is positive, at about 3 volts. The Q Amp has a zero voltage output when the JFET-Drain (connected to the input of the AD840) via Q1(common base amp) and Q2(emitter follower amp) is at about 3 volts. Since the AD840 is a non-inverting amplifier, an increase in the JFET-Drain voltage produces a positive voltage at the output of the Q Amp. This positive output at the input of the, long time-constant, inverting integrator(OP627), begins driving the JFET-Source in a more negative direction, causing a larger current flow in the JFET and thus a decrease in the JFET-Drain voltage, opposing the original increase. Thus the integrator's task is to keep the DC output of the Q Amp at zero volts.

The fast loop also keeps the JFET-Gate near zero volts, for fast signals, by neutralizing the charge injected into the gate node by the detector via the JFET-Gate, DC blocking capacitor situated between the Detector

and the JFET-Gate. This neutralizing charge is supplied from the output of the Q Amp through a parallel combination of resistance and capacitance which we call the “**Feedback Network**”. The amplitude of the Q Amp output pulse is determined by the capacitance in the feedback network and the quantity of charge from the detector, since $V=Q/C$. For a given, the output voltage is inversely proportional to the value of the Feedback Network C. Both loops then, function to keep the JFET-Gate near zero volts.

The basic design philosophy of the discrete amplifier is as follows. In order to minimize the effect of negative feedback via the Drain-Gate capacitance (Miller effect), the Drain impedance is kept as low as possible. If the impedance were zero, then any changes in Drain current would result in zero changes in Drain voltage and thus no negative feedback. Q_1 is a common-base stage, which provides a very low input impedance and a high output impedance. The current gain slightly less than one. Q_2 , on the other hand, has a very high input impedance and a very low output impedance. The high input impedance is required in order to keep the voltage gain of the first stage (Q_1) high. Q_2 has the low output impedance in order to be able to drive the cable going to the feedback resistor connected to the JFET Gate. There is also an option to let Q_2 drive an intermediate, push-pull emitter follower, amplifier made up of Q_3 and Q_4 (in the dotted box).

This amplifier provides more drive capability, should the need exist. If there is no need for this amplifier, the ten components inside the dotted line-box may be left off the board, and a jumper wire inserted at “S1”.

FETTemp Description: (Steve Morrison)

This module supplies the signal, called variable (supplied from the backplane), used by the QET module’s calibrate mode. There are two inputs to this module. A single ended or differential signal can be applied from a waveform generator through the floating front panel LEMO connector or a 10Hz signal can be received from the backplane. The output is a true differential signal to the backplane. It will be a buffered copy of either the signal to the front panel LEMO or the 10Hz from the backplane. A front panel switch selects which source is passed to the output. When the QET module is in calibrate mode, this signal is passed to the sensor bias.

This module contains 2 batteries that are used to supply current to the FET heater. The current is controlled by a momentary switch, that is mounted on the module’s front panel.

Power Control Circuitry

Power control circuitry, version 1:(Tom Crenna)

This module utilizes the following voltages: +15FEin, -15FEin, +15in, -15in, and +5Din., which are available at the backplane. When this module receives power, either by being plugged into an energized backplane, or by having this module plugged in, when the subrack power supplies are energized, there is a “POWER ON SEQUENCER” circuit that delays the application of the various voltages to the on board circuitry. The MAX8216CSP, monitors the five voltages at the connector, and when all voltages are at the proper value, begins the sequence of applying the voltages to the remainder of the module circuitry. When the MAX 8216 is satisfied that the voltages are correct, the five wired-OR outputs go high, removing the “CLEAR” from the 74HC174 and removing the “RESET” from the ICM7555CBA. The ICM7555CBA is configured as a 2 Hz oscillator, which causes a series of high levels to get shifted from Q1 to Q6 every 500 milliseconds. First Q1 goes high, then Q2 etc. until all six outputs are high, which requires 2.5 seconds. When the sixth output (power-on-reset) goes high, the 2Hz clock is “RESET”. On board jumpers are used to determine which outputs of the 74HC174M will be used to control any of the five voltages. Initially, all of the 15 Volts will be controlled from Q1 and the 5Volts will be controlled from Q2. Q1 going high will energize the LED’s in the PS2703-2, which will in turn, connect the 15Volt supplies to the rest of the Module circuitry. Q2 going high will turn on the IFR7416(Q1) and thus supply the 5 Volts to the module circuitry requiring it. Front panel LED displays are provided in order to visually monitor the application of the module voltage levels.

Power control circuitry, version 2: (Wayne Johnson revised 5/14/99)

The Zip module can be powered up by plugging the module into a crate that is already powered up or by turning on the crate power supply with the module already plugged in. FET switches (Q1, Q2, Q3, Q4: IRF7416, IRF7413) are used to connect the fused backplane supplied voltages to the board circuitry voltage planes. The FET switches are controlled by the power control circuitry which uses a voltage monitor chip (U1B:MAX8216), a programmed sequencer chip (U104:CY37256P160-83AC) and a FET driver (U5B: PS2703-2).

The voltage monitor senses the fused backplane voltages and when all of the voltages are at their proper level the sequencer is enabled to begin turning on the FET switches.

When enabled, the sequencer starts a 2 Hz clock. The first action taken by the sequencer is to time delay the turn on of the FET switches based on the slot location of the module, 1 clock pulse of delay per slot. Example: slot 4 will have 4 clock pulses (2 seconds) of delay before turning on a FET switch. Once the time delay has expired the sequencer then enables the turn on of the FET switches in an order designated by the user. The sequence order for turn on is established by the user in the VHDL code that is programmed into the sequencer, Control Logic chip (U104). See ZIP LOGIC ADDRESSING section for an explanation of the code. After the final FET switch is turned on the clock is disabled and the sequencer begins monitoring the output of the voltage monitor, the FET switches are kept on while the voltage monitor output indicates all supplies are ok. When the voltage monitor output indicates a power supply problem all of the FET switches are turned off disconnecting the board circuitry voltage planes from the backplane supplied voltages.

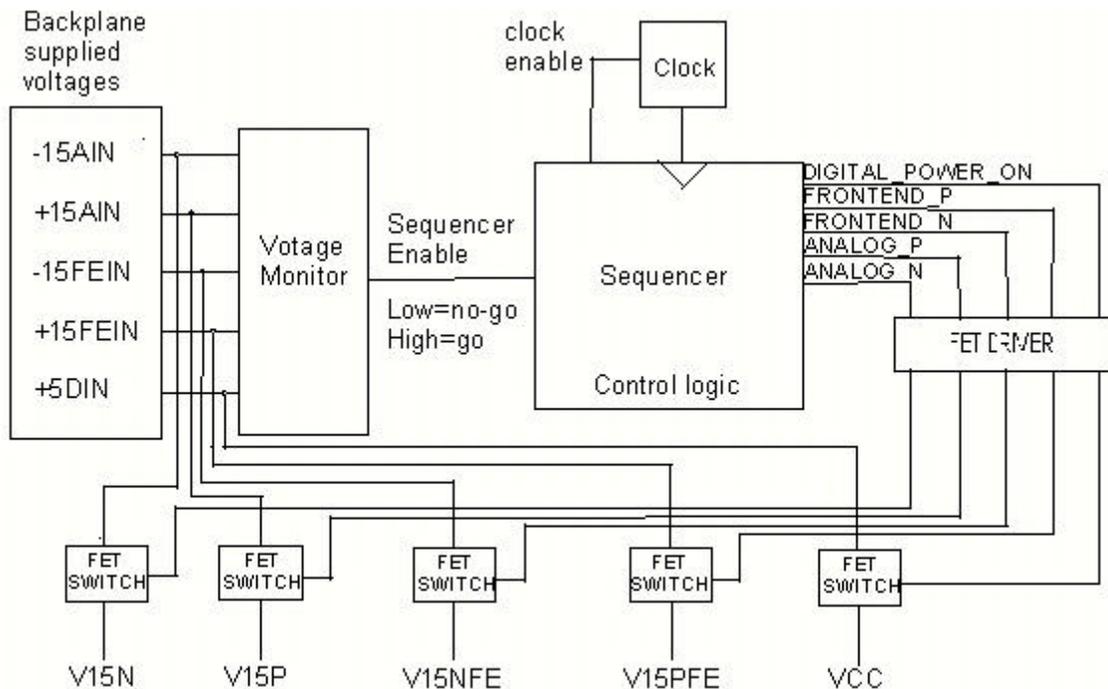


figure 1: power control circuit function diagram

Digital Interface (Wayne Johnson revised 5/7/99)

In order to appear as a single gate load to the crate backplane, all of the "address", "read", "write" and "data" lines are buffered. The address, read, and write buffers are unidirectional, always passing the backplane signals to this module, whereas the data buffers are bi-directional, with the direction being controlled by the write line when this particular module is being addressed.

The address, slot number, of each module is determined by the local address hardwired for each slot location in the backplane. Each slot in the backplane utilizes 5 connector pins to supply that slot address to any module plugged into it. The left-most slot (facing the subrack) is slot 0, with the slot addresses incrementing by 1 with each move to the right, giving an address of 21 to the far right slot. An on board 5-bit address comparator compares the local address with address bits A8 through A12 to determine if this module is being addressed. If this module is being addressed, then the data buffer direction is set based on the condition of the “write” line.

ZIP Module ADDRESSING (Wayne Johnson) May 14, 1999

The module addressing is done in two groups and uses VHDL programmed CPLDs for handling of the Address and Data Bits. The first group (addrlogic) decodes the Address Bits and the second group (chargeamp, csr_logic3 and ziprelay2) decodes the Data Bits. The charts: [Chart 1:Section and Subsection decoding for the ZIP Electronics board](#) and [Chart 2:Zipmodule addressing matrix](#), show the relationship of the sections and subsections to the Address bits, the Data bits and the group project names (in parenthesis above).

The first group handles the Address bits and decodes Module, Section and Subsection selection. When a Module, Section and Subsection have been selected then the Data Buss is either written to or read from. The data bits are then utilized to set/read board operating parameters, in ex.: gain, polarity, pulse width, enable/not enabled, etc.

Module Selection:

Module selection is accomplished by comparing Address bits 8 –12 to the slot number where the module is mounted. The slot number is hardwired into the back plane of the crate and is unique to each slot in the crate. The slot number is connected to the module through the back plane connector and is routed to the Control logic chip (U104)where the comparison is done. When address bits 8 –12 equal the slot number then the Module is selected and further decoding of the Section and Subsection is done. The address byte combinations versus the slot numbers are shown in Chart 1 – Part 5.

Section Selection:

Section selection is accomplished by decoding Address bits 4 –7 to identify one of sixteen possible sections. Chart 1-Part 1 shows the sections that are presently used, name of the circuit being enabled and the address used to select each section.

Subsection Selection:

Subsection selection is accomplished by decoding Address bits 0 –3 to identify one of sixteen possible sections. Chart 1-Part 1 shows the subsections that are presently used, name of the circuit being enabled and the address used to select each section.

Chart 2 shows the matrix used for addressing the sections and subsections.

Decoded outputs:

There are four different types of output signals decoded within the subsection. They are DAC control outputs, CSR control outputs, module information request, and test.

DAC Control Outputs:

DAC Control pulses enable the addressed DAC subsection to either input (write) from the data buss and set the output voltage to a specified DC level, or output (read) to the data buss the digital value that the output is set to.

CSR Control Outputs:

CSR Control outputs are pulses that enable the transfer of data buss information used for the setting or reading of the various systems operating parameters. The CSR subsections are listed in Chart 1-Part 2 along with the corresponding system parameter that each of the data bits controls.

Module Information:

Module information is a read operation which transfers the sixteen module identification bits to the buss for decoding the:

1. Board serial number, bits 0 –8
2. Board version, bits 8 –11
3. Board type, bits 12 –15

Module identification bits are hard wired on the board. The module's identification is set by cutting traces that are connected to +5V and ground.

Test:

Test is a write only control, that outputs a pulse, used to trigger a signal to the detector, which produces an output signal that is used for testing detector systems.

Group 2:

This group of VHDL programmed chips handles the information on the data buss to set levels or toggle latching relays to enable the user to set board and system operating parameters. Chart 1 – Part 2 shows the CSR controls that are decoded by group 1 and the board signals that are set by the corresponding data bits when that CSR control is enabled.

Clocks:

Clocks are used by some of the CSR subsections for incrementing counters. Each CPLD in Group 2 has a clock connected to an input. A clock is enabled when a CSR control input to the CPLD is enabled and disabled after all of the CSR's outputs have been sequenced through.

CSR outputs:

There are two types of outputs generated when a CSR is enabled. They are either a latched output (ground, 5V) or a 5V pulse.

Latched output:

The latched output is a permanent level that is set until changed to a different setting. See figure 1: latched output function diagram.

Pulsed output:

The 5V pulse is used to toggle a latching relay. The duration of the pulse is long enough to ensure that the relay latches into the new setting. The pulse width is set by the clock speed and the number of clock pulses that the counter needs to count in order to equal the counter setting that is set in the VHDL code for each pulse type. See figure 2: sequenced, pulsed output function diagram.

The pulsed outputs are analyzed and sequenced so that only those relays that are changing state will be pulsed. The setting of the relay is compared to the new information that the CSR receives (wibd) and the present setting of the relay. The relay is pulsed if there is a change in setting, it is skipped if there is no change in setting. Relays that require pulses will be sequenced so that only one relay is pulsed at a time. This reduces the amplitude of the momentary current load that is caused by the activation of the relays.

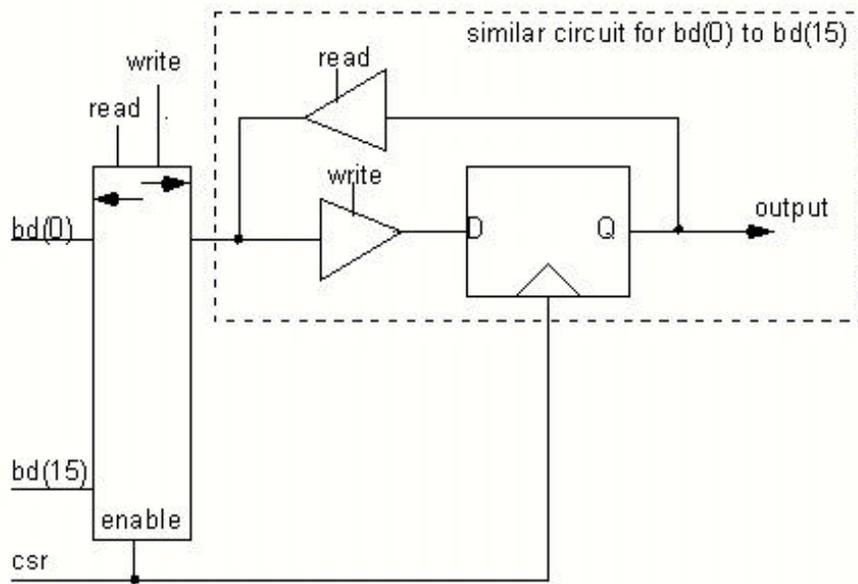


figure 2: latched output function diagram

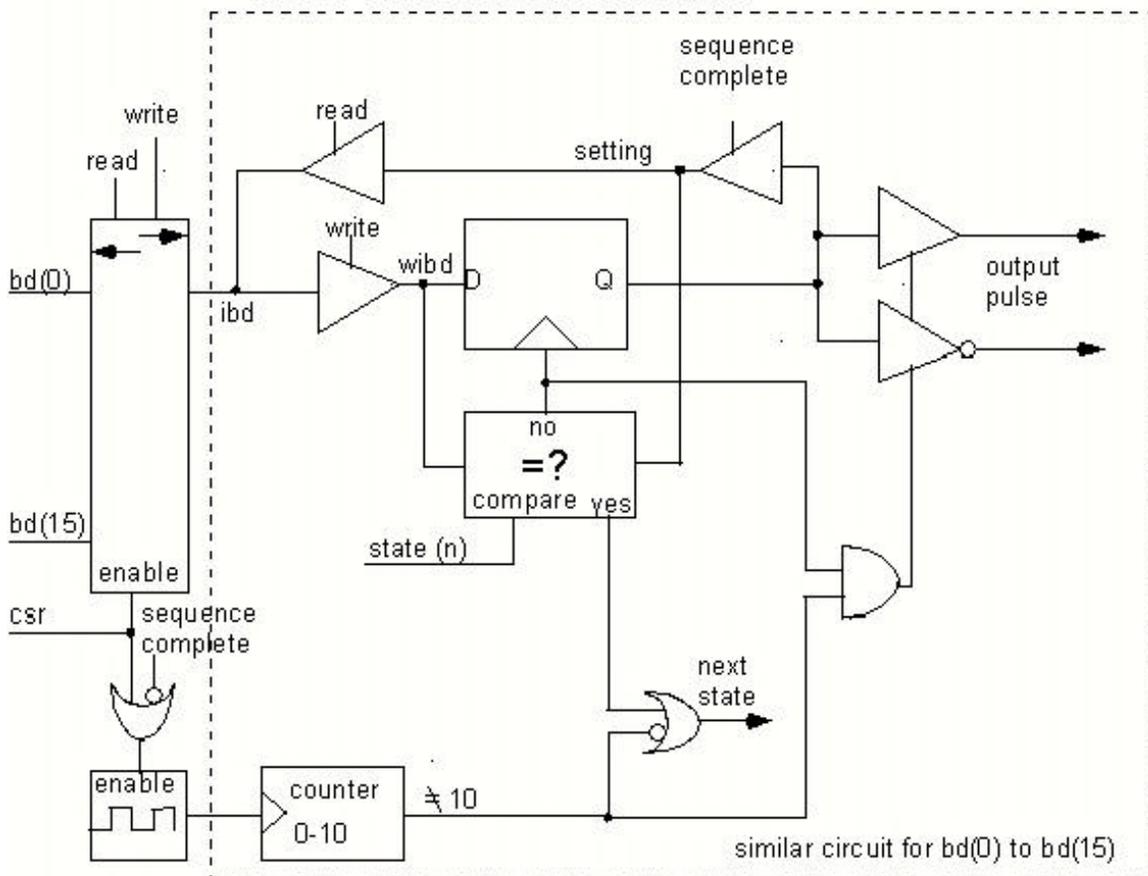


figure 3: sequenced, pulsed output function diagram

Digital To Analog Converters (DAC's)(Bruce Merkel Revised 5/10/99)

There are seven, 12 bit, quad output DAC devices on this module, giving a total of 28 DAC outputs. Each DAC output has a range of +/- five volts, controllable in increments of approximately 2.44 millivolts / Bit. For each device, the four outputs are identified as 0, 1, 2 and 3. A 'system reset' will set the four outputs of each device to zero volts. The DAC output voltage is determined by the following formula, $V_{out} = 5 \text{ volts} - (10/4096)N$, where N is the binary code(in decimal) written to the DAC.

- The QET portion of this 9U ZIP module uses all four outputs of the QET Bias DAC (U32). Each output controls the bias of one of the four QET sensors. Outputs 0, 1, 2 and 3 control sensors A, B, C and D respectively.

Each of the four SQUID electronics sections (A, B, C and D) of the ZIP module uses three DAC devices.

- Squid Bias DAC (U34) outputs 0, 1, 2, and 3 go to the four squid front end sections A, B, C, and D respectively. This DAC is used to bias the SQUID at the most sensitive operating point.
- The Squid Gain DAC (U36) outputs 0, 1, 2, and 3 go to the squid Variable Gain Amplifier section for squids A, B, C, and D. This DAC is used to control the second stage, voltage controlled, variable gain amplifier, with the DAC output voltage determining the gain, i.e., five volts out of the DAC sets the amplifier to a gain of 5.
- The Squid LOCKPOINT DAC (U33) outputs 0, 1, 2, and 3 go to the squid front end and control the offset voltage of the first stage, (input amplifier). The +/- 5 volt output of the DAC translates to +/- 50 millivolts at the input to the first stage.

The ZIP board has six Driver channels, four to receive the four SQUID outputs, and two to receive the two Qamp outputs. Each Driver requires one DAC output to control it's input offset voltage.

- The Squid Driver DAC (U31) outputs 0, 1, 2, and 3 go to their respective SQUID driver offset amplifiers A, B, C, and D.
- The Qamp drivers utilize two of the Q Driver DAC (U37) outputs; 0: $Q_{amp \text{ Outer}}$ and 1: $Q_{amp \text{ Inner}}$. The other two outputs of Q Driver DAC are used for a test output (2) and a spare output (3).
- The Q Bias DAC (U35) is used to control the Q(charge) Bias section of the ZIP module. The first two outputs (0, & 1) control Q-outer and Q-inner bias voltage, the second two outputs (2, & 3) control LED BIAS current magnitude and the ZAP DAC voltage.

Buffers (Bruce Merkel, Revised 5/17/99)

The buffer is a unity gain amplifier used to translate signals referenced to Analog Ground (AGND), to signals referenced to Front End Ground (FEGND). The DAC outputs that are buffered are: Squid Bias, Squid Gain, Squid Lockpoint, QET Bias, Q_{inner} Bias and the Q_{outer} Bias. The Buffers are located at the place where the signal crosses over from the Analog Ground reference (AGND) to Front End Ground reference (FEGND). If a voltage difference exists between the grounds, the buffer acts to cancel that difference.

The output signal from the buffer (U1xx:LT1124CS8) is sent to a low pass filter with a 3dB roll off frequency of 13.5 Hz. The filter consists of a series resistor (R1xx: 4.99k) and a pair of Back to Back polarized capacitors (C1xx, C2xx). Two capacitors are needed in this configuration because the output of the buffer is bipolar.

References and Regulators (Bruce Merkel Revised 5/10/99)

The DAC Precision Voltage Reference AD588KQ (U1xx) generates a +/- 5 Volt reference which is used by the DAC +/-10 volt and DAC +/-5 volt regulators. The reference voltage comes into the positive input of a dual high speed precision OP-AMP LT1125S8 (U3xx). The output of the amplifier feeds the common pin of a 5 Volt regulator. Depending on the output voltage setting resistors on the regulator, the output voltage is either 10 or 5 volts. The +/- 10 Volt output is used by the DAC buffers, the DAC devices and

the Squid, Variable Gain Amplifiers. The +/- 5 Volt output is used by the DAC's and the -5 volt output is also used by the Squid Variable Gain Amplifiers and the QET Front End.

The Qamp 10 volt reference, is generated with a REF102AU (U6xx) and then buffered and filtered with an OPA27GU (U3xx) operating at unity gain. The buffered reference voltage is then supplied to the two 14 volt regulators which provide the +/- 14volts required to operate the two Q amplifiers. One amplifier for Q inner, and one amplifier for Q outer.

The 14 Volt regulators take the 10 volt buffered reference, and generate a separate +14 volts and -14 volts for each of the two Q amplifiers. OPA27GU (U5xx) regulates the + 14 volt output and OPA27GU (U4xx) regulates its -14 volt output.

The LM78L05 (U119) and the LM79L05 (U120) generate the +/-5QD voltages for the squid logic, from the Analog +/- 15 volts. The LM7805 (U122) and the LM7905 (U121) generates the +/-5Q voltage for the rest of the squid blocks from the Front End +/- 15 volts.

The MIC5206-5.0BMM (U126) generates a low noise 5 volts for the LED Driver, QBIAS_FE and the QET SELECTOR from the Front End +15 volts.

Zip Module LED Pulse Control(Tom Jankovsky))

Zip Module LED Current Control(Tom Jankovsky))

Zip Module LED Pulse Source(Tom Jankovsky))

Zip Module External Test Receiver(Steve Morrison)