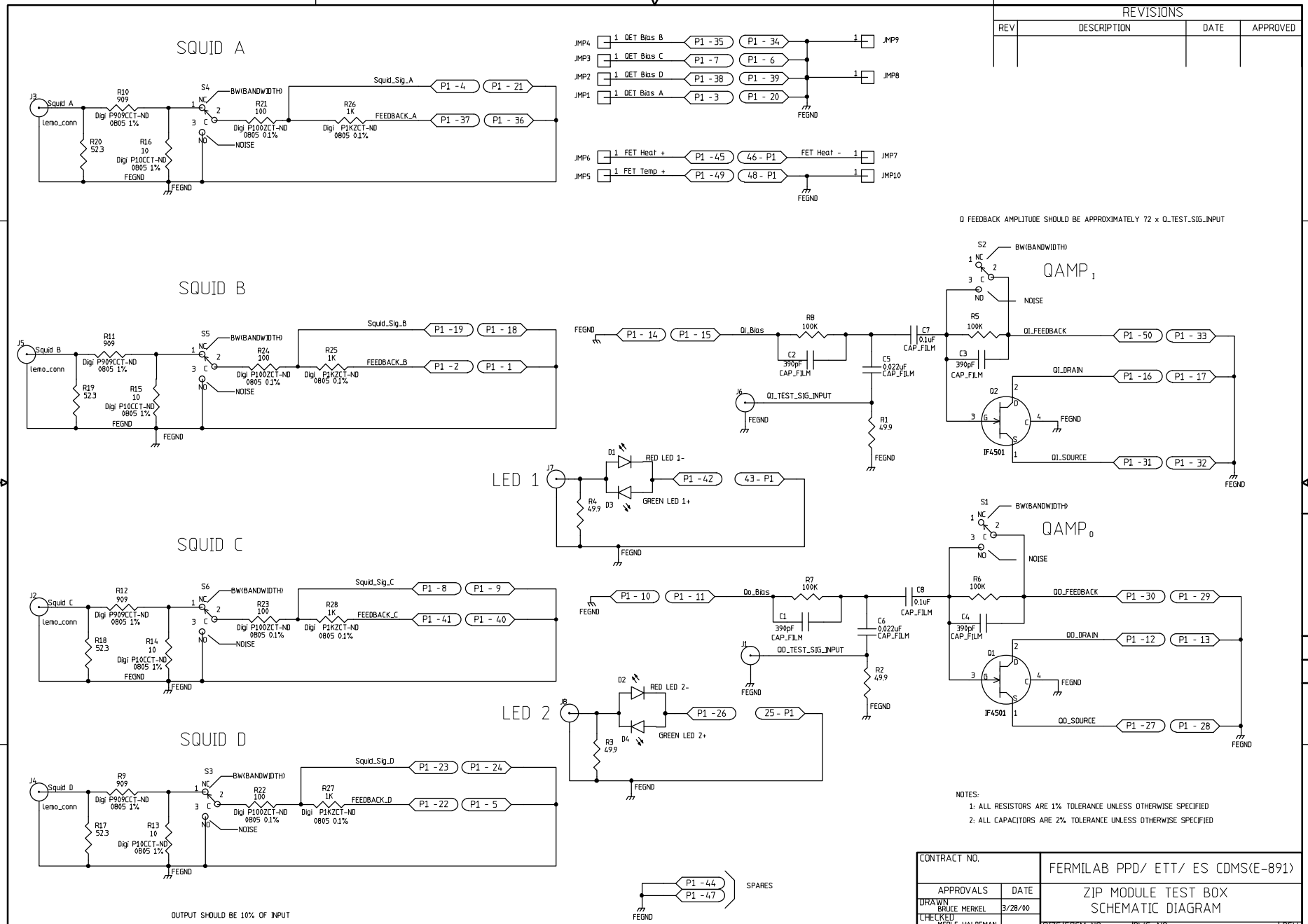


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

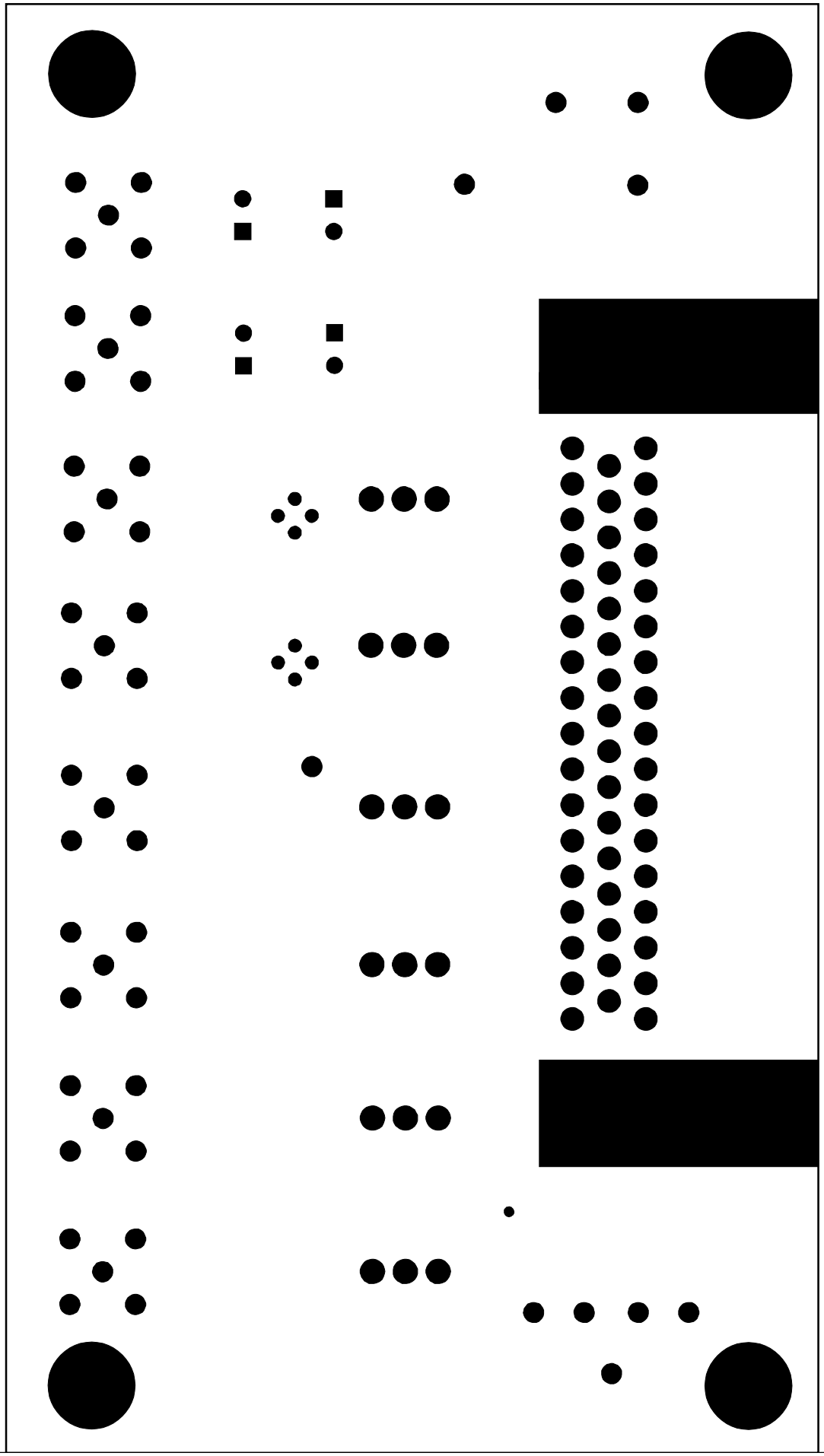
NOTES:

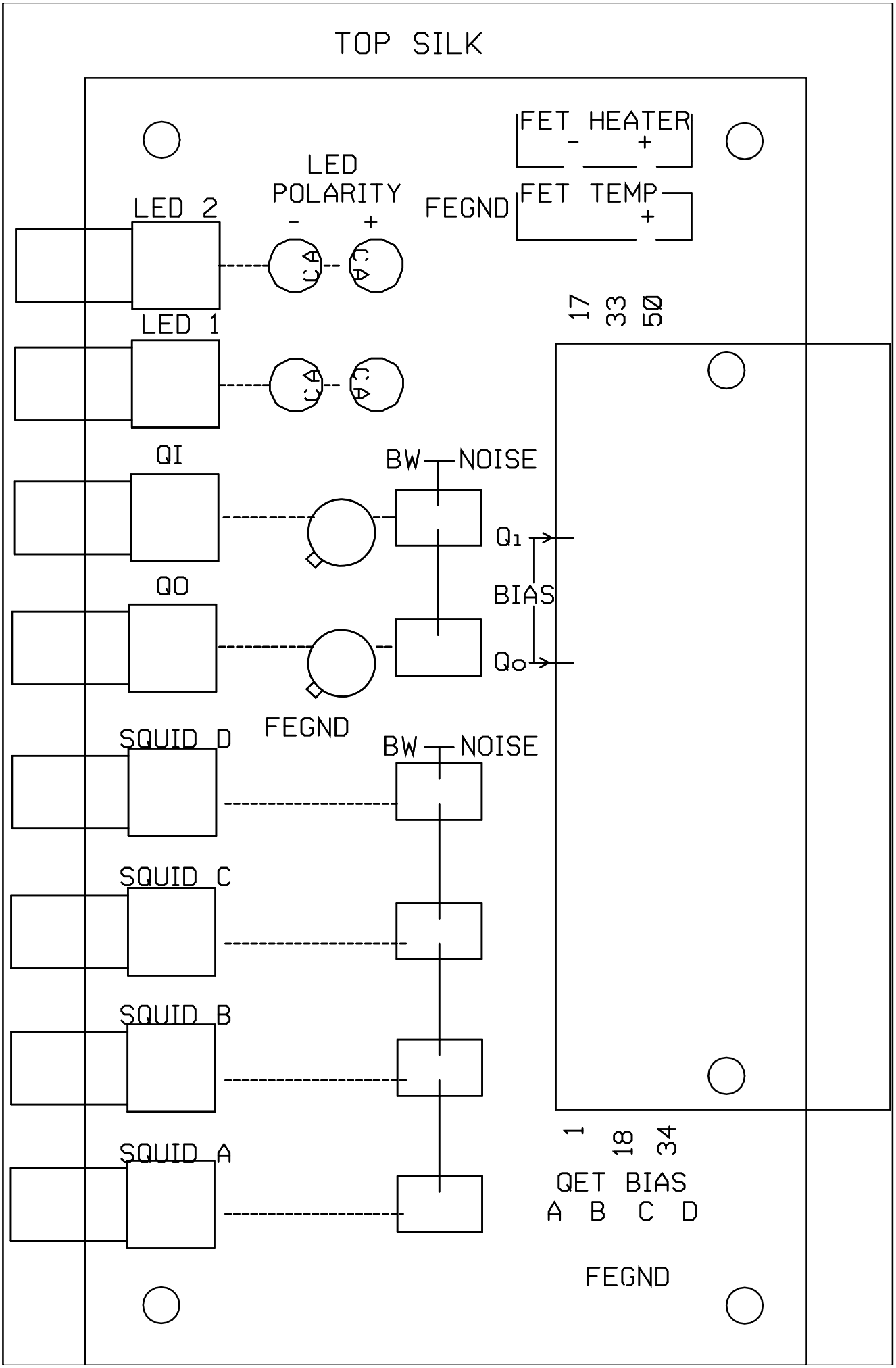
1: ALL RESISTORS ARE 1% TOLERANCE UNLESS OTHERWISE SPECIFIED

2: ALL CAPACITORS ARE 2% TOLERANCE UNLESS OTHERWISE SPECIFIED

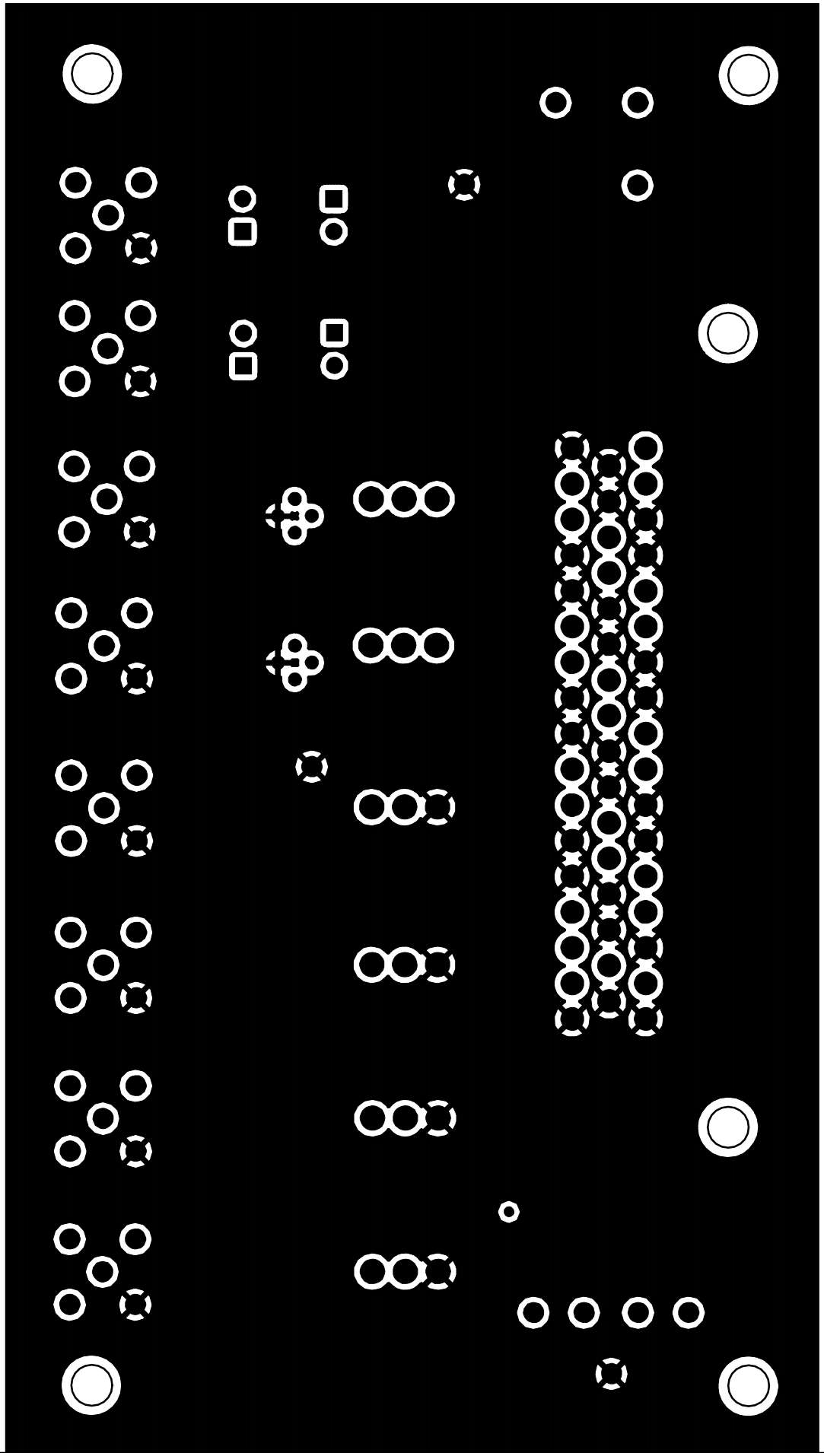
CONTRACT NO.		FERMILAB PPD/ ETT/ ES CDMS(E-891)		
APPROVALS	DATE	ZIP MODULE TEST BOX SCHEMATIC DIAGRAM		
DRAWN BRUCE MERKEL	3/28/00			
CHECKED MERLE HALDEMAN		SIZE C	FSCM NO.	DWG. NO.	REV
ISSUED		SCALE N/A		SHEET 1 OF 1

SOLDER MASK TOP

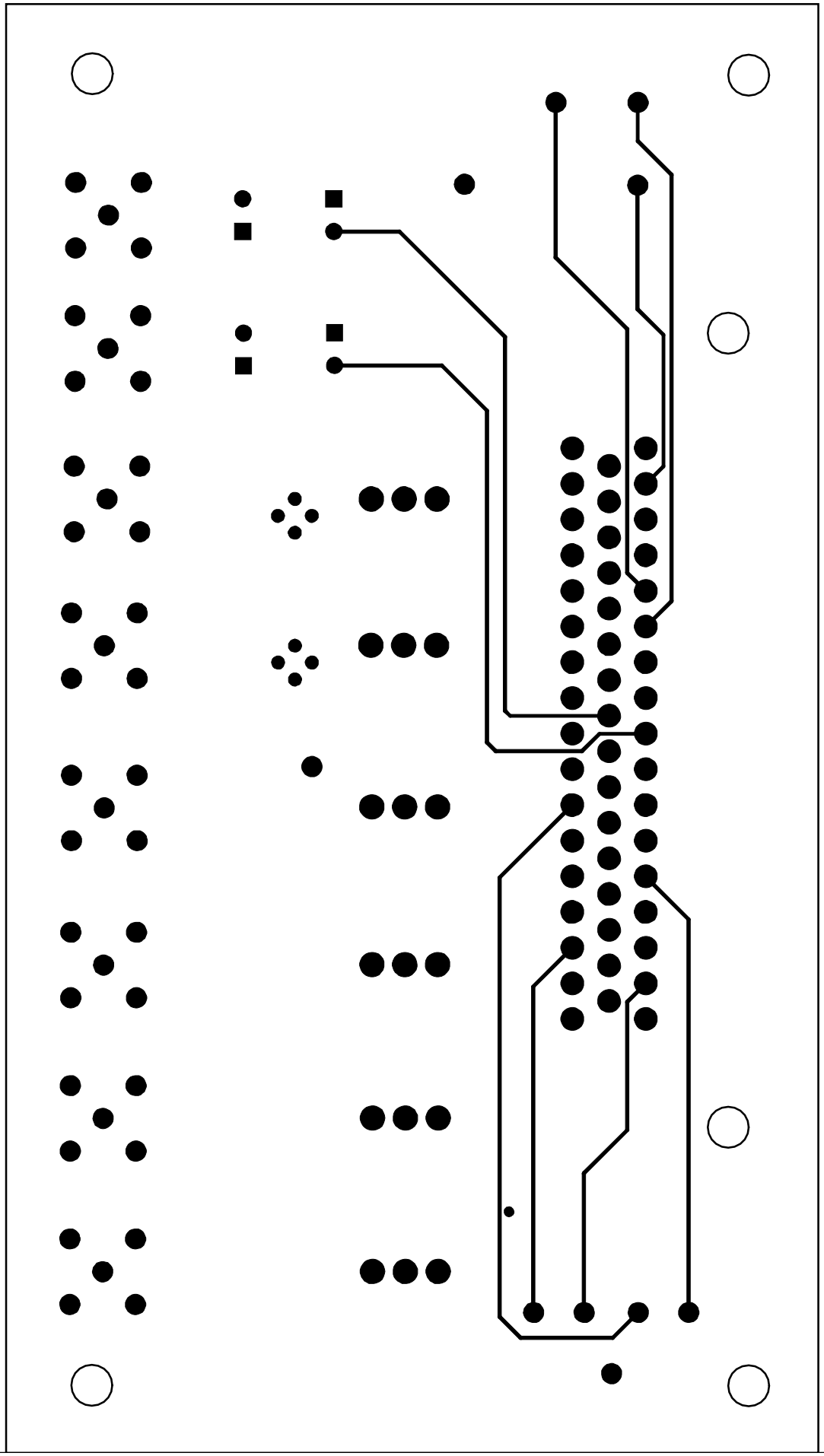



TOP SILK
FET HEATER
-
+
LED
POLARITY
-
+
FEGND
FET TEMP
+
LED 2
LED 1
17
33
50
QI
BW
NOISE
Q1
BIAS
QO
Qo
FEGND
SQUID D
BW
NOISE
SQUID C
SQUID B
SQUID A
1
18
34
QET BIAS
A B C D
FEGND

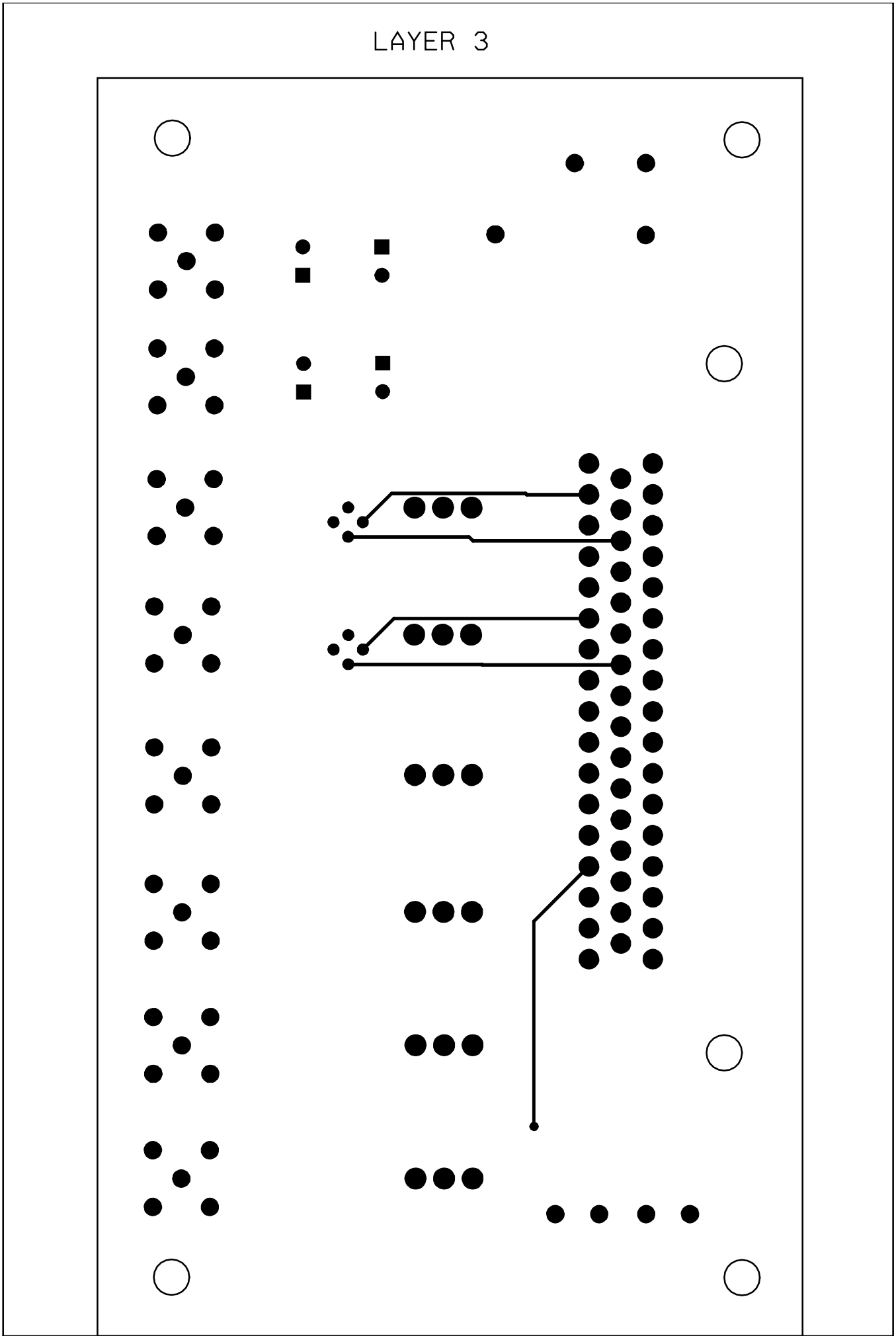
TOP LAYER



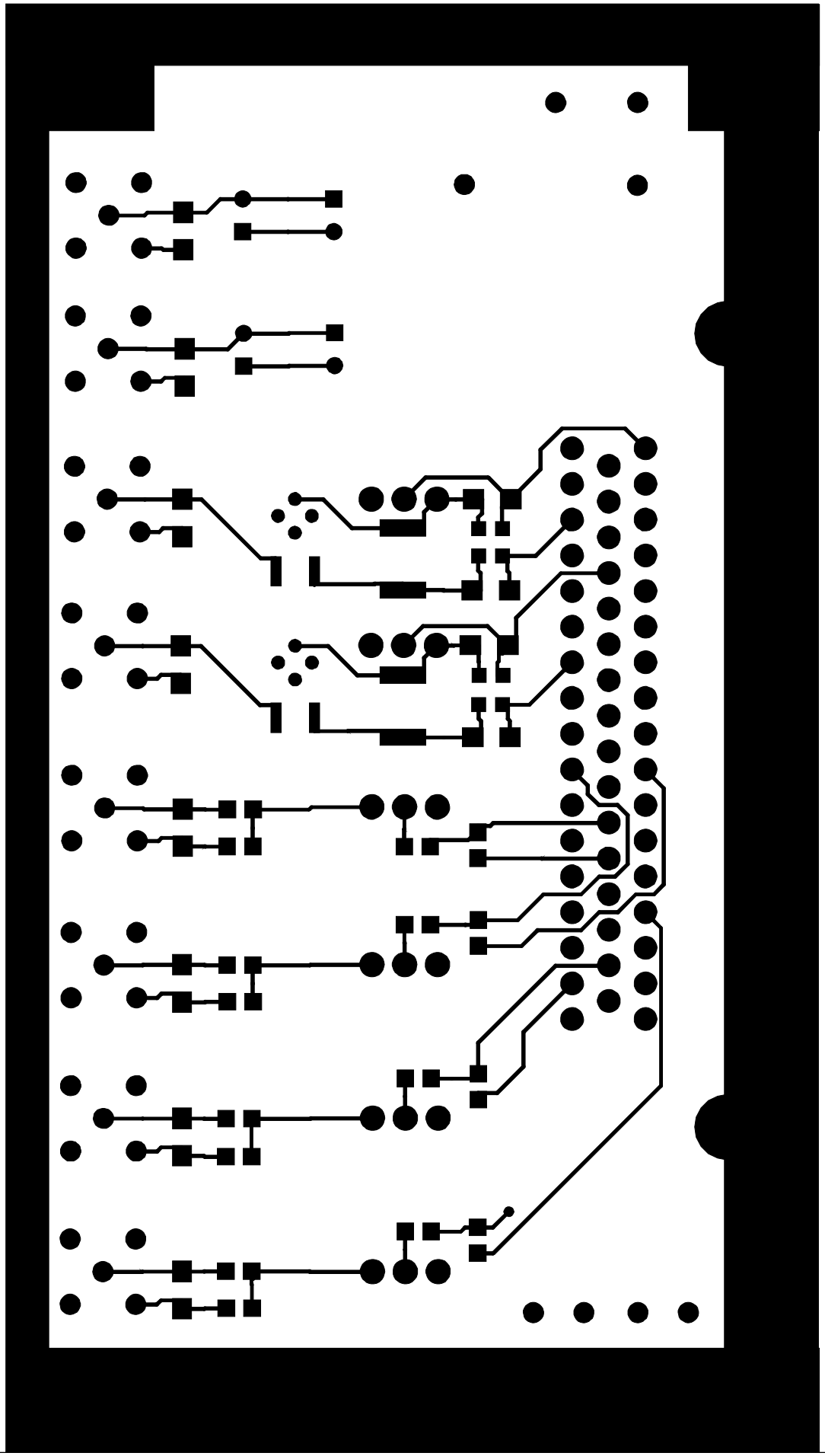
LAYER 2



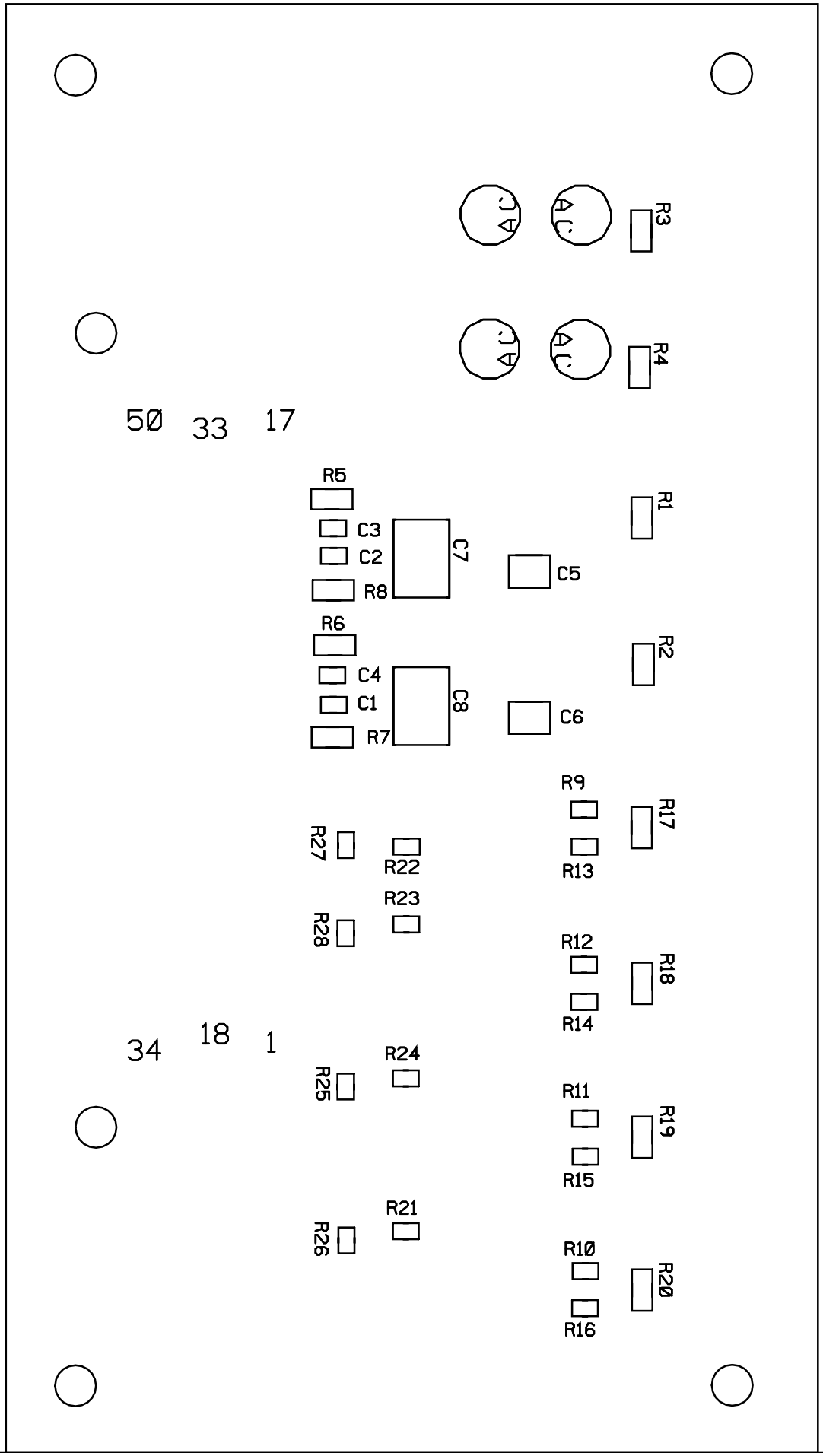
LAYER 3



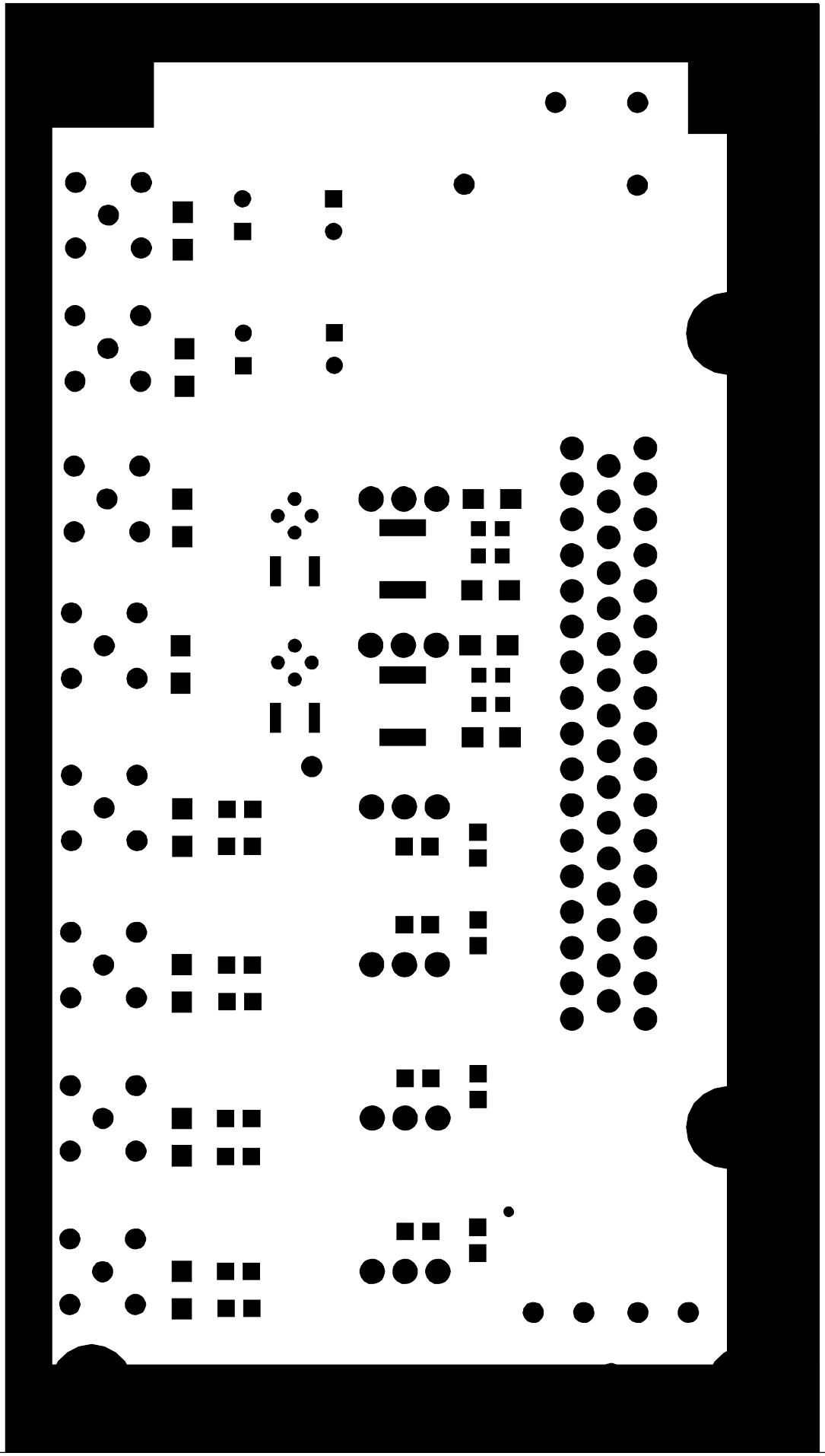
BOTTOM LAYER

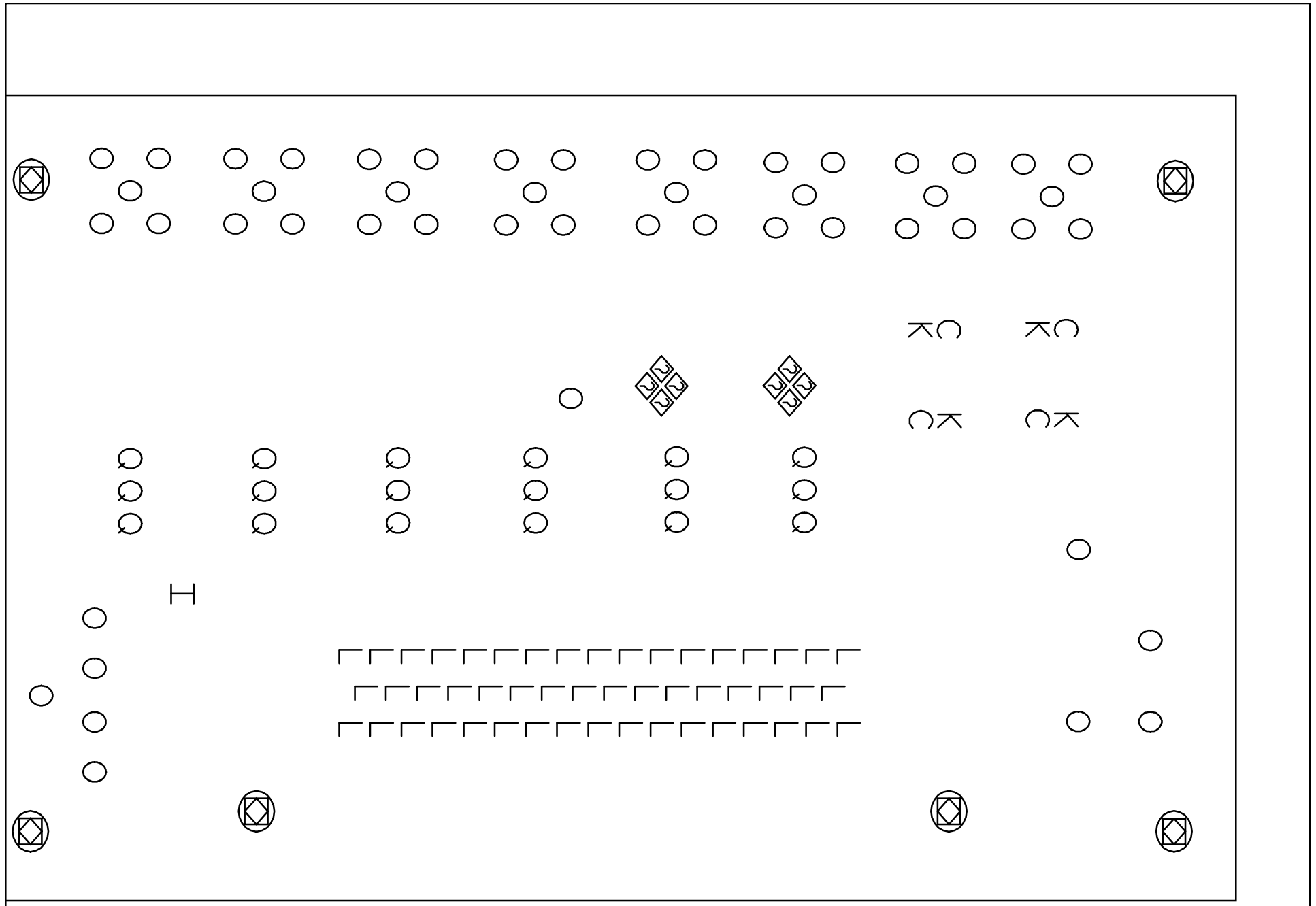


BTM SILK

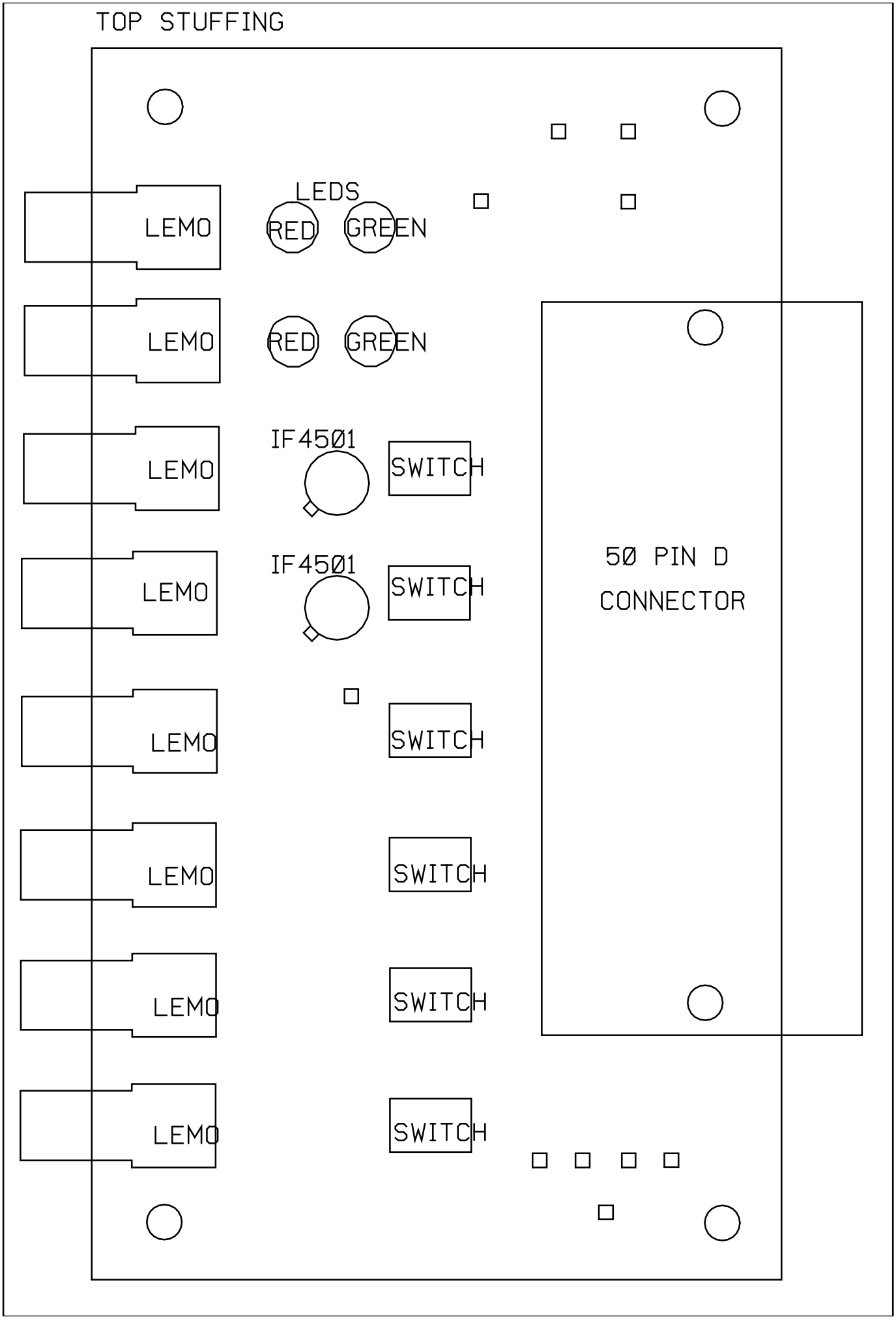
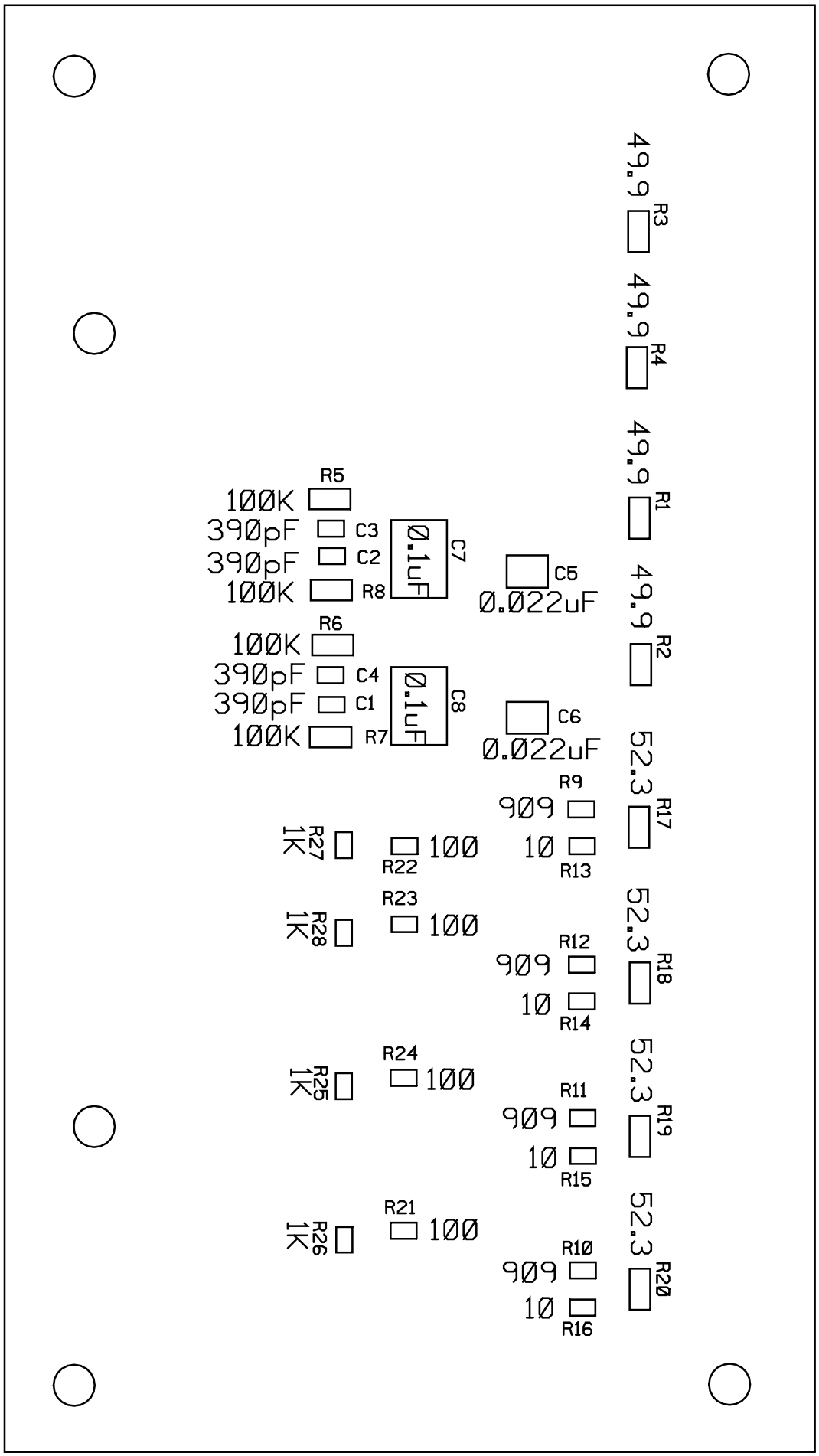

R3
R4
50
33
17
R5
R1
C3
C2
C7
C5
R8
R6
R2
C4
C1
C8
C6
R7
R9
R17
R27
R22
R13
R23
R28
R12
R18
R14
34
18
1
R24
R25
R11
R19
R15
R21
R26
R10
R20
R16

SOLDER MASK BOTTOM





Through Holes			
Symbol	Diameter(in)	Plated	Quantity
C	0.0280	Yes	4
I	0.0150	Yes	1
K	0.0280	Yes	4
L	0.0540	Yes	50
O	0.0380	Yes	50
Q	0.0460	Yes	18
◇	0.0241	Yes	8
⊠	0.1250	Yes	6


TOP STUFFING
LEDS
RED
GREEN
LEMO
LEMO
RED
GREEN
LEMO
IF4501
SWITCH
LEMO
IF4501
SWITCH
50 PIN D
CONNECTOR
LEMO
SWITCH
LEMO
SWITCH
LEMO
SWITCH
LEMO
SWITCH

BOTTOM STUFFING