Relay Rack 6 N02

N02S01 LRS 4616 Level Translator	N02S02 PS 710 Octal Disc.	N02S03 PS 710 Octal Disc.	N02S04 LRS 429 Fan In/Out	N02S05 LRS 365 Coinc. Unit	N02S06 LRS 429 Fan In/Out 1 X 16	N02S07 LRS 429A 1X16 . Fan Out	N02S08 LRS 222 Gate Gen.	N02S09 LRS 429A 2X8 . Fan Out	N02S10 (Empty)	N02S11 (Empty)	N02S12 (Empty)
1) Nout: T00 C02S02 In 0 S02 Ch1 In 2) Nout: T01 C01S02 In 1 S03 Ch1 In 3) Nout: T02 C01S02 In 2 S02 Ch2 In 4)Nout: T03 C01S02 In 3 S02 Ch2 In 5)Nout: T04 C01S03 In0 S03 Ch3 In 6)Nout: T05 C01S03 In 1 S03 Ch3 In 7) Nout: T06 C01S03 In 2 S02 Ch4 In 8) Nout: T07 C01S03 In 2 S02 Ch4 In 9) Nout: T08 C01S04 In 0 S02 Ch5 In 10) Nout: T09 C01S04 In 1 S02 Ch5 In 11) Nout: T10 C01S04 In 2 S03 Ch6 In 12) Nout: T11 C01S04 In 3 S03 Ch6 In 13) Nout: T12 C01S05 In0 S02 Ch7 In 14) Nout T13 C01S05 In 1 S03 Ch7 In 15) Nout: T14 C01S05 In 2 S03 Ch8 In 16) Nout T15 C01S05 In 3 S03 Ch8 In	1) In: S01 Ch1 Out: T00SG: C01S08 T00SR C01S10 2) In: S01 Ch3 Out: T02SG C01S08 T02SR C01S10 3) In: S01 Ch5 Out: T04SG C01S08 In 4 T04SR C01S10 In 4 4) In: S01 Ch7 Out: T06SG C01S08 In 6 T06SR C01S10 In 6 5) In: S01 Ch9 Out: T08SG C01S09 In 0 T08SR C01S11 In 0 6) In: S01Ch11 T10SG C01S09 In 2 T10SR C01S11 In 2 7) In: S01Ch13 Out: T12SG C01S09 In 4 T12SR C01S11 In 6 8) In: S01Ch15 Out: T14SG C01S09 In 6 T14SR C01S11 In 6	1) In: S01 Ch 2 Out: T01SG C01S08 In 1 T01SR C01S10 In 1 2) In: S01 Ch4 Out: T03SG C01S08 in 3 T03SR C01S10 in 3 3) In: S01Ch6 Out: T05SG C01S08 in 5 T05SR C01S10 in 5 4) In: S01Ch8 Out: T07SG C01S08 in 7 T07SR C01S10 in 7 5) In: S01 Ch10 Out: T09SG C01S09 in 1 T09S C01S11 in 1 6) In: S01Ch12 Out: T11SG C01S08 in 3 T11SR C01S10 in 3 7) In: S01Ch14 Out: T13SG C01S09 in 5 T13SR C01S11 in 5 8) In: S01Ch16 Out: T15SG C01S09 in 7 T15SR C01S11 in 7	In: 00 – 03 C01S02 t OR out In: 04 – 07 C01S03 OR Out In: 08 – 11 C01S04 OR Out In: 12 – 15 C01S05 OR Out Out: PID Trig N2S05 Ch1 in A PID Trig N2S05 Ch2 in A	Upper: Veto CD Coinc. = 2 In A: PID Trig N02S04 Ch4 Out In B: Multi–Trig N01S05 Ch1 Out Out: S06 Ch2 In C01S13 Ch15 INT1 –> TDC Lower: Veto BCD Coinc. = 1 In A: PID Trig S04 Ch 3 Out Out: S06 Ch4 In C01S13 Ch14 INT2 –> TDC	In: S05 Ch1 Out S05 Ch2 Out C01S12 Out 0 Mu Trig C01S12 Out 3 Out: TOF–E Trig RR15 PP3A TOF–W Trig RR16 PP4A CKOV Trig PPA9 N02S07 Input 1 Exp Trig RR03N11In1 PPD1 S08Lower Chan start Beam PPC Trig VME S02 Int 2 RICH PPC Trig. PP1A DC Trig PP2A GT0 –> PP1 N2S9 BC1 Trig N01S09Ch3in BC2 Trig N01S09Ch5in BC3 Trig N01S09Ch7in	In: S06 Output Out: TPC [A D] IRQ2 C01S15Ch5 RFD04 Input C1S11 in 10 C1S9 In 10 C1S20 Start C1S22 Start (Common Stop for 3327) (80 + 32 ns Delay Cable)	A: Start: $\overline{\text{N02}}$S09 Out 2 Stop: N01S05 lower Out NIM: N02S09 Lower Input B: Start: N02S06 Out 3 NIM: N02S09 Lower Input	In: RICH PPC Busy PP1B N1S12 NIM Out TPC Busy N03S10 Ch1 Out Dc's Busy PPB2 N03S10 Out: C7–18 Gate N02S09 Ch3 in 12 ns cable $\overline{\text{Out}}$: End PPCBusy N01S06 Start Upper N02S08 Start Upper In: S08 Ch1 N S08 Ch2 N S09 Ch1 Out S06 Ch3 Out Out: C01S02 Inhib C01S03 Inhib C01S04 Inhib C01S05 Inhib C01S08 Inhib C01S09 Inhib C01S12 Inhib			