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Updated

Command data format for PSI43 interface board

Introduction.

PSI43 interface board will use eight DCO0..DCO7 data lines as a 8-bit data word. These outputs are latched by the ASIC's test box internal latch. The input lines DCI0..DCI7 will be used to read status outputs from the PSI43 interface board. These inputs are not latched by the ASIC's test box, therefore, PSI43 interface board logic will have a latch to keep the status lines stable. Sixteen PO0..PO15 (pulsed) outputs will be used as address lines and various trigger pulses as following. In order to set an address, these outputs have to be set to the *inverted* value of each address bit. As a pulsed output, a quiescent value of logical one (high) will cause positive output pulse. A quiescent value of zero (low) will cause a negative output pulse.

PO0	- Data/address strobe (positive pulse)
PO1	- PSI43 chip reset (positive pulse)
PO2..PO7	- Register/memory address within PSI43 interface board
PO8	- Interface board reset
PO9	- I2C FIFO 9 th bit value
PO10	- I2C single command start (positive pulse)
PO11	- PSI43 reset (timing reset, positive pulse)
PO12	- Reserved (connected to the timing sequencer CPLD)
PO13	- start single sequencer cycle (positive pulse)
PO14	- clear status register (positive pulse)
PO15	- Reserved (connected to the timing sequencer CPLD)

The quiescent state of the lines PO2..PO7 will determine the internal register/memory address within PSI43 interface board. Each command from the ASIC test box will be generated by setting two bytes DCO0..DCO7 and PO2..PO7 and generating a pulse by PO0 bit. A separate bit (PO1) will reset PSI43 chip to a default state. Reserved lines PO12 and PO15 will be used if necessary to start activities within PSI43 interface board. A status byte will be available at any time for the ASIC test box to readout. Zero value will be a default (no errors) status. Summarizing, each command to the PSI43 interface board (interface board command) will require two data bytes written from Z80 processor and one Z80 command to generate strobe pulse. It will be a good idea to implement this as a separate subroutine to reduce execution time.

Single interface board commands will be used to setup analog multiplexer address. The address provided by the command will be latched within PSI43 interface board and will stay stable until changed. The I2C address of the PSI43 chip will use different command address, but will work the same way: a register will hold written value until it is changed.

Similarly, a single command will control status of the timing sequencer. We need at least a single step and continuous mode for the sequencer. We use line PO13 to start single

cycle of the sequencer. Internal counters will be preset by a set of similar single commands.

There are two modes for generation I2C commands. For most frequently used set of commands (like setting up all the pixel cells) a FIFO memory is used. The sequence of commands has to be loaded first into the FIFO and “Start I2C command stream” bit at address 02 should be used to start FIFO commands stream. To repeat FIFO commands stream or reset the FIFO a single command has to be issued at address 02 with appropriate bits set. For single I2C commands, their data has to be loaded first into four registers within the I2C CPLD (addresses 4..7), and, line PO10 can be used to generate the command. The same command can be generated any number of times by issuing pulse on the PO10 line.

PSI43 interface board commands.

1. Write I2C command data byte to FIFO, 01

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	1	0	0	0	0	0							

Note: Setting PO9 bit provides a 9th bit value for the I2C FIFO.

The following is an example of FIFO programming:

Word #	9th bit	Data byte	Comment
1	1	Command byte 1	One byte command data
2	0	Don't care	Set to zero
3	1	Command byte 1	Three byte command data
4	1	Command byte 2	Three byte command data
5	1	Command byte 3	Three byte command data
6	0	Don't care	Set to zero
7	1	Command byte 1	Four byte command data
8	1	Command byte 2	Four byte command data
9	1	Command byte 3	Four byte command data
10	1	Command byte 4	Four byte command data
11	0	Don't care	Set to zero

2. FIFO commands stream control register, 02

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	ST	RT	RF	X	X	X	X	X	0	1	0	0	0	0

Note: ST - Start I2C command stream (1 – start)
 RT - Reload FIFO (1 - retransmit)
 RF - Reset FIFO (1 – reset)

3. Set chip's I2C interface address, 03

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	IA0	IA1	IA2	IA3	X	X	X	X	1	1	0	0	0	0

IA0..IA3 - PSI43 I2C address

4. Write 1st I2C command data byte to CPLD register, 04

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	0	0	1	0	0	0							

5. Write 2nd I2C command data byte to CPLD register, 05

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	1	0	1	0	0	0							

6. Write 3rd I2C command data byte to CPLD register, 06

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	0	1	1	0	0	0							

7. Write 4th I2C command data byte to CPLD register, 07

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	1	1	1	0	0	0							

8. Set analog MUX address, 08

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	MA0	MA1	MA2	X	X	X	X	X	0	0	0	1	0	0

9. Set PSI43 interface board control register, 09

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	ON	X	X	X	X	X	X	X	1	0	0	1	0	0

ON - Buffer Board ON/OFF (1 – ON, 0 - OFF)

10. Set Calibrate pulse crossing number, 10

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	0	0	0	0	1	0							

11. Set L1 trigger pulse crossing number, 11

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	any	1	0	0	0	1	0							

12. Set clock frequencies for I2C and PSI43, 12

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	I40	I20	I10	I05	P40	P20	P10	P05	0	1	0	0	1	0

All bits set to 0 - default clock frequency (40 MHz)

I40 - I2C clock 40 MHz (1 – ON), P40 - PSI43 clock 40 MHz (1 – ON)
 I20 - I2C clock 20 MHz (1 – ON), P20 - PSI43 clock 20 MHz (1 – ON)
 I10 - I2C clock 10 MHz (1 – ON), P10 - PSI43 clock 10 MHz (1 – ON)
 I05 - I2C clock 5 MHz (1 – ON), P05 - PSI43 clock 5 MHz (1 – ON)

13. Set token signal delay for PSI43, 13

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	TD0	TD1	TD2	TD3	X	X	X	X	1	1	0	0	1	0

All bits set to 0 – illegal value, valid values are 01..0F

14. Set trigger timing control register, 14

Data/Address	D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5
Value	ON	X	X	X	F2	F4	F8	F16	0	0	1	0	1	0

ON - Sequencer ON/OFF (1 – ON, 0 - OFF)
 F2..F16 = 0 - Default trigger frequency TF = PSI43 clock/256
 F2 = 1 - TF = PSI43 clock/512
 F4 = 1 - TF = PSI43 clock/1024
 F8 = 1 - TF = PSI43 clock/2048
 F16 = 1 - TF = PSI43 clock/4096
 Any two bits F2..F16 set simultaneously produce default frequency

PSI43 interface board status byte.

Data bit	D0	D1	D2	D3	D4	D5	D6	D7
Name	NC	TKO	NC	TTO	EF	FF	E1	E0

TKO - Token Out signal latched
 TTO - Token timeout (no token received)
 EF - I2C FIFO empty flag (1 – empty)
 FF - I2C FIFO full flag (1 – full)
 E0 - Error 0 (FIFO empty when a start I2C issued)
 E1 - 9th bit has a wrong value

Note: This register is cleared by issuing PO14 pulse.