

PSI43 Pixel Chip Pin Description

The following is an excerpt from the original PSI43 v.2 documentation and e-mail exchange with R.Horisberger.

Pin #	Pin Name	Pin Description	Comment
1,2	GNDA	Analog ground	Not connected to GNDD
3,4	GNDD	Digital ground	Not connected to GNDA
5	Cap (DAC)	DAC regulator filter cap	Value=100 nF
6,7	VD-	Digital Voltage (power)	VD nom = -5.5V
8	token_out-	Token signal output, diff.	LVDS levels, Vcm= -1.2V
9	token_out+	Token signal output, diff.	LVDS levels, Vcm= -1.2V
10	Cap (D)	VD regulator filter cap	Value=100 nF
11	trig_out-	Trigger signal output, diff.	LVDS levels, Vcm= -1.2V
12	trig_out+	Trigger signal output, diff.	LVDS levels, Vcm= -1.2V
13	i2c_dat-	PSI2C sda data input, diff.	LVDS levels, Vcm= -1.2V
14	i2c_dat+	PSI2C sda data input, diff.	LVDS levels, Vcm= -1.2V
15	i2c_clk-	PSI2C scl clock input, diff.	LVDS levels, Vcm= -1.2V
16	i2c_clk+	PSI2C scl clock input, diff.	LVDS levels, Vcm= -1.2V
17	Cap (LVDS)	LVDS regulator filter cap	Value=100 nF
18	V_iref	Current Reference DAC input	Reference voltage control
19	i2c_a0	PSI2C Address bit 0, input	CMOS level VD-..0
20	i2c_a1	PSI2C Address bit 1, input	CMOS level VD-..0
21	i2c_a2	PSI2C Address bit 2, input	CMOS level VD-..0
22	i2c_a3	PSI2C Address bit 3, input	CMOS level VD-..0
23	aout-	Analog Output Signal, diff.	Current source, R=100 ohms
24	aout+	Analog Output Signal, diff.	Current source, R=100 ohms
25	GNDD	Digital ground	Not connected to GNDA
26	reset	Chip Reset input	CMOS level VD-..0
27	Cap (H)	Sample/Hold Voltage filter cap	Value=100 nF
28	cal_trig_res-	Combined Control Signal, diff.	LVDS levels, Vcm= -1.2V
29	cal_trig_res+	Combined Control Signal, diff.	LVDS levels, Vcm= -1.2V
30	clk-	Clock Input, diff.	LVDS levels, Vcm= -1.2V
31	clk+	Clock Input, diff.	LVDS levels, Vcm= -1.2V
32	token_in-	Token Input, diff.	LVDS levels, Vcm= -1.2V
33	token_in+	Token Input, diff.	LVDS levels, Vcm= -1.2V
34	Cap (A)	VA regulator filter cap	Value=100 nF
35	V_vref	Voltage Reference DAC input	Reference voltage control
36,37	VA-	Analog Voltage (power)	VA nom = -2.5V
38,39	VH-	Sample/Hold Voltage (power)	VH nom = -3.8V..-5.0V
40,41	VC-	Comparator Voltage (power)	VC nom = -3.0V
42	Cap (C)	VC regulator filter cap	Value=100 nF

Note: CMOS levels correspond normal positive CMOS levels shifted to -VD, i.e. logical 1 is zero volts, and logical 0 is -VD