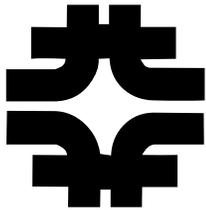


CMS Pixel Chip PSI46 - preliminary tests for V2 -



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U S C M S

The Compact Muon Solenoid Collaboration

PSI46 NEW Test procedure

The proposed steps during a chip test are:

- Set interface board I2C address (adrs1), calibrate pulse number (ncal), trigger pulse number (ntrig), token delay (tokendel), PSI46 and I2C frequency (freq) and I2C clock to 'external'. These parameters are not changed during test.
- Load interface board FIFOs with
 - a) PSI46 DAC settings (suggested values from PSI) and
 - b) program data for all pixels in 'unmask' mode with trim=8 (0 to 16)
- Set programmable power supply ON (psdig=2V, psana=1.5V) and do chip reset
- Read power supply currents and voltages (first time)
- Start FIFO stream download to PSI46
- Read power supply currents and voltages (second time)
- Issue a single trigger sequence, do timing reset and do clear calibration (clears all pixels data)
- Test DACs' linearity for six values: use 0x00,40,80,C0,FF and default for 8bit DACs, use 0x00,4,8,C,F and default for 4bit DACs
- Start a pixel cycle: Set mask=1 (pixel enabled) and trim bits to a minimum value. Increase VCAL until pixel responds. Store this data. Flag if more than one pixel is responding. Double VCAL and disable pixel. Verify that pixel is not responding. Enable pixel and increment trim bits. Repeat VCAL cycle. When done with all mask and trim bits, go to new pixel and repeat. Do this for all 52*80 pixels.
- Set programmable power supply OFF
- Start data_analysis program and write report file

PSI46 DACs' Linearity

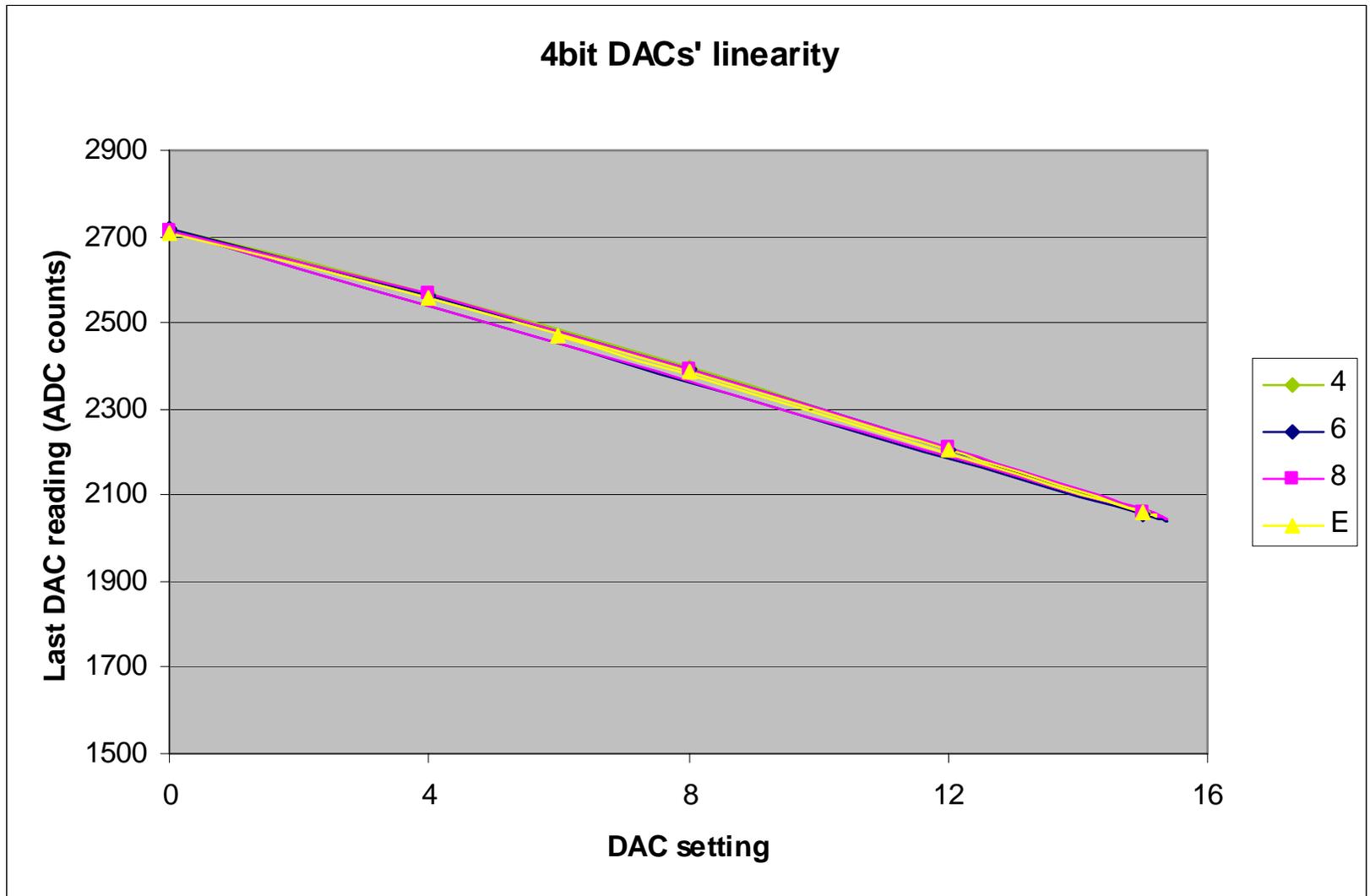
```
*****
REPORTING DAC LINEARITY TEST RESULTS
DAC(hex) PASS/FAIL Slope Intercept RSQ
1          0          0          0
2          0          0          0
3    PASS   -2.72     2766     -1
4    PASS  -44.43     2733     -1
5    PASS   -2.66     2762     -1
6    PASS  -43.37     2723     -1
7    PASS   -2.67     2764     -1
8    PASS  -43.33     2724     -1
9    PASS   -2.69     2769     -1
A    PASS   -2.7      2773     -1
B    PASS   -2.69     2770     -1
C    PASS   -2.72     2779     -1
D          0          0          0
E    PASS  -43.31     2724     -1
F    PASS   -2.63     2752     -1
10   PASS   -2.64     2753     -1
11   PASS   -2.66     2758     -1
12   PASS   -2.65     2756     -1
13   PASS   -0.15     2341    -0.06
14   PASS   -2.8      2791     -1
15   PASS    0.11     2190    0.08
16   PASS   -2.67     2764     -1
17   PASS   -2.67     2763     -1
18   PASS   -2.67     2764     -1
19   PASS   -2.74     2734     -1
1A   PASS   -2.71     2727     -1
1B   PASS   -0.02     2157    -0.64
FE   PASS   -1.73     2674    -0.61
FD   FAIL DACLinLength error  0      0      0
*****
```

- Each DAC data is interpolated with a straight line.
- The report file shows the DAC address (in hex), the SLOPE and INTERCEPT of the fit-line and also a statistical indication of linearity (RSQ is the Pearson product momentum correlation coefficient).
- There is also a PASS/FAIL parameter reported. If the pixel response has more 'bits' than UltraBlack, Black and LastDac, a DACLinLength error is reported.

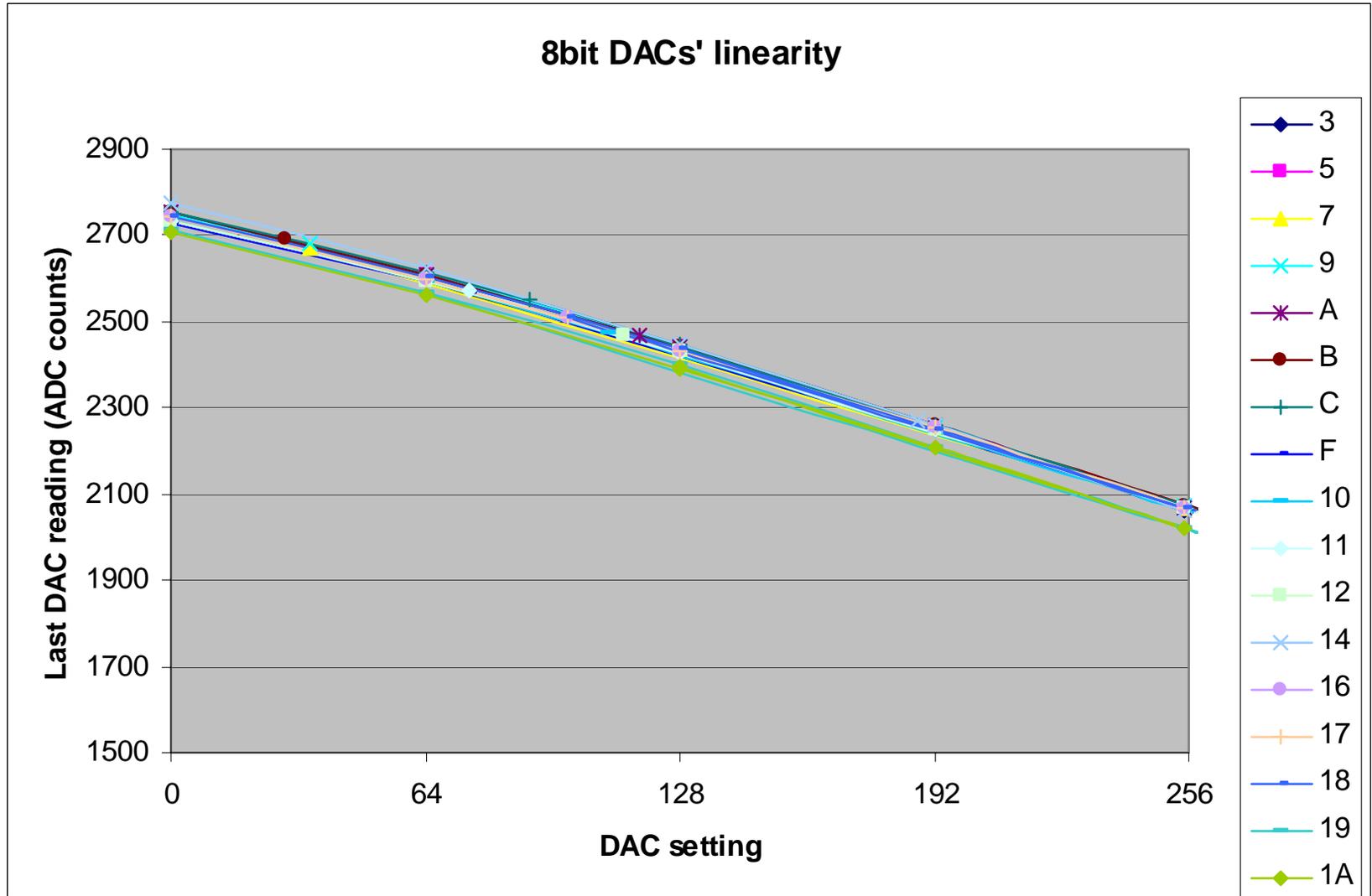
QUESTIONS/ DECISIONS:

- Why some DACs are linear, some other aren't? How to measure and qualify DACs that control the analog output amplitude?
- How to evaluate some DACs that control the power supply regulators of the chip (0x01 and 0x02) and/or other DACs like 0x0D (all three not measured here)?
- What criteria should be used to accept/reject a chip based on the above DACs linearity measurements?
- Temperature DAC 0x1B is a read-only register. It provides an analog output proportional with chip temperature (see slides 7 and 8).

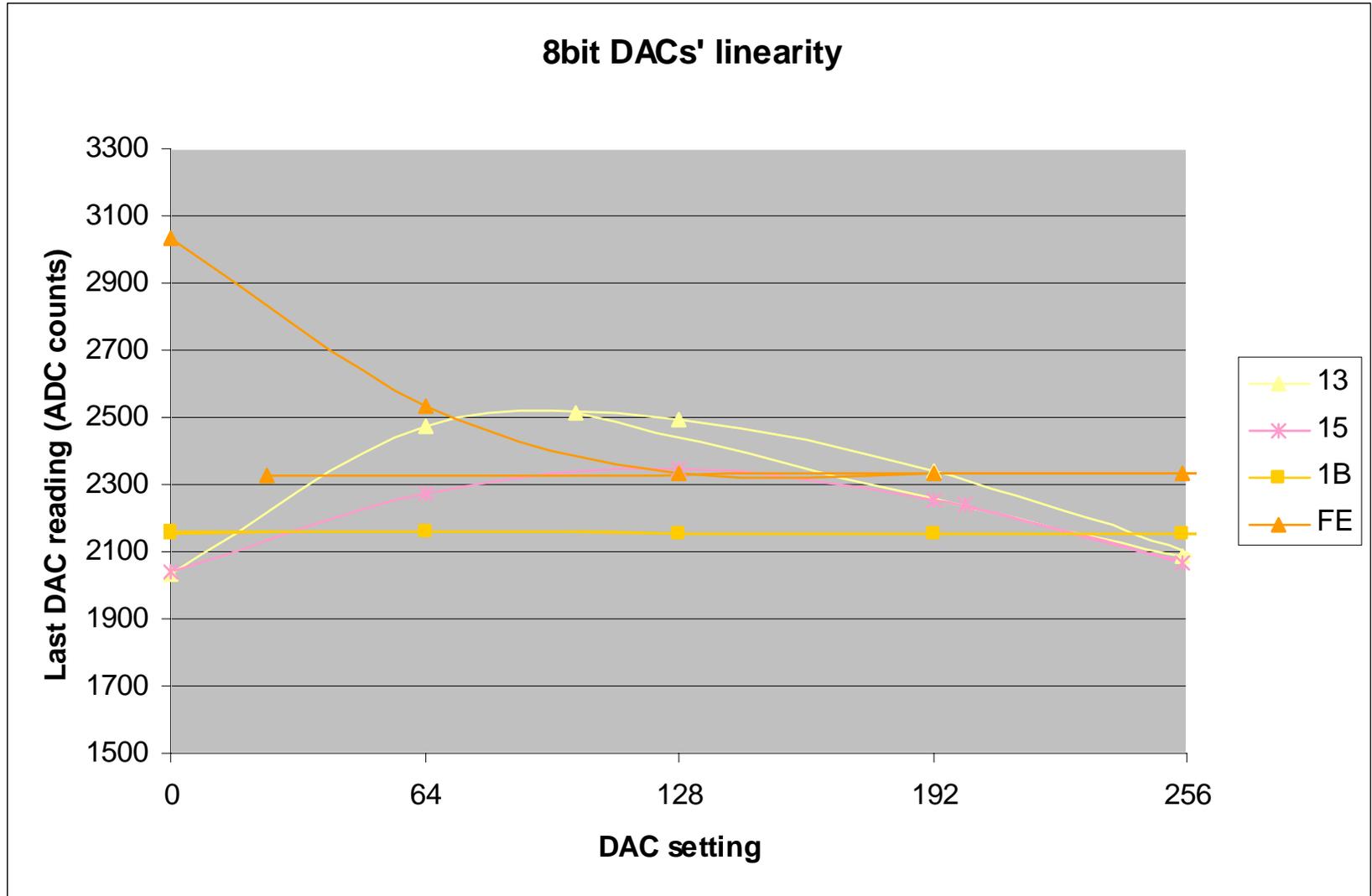
PSI46 DACs' Linearity(1)



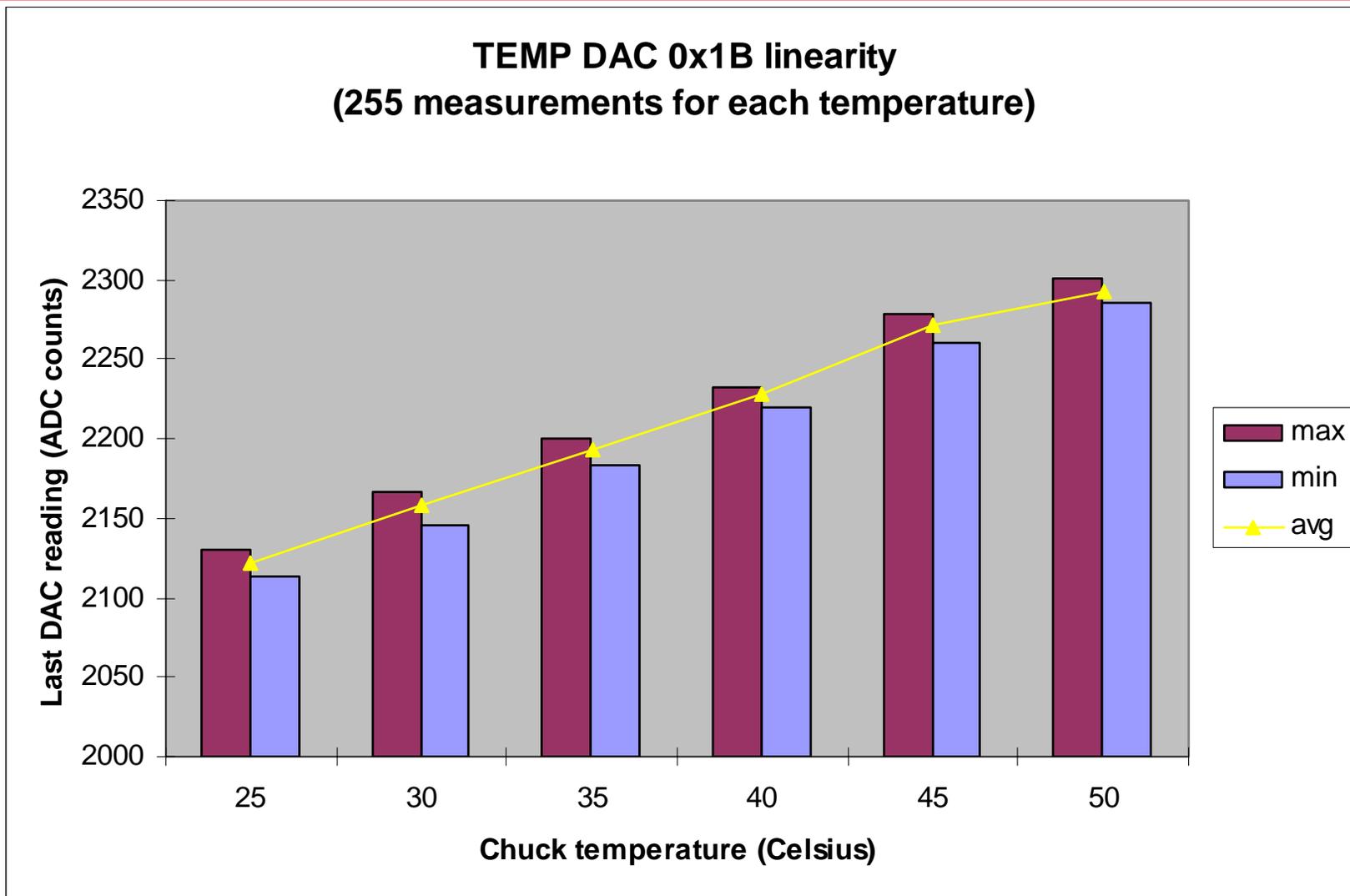
PSI46 DACs' Linearity(2)



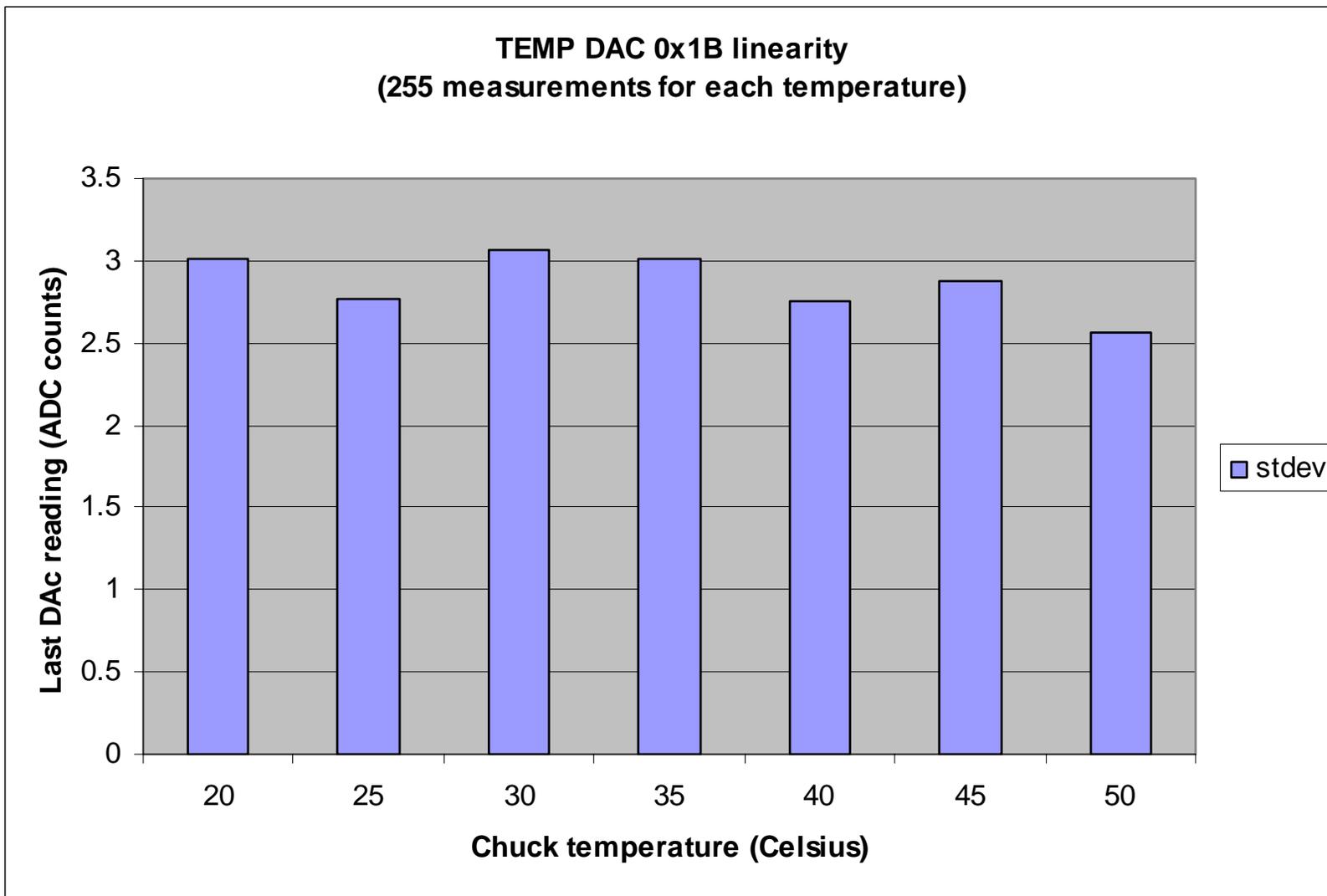
PSI46 DACs' Linearity(3)



Temperature Register (1)



Temperature Register (2)



One pixel measured 100 times

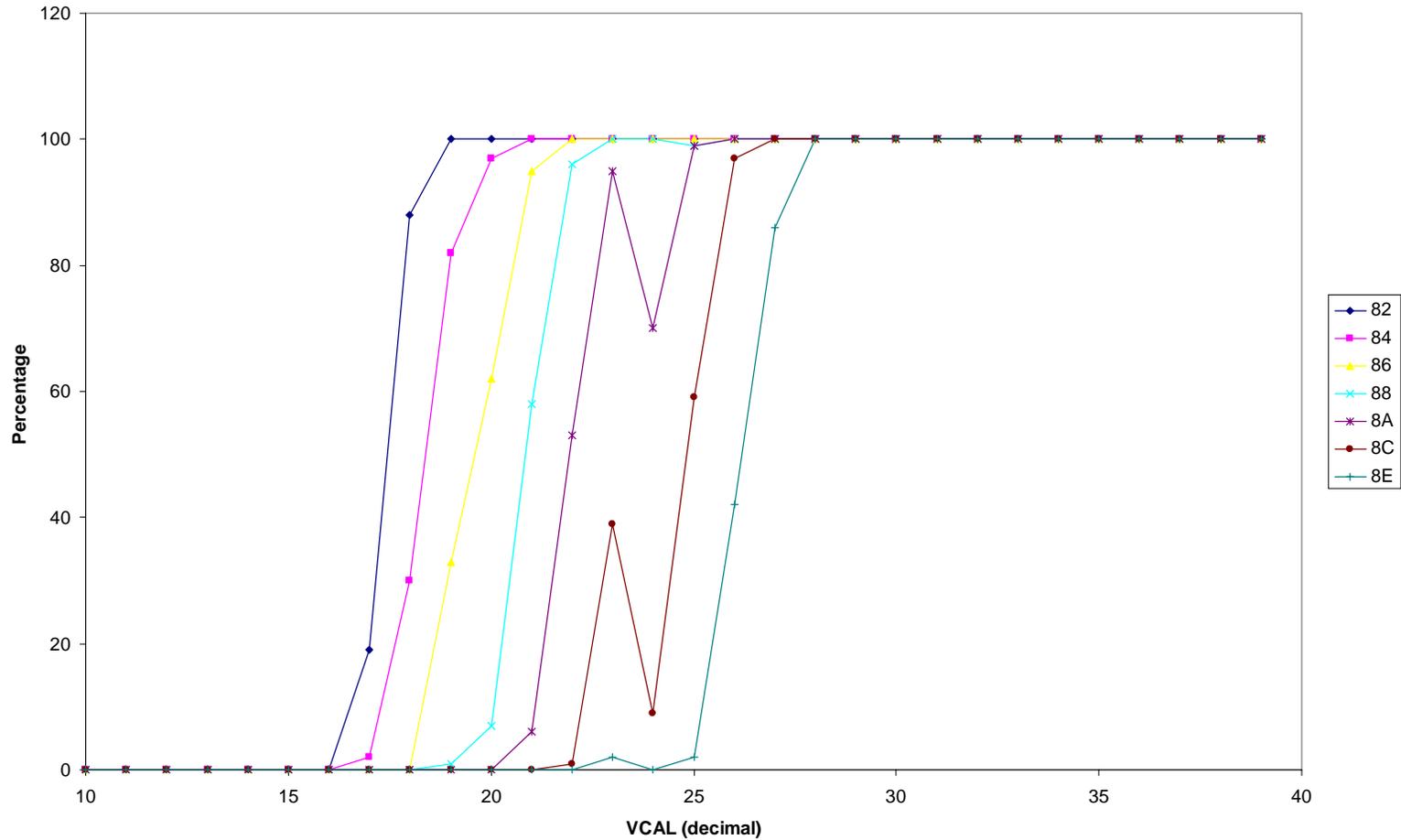
- Six pixels from the same chip are presented on slides 10,11,12,13,14,15.
- The pixels are located in columns 0 and 28, rows 0, 40 and 79.
- The TRIM bits were set to: 2,4,6,8,10,12,14 (decimal value, their range is 0 to 15)
- The VCAL was set to: 10,11,12,13.....39 (decimal value, its range is 0 to 255)
- In each of the above matrix points (30 VCALs times 7 TRIMs = 210 points), the pixel response was measured 100 times in order to have a reasonable statistical estimate of its threshold. Thus a total of 21000 measurements were performed for each pixel.
- The purpose of this test, which is time consuming and is not likely to be included in the production test (?), was to have a detailed picture of a pixel response for a complete array of TRIM and VCAL values.

QUESTIONS/ DECISIONS:

- For all six pixels there is a curve break at VCAL=24 (see slides 10 to 12). Is this a VCAL decoder problem? Or a VCAL broken bit register problem? Or just a particular behavior for this chip? But then, since we can see it in different columns and rows (columns 0 and 28, rows 0, 40 and 79), that means it is related to something common on this chip.
- In a similar way, it seems that two TRIM curves overlap at VCAL=15 (see slides 13 to 15) . Similar questions arise.
- In order to investigate this behavior and to eliminate suspicions about possible measurement errors or test-board problems, two more tests were done:
 - First, the VCAL DAC linearity was (re)measured in increments of only one bit. A straight line was used to fit data using the new 255 points (see slides 16, 17). For each setting point only one measurement was taken. We found nothing strange around VCAL=25 or VCAL=15.
 - Second, the measurement for particular DAC settings, i.e. around VCAL=15 and 25, were repeated 255 times (see slides 18, 19 and 20) for each setting. A change in the slope of VCAL vs. DAC setting can be observed and its 'direction' is in consistence with the curve break or overlap seen in slides 10 to 15.
- Based on the above tests, we can say that the VCAL curve break or overlap is not due to measurement error or test-board problems. We claim that it is due to a defect inside this chip, related perhaps with VCAL register digital to analog conversion (15=b01111, 16=b10000, 23=b10111, 24=b11000). Then the obvious question will be if there is a faster method to find out defects like this one.

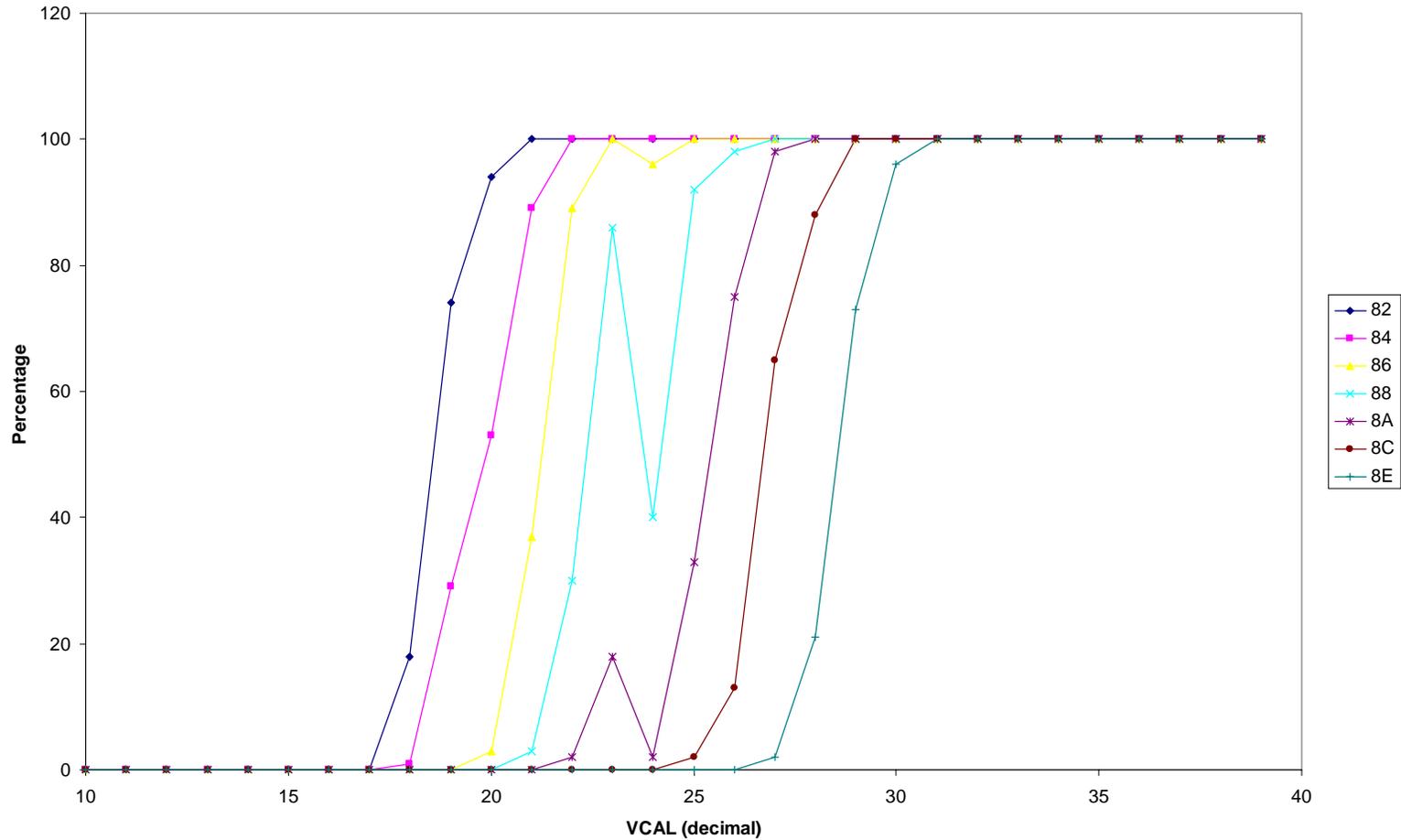
One pixel measured 100 times (1)

Pixel response probability (Column=0 Row=0 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)



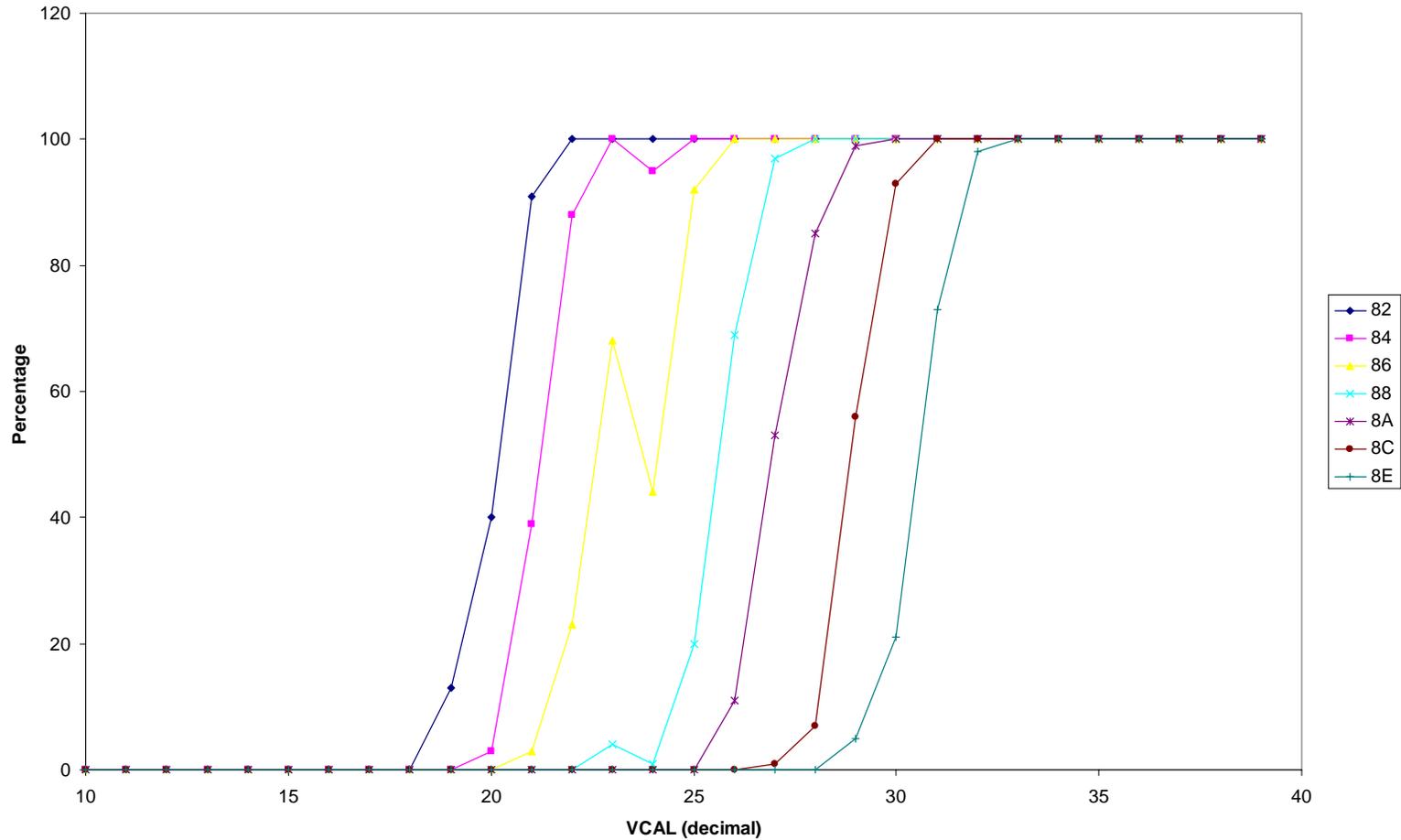
One pixel measured 100 times (2)

Pixel response probability (Column=0 Row=40 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)



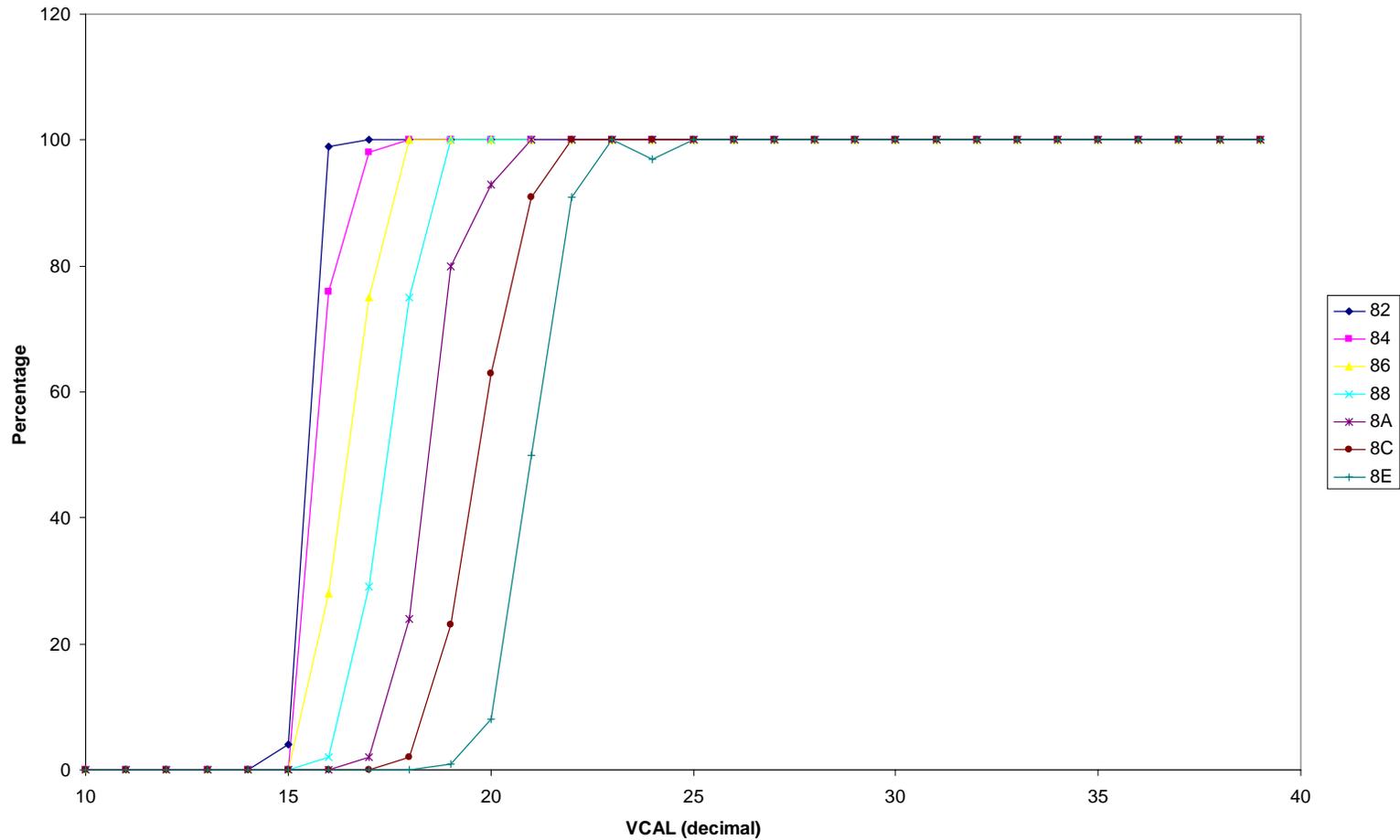
One pixel measured 100 times (3)

Pixel response probability (Column=0 Row=79 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)



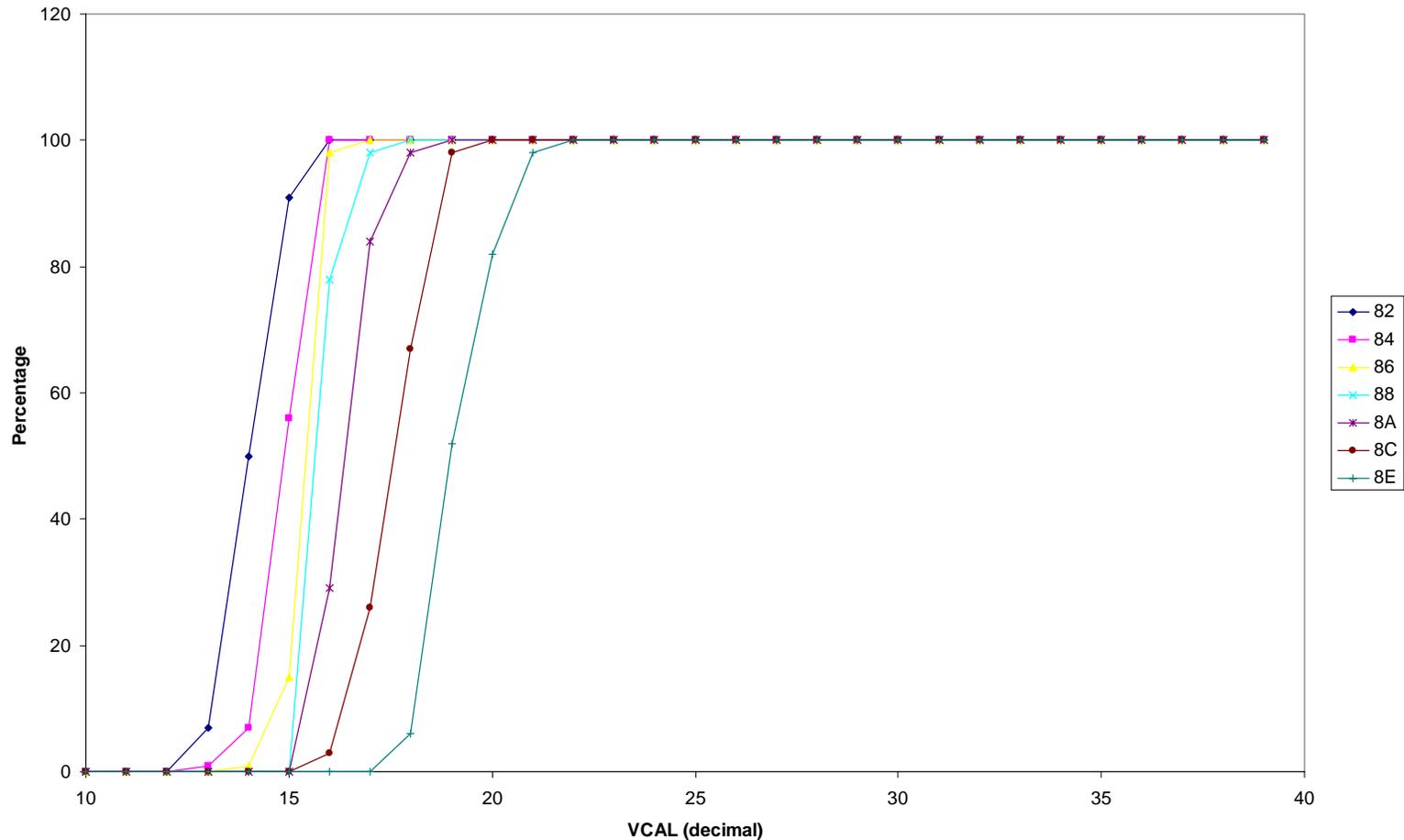
One pixel measured 100 times (4)

Pixel response probability (Column=28 Row=0 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)



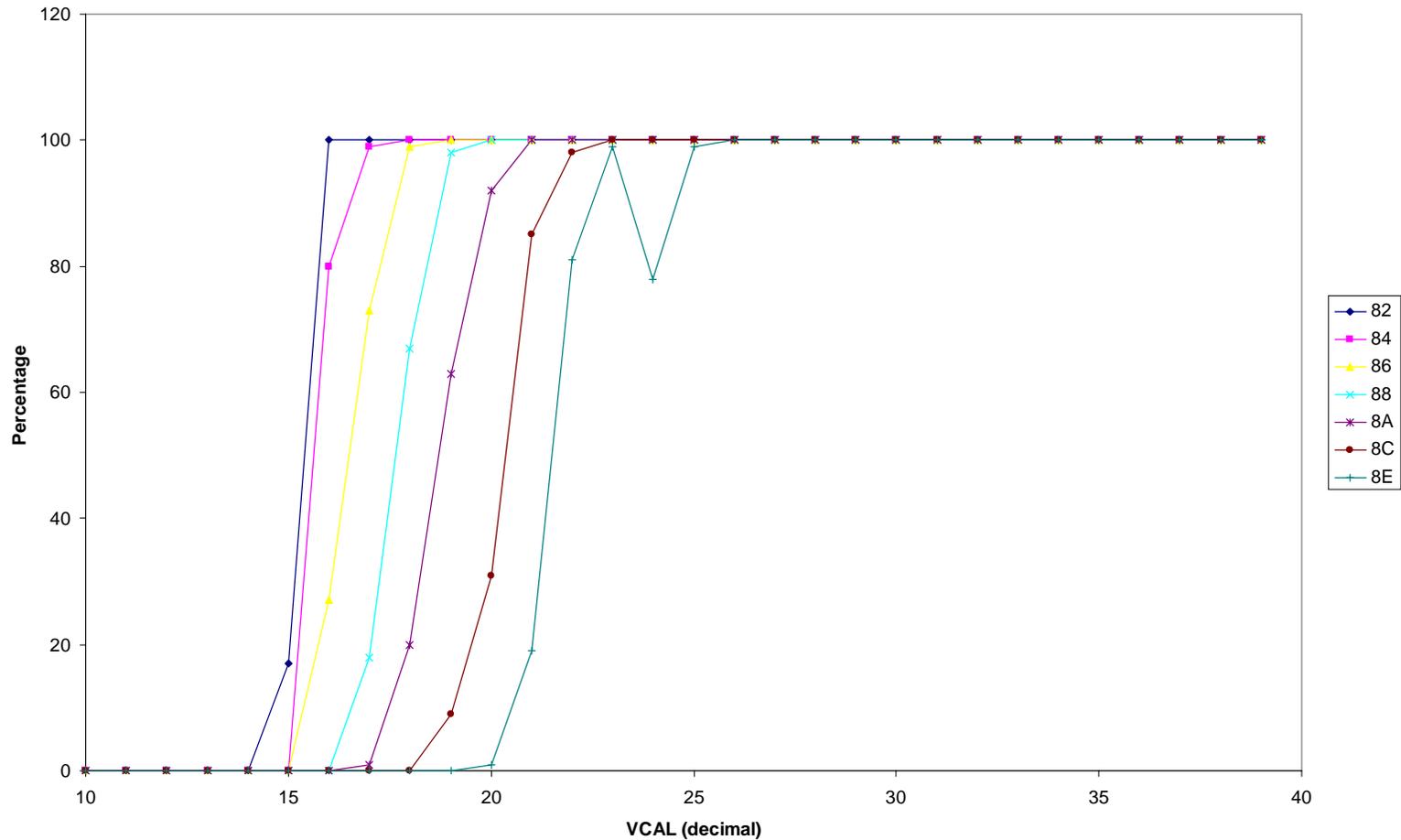
One pixel measured 100 times (5)

Pixel response probability (Column=28 Row=40 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)

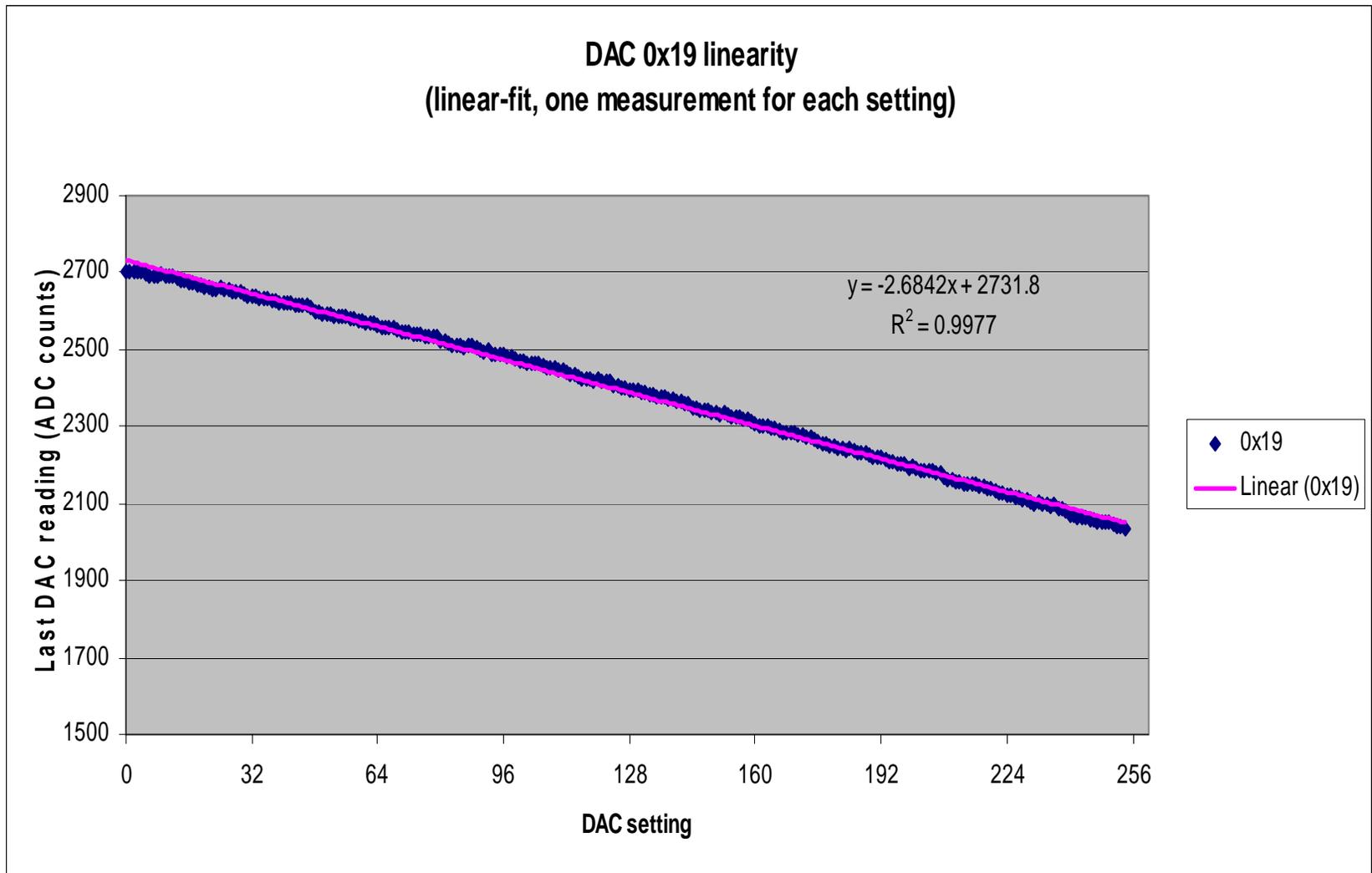


One pixel measured 100 times (6)

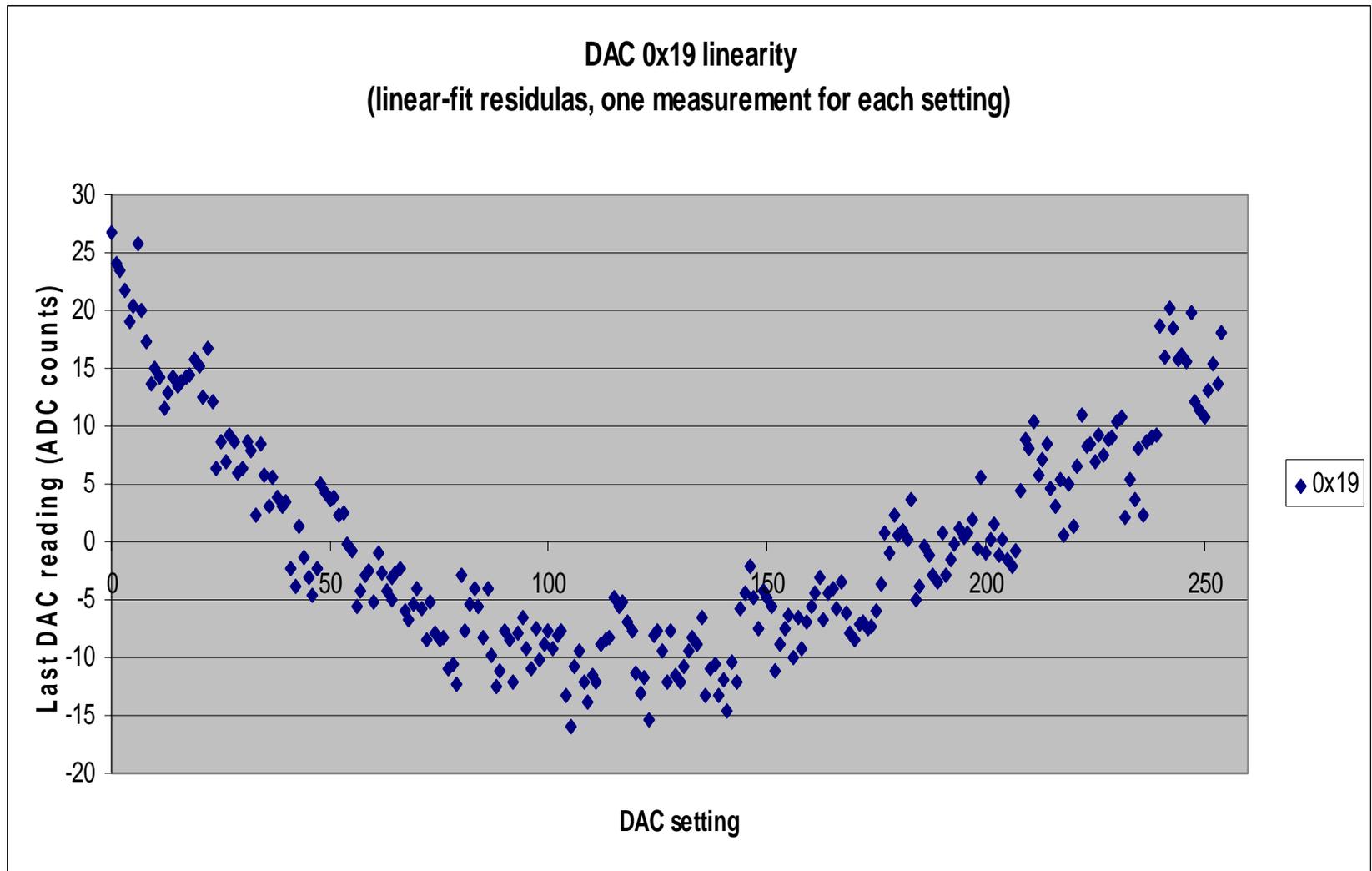
Pixel response probability (Column=28 Row=79 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex)



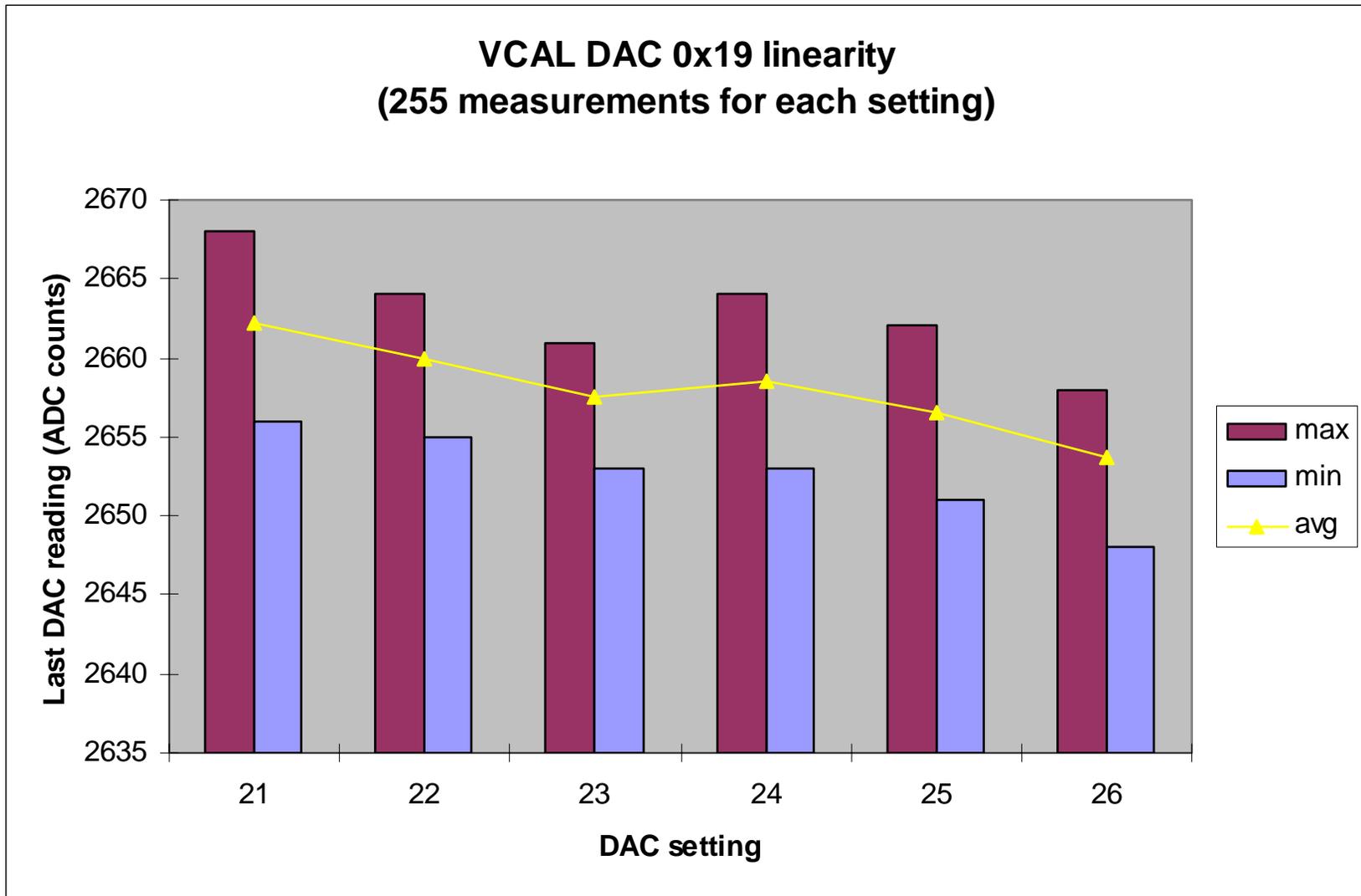
PSI46 DACs' Linearity(4)



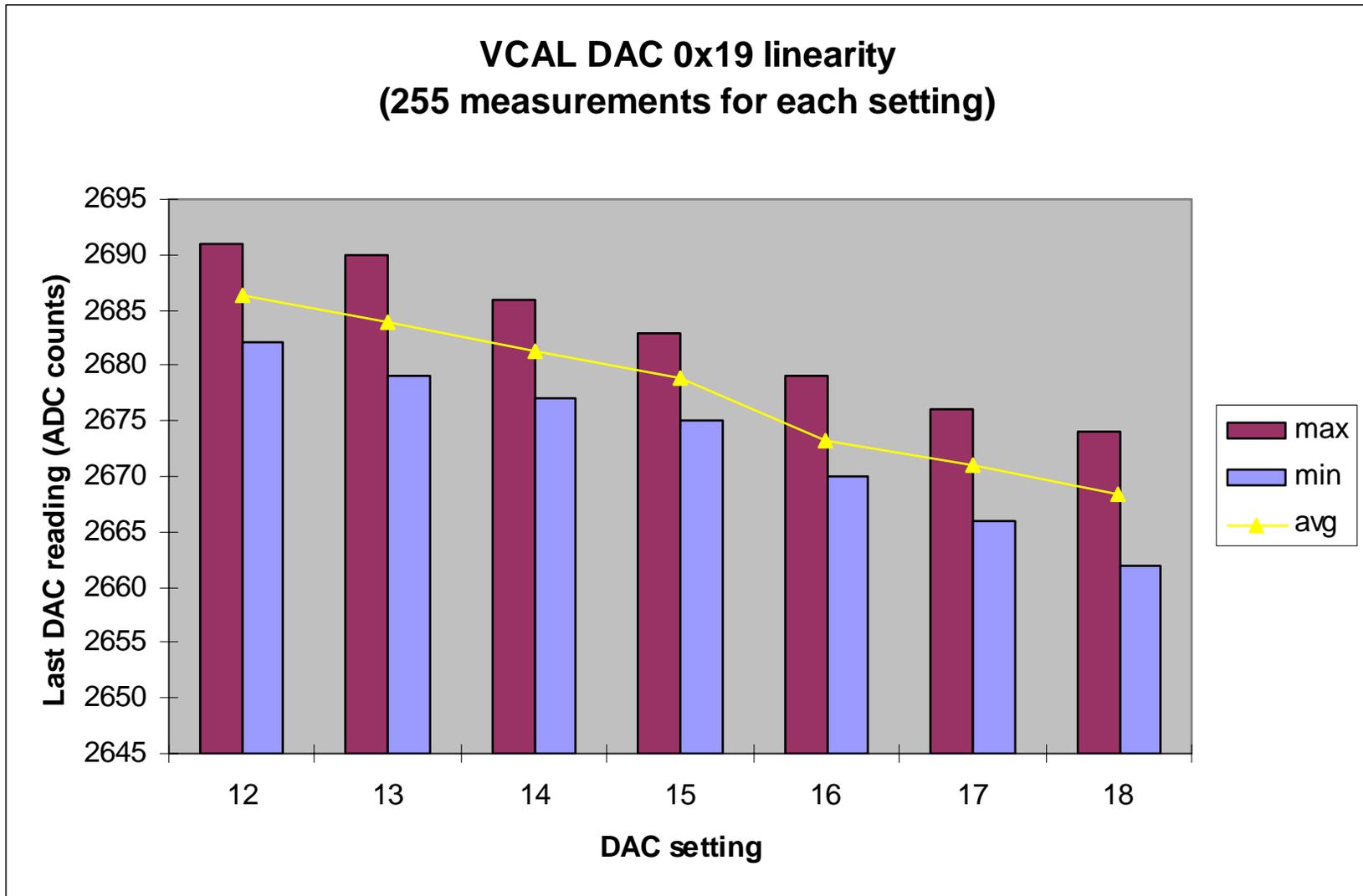
PSI46 DACs' Linearity(5)



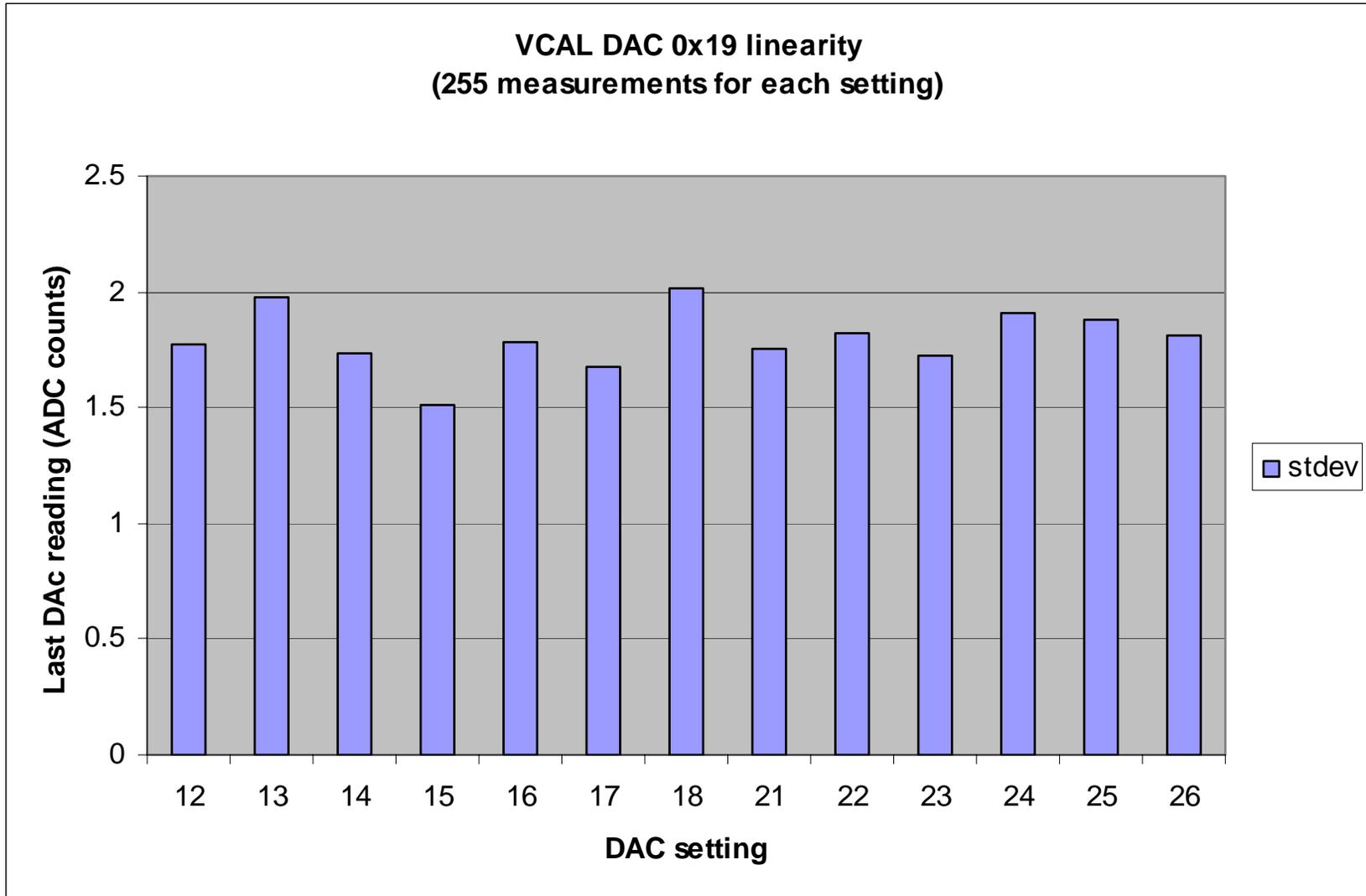
Why we have the break (1)



Why we have the break (2)



Why we have the break (3)



Measuring all pixels

PIXEL MEASUREMENT ALGORITHM (see also the short description from slide 2).

- Starting with a TRIM_min value, the TRIM bits are incremented in TRIM_step up to a TRIM_max value.
- For each TRIM setting, the VCAL is incremented from VCAL_min to VCAL_max in VCAL_step.
- When the pixel responds with an analog data that contains exactly one hit response data length (pedestal, ultra black, black, last dac, two double column bits, three row bits and one charge bit, I.e. 10 'bits'), the digitized analog data is recorded and VCAL loop is exited. The TRIM and VCAL values are also recorded. If the data length is <>10bits (pixel responded with one hit) and also <>4bits (no hit response from pixel), an error flag is asserted and the VCAL loop is exited.
- After the VCAL loop is exited, the pixel is disabled, the exit-loop value of VCAL is doubled and the pixel response with only ultra black, black and last dac is verified. Any other response data length is flag as an error.
- Then VCAL is restored to exit-loop value, subtracted two VCAL_steps, the TRIM is incremented to a new (higher) value, the pixel is (re)enabled and the digitized analog output data length is monitored for each VCAL increment until the pixel fires again. The TRIM cycle is repeated up to TRIM_max.

TESTING TIME

- Based on previous 100 pixel measurements I opted for: VCAL_step=0x02, VCAL_min=0x02, VCAL_max=0x40.
- I just picked TRIM_min=0x02 and did the test for three values of TRIM_step:0x02, 0x03 and 0x06 which says that TRIM loop is repeated 7, 5 and 3 times respectively for each pixel (TRIM can't exceed 0x0F).
- Test time (just for this particular routine) varied from 360sec to 245sec and 140sec respectively.
- Test time is somehow proportional with computer processor's speed and is affected by the RAM size. The above timings are for a PC with 1GHz x86 and 512Mb RAM. The testing time increases 2-3 times for a 500MHz PC with 128Mb RAM. The RS232 is at a maximum (available now) 115K baud rate for the test-box.

SLIDES

- Slides 22, 23 and 24 show how data is reported in a text file, with slide 22 reporting the 'as measured' data when pixel fires, slide 23 being a statistic for each pixel, and slide 24 a final statistic over all pixels.
- Slide 25 is a graphical example of the linear-fit reported in slide 23. Slides 26 and 27 shows the slope and intercept of the linear-fit over all 4160 pixels.
- Slide 28 shows the column analog levels over all 4160 pixels. Slide 29 is the similar one for row levels. Slide 30 is just a blowup of row levels on first 240 pixels. They look nice, being well separated, but this is just one chip! We don't know how much they will offset between chips and wafers.

Measuring all pixels (1)

PC	PR	MT	ERR	VCAL	PED	UB	B	LD	CO	C1	A0	A1	A2	Q
1	1	2	0	10	2048	764	1927	2688	1753	1670	3063	2495	3144	2512
1	1	4	0	12	2049	765	1929	2682	1755	1667	3059	2496	3144	2512
1	1	6	0	14	2048	762	1926	2677	1755	1671	3064	2496	3146	2517
1	1	8	0	14	2047	761	1927	2676	1756	1668	3063	2496	3147	2516
1	1	10	0	14	2047	764	1930	2679	1757	1668	3060	2494	3146	2517
1	1	12	0	16	2048	767	1929	2671	1752	1669	3061	2495	3146	2516
1	1	14	0	16	2047	766	1928	2670	1754	1667	3058	2494	3144	2520
1	2	2	0	12	2046	758	1927	2681	1757	1668	3063	2497	2453	2460
1	2	4	0	14	2047	767	1927	2676	1753	1668	3063	2500	2448	2461
1	2	6	0	16	2047	759	1927	2671	1753	1668	3070	2496	2452	2462
1	2	8	0	16	2048	764	1927	2666	1753	1668	3064	2497	2449	2460
1	2	10	0	16	2050	766	1927	2668	1751	1671	3061	2499	2450	2453
1	2	12	0	18	2045	764	1928	2665	1752	1667	3059	2496	2448	2456
1	2	14	0	18	2047	765	1927	2665	1757	1669	3058	2498	2448	2457
1	3	2	0	10	2047	764	1928	2688	1757	1668	3061	2496	1744	2382
1	3	4	0	10	2048	766	1928	2684	1754	1671	3061	2496	1744	2383
1	3	6	0	14	2048	766	1928	2678	1759	1671	3061	2494	1742	2382
1	3	8	0	14	2048	763	1924	2678	1754	1670	3062	2495	1744	2384
1	3	10	0	16	2048	766	1928	2669	1753	1666	3062	2495	1743	2381
1	3	12	0	16	2048	765	1928	2668	1751	1670	3061	2493	1744	2384
1	3	14	0	16	2048	766	1928	2672	1755	1672	3061	2494	1742	2380

WHAT IS REPORTED

- A complete report of what is measured contains (see above report sample) pixel column and row, trim bits, error, calibration voltage when pixel fired, pedestal, ultra black, black, last dac, column and row analog levels and pixel charge.

Measuring all pixels (2)

PC	PR	ERR	SLOPE	INTERCEPT	R^2	PED	UB	B	CO	C1	A0	A1	A2
1	1	0	0.46	10	0.94	2048	764	1928	1755	1669	3061	2495	3145
1	2	0	0.46	12	0.94	2047	763	1927	1754	1668	3063	2498	2450
1	3	0	0.57	9.14	0.92	2048	765	1927	1755	1670	3061	2495	1743
1	4	0	0.64	8.57	0.95	2048	765	1927	1753	1670	3062	2144	3110
1	5	0	0.46	11.14	0.88	2047	763	1928	1754	1670	3063	2146	2416
1	6	0	0.36	12.57	0.81	2047	764	1927	1753	1669	3062	2145	1711
1	7	0	0.32	13.14	0.77	2048	763	1928	1753	1669	3063	1789	3076
1	8	0	0.39	12	0.87	2047	764	1928	1753	1670	3064	1787	2384
1	9	0	0.5	10	0.94	2047	763	1928	1754	1669	3062	1787	1676
1	10	0	0.5	9.43	0.97	2047	765	1928	1755	1670	2728	3406	3213
1	11	0	0.5	11.43	0.97	2047	764	1928	1755	1669	2730	3406	2532
1	12	0	0.32	12.29	0.88	2047	764	1928	1754	1669	2728	3406	1831
1	13	0	0.36	12.57	0.81	2047	764	1928	1754	1669	2728	3161	3200
1	14	0	0.36	11.71	0.81	2047	764	1928	1754	1670	2729	3163	2513
1	15	0	0.5	11.43	0.97	2047	763	1928	1753	1669	2729	3163	1806
1	16	0	0.61	10.86	0.98	2047	764	1929	1754	1669	2729	2826	3175
1	17	0	0.54	10.29	0.92	2047	764	1928	1754	1671	2728	2827	2481
1	18	0	0.39	12.29	0.89	2047	764	1928	1754	1669	2728	2827	1775
1	19	0	0.43	11.43	0.95	2048	764	1928	1754	1669	2729	2464	3144
1	20	0	0.61	8.57	0.95	2047	764	1928	1754	1670	2730	2464	2446

WHAT IS REPORTED

- A statistical summary report contains (see above) pixel column and row, then error, slope, intercept and Pearson's correlation coefficient for the linear-fit of VCAL (at which each pixel fired) vs. TRIM, and then the average values (over all TRIM-VCAL firing-points) of pedestal, ultra black, black and columns and row analog levels.
- NOTE. The pixel charge should also have a linear dependence of VCAL and I can add a fit-line parameters for charge vs. vcal. But at this moment I didn't implement it, since this version of PSI chip has a known charge output design problem.

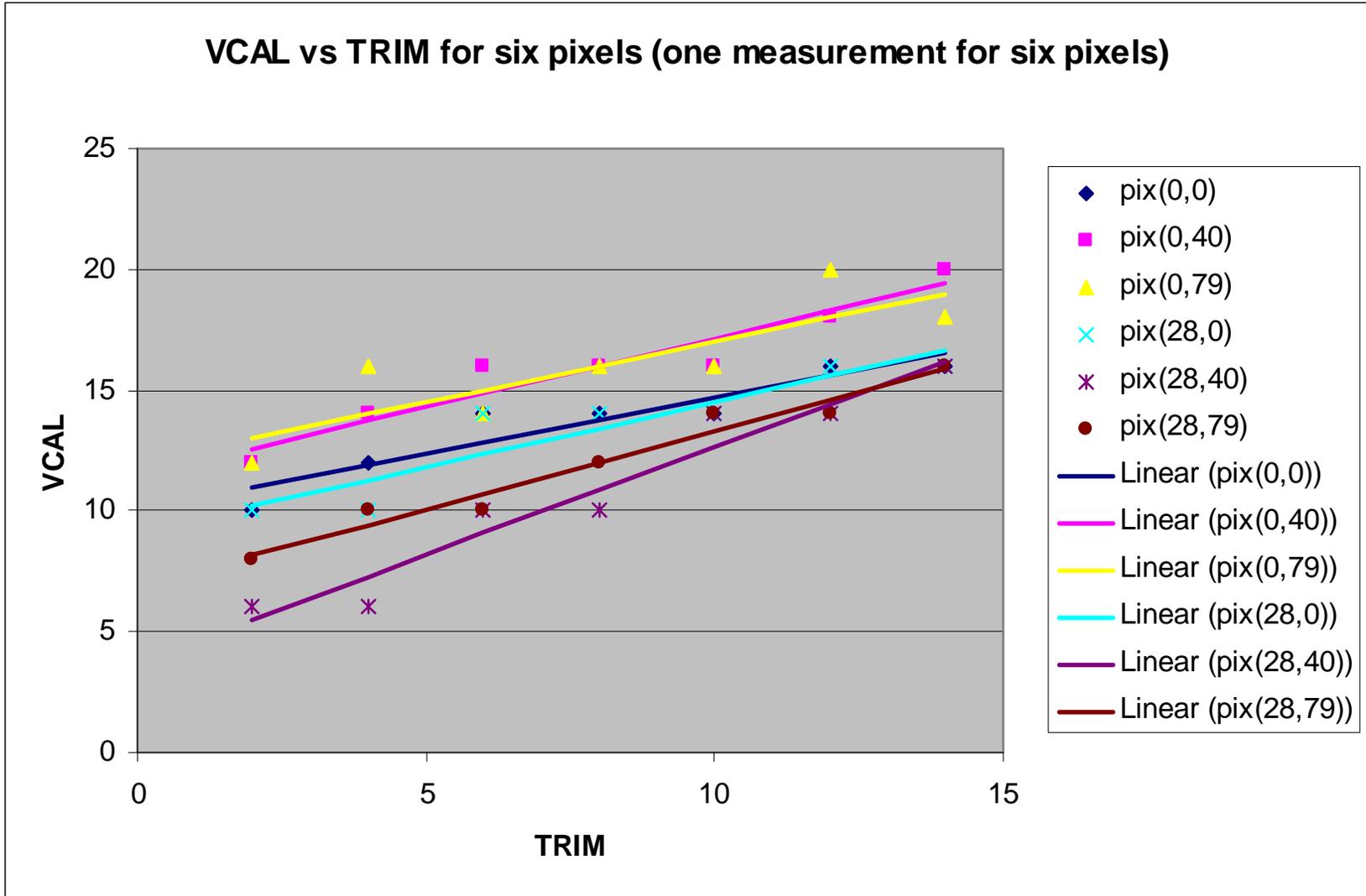
Measuring all pixels (3)

```
*****
PARAM      AVERAGE  MIN      MAX      ENTRIES
*****
TVS        0.55      0.21     0.96     4160
TVI        8.8       2        14.29    4160
TVR2       0.93      0.69     0.99     4160
PED        2051     2047     2053     4160
UBK        768      763      771      4160
BK         1929     1927     1932     4160
CLev1      1750     1668     1813     1760
RLev1      1749     1653     1845     2288
CLev2      2109     2028     2169     1760
RLev2      2104     2011     2198     2392
CLev3      2454     2380     2487     1600
RLev3      2453     2360     2544     2418
CLev4      2817     2742     2848     1600
RLev4      2809     2724     2900     2262
CLev5      3141     3075     3182     960
RLev5      3140     3057     3225     1794
CLev6      3374     3321     3426     640
RLev6      3382     3301     3468     1326
```

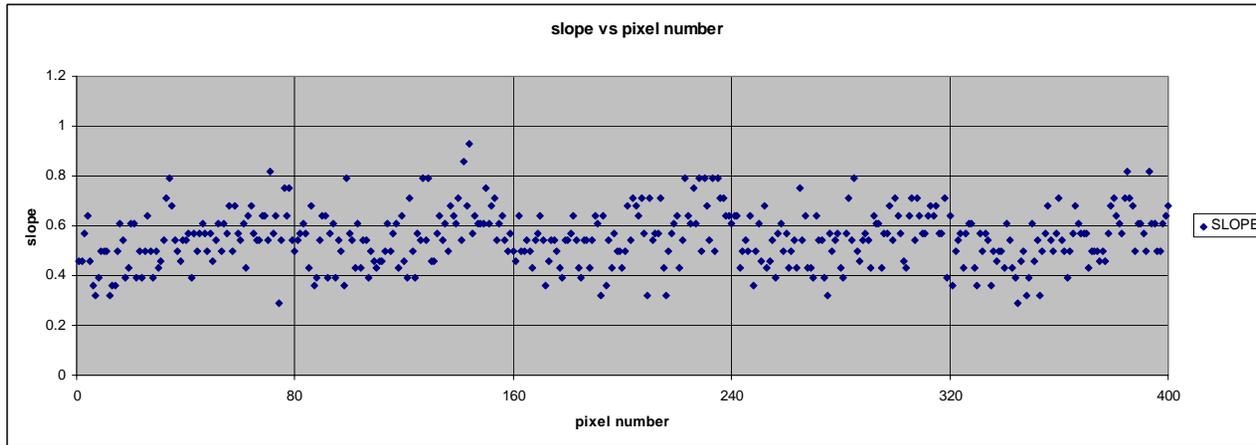
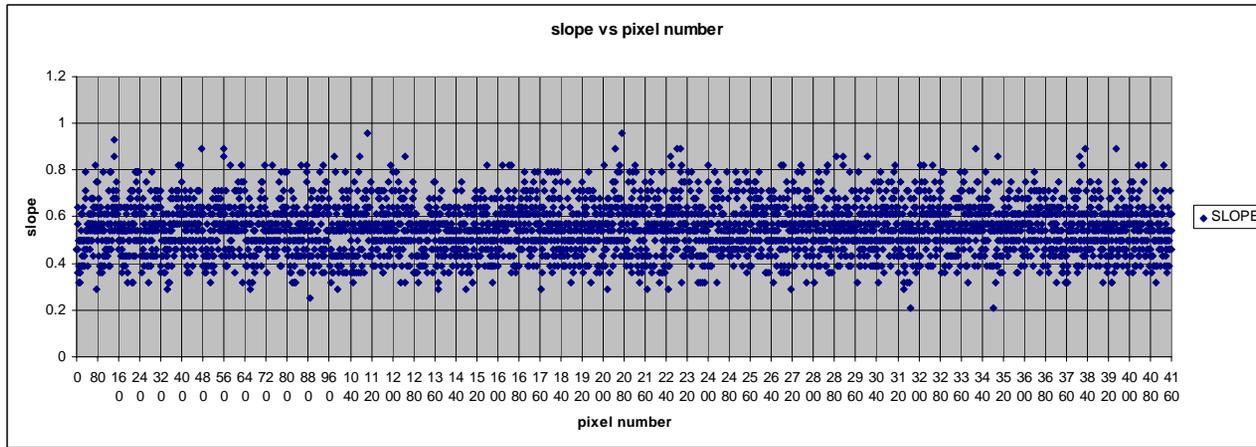
WHAT IS REPORTED

- A quick summary report that contains the average, minimum and maximum values as well as the number of entries for: TVS=Trim-Vcal Slope, TVI=Trim-Vcal Intercept, TVR2=Trim-Vcal linear-fit correlation, PED=pedestal, UBK=Ultra Black, BK=Black, followed by the 6 analog levels (in ADC counts) for rows and columns. This statistics is done over all (52*80=4160) pixels without errors.

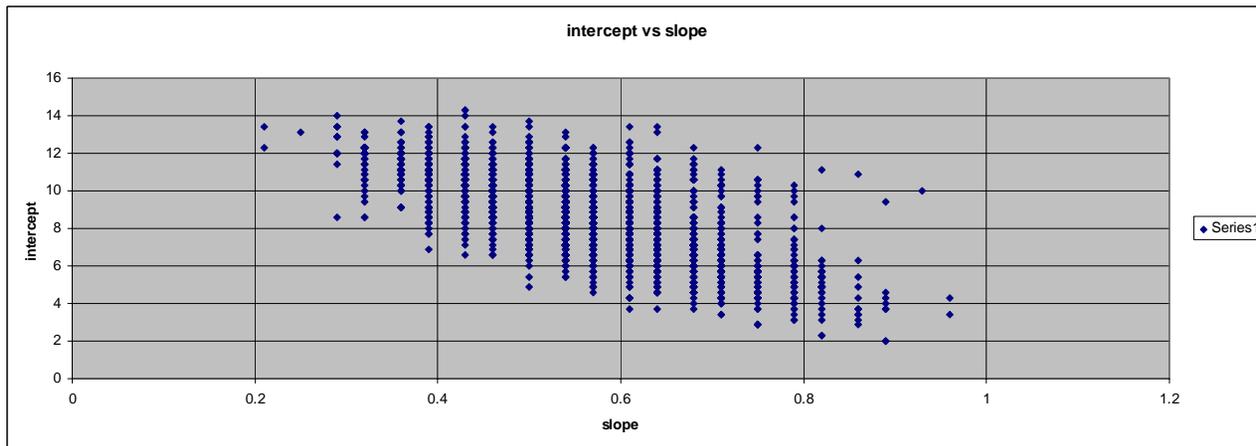
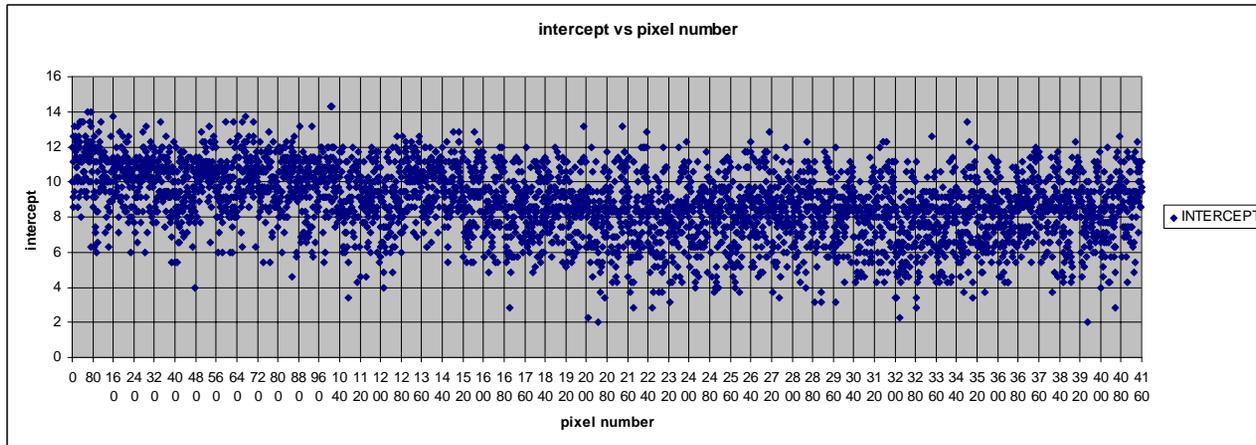
Measuring all pixels (4)



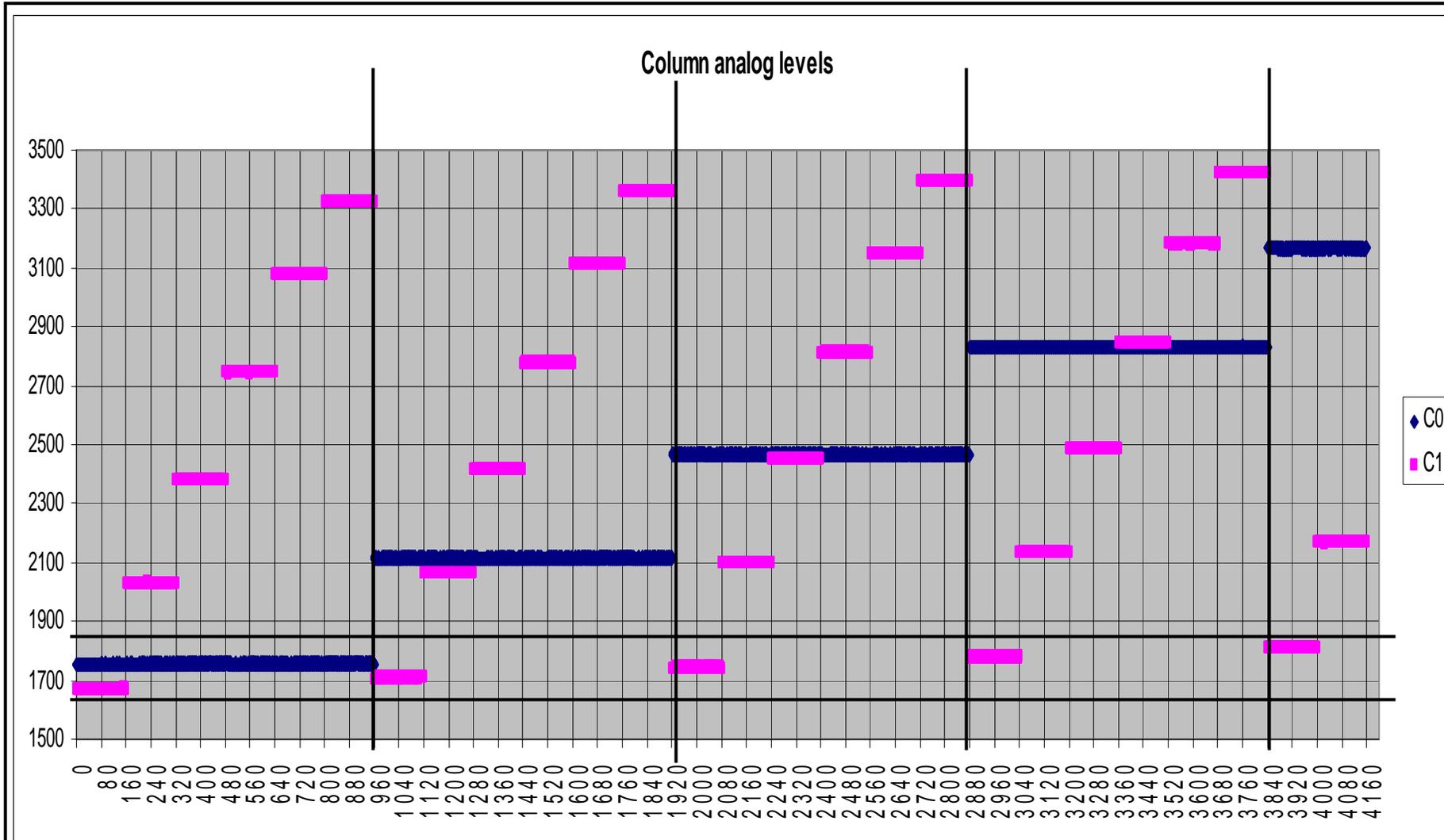
Measuring all pixels (5)



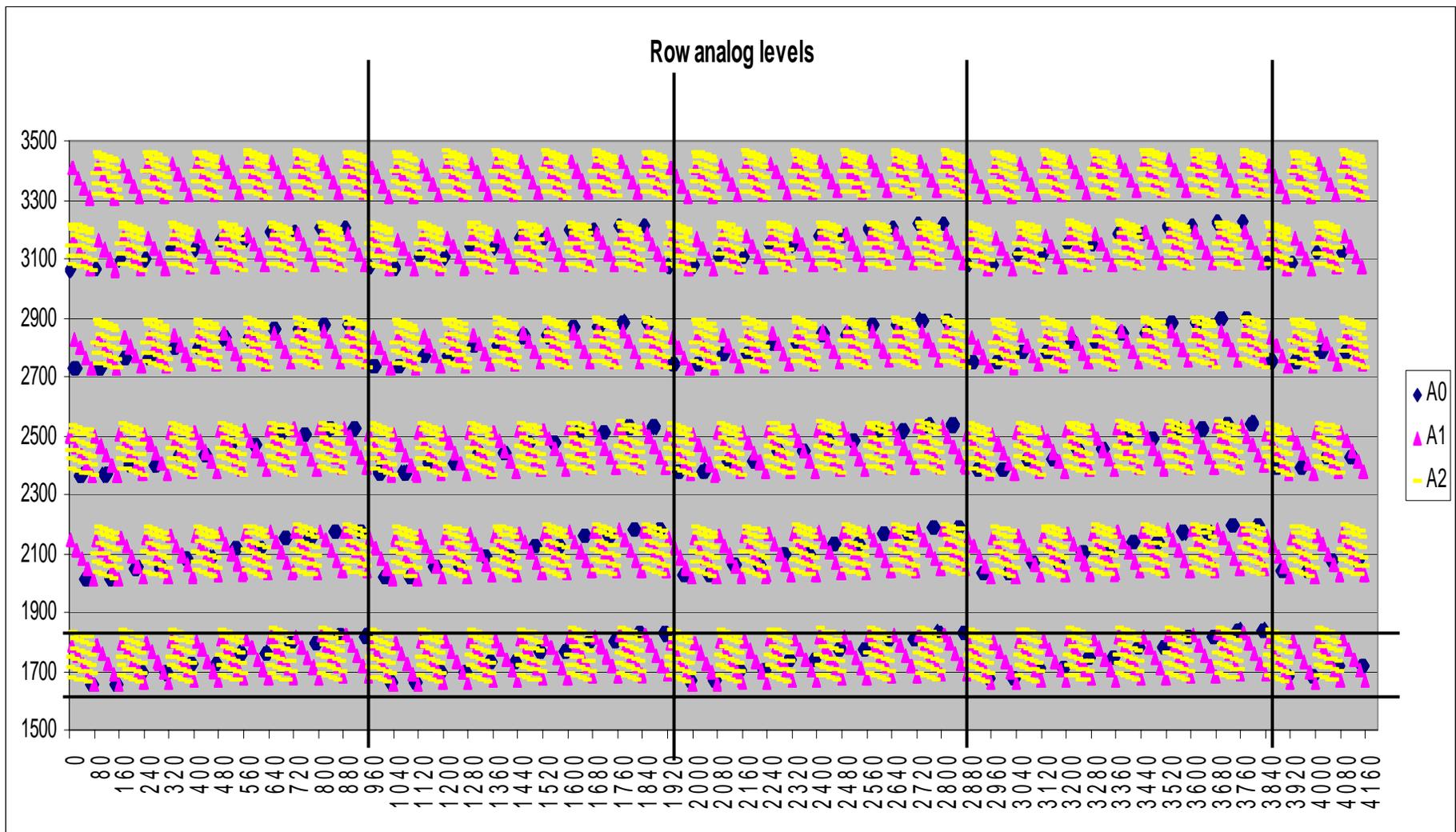
Measuring all pixels (6)



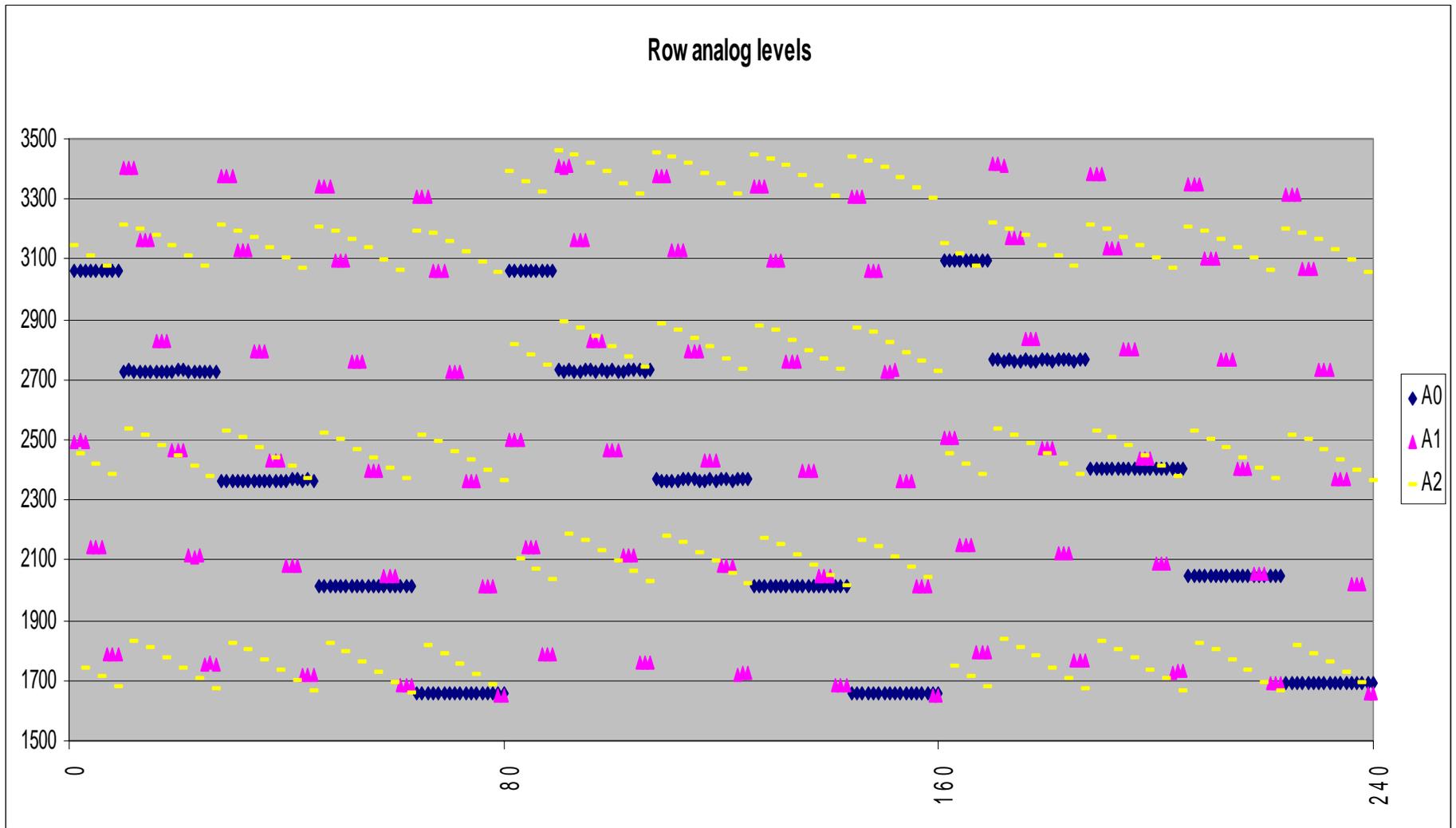
Measuring all pixels (7)



Measuring all pixels (8)



Measuring all pixels (9)



Other dependencies

- Two other dependencies were investigated.

VTRIM register 0x0B

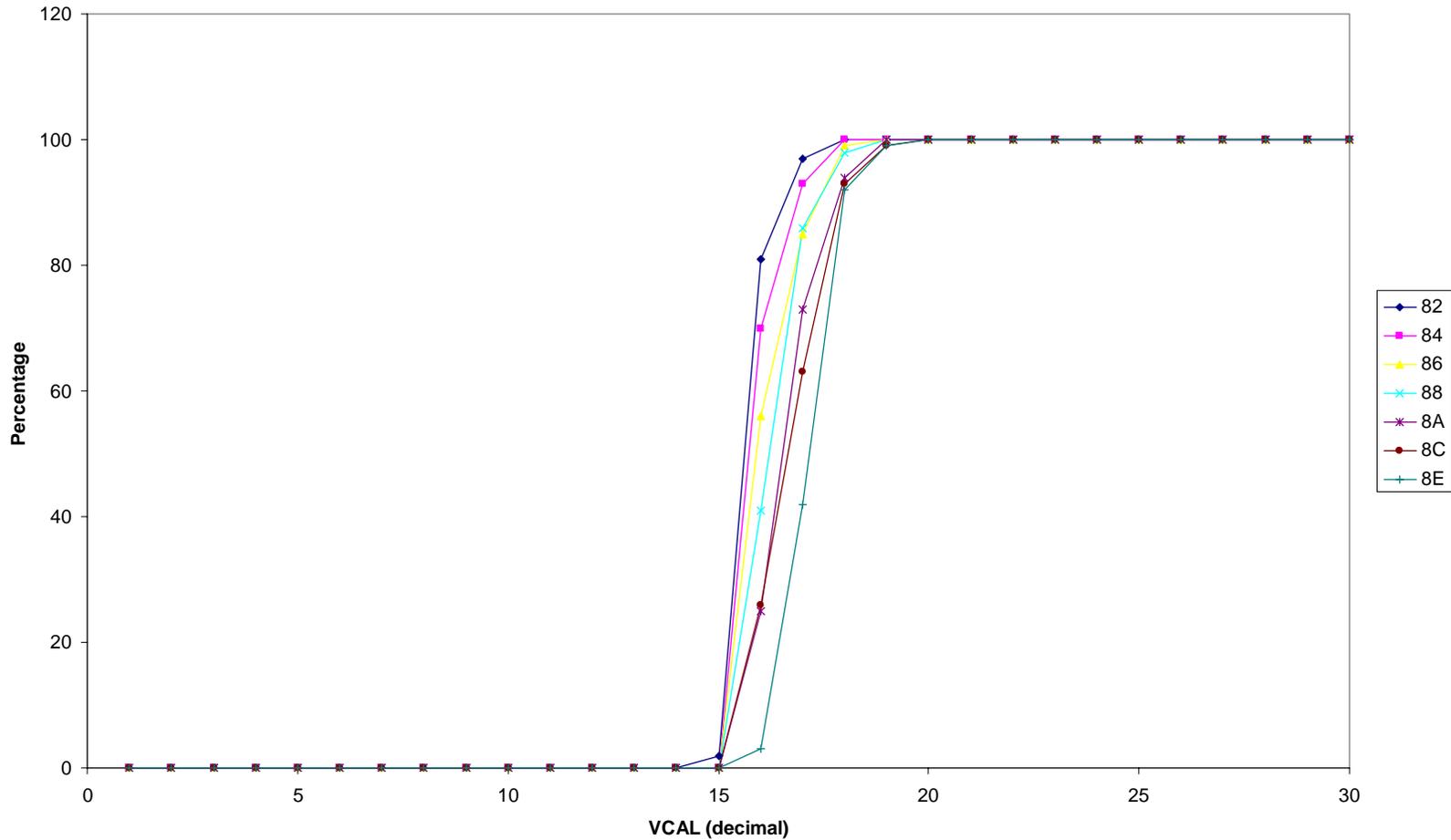
- Slides 32 to 34 shows the same pixel (column=0, row=0) measured 100 times on each VCAL setting point (decimal) with mask and trim register as curve parameter (hex). The VTRIM register was assigned different values: 0x00 in slide 32, 0x10 in slide 33 and 0x20 in slide 34. For some reasons the chip started to give mixed single and multiple hit responses (regardless of VCAL) when VTRIM register setting was increased to 0x30 and this data is not presented here.
- As it can be observed, only slide 33 looks similar with any of slides 10 to 15. On those ones the VTRIM register was set to the 'default' value (0x1D) which is reasonable close to the 0x20 setting on slide 33.
- I was expecting that a change in VTRIM will shift this family of curves to the left or to the right. Instead, it seems that changes in VTRIM are bringing closer or taking apart the curve family. Is this the correct (designed) dependence?

Trigger latency register WBC=0xFE and test pulse delay register CALDEL=0x1A

- Slide 35 shows the same pixel (column=0, row=0) measured 100 times on each CALDEL setting point (decimal) with WBC register as curve's parameter (0x16,17,18,19). The VTRIM register was assigned the default 0x1D, the mask and trim register was set to 0x88 (enable pixel and trim bits=8) and VCAL register set to default 0x14.
- A nice chaining can be observed. The width (measured at 100% probability response) is also quite equal, about 55 decimal settings in CALDEL for each of the four WBC settings.

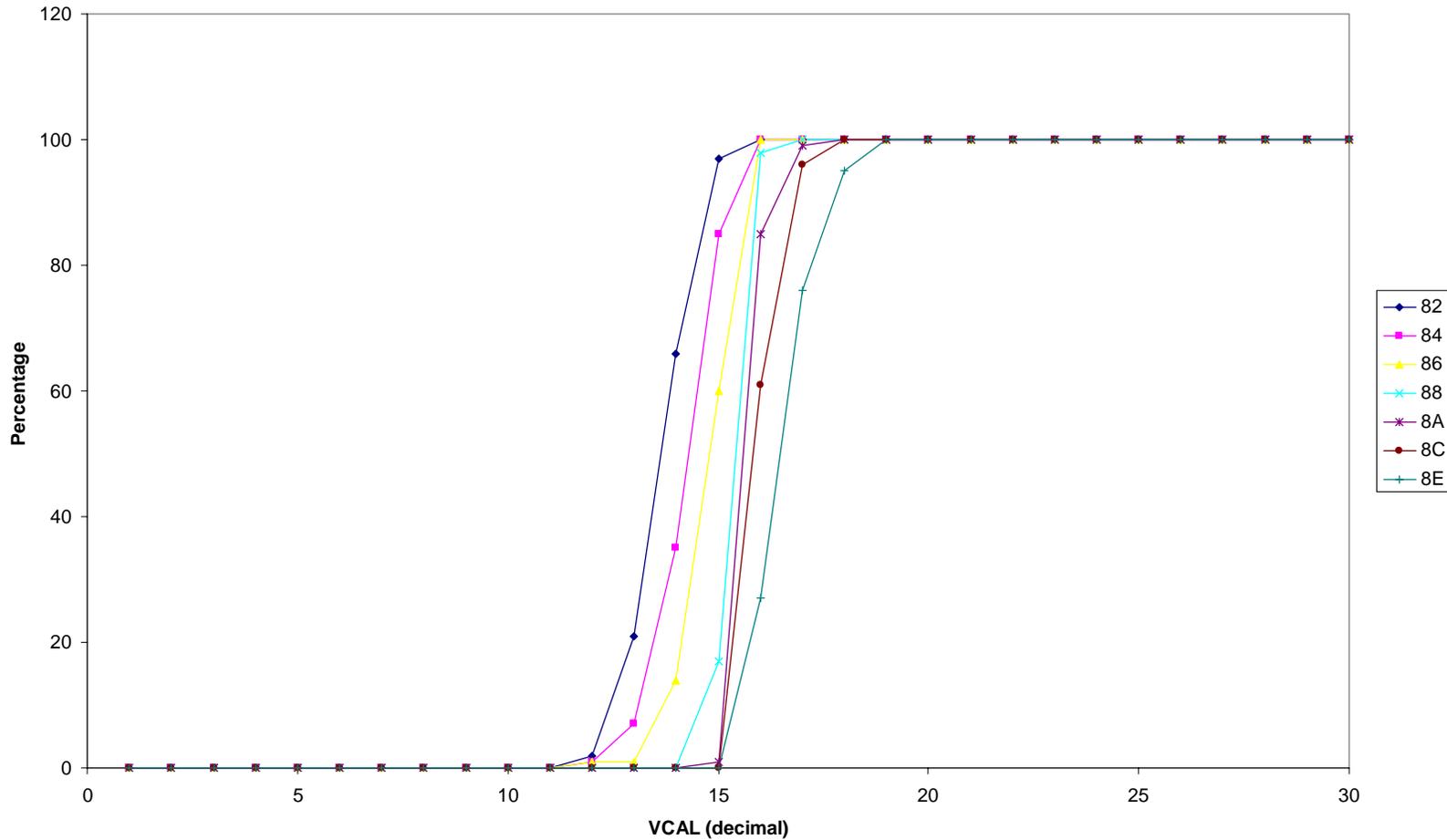
One pixel measured 100 times (7)

Pixel response probability (Column=0 Row=0 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex) when VTRIM setting is 0x00



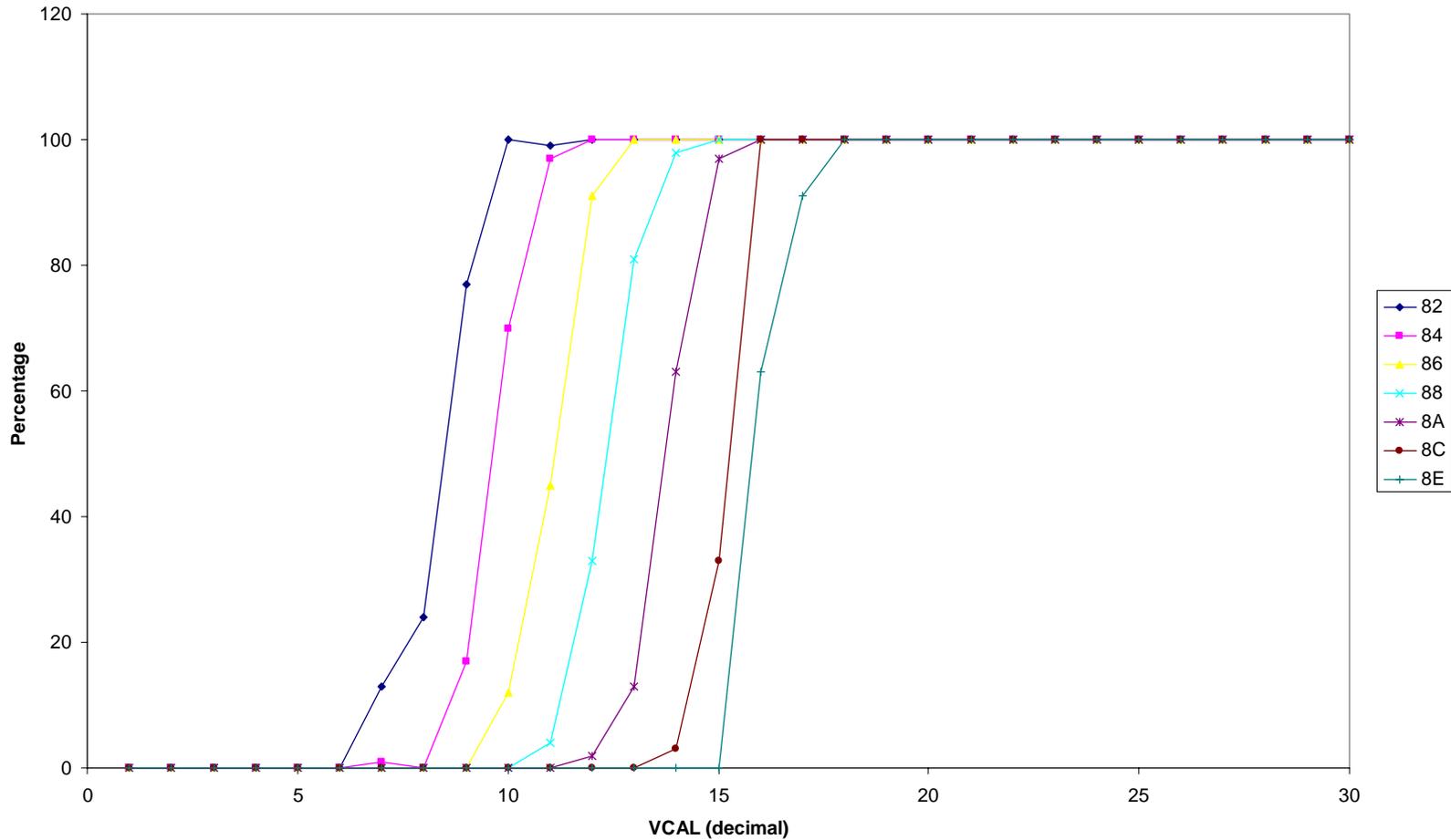
One pixel measured 100 times (8)

Pixel response probability (Column=0 Row=0 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex) when VTRIM setting is 0x10



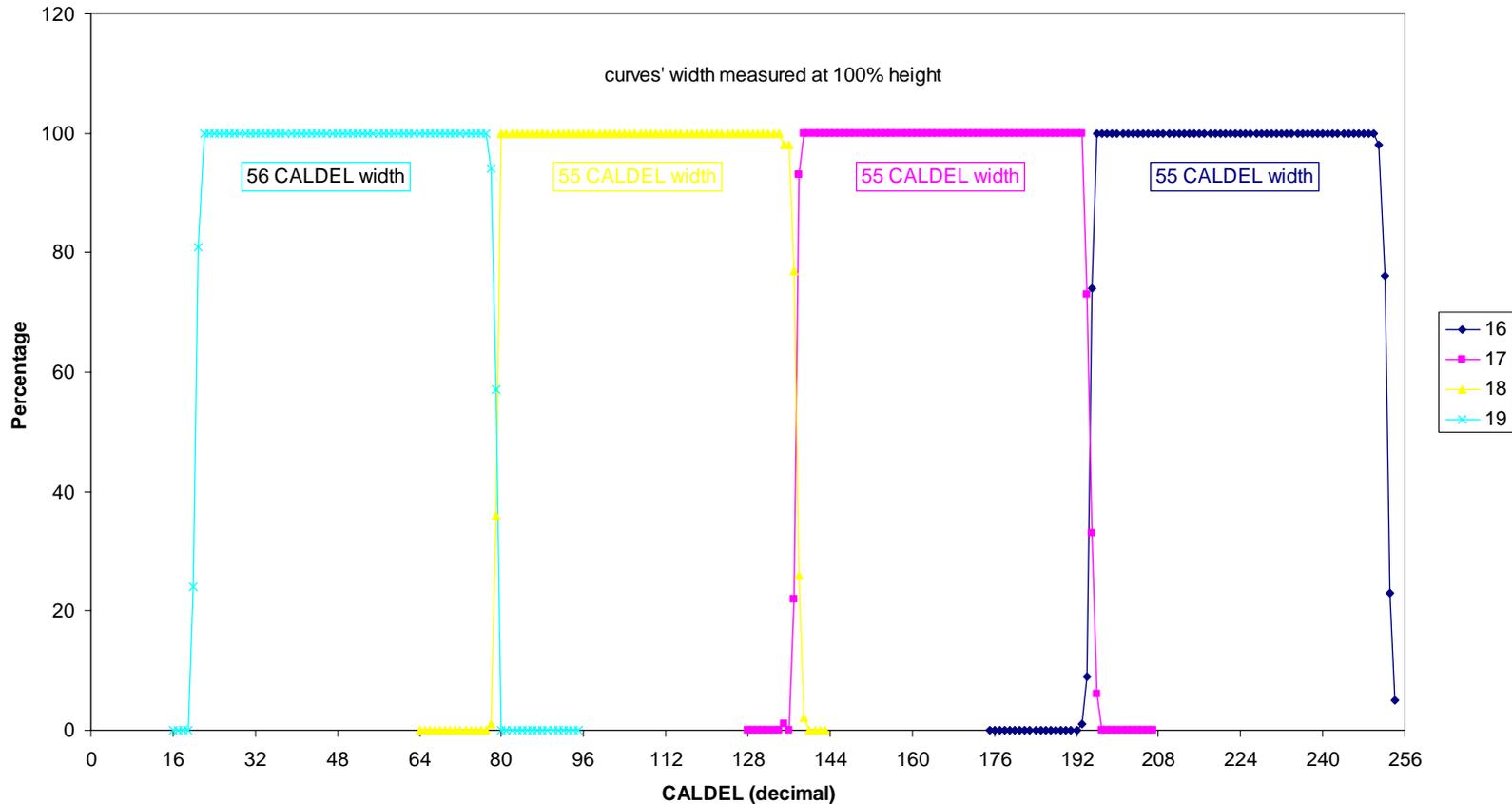
One pixel measured 100 times (9)

Pixel response probability (Column=0 Row=0 decimal) as a function of VCAL settings (decimal) for different trim bit values (hex) when VTRIM setting is 0x20



One pixel measured 100 times (10)

Pixel response probability (Column=0 Row=0 decimal) as a function of CALDEL settings (decimal) for different trigger latency WBC settings (0x16,17,18,19) and with constant masktrim bits = 0x88 and VCAL = 0x14 (curves thresholds are VCAL dependent)



Sort of conclusions...

- So many conclusions and questions can be drawn that the following list is far from being complete....
- Probably the most important is that we need feedback from CMS Pixel to have a similar (preferable identical) testing procedures and PASS/FAIL criteria.
- Some of my questions are mentioned already, some others can be inferred looking at the data in each slide. Any questions, suggestions, answers, are welcome.
- Summary of what I DID NOT exercised:
 - Supply current (analog and digital) vs. supply voltage (analog and digital).
 - I2C address was fixed (range is 0 to 15)
 - I2C frequency was fixed (40MHz).
 - Miscellaneous tests that I also don't understand, like 'overflow reset', 'double column time stamp buffer', 'double column data buffer'.
 - Currently I'm calibrating one pixel at a time. It might be important to 'check' the readout when more pixels are calibrated, in some particular pixel-map configurations.
- How should we organize testing results? It is easy to report data in a text file. If we want to report all pixel data as presented in slides 22, 23 and 24, one chip file occupies 3.5 to 7.0Mb (for 3 up to 7 TRIM bits values respectively). If I'm writing to a Microsoft 3.51 database, the 7Mb .txt file shrinks to ~1.3Mb .mdb file, with the potential advantage of being able to do any query and plots over multiple chips and wafers.