

**Fermi National Accelerator Laboratory**

## **The PPD/ETT ASIC TEST SYSTEM**

### **Electrical and Mechanical Specifications for an ASIC Test Bed Printed Circuit Board**

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- 1. THE PPD/ETT ASIC TEST SYSTEM OVERVIEW ..... 2
  - 1.1 ASIC Test Bed PC Board Function and Purpose..... 2
  - 1.2 ASIC Test Bed PC Board Illustration ..... 2
- 2. MECHANICAL SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD..... 3
  - 2.1 PCB Materials ..... 3
  - 2.2 PCB Physical Size ..... 3
  - 2.3 Connector Locations ..... 3
    - 2.31 Power Connectors ..... 3
    - 2.32 Input/Output Connectors ..... 4
  - 2.4 Mounting/Tooling Holes ..... 5
- 3. ELECTRICAL SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD ..... 6
  - 3.1 Power Supply Voltages ..... 6
  - 3.2 Power Supply Currents ..... 6
  - 3.3 Circuit Protection..... 6
- 4. INPUT/OUTPUT SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD..... 7
  - 4.1 Connectors on the ASIC Test Bed Printed Circuit Board ..... 7
  - 4.2 Connector Pinouts ..... 7
    - 4.21 Power Connectors ..... 7
    - 4.22 Analog I/O Connectors ..... 8
    - 4.23 Digital I/O Connectors ..... 10
- 5. OTHER SPECIFICATIONS ..... 13
  - 5.1 Connector/Cable Part Numbers ..... 13
  - 5.2 Cooling Requirements..... 13

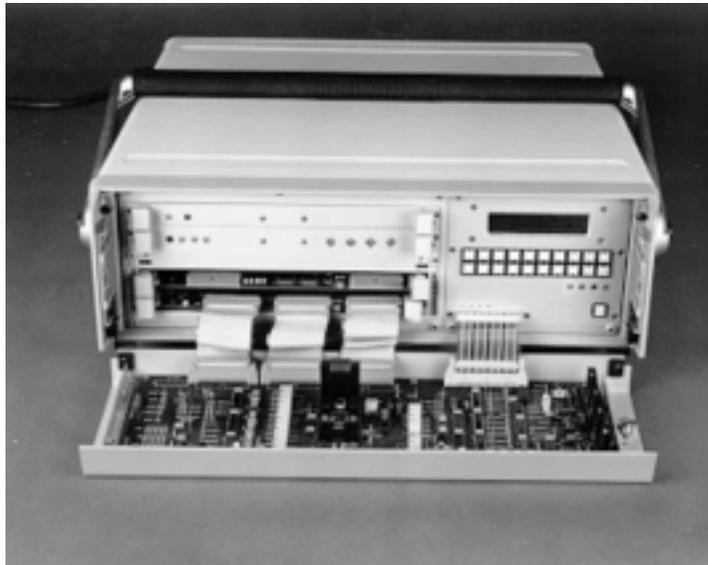
## 1. THE PPD/ETT ASIC TEST SYSTEM OVERVIEW

### 1.1 ASIC Test Bed PC Board Function and Purpose

The ASIC Test Bed Printed Circuit board is a "personality" module or custom interface board for the PPD/ETT ASIC Test System. The ASIC Test System was created to fill the need for a small (portable), low cost (< \$12,000), flexible test stand to test custom Application Specific Integrated Circuits (ASIC's) being developed by Fermilab's Engineering and Technical Teams Electrical Support Group (ETT/ES). This chip level test system has evolved into a practical method for testing the more than 10,000 custom integrated circuits and 3,500 KTeV DPMT VI PC boards that were produced for Fermilab fixed-target experiments E799 and E832.

### 1.2 ASIC Test Bed PC Board Illustration

Shown below is a photograph of the ASIC Test System with attached DBC2 ASIC Test Bed PC Board.



The keypad on the right can control the operation of the entire ASIC Test System. Just above the keypad is the 24 character by 2 line LCD display. Device Under Test (DUT) error codes and system information are usually displayed here. The horizontal slots on the left contain the major functional blocks of the ASIC Test System such as the CPU and RAM/Display cards plus one or more Analog and Digital I/O cards. The cabling connects the Test Bed PCB and the Analog and Digital I/O cards. To get a rough idea of the physical size of the entire system, the DBC2 Test Bed PC Board in the foreground is 15.2" in length. The units height is 6" and its depth is approximately 20".

## 2. MECHANICAL SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD

### 2.1 PCB Materials

The circuit board is usually made from 0.062" thick FR-4 epoxy fiberglass laminate although, in cases where an extra rigid design is required, a board thickness of 0.093" can be used. The PCB design can consist of four, six, or eight layers (multiple signal, and or power/ground planes) of this material. A minimum of four layers is recommended, with the following layer stack; internal power and ground layers of 1 oz. copper and two external signal layers.

### 2.2 PCB Physical Size

The ASIC Test Bed Printed Circuit Board has a total surface area of 76 sq. in. The pc board is rectangular in shape and has exterior dimensions of 15.200" x 5.000" (See Figure 1 below). Tolerances on these dimensions are not critical;  $\pm 0.010$ " should be adequate.

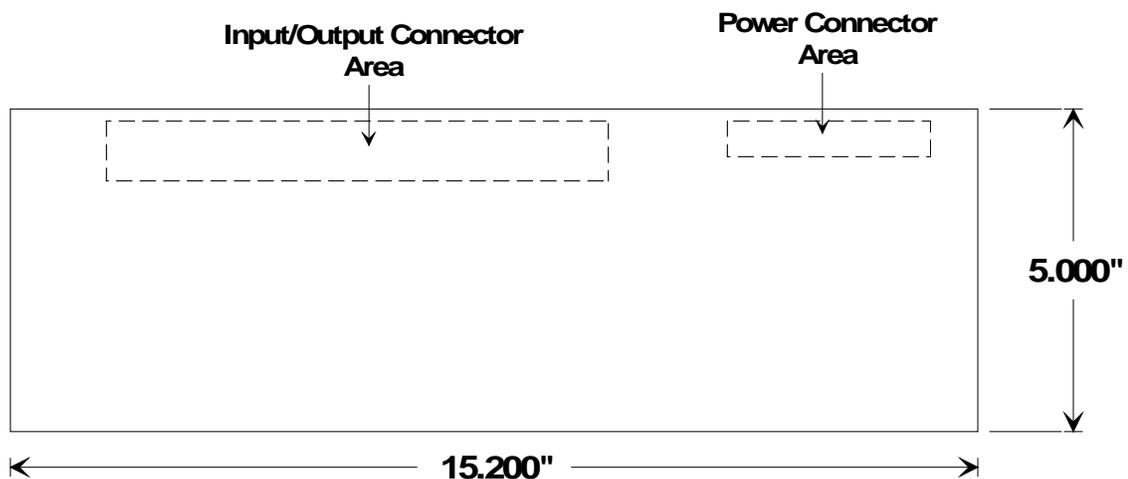


Figure 1. ASIC Test Bed Printed Circuit Board dimensions.

### 2.3 Connector Locations

As can be seen in Figure 1, there are two general areas for location of I/O and power connectors on the ASIC Test Bed Printed Circuit Board. While it is not absolutely necessary to follow the placement guidelines here for connector position, it does make the ribbon cable connections to the ASIC Test System as short and painless as possible.

#### 2.31 Power Connectors

A single 3M 40-pin header and ribbon cable is used to bring power onto the ASIC Test Bed Printed Circuit Board. The connector position and pin 1 orientation relative to the circuit board are shown in Figure 2. The pinout for this connector is listed in section 4.21 and the part number in 5.1.

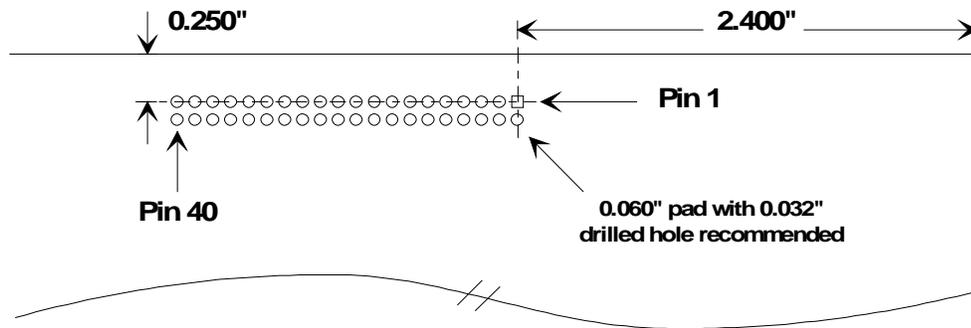


Figure 2. Power Connector location for ASIC Test Bed Printed Circuit Board.

### 2.32 Input/Output Connectors

A Yamachi 64-pin header and fine pitch (0.025") ribbon cable are used to make the I/O connections on the ASIC Test Bed Printed Circuit Board. The nature of the device being tested dictates how many I/O connectors are required on the ASIC Test Bed Circuit Board. A simple device may only need one or two I/O connectors, while a more complex design may need five with a maximum of eight. The I/O connector position and pin 1 orientation relative to the circuit board are shown in Figure 3. The pinout for this connector is listed in section 4.22 and the part number in 5.1.

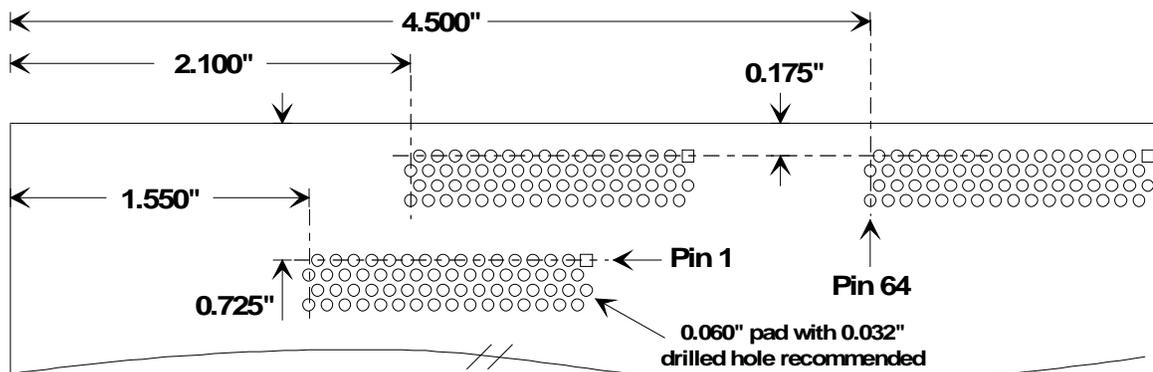


Figure 3. I/O Connector locations for ASIC Test Bed Printed Circuit Board.

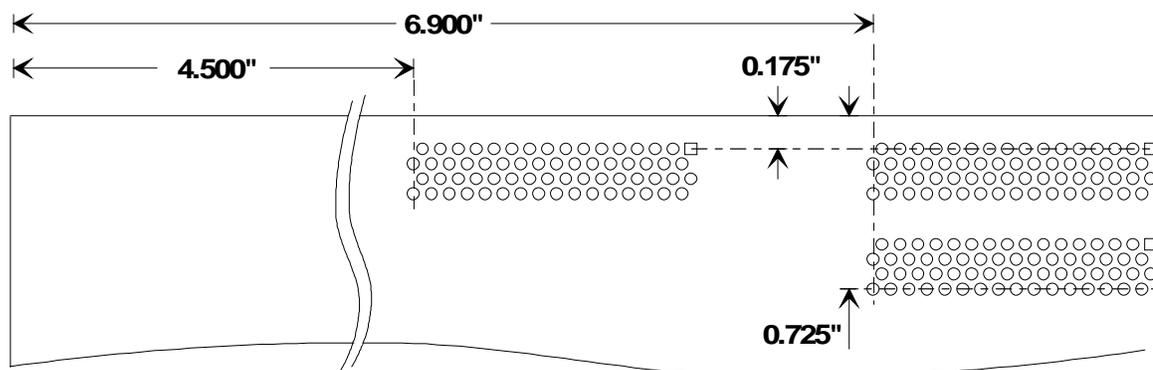
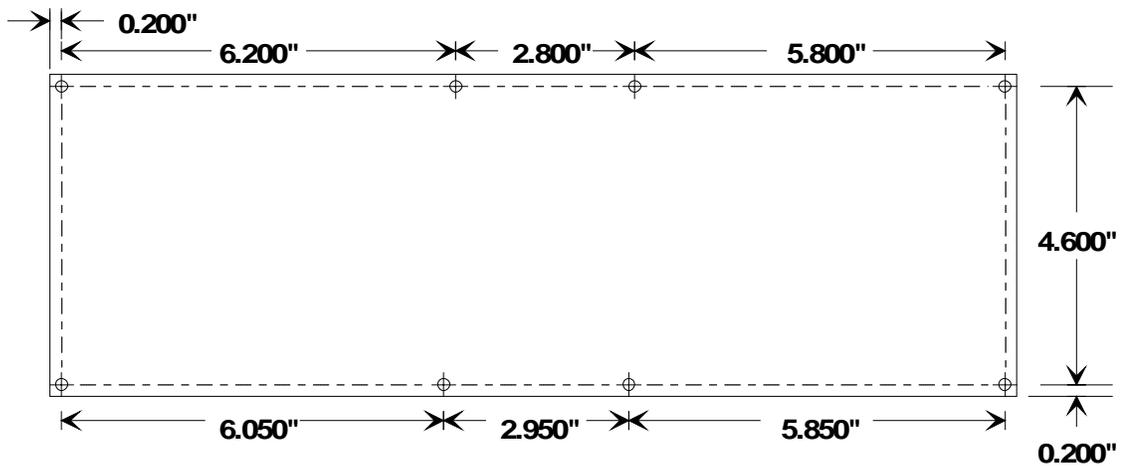


Figure 4. Additional I/O Connector locations.

## 2.4 Mounting/Tooling Holes

The ASIC Test Bed Printed Circuit Board has eight (8) standard positions for mounting/tooling holes along its perimeter. A minimum of four corner tooling holes recommended are on a design. If space allows, all holes should be placed on the design. The recommended size for these holes is 0.110". See Figure 5 below for the exact location of the tooling holes.



**Figure 5.** Tooling hole locations for the ASIC Test Bed Printed Circuit Board.

### 3. ELECTRICAL SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD

#### 3.1 Power Supply Voltages

The ASIC Test Bed Printed Circuit Board has four power supply voltages available: +24V,  $\pm 12V$ , and +5V. These are brought onto the board through a 40 pin 3M ribbon cable connector and are normally provided by the ASIC Test System Box. Other values of supply voltage, when needed, can be generated through the use of linear regulators or DC to DC converters.

#### 3.2 Power Supply Currents

The table below details the maximum current capacity for each of the power supply voltages available on the ASIC Test Bed Printed Circuit Board.

Supply Voltage	Available Current
+24V	2.0 Amps
$\pm 12V$	0.5 Amps
+5V	1.5 Amps

#### 3.3 Circuit Protection

On board fuses are recommended for all ASIC Test Bed Printed Circuit Board power supply voltages. Recommended fuse types are:

**Through Hole:**

Littlefuse PICO II Very Fast-Acting Fuse, Series 251

Littlefuse Picofuse Very Fast-Acting Fuse, Series 266

**Surface Mount:**

Littlefuse NANO<sup>2</sup> SMF Very Fast-Acting Fuse, Series 451

These devices fill the requirements of protecting the device under test and the Test Bed Printed Circuit Board, while consuming very little board space.

## 4. INPUT/OUTPUT SPECIFICATIONS FOR THE ASIC TEST BED PC BOARD

### 4.1 Connectors on the ASIC Test Bed Printed Circuit Board

There are only two connector types on the ASIC Test Bed Printed Circuit Board. Input/Output (I/O) signals flows through one type, and system supply voltages flow through the other. The connection of I/O signals between the ASIC Test System Box and the ASIC Test Bed Printed Circuit Board is accomplished through the use of short fine pitch (0.025") ribbon cables. The number of these I/O connectors on any given ASIC Test Bed Printed Circuit Board can vary. As a minimum, there could be one or two, while the maximum could be as high as nine.

### 4.2 Connector Pinouts

The following sections contain the connector pinout listings for power and I/O connectors that are present on the ASIC Test System Box

#### 4.21 Power Connectors

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	Regulated +24.0 V Supply	2	System Ground
3	Regulated +24.0 V Supply	4	System Ground
5	Regulated +24.0 V Supply	6	System Ground
7	Regulated +24.0 V Supply	8	System Ground
9	Regulated +24.0 V Supply	10	System Ground
11	Regulated +24.0 V Supply	12	System Ground
13	Regulated +24.0 V Supply	14	System Ground
15	Regulated +24.0 V Supply	16	System Ground
17	Regulated +24.0 V Supply	18	System Ground
19	No Connection	20	System Ground
21	Regulated +5.00 V Supply	22	System Ground
23	Regulated +5.00 V Supply	24	System Ground
25	Regulated +5.00 V Supply	26	System Ground
27	Regulated +5.00 V Supply	28	System Ground
29	Regulated +12.0 V Supply	30	System Ground
31	Regulated +12.0 V Supply	32	System Ground
33	Regulated +12.0 V Supply	34	System Ground
35	Regulated -12.0 V Supply	36	System Ground
37	Regulated -12.0 V Supply	38	System Ground
39	Regulated -12.0 V Supply	40	System Ground

## 4.22 Analog I/O Connectors

Signal Description:

**RAMDAC (X)** Eight bit DAC outputs with a voltage swing from 0 to +5.0V, capable of 50 MHz conversion rates. **ADCIN (X)** These are the inputs to four 16-bit Analog to Digital Converters. Maximum voltage swings on these inputs are 0 to +10.0V This ADC has a maximum conversion rate of 17  $\mu$ s (~58 kHz) for 16-bits. **DCDAC (X)** Sixteen bit DAC outputs with a voltage swing from 0 to +10.0V, because of the serial load format of the DAC these are relatively slow signals.

**Analog I/O Connector Pinout (J4)**

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	Signal Ground	2	RAMDAC (0)*
3	RAMDAC (0)	4	Signal Ground
5	RAMDAC (1)*	6	RAMDAC (1)
7	Signal Ground	8	Signal Ground
9	RAMDAC (2)*	10	RAMDAC (2)
11	Signal Ground	12	Signal Ground
13	RAMDAC (3)*	14	RAMDAC (3)
15	Signal Ground	16	Signal Ground
17	RAMDAC (4)	18	RAMDAC (4)*
19	Signal Ground	20	Signal Ground
21	RAMDAC (5)*	22	RAMDAC (5)
23	Signal Ground	24	Signal Ground
25	RAMDAC (6)	26	RAMDAC (6)*
27	Signal Ground	28	Signal Ground
29	Signal Ground	30	Signal Ground
31	ADCIN (2)*	32	ADCIN (2)
33	Signal Ground	34	Signal Ground
35	ADCIN (3)*	36	ADCIN (3)
37	Signal Ground	38	Signal Ground
39	ADCIN (0)*	40	ADCIN (0)
41	Signal Ground	42	Signal Ground
43	ADCIN (1)*	44	ADCIN (1)
45	Signal Ground	46	Signal Ground
47	DCDAC (7)*	48	DCDAC (7)
49	DCDAC (6)*	50	DCDAC (6)
51	DCDAC (5)*	52	DCDAC (5)
53	DCDAC (4)*	54	DCDAC (4)
55	DCDAC (3)*	56	DCDAC (3)
57	DCDAC (2)*	58	DCDAC (2)
59	DCDAC (1)*	60	DCDAC (1)
61	DCDAC (0)*	62	DCDAC (0)
63	Signal Ground	64	Signal Ground

Signal Description:

**FIFO 0, 1, 2, 3 (X)** Unbuffered TTL level inputs, that connect directly to four 2048 x 8 FIFOs. These inputs can accept a new data word every 15 ns (66.6 MHz). **FIFO 0, 1, 2, 3 ST** TTL level write clock input for FIFO's 0, 1, 2, 3 (X), minimum pulse width high/low for this input is 6 ns. **DCI (XX)** Sixteen buffered, but not registered, TTL level inputs.

**Analog I/O Connector Pinout (J3)**

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	Signal Ground	2	FIFO 0 (0)
3	FIFO 0 (1)	4	FIFO 0 (2)
5	Signal Ground	6	FIFO 0 (3)
7	FIFO 0 (4)	8	FIFO 0 (5)
9	Signal Ground	10	FIFO 0 (6)
11	FIFO 0 (7)	12	FIFO 0 ST
13	Signal Ground	14	FIFO 1 (0)
15	FIFO 1 (1)	16	FIFO 1 (2)
17	Signal Ground	18	FIFO 1 (3)
19	FIFO 1 (4)	20	FIFO 1 (5)
21	Signal Ground	22	FIFO 1 (6)
23	FIFO 1 (7)	24	FIFO 1 ST
25	Signal Ground	26	FIFO 2 (0)
27	FIFO 2 (1)	28	FIFO 2 (2)
29	Signal Ground	30	FIFO 2 (3)
31	FIFO 2 (4)	32	FIFO 2 (5)
33	Signal Ground	34	FIFO 2 (6)
35	FIFO 2 (7)	36	FIFO 2 ST
37	Signal Ground	38	FIFO 3 (0)
39	FIFO 3 (1)	40	FIFO 3 (2)
41	Signal Ground	42	FIFO 3 (3)
43	FIFO 3 (4)	44	FIFO 3 (5)
45	Signal Ground	46	FIFO 3 (6)
47	FIFO 3 (7)	48	FIFO 3 ST
49	DCI (00)	50	DCI (01)
51	DCI (02)	52	DCI (03)
53	DCI (04)	54	DCI (05)
55	DCI (06)	56	DCI (07)
57	DCI (08)	58	DCI (09)
59	DCI (10)	60	DCI (11)
61	DCI (12)	62	DCI (13)
63	DCI (14)	64	DCI (15)

### 4.23 Digital I/O (Mark I) Connectors

Signal Description:

**DCO (XX)** Eight registered TTL level outputs, very slow, can be set to logic 0 or 1. Outputs can sink 24 ma. and source 2.6 ma. **RAM1, 2 (XX)** These are the TTL level outputs of the Digital I/O cards six synchronous 2048 x 8 FIFO's, these signals are capable of running at 66.6 MHz. Outputs can sink 8 ma. and source 2 ma. **Pulsed (XX)** These signal lines output a TTL level pulse with approximately 100ns width. The signals can be used as resets, triggers, etc. The quiescent state of these signals may be independently changed to either logic 0 or 1.

**Digital I/O (Mark I) Connector Pinout (Slow Output J12)**

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	DCO (00)	2	DCO (01)
3	DCO (02)	4	DCO (03)
5	DCO (04)	6	DCO (05)
7	DCO (06)	8	DCO (07)
9	Pulsed (00)	10	Pulsed (01)
11	Pulsed (02)	12	Pulsed (03)
13	Pulsed (04)	14	Pulsed (05)
15	Pulsed (06)	16	Pulsed (07)
17	Signal Ground	18	Pulsed (08)
19	Pulsed (09)	20	Pulsed (10)
21	Signal Ground	22	Pulsed (11)
23	Pulsed (12)	24	Pulsed (13)
25	Signal Ground	26	Pulsed (14)
27	Pulsed (15)	28	No Connection
29	Signal Ground	30	RAM1 (00)
31	RAM1 (01)	32	RAM1 (02)
33	Signal Ground	34	RAM1 (03)
35	RAM1 (04)	36	RAM1 (05)
37	Signal Ground	38	RAM1 (06)
39	RAM1 (07)	40	RAM1 (08)
41	Signal Ground	42	RAM1 (09)
43	RAM1 (10)	44	RAM1 (11)
45	Signal Ground	46	RAM1 (12)
47	RAM1 (13)	48	RAM1 (14)
49	Signal Ground	50	RAM1 (15)
51	RAM2 (00)	52	RAM2 (01)
53	Signal Ground	54	RAM2 (02)
55	RAM2 (03)	56	RAM2 (04)
57	Signal Ground	58	RAM2 (05)
59	RAM2 (06)	60	RAM2 (07)
61	Signal Ground	62	RAM2 (08)
63	RAM2 (09)	64	RAM2 (10)

Signal Description:

**RAM2, 3 (XX)** These are the TTL level outputs of the Digital I/O cards six synchronous 2048 x 8 FIFO's, these signals are capable of running at 66.6 MHz. Outputs can sink 8 ma. and source 2 ma. **Theta 1, 2, 3** TTL level system clocks running at 10, 5, and 2.5 MHz. Outputs can sink 64 ma. and source 8 ma. **RAM4T (XX)** Outputs can sink 8 ma. and source 2 ma. **Fast PLS (XX)**

**Digital I/O (Mark I) Connector Pinout (Fast Output J11)**

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	Signal Ground	2	RAM2 (11)
3	RAM2 (12)	4	RAM2 (13)
5	Signal Ground	6	RAM2 (14)
7	RAM2 (15)	8	RAM3 (00)
9	Signal Ground	10	RAM3 (01)
11	RAM3 (02)	12	RAM3 (03)
13	Signal Ground	14	RAM3 (04)
15	RAM3 (05)	16	RAM3 (06)
17	Signal Ground	18	RAM3 (07)
19	RAM3 (08)	20	RAM3 (09)
21	Signal Ground	22	RAM3 (10)
23	RAM3 (11)	24	RAM3 (12)
25	Signal Ground	26	RAM3 (13)
27	RAM3 (14)	28	RAM3 (15)
29	Signal Ground	30	Theta 1
31	Signal Ground	32	Theta 2
33	Signal Ground	34	Theta 3
35	Signal Ground	36	RAM4T (00)
37	Signal Ground	38	RAM4T (01)
39	RAM4T (02)	40	RAM4T (03)
41	Signal Ground	42	RAM4T (04)
43	RAM4T (05)	44	RAM4T (06)
45	Signal Ground	46	RAM4T (07)
47	RAM4T (08)	48	RAM4T (09)
49	Signal Ground	50	RAM4T (10)
51	RAM4T (11)	52	RAM4T (12)
53	Signal Ground	54	RAM4T (13)
55	RAM4T (14)	56	RAM4T (15)
57	Signal Ground	58	Fast PLS (00)
59	Signal Ground	60	Fast PLS (01)
61	Signal Ground	62	Fast PLS (02)
63	Signal Ground	64	Fast PLS (03)

Signal Description:

**FIFO1, 2, 3, 4 (XX)** Are the TTL level inputs of the Digital I/O cards synchronous 2048 x 8 FIFO's. These inputs can accept a new data word every 15 ns (66.6 MHz). **FIFO1, 2, 3, 4 STB** TTL level write clock input for FIFO's 0, 1, 2, 3 (XX), minimum pulse width high/low for this input is 6 ns. **DCI (XX)** Sixteen buffered, but not registered, TTL level inputs.

**Digital I/O (Mark I) Connector Pinout (Input J10)**

Pin Number:	Pin Name/Function:	Pin Number:	Pin Name/Function:
1	Signal Ground	2	FIFO1 (00)
3	FIFO1 (01)	4	FIFO1 (02)
5	Signal Ground	6	FIFO1 (03)
7	FIFO1 (04)	8	FIFO1 (05)
9	Signal Ground	10	FIFO1 (06)
11	FIFO1 (07)	12	FIFO1 STB
13	Signal Ground	14	FIFO2 (00)
15	FIFO2 (01)	16	FIFO2 (02)
17	Signal Ground	18	FIFO2 (03)
19	FIFO2 (04)	20	FIFO2 (05)
21	Signal Ground	22	FIFO2 (06)
23	FIFO2 (07)	24	FIFO2 STB
25	Signal Ground	26	FIFO3 (00)
27	FIFO3 (01)	28	FIFO3 (02)
29	Signal Ground	30	FIFO3 (03)
31	FIFO3 (04)	32	FIFO3 (05)
33	Signal Ground	34	FIFO3 (06)
35	FIFO3 (07)	36	FIFO3 STB
37	Signal Ground	38	FIFO4 (00)
39	FIFO4 (01)	40	FIFO4 (02)
41	Signal Ground	42	FIFO4 (03)
43	FIFO4 (04)	44	FIFO4 (05)
45	Signal Ground	46	FIFO4 (06)
47	FIFO4 (07)	48	FIFO4 STB
49	DCI (00)	50	DCI (01)
51	DCI (02)	52	DCI (03)
53	DCI (04)	54	DCI (05)
55	DCI (06)	56	DCI (07)
57	DCI (08)	58	DCI (09)
59	DCI (10)	60	DCI (11)
61	DCI (12)	62	DCI (13)
63	DCI (14)	64	DCI (15)

## 5. OTHER SPECIFICATIONS

### 5.1 Connector/Cable Part Numbers

The ASIC Test Bed Printed Circuit Board uses the following manufactures and part numbers for power, I/O connectors and cabling.

Connector/CableType :	Manufacture:	Part Number:	Description:
Power	3M Electronic Products	3432-6302	40-pin 0.100" x 0.100" Latch/Ejector Header, Straight, 4 Wall
Power Cabling	3M Electronic Products	3302/40	0.050" Pitch, 28 AWG 40-Conductor Flat Ribbon Cable
Input/Output	Yamachi	NFP-64A-0104	64-pin Header, Straight Solder, No Latch Lever
Input/Output Cabling	Spectra Strip	133-3013-064	0.025" Pitch, 64-Conductor Flat Ribbon Cable

### 5.2 Cooling Requirements

The ASIC Test Bed Printed Circuit Board is essentially cooled by convective airflow. All devices that may dissipate large amounts of power (e.g. on board linear voltage regulators) should be adequately heat sunked.

## 6. Revision History

March 26, 1999

Added recommended drilled hole sizes for tooling holes.

Corrected DCI/DCO error in Digital I/O Input Mark I connector (J10) pinout.