



FPix Electronics at FNAL

People involved:

- **Boris Baldin, EED (50%)**
- **Michael Matulik, EED (50%)**
- **Sergey Los, CMS (20% now, 50% in September 2003)**
- **W.Wester, C.Gingu, EED ASIC Testing group**

Current tasks:

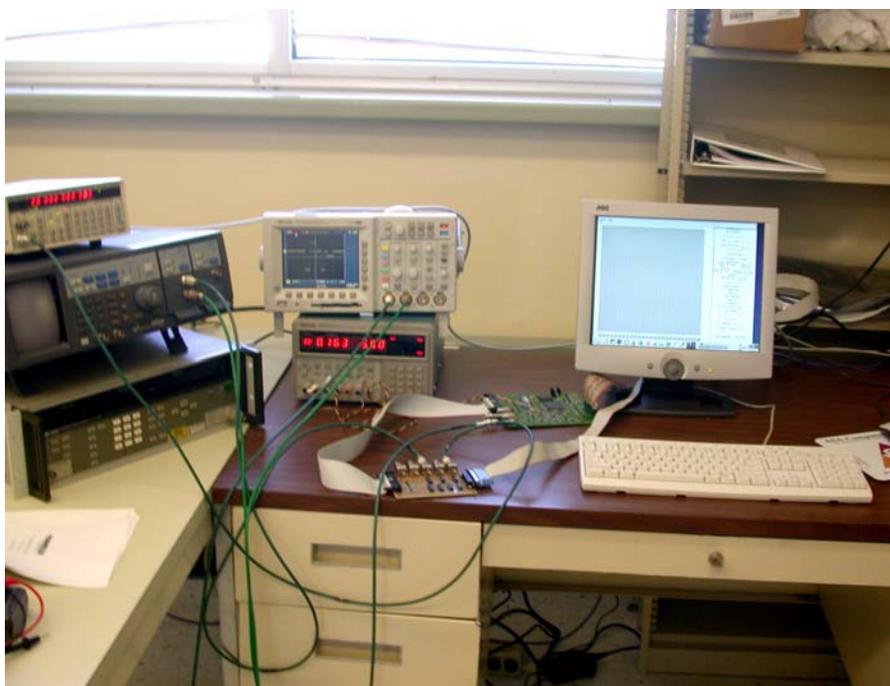
- **FPix system design issues – B.Baldin**
- **New VHDI and HDI designs – M.Matulik**
- **FPix front-end electronics infrastructure design – S.Los**
- **Technical support for ROC wafer test stand at FNAL – B.Baldin**
- **ROC wafer testing – W.Wester**



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Infrastructure for ROC testing at FNAL

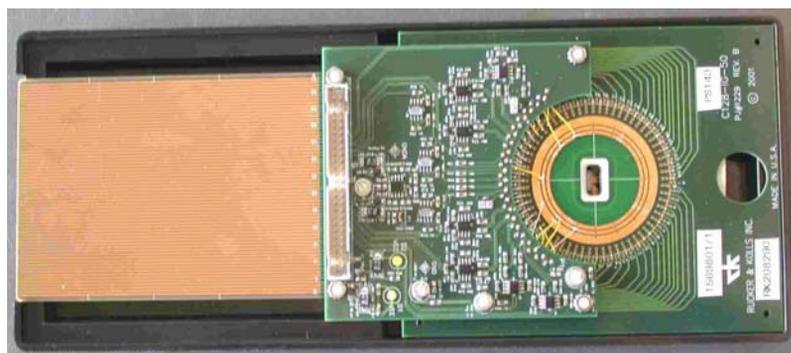
- Rutgers University test fixture for VHDI tests (two available at SiDet, FNAL)
 - Requires HDI adapter board to connect the VHDI
 - Allows various tests on ROC chips mounted on VHDI



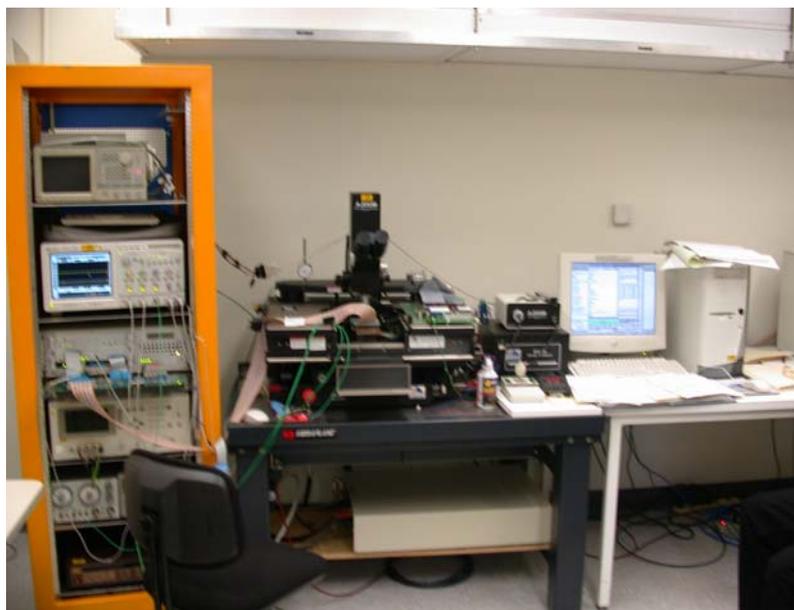


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- PSI43 Buffer Board (not to scale) mounted on Rucker & Kolls probe card features level converters from standard CMOS and LVDS to negative CMOS and negative LVDS levels



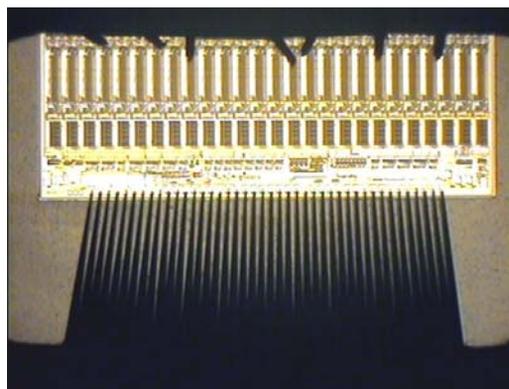
- Allows automated wafer and single chip testing



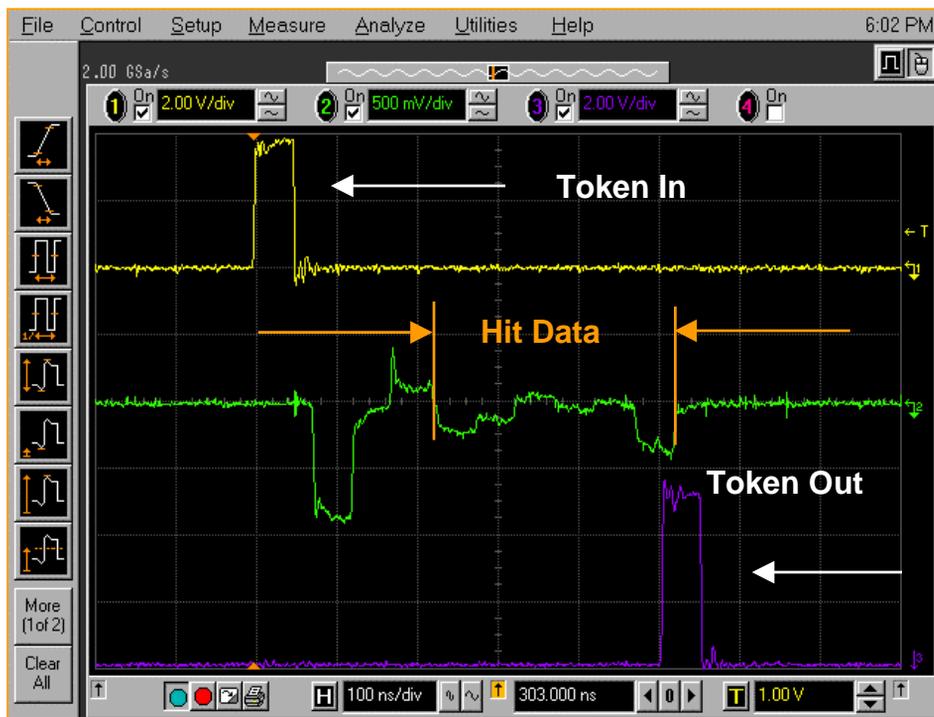


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- Photograph of the wire probes on PSI43 pads (42 probes @ 150 μ pitch)



- PSI43 #9 response to a single cell calibration trigger sequence





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Preliminary ROC chip test results

- Five single diced chips (#8 to #12) tested during debugging of the ROC wafer test stand
- Chips #9 and #11 respond to a calibration trigger sequence
- Chip #8 responds to I2C commands, but shows no hit data
- Chips #10 and #12 are dead ($V_d=0$, high current consumption)



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Future plans

- Finalize testing procedure and begin DMILL ROC wafer testing in 1..2 weeks
- Finish setup of the Rutgers University test fixture (needed software, HDI adapter board)
- Consider engineering design issues for the front-end electronics infrastructure (including so called Port Card)
- Modify ROC wafer testing hardware for 0.24 μ IBM version of the chip
- Consider possible hardware options of Plaquette testing at FNAL (need new design?)